EP-ESE/SY-BI Collaboration Seminar

June 2021

BLM SYSTEM:
RADIATION TOLERANT DEVELOPMENTS

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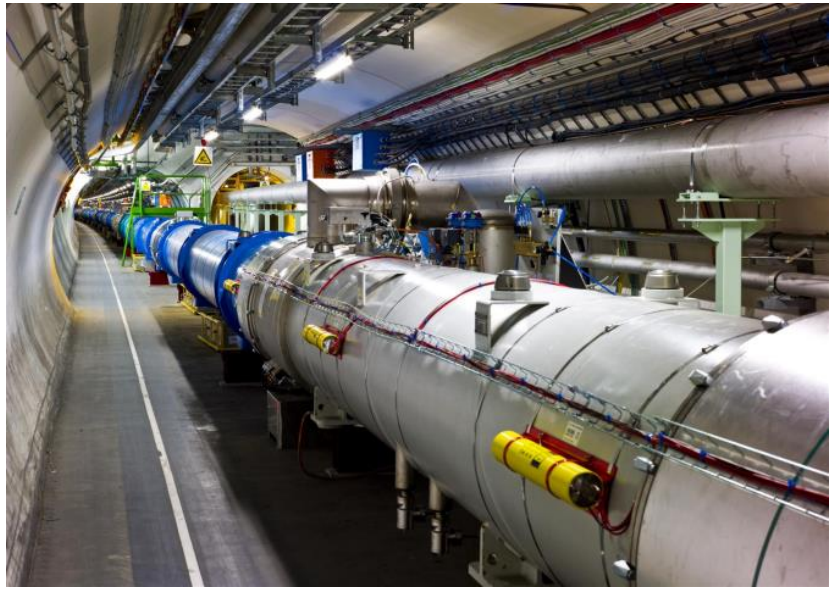
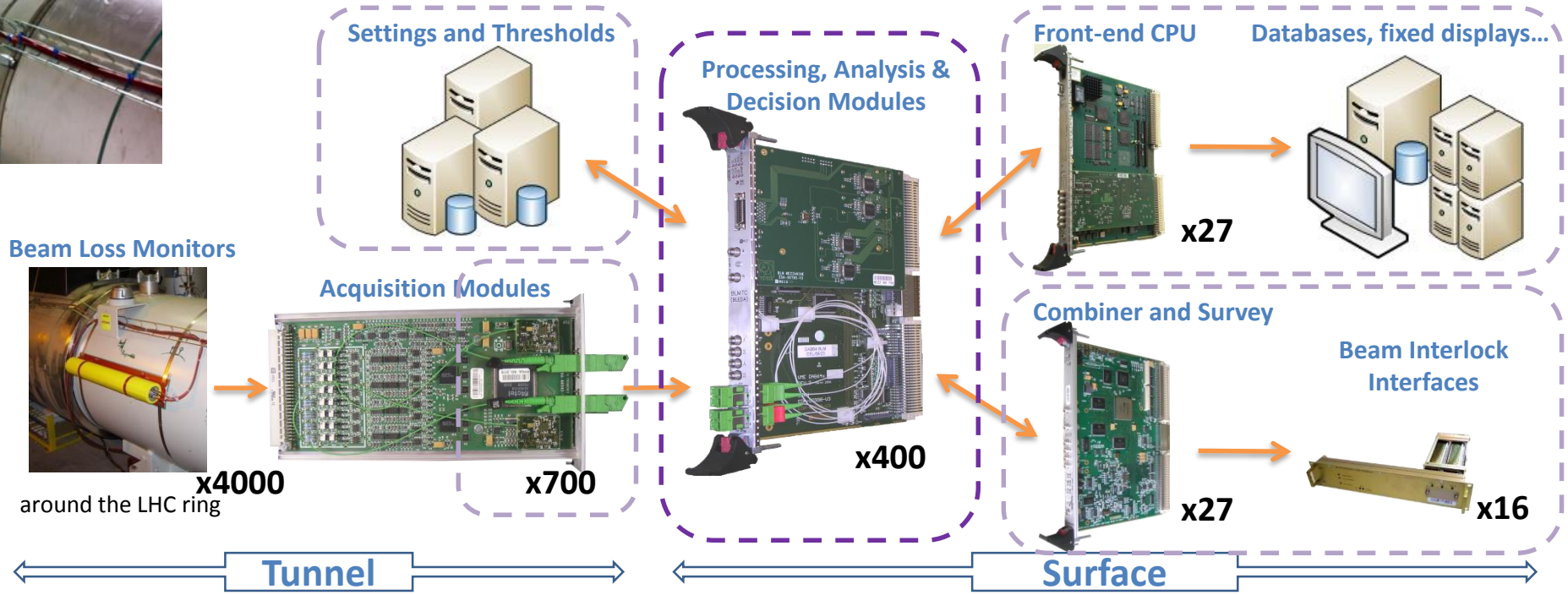
SYSTEM OVERVIEW

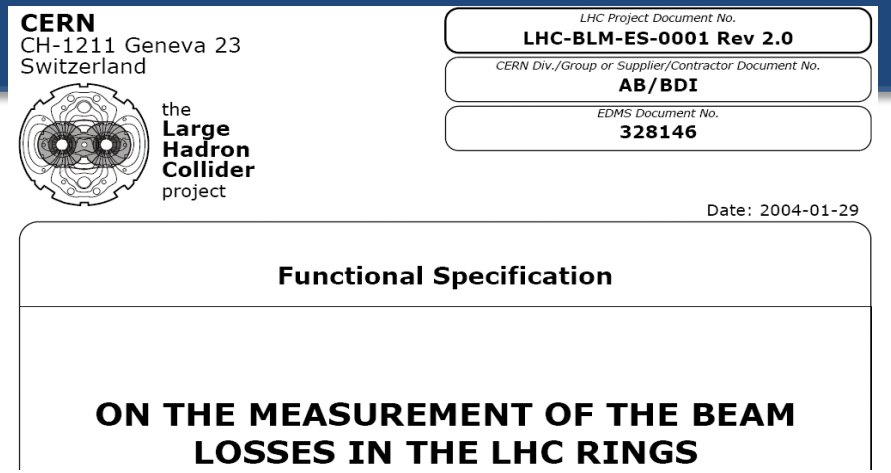
LHC BLM System Overview



- Highly critical system for the protection of LHC
- Deployed all around the 27 km of the tunnel
- Speed, Reliability, Fail-safety is required
- Large amount of measurement data are published continuously



Specifications



CERN
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Switzerland

the Large Hadron Collider project

LHC Project Document No.
LHC-BLM-ES-0001 Rev 2.0

CERN Div./Group or Supplier/Contractor Document No.
AB/BDI

EDMS Document No.
328146

Date: 2004-01-29

Functional Specification

ON THE MEASUREMENT OF THE BEAM LOSSES IN THE LHC RINGS

5. USE OF THE BLM'S FOR MACHINE PROTECTION

The strategy for machine protection impacts on the BLM design in two ways, its time response and the reliability.

Protection of the machine from beam losses has two aspects:

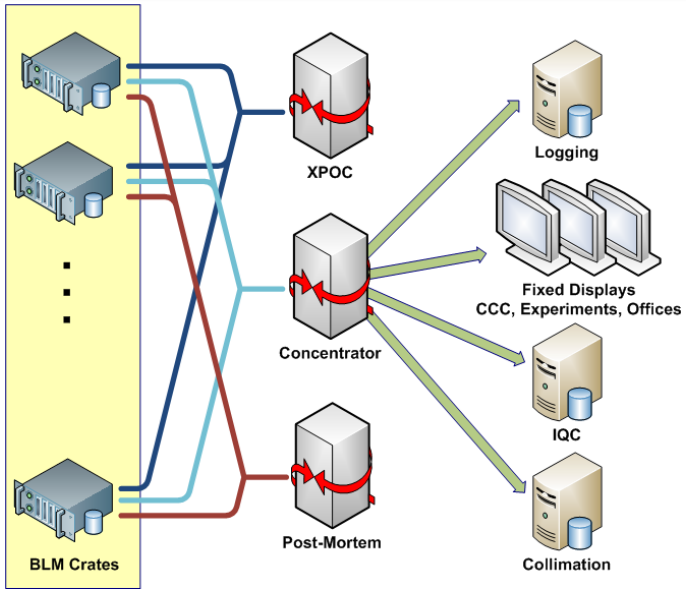
- protection against beam losses that could lead to damage of equipment,
- protection against beam losses that could lead to a quench of a magnet.

Since a repair of superconducting magnets would take several weeks, the protection against damage has highest priority and damages should be strictly avoided (**SIL 3, 1E-8 to 1E-7 1/h**).

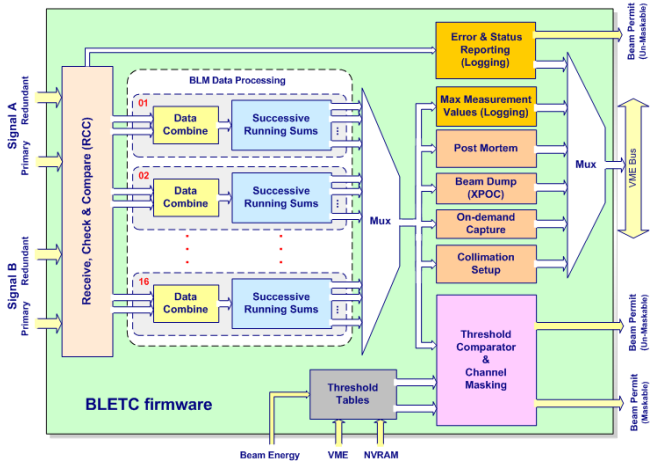
In case of a quench, the quench protection system would prevent equipment damage. However, the beam would be lost and re-establishing operation would take several hours. Therefore the number of quenches should be minimized

LHC BLM System Data

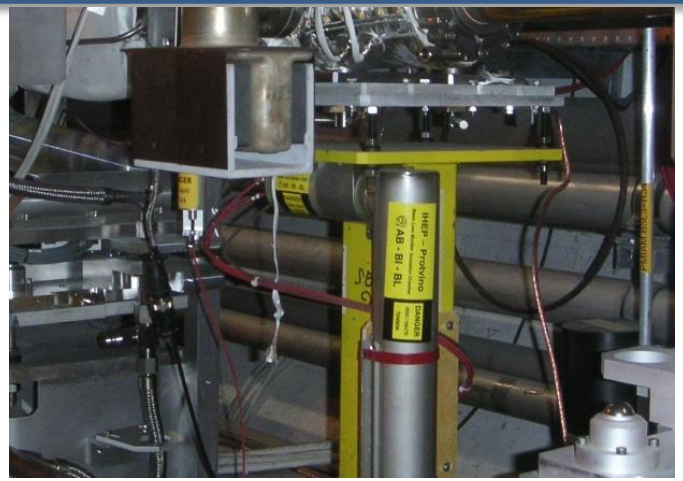
- High data volumes & multiple applications
  - 8.6 billion records/day , 100’000 variables, 300 GB/day
- Recording at 1Hz in a Logging DB via a Data Concentrator
  - Measurements and Thresholds used
  - System statuses and diagnostic data



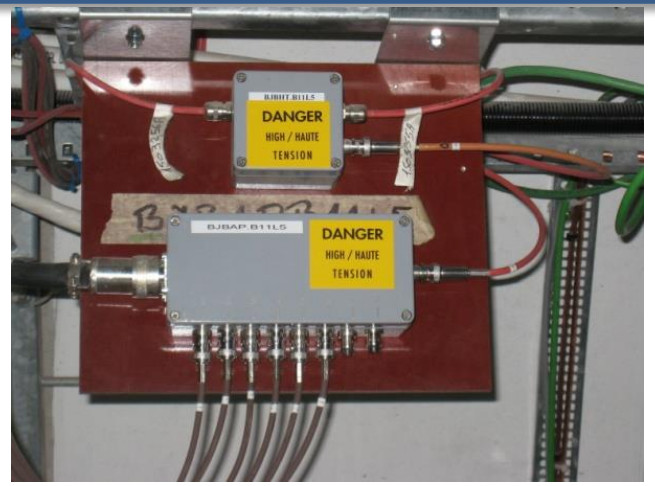
- Designed system monitoring processes to **protect** and **predict failures** from degradation and aging
  - System is self-tested continuously
  - Automatic external regular checks



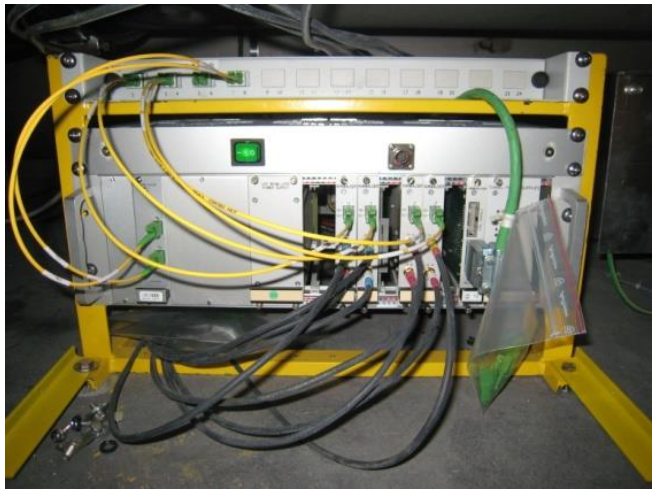
LHC Tunnel Installation



Detector positions



Signal and HV distribution



ARC electronics

DS & LSS electronics

Future Specifications Summary

- Equal/similar specifications needs for SPS and LHC
  - Deployment at LHC during LS4, i.e. after validation in SPS
  - Harmonisation across the Accelerator Complex with two systems to maintain (PS Complex and LHC/SPS systems)
    - Reduce effort in procurement, testing and spares management
- Main functionalities
  - Radiation tolerant electronics up to 1 kGy
  - 10 µs acquisition period & real-time processing
  - 8 orders of dynamic range (from few pA to 1 mA)
  - On-board diagnostics and telemetry
  - Bidirectional communication with the acquisition electronics

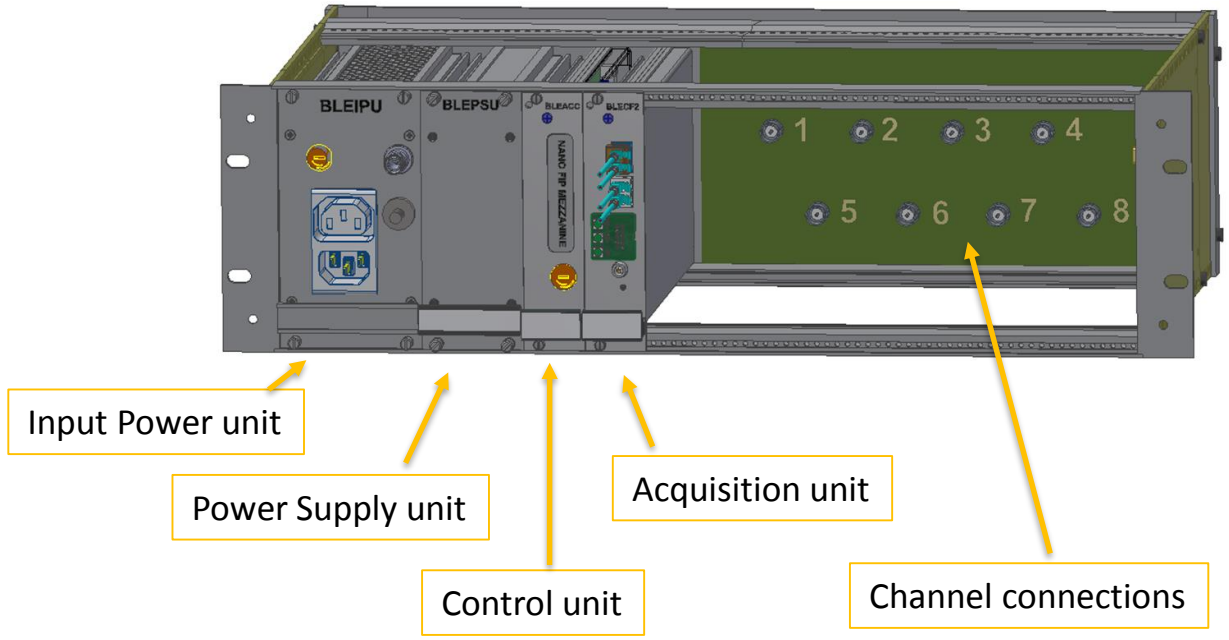
Deployment Strategy

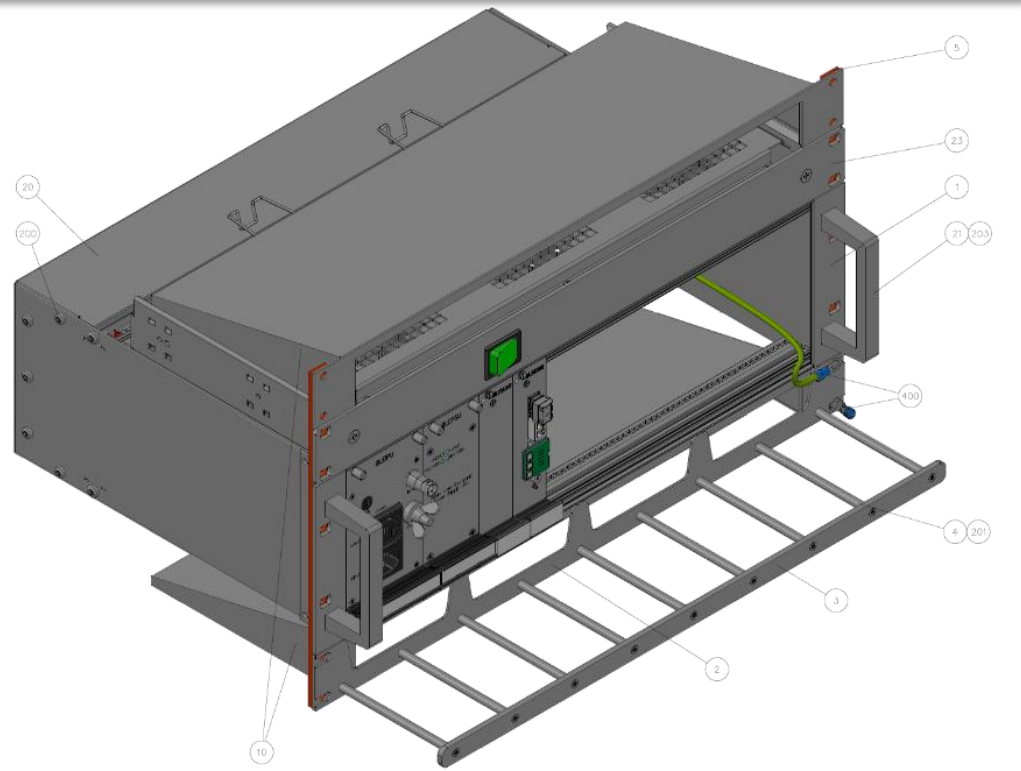
- LS3 populate SPS Ring with new system
  - New crate with standard CFC v2 module
    - ARC: front end in the tunnel with fibre connection
    - LSS: copper cables from the detector to the surface.
  - Some locations to be populated with the BLMASIC for development.
- LS3 upgrade processing electronics at LHC
  - First step for the system consolidation
  - Temporary use of fibre optic elements (adapters and SFP receivers)
- LS4 upgrade acquisition electronics at LHC
  - Deploy new crate and CFC v2 at the LHC tunnel
  - Deploy in parallel BLMASIC modules in strategic locations
    - Aim for the new triplets and long cables at collimation areas
    - Acquisition electronics in the tunnel

DEVELOPMENT PROGRESS

Acquisition crate (SPS)

- First functional version of the crate ready including power supplies and backplane
- Working on the remote control card (via nanoFIP) and acquisition modules





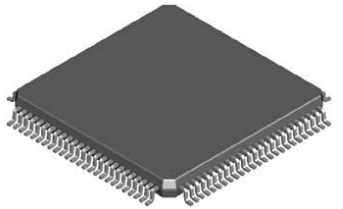
All connections from the front side
Electronics enclosed in a mini-rack

Acquisition Electronics

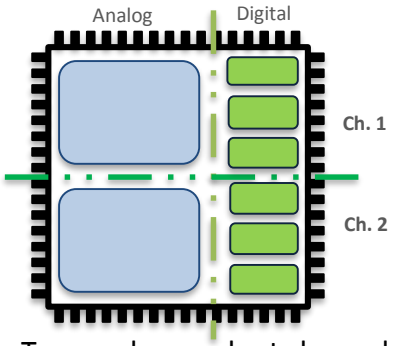
- Two distinct designs on-going
  - BLECF v2 (upgrade) with distinct components (COTS & ASIC)
  - BLMASIC encapsulating both analogue & digital functions in rad-hard ASIC
- Commonalities pursuit
  - Size and form factor, i.e. one cartridge of 6HP
  - Backplane connection and power scheme
  - Communication (lpGBT & SM-VTRx)
  - Acquisition frequency and range
- Additional advantages (TBC)
  - Interchangeable where necessary
  - Main processing blocks common

BLMASIC: Current-to-Frequency or Δ/Σ Converter

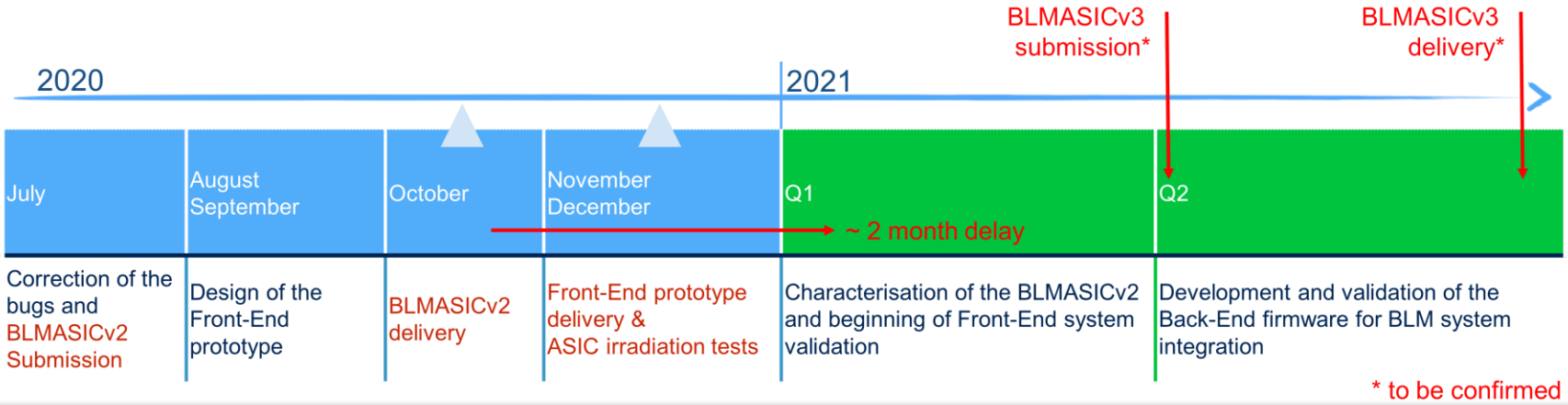
- Two analogue-to-digital converter circuits under investigation:
  - Current-to-Frequency (CFC) & Δ/Σ converter
  - v2 achieved linearity and low current measurement specs
  - Preliminary results from x-ray irradiation exceeds specs
- Next version (v3) will focus on the CFC type only
  - Address ESD, power and minor digital part issues
- Some delays due to COVID-19
  - Dependency on foundries and packaging of the devices



Standard 64-pin Quad Flat Package (10x10 mm)



Two analog readout channels per chip (4x4 mm)

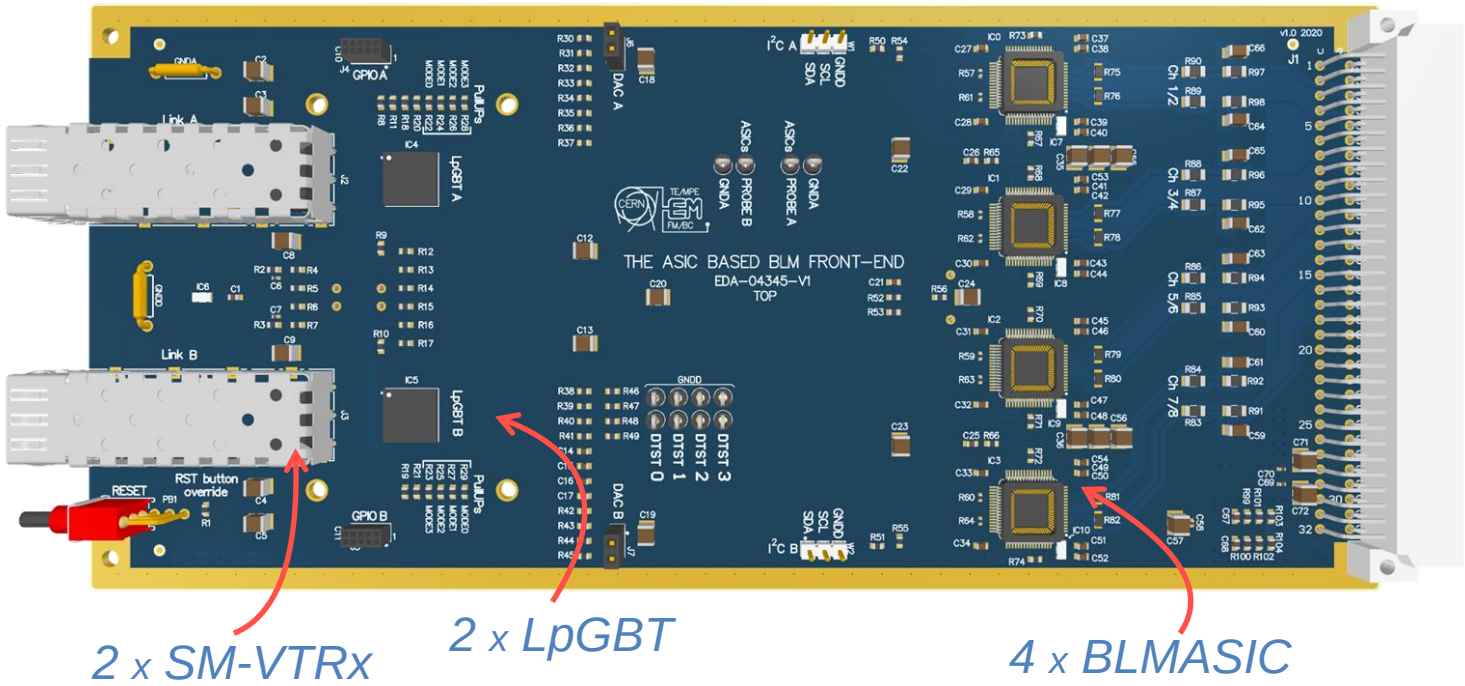


BLEIC: Printed Circuit Board Prototype (1/2)

New prototype PCB design complete

- Includes all functionalities expected from the final system
- Can accept any of the two analogue-to-digital converter circuits under investigation:
  - Current-to-Frequency
  - Δ/Σ
- Common digital parts, control and form with standard BLM acquisition board.
- Secured prototypes of the other custom parts, e.g. the SM-VTRx and LpGBT.

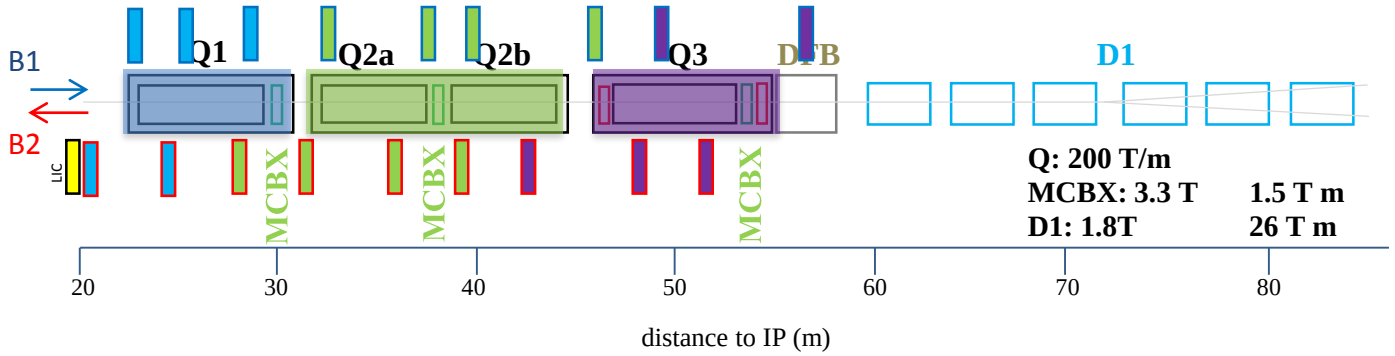
Currently at production a variant able to accommodate both BLMASIC v2 & v3



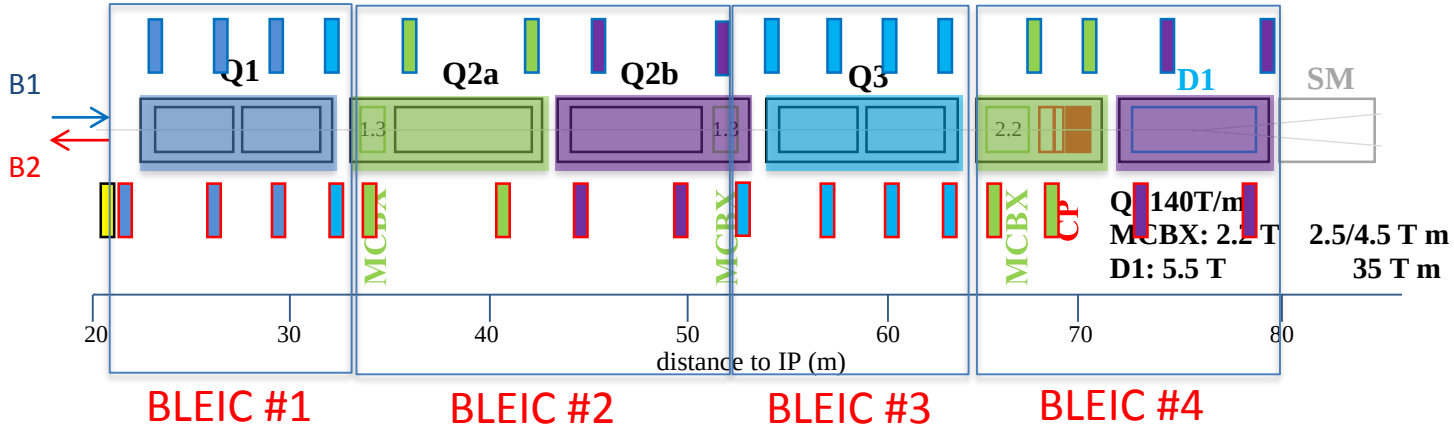
BLEIC: LS3 Triplet Layout BLM detectors

Work in progress

LHC triplet layout



HL-LHC triplet layout



Option 2: BLECF // (BLEIC/2)

Half channel redundancy

Number of detectors: IP-side			
	Present System Run 3	HL-LHC Upgrade Run 4	New in Run 4
BLECF – standard	18	32	14
BLEIC – new	0	**16**	16
subtotal	18	48	30

Number of detectors: IP1 + IP5 (both sides)			
	Present System Run 3	HL-LHC Upgrade Run 4	New in Run 4
BLECF – standard	72	128	56
BLEIC – new	0	**64**	64
Total IP1+IP5	**72**	**192**	**120**

1 multiwire cable / module
1 BLEIC module = 8 channels

RAD-TOL/HARD COMPONENTS

BLECF v2: Current-to-Frequency Converter

Specifications

- ☑ Reliability level SIL3 (1E-7 to 1E-8 failure/h)
- ☑ Measurement range 2.5pA to 1mA
- ☑ Input protection
  - Current ~ 10A @100us
  - Voltage ~ 1500V @100us
- ☑ Test features for system check
  - Survey of the card voltage supplies
  - Survey of detector high voltage supply

- ☒ Radiation tolerant up to 500 Gy
  - Increase to ~ 1 kGy
- ☒ Integration time of 40 µs
  - Decrease to 10 µs
- ☒ Redundant optical data transfer to surface
  - Redundant bidirectional link
  - Add control over fibre

LHC acquisition module (BLECF)

Components

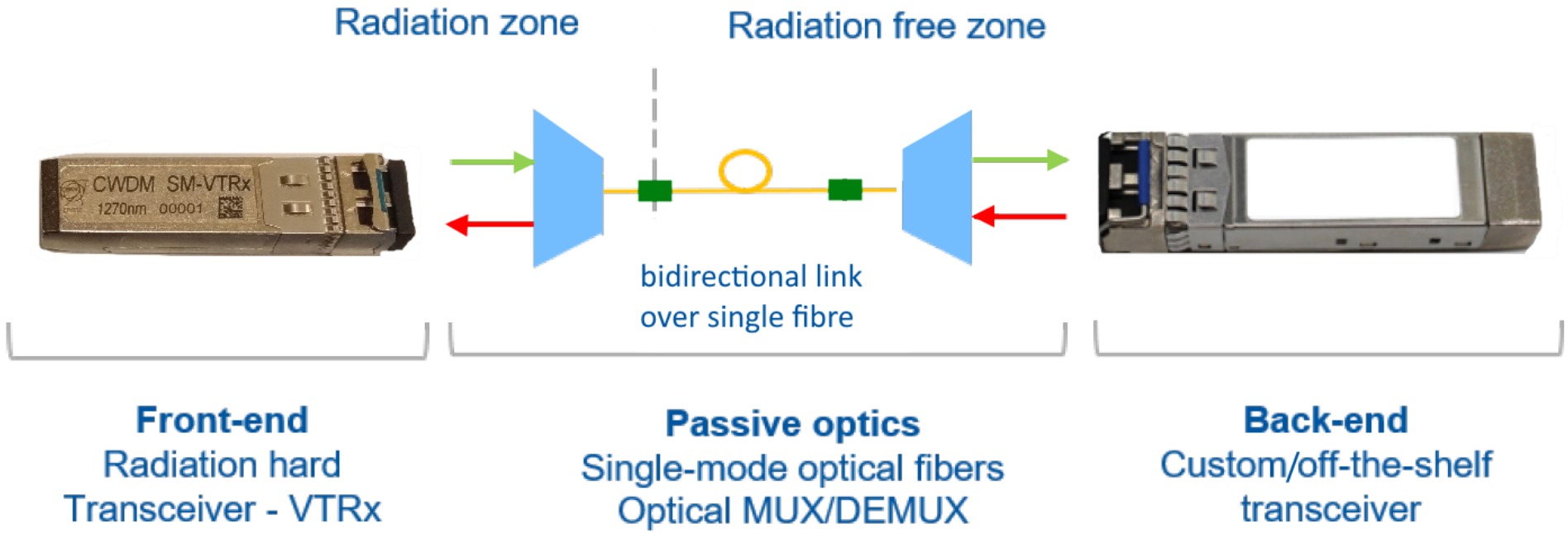
- 8 inputs Current-to-Frequency Converter (COTS)
  - ➢ Op-Amp: OPA627 -> OPA657, LTC6268, LTC6244
  - OneShot: 74HC123 -> 74LS123, 74HCT12
  - Comparator: NE521
  - Switch: J176 -> searching for new JFET or MOSFET
- AD41240 ADC (EP-ESE) ➢ No alternative found; new production - done
- LM4140 voltage reference ➢ Searching
- Antifuse FPGA for data collection ➢ Aim to deprecate
- Redundant GOH from CMS (EP-ESE) ➢ Replace with LpGBT & SM-VTRx
- CRT910 Line driver (EP-ESE) ➢ New ASIC to design & produce
- AD5346 DAC ➢ New DAC or SCT from LpGBT

Rad-hard components

- Produced the AD41240 ADC
  - Necessary due to End of Life (EOL) for CMOS6SF (250nm) products
  - 24 wafers produced and stored at EP-ESE long-term storage (~25 kpcs)
  - To be packaged and tested when we give the green light (some additional costs)
- Reserved
  - lpGBT (2640 pcs – includes 20% spare)
  - SM-VTRx (3200 pcs – incl. 30% spare)
    - Order under preparation for the transmitter part (i.e. TOSA)
- Missing/searching
  - Voltage regulators (e.g. LHC7913 and LHC4913 from STMicroelectronics)
  - See presentation from William
- Open requests (need designs to advance further)
  - SCE (for slow control and additional diagnostics)
  - Level shifters for ADC connections (EP-ESE to design & produce with 1 year warning)
  - FPGA (for data collection and control)

Optical Link Configuration

- Bi-directional communication over single fibre with wavelength multiplexing
- Radiation qualified components
- New version of SM-VTRx packaged as SFP module
  - Note, pins don't follow SFP standard



CONCLUSIONS

Summary

- Consolidation (with additional functionalities) of the BLM systems at SPS and LHC is being planned
- Equal or similar functional needs
  - Deployment at SPS in LS3 & LHC in LS4, i.e. after validation in SPS
  - Harmonisation across the Accelerator Complex with two systems to maintain (i.e. the PS Complex and the LHC/SPS systems)

    Pro: Reduce effort in procurement, testing and spares management

    Con: Complex design effort with more parameters to account for.
- Main functionalities
  - Radiation tolerant electronics up to 1 kGy
  - 10 µs acquisition period & real-time processing
  - 8 orders of dynamic range (from few pA to 1 mA) measurements
  - On-board diagnostics and telemetry
  - Bidirectional communication with the acquisition electronics

Acknowledgements

- ADC & other rad-hard ICs:
  - Kostas Kloukinas
  - Alessandro Marchioro
- BLMASIC:
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  - Luca Giangrande
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  - Paulo Moreira
- SM-VTRx
  - Jan Troska
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  - Salvatore Danzeca
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  - Daniel Ricci

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THANK YOU