Report from TF7

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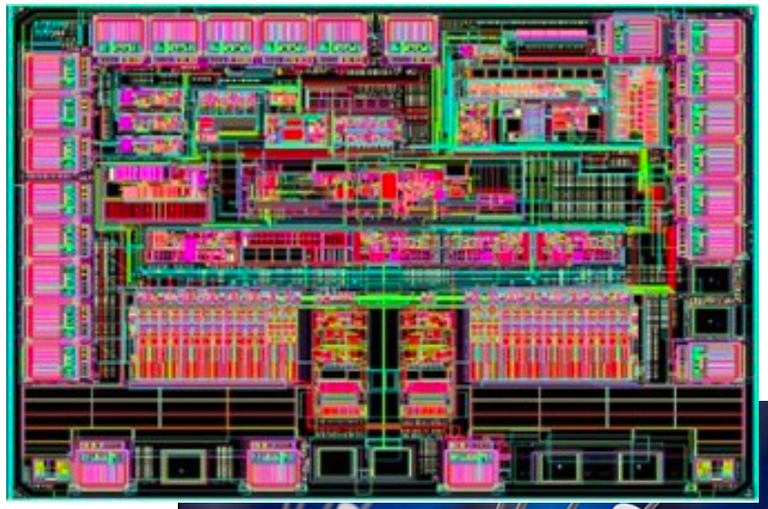
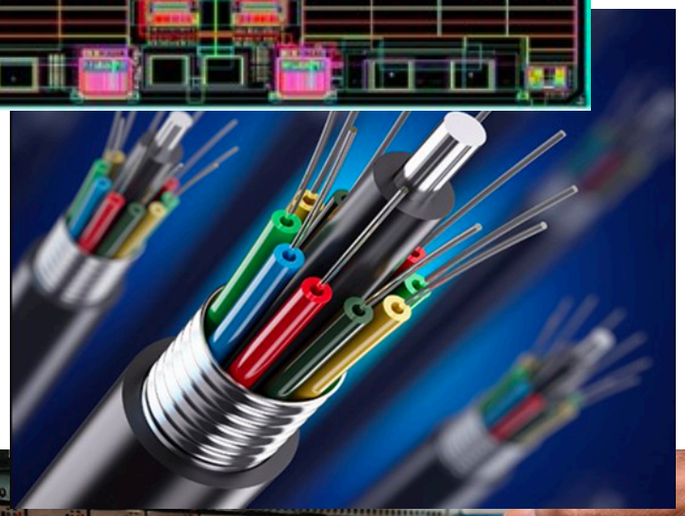
Organisation

- Electronics is a vast area
- What was in:
  - Theme 1: On-detector ASICs and components ('the front end')
  - Theme 2: Links, powering, integration ('the middle end')
  - Theme 3: Data processing, control and acquisition ('the back end')
- What was out:
  - Sensors (-> TFx)
  - Cooling, mechanics, integration (-> TF8)
  - Offline computing and online software (-> ???)
- Software is a major challenge, do not ignore!
  - Vast and increasing amounts of effort in this area
  - Direct effects on detector and readout design
- Systems aspects considered from the start
  - Can no longer treat the three themes as independent topics
  - What is 'back end' today may be 'front end' tomorrow





Information Gathering

- Input sessions
  - Informative talks by wide range of future activities
  - Electronics requirements usually given 'implicitly'; not much mention of back end
    - i.e. driven by assumptions on detector design – but sometimes meeting assumptions will be tough
  - Electronics and integration often considered side-by-side
- Questionnaire
  - Panel determined focus of survey, but also room for free commentary
  - Determined assault on our 38 highly focussed questions by the community
  - Broad consensus on many points
- Symposium
  - Day-long discussion (~300 peak attendance), great keynote / topical talks
  - Broad consensus formed on the key issues
- Key themes from the community inputs
  - There are huge challenges ahead for some future facilities
  - Much discussion about community organisation, collaboration, sociology
  - We need to find some new ways of working to deliver the next systems

TF7 Matrix

	Front end	L, P & I	Back end	
HL-LHC	🔴	🔴	🟢	
Long-baseline neutrinos	🟢	🔵	🟡	
ee collider	🔴	🔴	🟢	Clear driver / show-stopper for future work
Hadron collider	🔴	🔴	🔴	Important factor for future work - basic R&D needed
Muon collider	🔴	🔴	🟢	Relevant - incremental R&D needed
Other accelerator-based physics	🟡	🟡	🟡	Could be done today - modest R&D needed
HI colliders	🟡	🟡	🟢	Empty: not relevant
Non-accelerator physics	🔵	🟡	🔵	
Test beams, facilities	🔵	🔵	🔵	
Infrastructure and tools	🔴	🔴	🟡	
Collaboration	🔴	🔴	🔴	

- Note: a lot of red, no empty spaces – electronics underlies ~everything

Requirements of Future Facilities

- Evolution of detectors (esp. inner tracking, calorimetry)
  - Finer spatial granularity -> more data, more processing, more power
  - Precise timing -> more data, more processing, more power
  - Closer coupling of readout to sensors
  - Extreme radiation hardness (FCChh, MC)
  - Less material, less power, less cost, less integration complexity
- Readout methodology
  - Much talk of 'triggerless readout', 'full data streaming', 'just keep it all', etc
    - For many detectors, this may lead to increases in material and power - c.f. the requirements above
  - #1 problem: power & readout bandwidth -> more intelligence on detector
- Rough 'political' summary
  - Energy frontier seems 'very hard' – but is also 'very far away' (?)
    - R&D to demonstrate feasibility, perhaps on brand new approaches
  - e+e- machines have major systems / optimisations demands
    - R&D towards integrated detectors subsystems meeting requirements
  - (Large) non-collider detectors have individual and unique challenges
    - R&D on clever ideas (which may be relevant to colliders later)

What are the Tools?

- Clear that we will inherit a lot from HL-LHC
  - Larger-scale integration than ever before (e.g. RD53 65nm ROC)
  - Use of high density electronics for calorimetry
  - Experience in development and application of precision timing
  - Software-based trigger / DAQ in COTS hardware
- How about industry?
  - In most areas, industry is far far ahead of us
    - We do not have reliable / guaranteed access to 'cutting edge' technologies
  - CMOS process proposed for near future HEP is 28nm (c.f. 7m FPGA, 5nm M1)
  - Detector links 10Gb/s, industry at > 25Gb/s (aggregated to >400Gb/s)
  - Most HL-LHC back end boards will use two-generations-old FPGAs
  - The costs and complexity of using the 'cutting edge' are unsustainable
    - At least, in our current model of working
- Who does the work?
  - For some technologies, rely fully on (consumer-driven) industry COTS
  - For others, may have to adapt our approach to commercial standards
  - For yet others, there is no industry alternative (ultra rad hard devices)

Findings: ASICs

- State of the art
  - 65 nm / 130 nm CMOS, radiation qualified by HEP
  - 50 ps timing capability (much lower in specialised TDCs)
  - Channel count, density, noise, rad hardness all improving incrementally
- Future challenges
  - More channels, more radiation, less mass, less power
- Future technologies
  - One node will not fit all requirements, probably need a few standards
    - 'Advanced node' at 28 nm or smaller; 'Cheap node' at 65 nm or larger; CIS node for pixels
    - Radiation qualification for < 28 nm transistor structures will be needed
  - 3D integration is now becoming routine in industry
    - Both to solve density issues and allow coupling of dissimilar technologies
    - 3D integration and low mass structures routinely used in consumer mobile electronics
  - More complex ASICs will require programmability / configurability
    - 'FPGA like' or 'CPU like' systems *may* allow a net power reduction on the detector
    - There will be compromises in complexity, design time and tool complexity

Findings: Links, Powering and Integration

- State of the art
  - 10 Gb/s multimode optical links, 0.65 W, 2e15 n/cm^2
  - Power densities > 10 kW/m^2, DC-DC / serial powering
  - Channels at > 10 k/cm^2, 50 um thinned assemblies, micro channel cooling
- Future challenges
  - More (much more) data density -> more efficient power usage
    - So secondary effects on converters, power system complexity, cooling, etc
  - Compatibility with commercial standards and equipment (Ethernet…)
  - Find more radiation tolerant onto technology
- Future technologies
  - More advanced optolinks (silicon photonics, WDM, beyond NRZ)
    - Photonics requires intense R&D on new packaging and test techniques
  - Low-power, low-mass electrical links for 'first metre'; wireless links?
  - High-efficiency, high-reliability devices for power systems (GaN / SiC)
    - Plus standard IP blocks for powering and power control
  - Redundancy features, long-term reliability assessment, qualification…

Findings: Back End

- State of the art
  - Large amounts of high-density FPGA-based electronics for trigger / DAQ
    - Quite a lot of 'data movement' functionality
  - New systems using newer co-processing tech (GPGPU)
    - Yet more modern tech (inference accelerators, ML offload, etc) not yet in the game
  - Combination of COTS network and custom links – different domains
- Future challenges
  - Moving intelligence (AKA data selection / reduction) close to the front end
  - Keeping pace with industry developments, getting technology access
    - We are tiny players compared to the computing 'hyperscalers'
    - Raw processing power per $ is vast, but hard to exploit without significant expertise
- Future technologies
  - Tighter integration of front-end with processing
    - Including adoption of AI / ML techniques where appropriate
  - Use of COTS network and processors on the detector
  - Huge increases in firmware and online software complexity

Cross-Cutting Issues

- Current situation
  - Ambitious advances made for HL-LHC (with significant prior R&D)
  - Not all developments have been successful or efficient
    - Often due to external factors, but also failures in design / verification steps
  - Significant duplication of effort, even with single projects
- Some key 'organisational' factors for future success
  - Concentration of expertise, whilst allowing the whole field to contribute
    - The 'Tier centres' model, e.g. for ASIC developments
  - Systems engineering approach, from the start
  - Adoption of standard high-quality tool chains and development practices
  - Exploitation of experience from outside HEP (via our groups and labs)
  - Skills, training and careers support – our people are highly 'stealable'
  - Open developments, common developments, cross-project standards
    - We no longer have the luxury of internal competition or single points of failure in groups
  - Focussed interactions with industry through central contact points

R&D Recommendations: ASICs

- A high granularity pixel readout chip with high resolution timing (10-100 ps) and charge measurement in 28 nm CMOS, with highly programmable features
- Integration of 'intelligent' signal processing features in detector readout chips
- Readout structures for monolithic sensors
- Study LGAD/AC LGAD and MPGD / RPC timing chips with 1-10 ps timing
- 3D integration technologies for high density interconnection of stacked layers of sensors and readout electronics
- Imaging/dual calorimeter readout chip for Si/SiPM readout
- Cryogenic readout chip for imaging LAr calorimetry
  - And other LAr applications…
- Integration of readout ASICs with silicon photonics (high readout bandwidth)
- CMOS nodes beyond 28 nm (FinFET, gate-all-around transistors) for digital and mixed-signal applications: radiation hardness, analog performance,...

R&D Recommendations: Integration

- Powering
  - Consolidate DC-DC and serial powering technology based on the operating experience of the HL-LHC experiments
  - Maintain serial powering expertise
  - Explore GaN technology, characterise radiation tolerance and investigate novel circuit topologies
  - Minimise the form factor of DC-DC converter modules
  - Transfer power IP blocks to small feature size transistor technologies
  - Explore unconventional power distribution schemes (power over fibre, wireless power transfer)
- Links
  - Investigate commercial standards for on-detector and off-detector links
  - Build expertise in applications and capabilities of photonic links
  - Develop photonic integrated circuit (PIC) common platform for HEP community, including design kit, IP blocks and EDA tools
  - Co-package ASIC, PIC and fibre
  - Investigate use cases and technologies for wireless signalling
  - Further recommendations under study

R&D Recommendations: Back End

- Technologies for readout and control
  - Precision timing distribution and fast control
  - Triggerless / timestamped / asynchronous readout for maximum efficiency
  - Standardised on-detector networks with redundancy
- Intelligence on the detector
  - Investigate feasibility of open programmable fabric IP and toolchain
    - For application in rad hard front end ASICs; low power but no need for high performance
  - Continued R&D towards advanced data reduction / pattern recognition on detector
- Develop new open community standards
  - IP interfaces, common IP blocks, communication protocols
  - Common modular electronics formats, both on and off detector
- Keep abreast of industry developments: 'back-end Openlab'
  - High-end COTS networking (400 GBE+, SDN) used in 'atypical modes'
  - Improved mass storage and memory technologies
  - Tracking of offload and accelerator technologies

Final Points

- Novel developments
  - Space must be made for responsive / radical / blue skies developments
    - These are the 'interesting parts' that keep our best people with us
  - Continuous horizon scanning is required – this means real work and real money
- Software and firmware
  - Software and firmware underlie all new developments
  - A 'development revolution' is needed, as for offline software 20 years ago
- Detector integration
  - TF7 and TF8 are largely studying the same topic
  - Electronics and mechanics have to be co-developed as a single system
- Organisation model
  - TF7 favours a (expanded, modified) 'CERN RD' collaboration model
  - Combination of short-lived and ongoing developments is necessary
  - Sponsorship, infrastructure, funding, career support: responsibility of major labs
    - Ideas and work are everyone's responsibility!
  - Need to return to open HEP-wide collaborative developments as the norm

What Next?

- TF7 draft report 90% complete
  - Will need shortening / editing for consistency
- Now seek to confirm with other Task Forces:
  - Missing elements of R&D
  - Requirements of detector systems not captured so far
  - Optimal co-development model for sensors and electronics
  - Opinions on prioritisation and timing of R&D from sensor point of view
- The overriding message
  - Success of electronics for LHC may have 'made it look easy'
    - It wasn't
  - For *all* future projects, it will certainly not be easy
    - Need to substantially increase electronics effort to maintain expertise and technology access
  - Please keep electronics limitations / costs / drivers in mind when planning for future detector R&D
  - Please consider co-development of sensors and electronics as the default