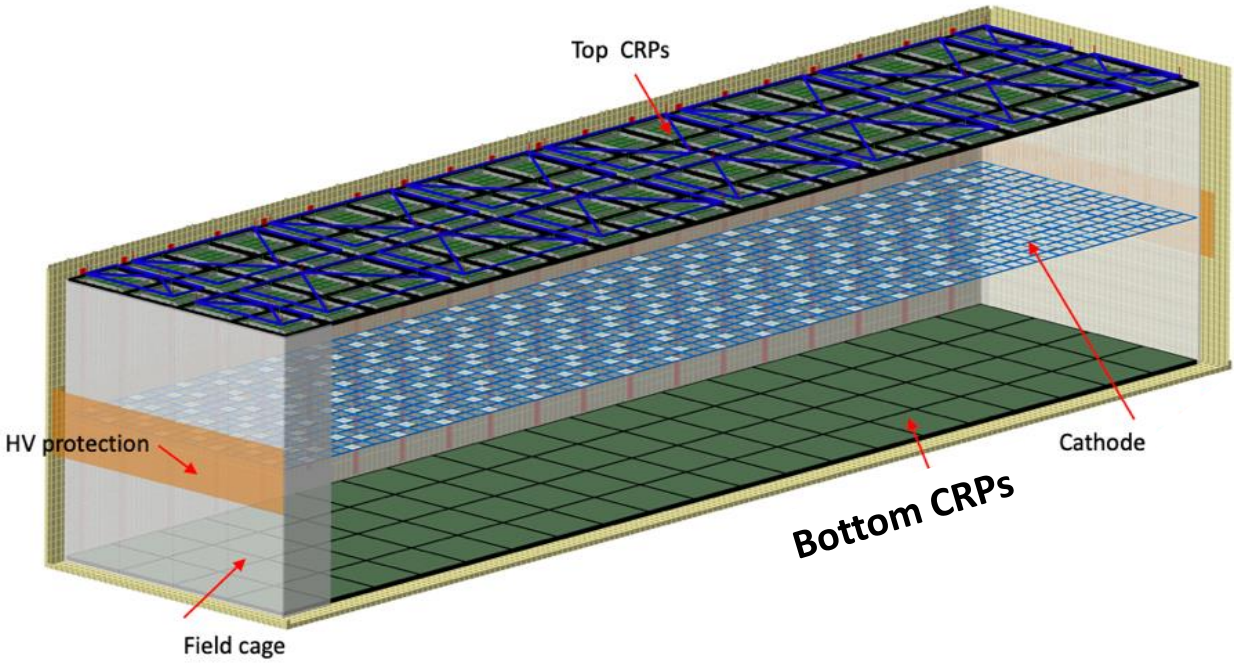
Bottom Electronics Overview and Requirements

Cheng-Ju Lin (Lawrence Berkeley National Lab)

Conceptual Design Review for Bottom CRP Electronics (FD2-VD)
28 May 2021

Bottom Cold Electronics



Scope:

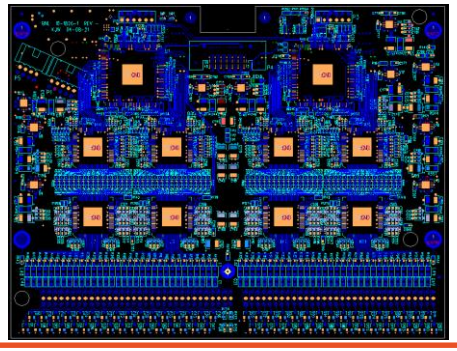
- Responsible for the electronics to read out 80 CRPs at the bottom of the cryostat
- Penetration and warm electronic crates
- Power supplies (including bottom CRP bias and FC termination) and DDSS

Bottom Cold Electronics

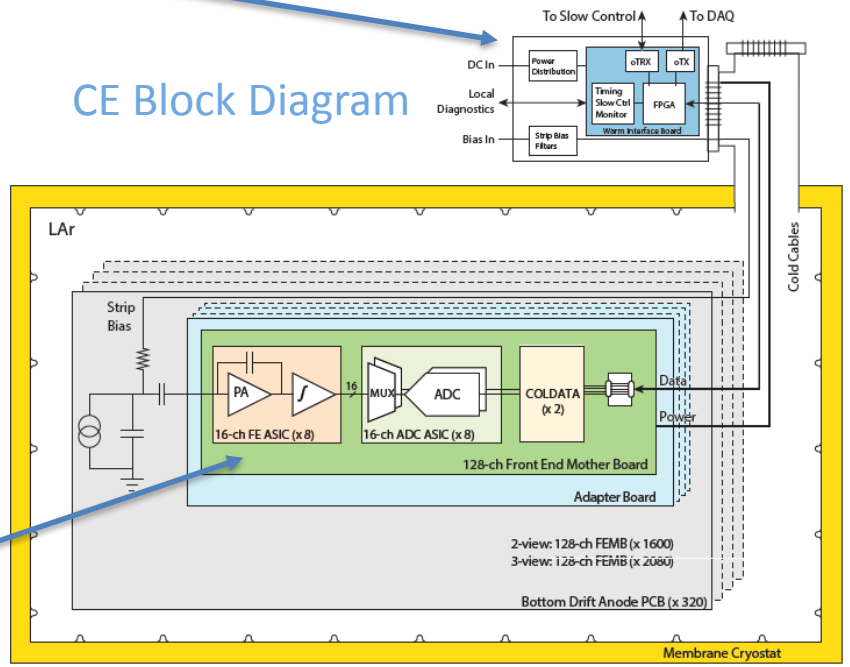
- CE requirements are similar between HD and VD
- Final version for FD1-HD will also be the ~version for FD2-VD
- Frontend motherboard (FEMB) with 3 types of ASICs to readout CRP strips
- FEMB mounted on the CRP to minimize noise. Digitized signal sent over long (~25m) cable to the warm electronics on top of the cryostat

Warm Interface Board

Monolithic FEMB with 3-ASICs :
LArASIC+ColdADC+COLDATA

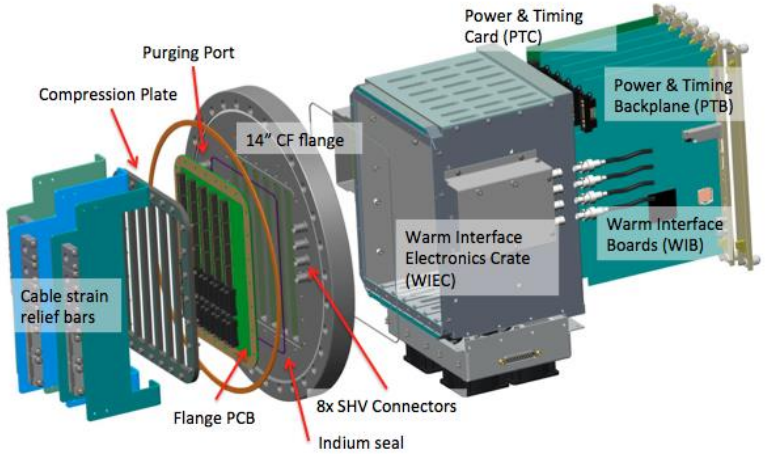


CE Block Diagram

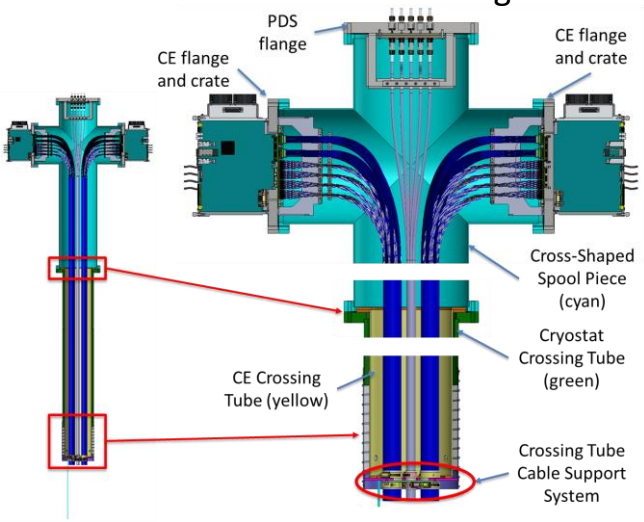


Warm Electronics

Warm Electronics Assembly

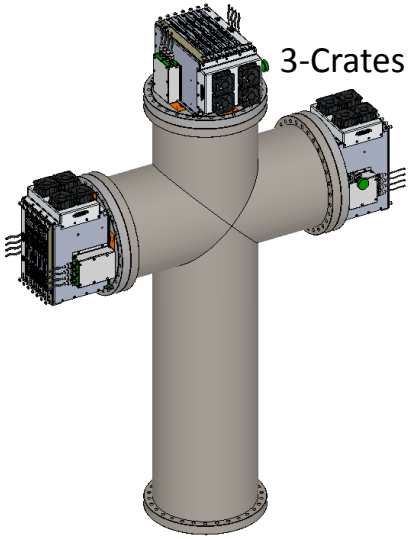


2-Crates Configuration



	DUNE SP LArTPC (half drift)	Vertical Drift 3-view config
LV supplies	25/2	17
Bias voltage crates	5	4*
Bias voltage channels	450 (+208 FC)	160
DDSS panels	30	18
Cryostat penetrations	75/2	40
WIECs	75	100
WIBs	375	520
PTCs	75	100

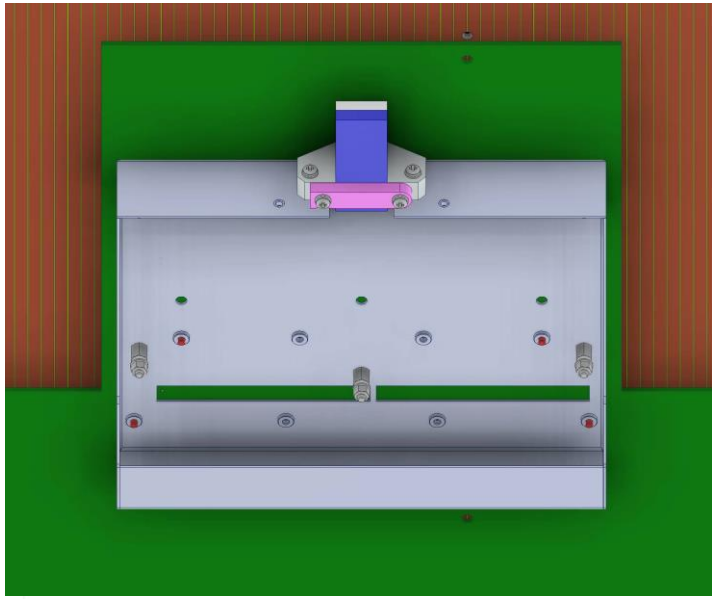
3-Crates Configuration



* Bottom CE also provides bias voltage to the field cage termination electrodes

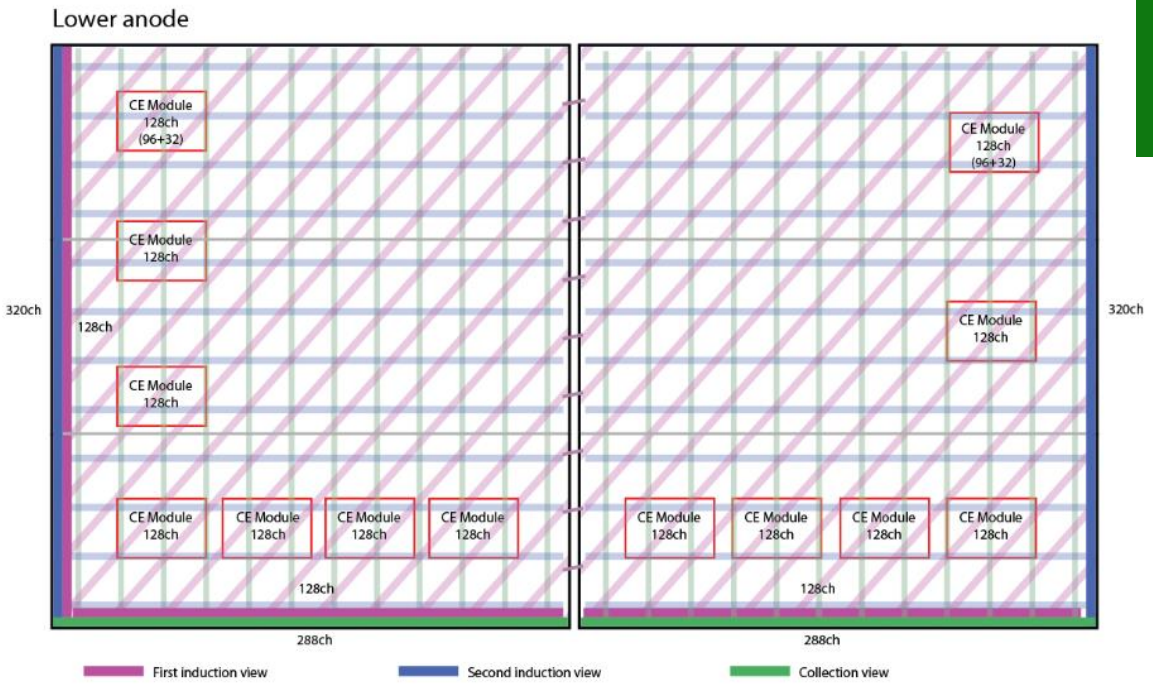
FEMB Layout on CRU (3-view design)

- Each CRU pair has 1600 channels
- Read out with 13 128-channel FEMBs
- 64 unused channels per CRU



FEMB Mounting Concept on the CRP Interface Board

Placement of FEMB on CRU

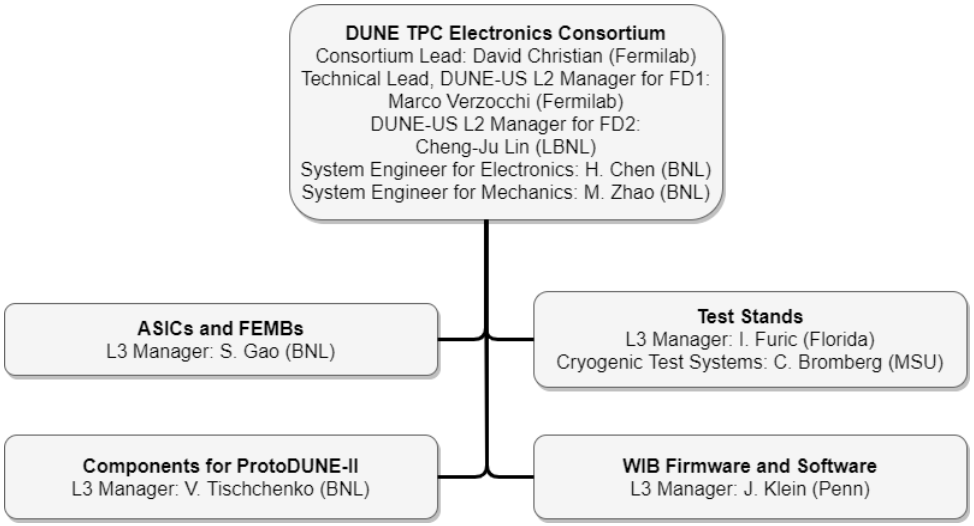


Possible CE Changes for FD2-VD

- Plan to keep design changes relative to FD1-HD to minimal
- CRP Consortium expressed concern about the weight of the CE boxes. For FD2-VD, will use aluminum CE box instead of SS to reduce weight
- Explore the possibility of connecting FEMB cables at the CRP Factory:
  - CRP installation is dominated by cabling (~4 tech/hrs per CRP) and testing (~1.5 hrs)
  - Have the FEMB cables pre-installed significantly simplifies the CRP installation inside the cryostat at SURF. Less fixture, manipulation and testing needed
  - Connect short cables from FEMBs to a patch panel on the side of CRP
  - May need a version of FEMB with a different connector
  - Prototyping and testing ongoing. See Manhong and Shanshan's talks for details
- Cryostat penetration design may need to be modified to accommodate Photon Detector System and maybe also the FC support system
- If White Rabbit Timing System is used for FD2-VD instead of the FD1-HD Timing system, significant modification to the warm electronics is needed. See Marco's talk on "Warm infrastructures"
- A request to change the CRP strip size. A change for CRP not CE. See Marco's talk on "Interfaces"
- Most other changes are minor (e.g. WIB firmware update for channel maps)

Institutions for FD2-VD Bottom CE

- Expect most (if not all) institutions involved in FD1-HD CE to continue in similar roles for FD2-VD
- QC test stands from FD1-HD will be re-used
- ASIC/FEMB testings: BNL, FNAL, LBNL, MSU, LSU, UC-Irvine, Cincinnati, Florida, Iowa State
- WIB/PTC hardware, firmware, and software: BNL, Florida, U. Penn
- Cold Cables: BNL
- Mechanical: BNL, CSU
- Power supplies and Detector Safety System: BNL, FNAL
- Integration and Installation: BNL, FNAL, LBNL
- Recruiting more institutions (e.g. UC-Davis, Hawaii, SLAC, etc.) to help out with above and additional online/offline software tasks



Bottom CE Requirements

Executive Board held requirements for FD1-HD are also valid for FD2-VD

TDR ID	Name	Primary Text	Value
SP-FD-2	System noise	The total system noise seen by each wire should be no more than 1000 enc of noise. It is expected that random noise on the FE amplifier will be the dominant contribution to the total system noise.	<1000 electrons
SP-FD-13	Front-end peaking time	The FE peaking time shall be set so as to optimize vertex resolution.	1 microsecond (goal: adjustable to be able to take advantage of lower noise if the noise depends on peaking time)
SP-FD-14	SP signal saturation level	~500,000 electrons	~500,000 electrons (goal: Adjustable so as to see saturation in less than 10% of beam-produced events)
SP-FD-19	ADC sampling frequency	The ADC sampling frequency shall be set so as to extract maximal information without unnecessarily increasing data rate.	~ 2MHz
SP-FD-20	Number of ADC bits	The ADC shall digitize the charge deposited on the wires with 12 bits precision	12 bits
SP-FD-21	SP cold electronics power consumption	The SP CE power consumption shall remain below 50 mW/channel	< 50mW/channel
SP-FD-25	Non-FE noise contributions	All non-FE noise contributions shall be much lower than the targeted system noise level	<< 1000 electrons

Bottom CE Requirements

- Most consortium held requirements for FD1-HD are also valid for FD1-HD
- Combination of requirements, design choice and specifications

TDR ID	Name	Primary Text	Value
SP-ELEC-2	Gain of the SP TPC elec. front-end amplifier	Gain of the front-end amplifier	10 mV/fC (adjustable in the range of 5-25 mV/fC)
SP-ELEC-3	SP TPC elec system synchronization	Maximum time difference between ADC samples on different wires	16 ns
SP-ELEC-4	Number of channels per SP TPC elec front-end motherboard	Number of channels in each front-end motherboard	128
SP-ELEC-5	Number of links between the SP TPC elec FEMB and the WIB	Maximum number and speed of links used for data transmission between the FEMB and the WIB	4 at ~ 1.28 Gbps
SP-ELEC-6	Nunber of SP TPC elec FEMBs per WIB	Number of FEMB connected to each WIB	4
SP-ELEC-7	Data transmission speed between the SP TPC elec WIB and the DAQ backend	Each WIB should transmit data to the DAQ backend at a speed of 10 Gbps	10 Gbps
~~SP-ELEC-8~~	~~Maximum diameter of conduit enclosing the SP TPC elec cold cables~~	~~Maximum diameter of conduit enclosing the cold cables while they are routed through the APA frame~~	~~6.35 cm~~

Bottom CE Requirements

- Additional requirements or specifications under consideration at the CE Consortium level
- Listing sample requirements here. See EDMS#2590797 for a complete list
- Data transmission:
  - FEMB can drive signal over cold cable > 25m (open eye diagram)
- ADC linearity requirements: INL, DNL and ENOB
- Warm interface crates, WIB, and PTC requirements:
  - WIB calibration
  - Clock jitter from WIB to FEMB
  - PTC output voltage ripple, etc.
- Power supply requirements:
  - Current and voltage requirements
  - Noise ripple, V/I readback rate, etc.
- Offline physics requirements:
  - ADC overflow logic
  - Double pulse resolution
  - Saturation recovery
  - Channel-to-channel cross talk, etc.

Bottom CE Risks

- Have started to evaluate bottom CE risks and mitigation plans
- A number of risks are already opened in the Fermilab risk registry

Project: LBNF / DUNE (6)

Uncertainty	RT-131-FD2-005	FD2: Fluctuations in the exchange rates cause variations of the costs of detector componen	100 %	-750 -- 750 k$	months	Open
Threat	RT-131-FD2-006	FD2: Single source vendor for CE components	10 %	1600 -- 3300 k$	8 -- 16 months	Open
Threat	RT-131-FD2-007	FD2: Insufficient un-costed labor at SURF for installation	50 %	97 -- 194 -- 292 k$	0 months	Open
Threat		FD2: Insufficient personnel to perform QC of cold electronic components during production	35 %	25 -- 50 -- 75 k$	1 -- 2 -- 3 months	Proposed
Threat		FD2: ASICs production delay	30 %	70 k$	0 months	Proposed
Opportunity		FD2: FEMBs are installed on the CRP without the CE boxes	5 %	220 k$	0 months	Proposed

- Will continue to define and refine risks associated with Bottom CE in the coming months

Summary

- FD1-HD readout electronics can be used to readout CRPs with “minimal” modifications
- Scope of the Bottom CE subproject is well defined. Some interface issues with other Consortia will need to be ironed out soon
- A joint FD1 and FD2 team of collaborators are contributing to the CE efforts
- Most FD1-HD requirements are applicable for VD with some additional ones unique to VD
- Also in discussion with I&I to formulate the installation plan at SURF
- System integration tests (See Serhan and Filippo’s talk) using the CERN cold box and NP02 to validate the design
- See rest of the talks in this Review for more details