FD2-VD Bottom CRP Electronics CDR: ASIC design status

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May 28, 2021

Fermilab DUNE

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- COLDADC Digitizer
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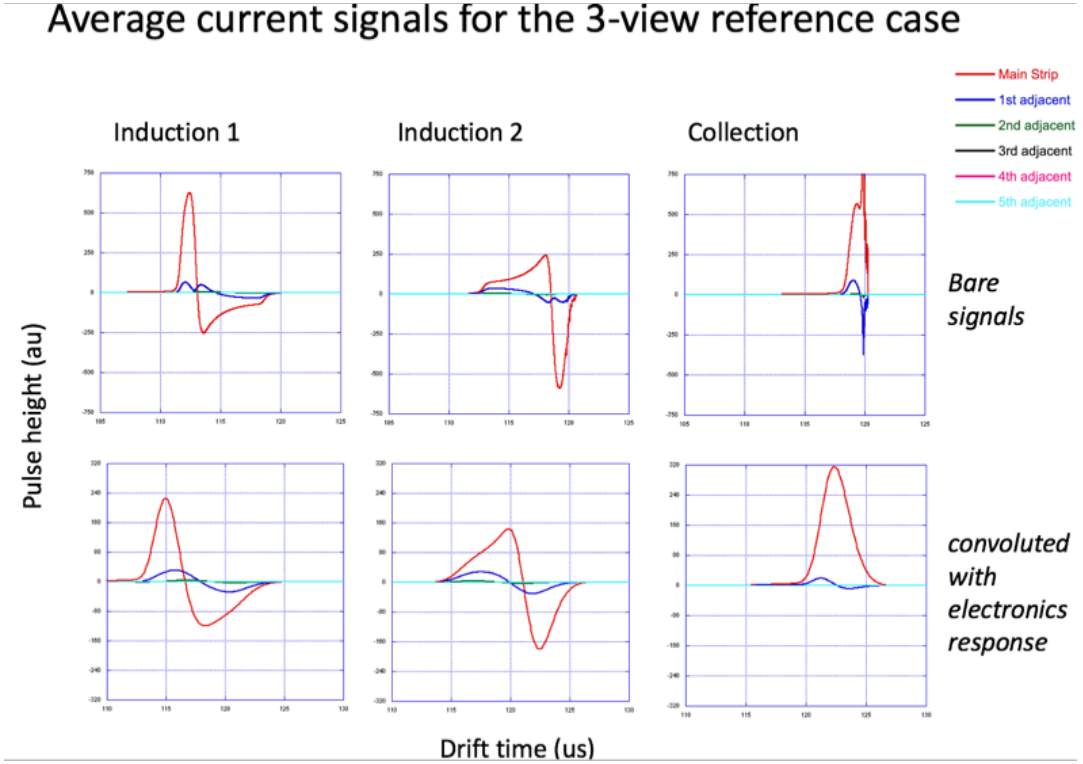
Comment on Vertical Drift

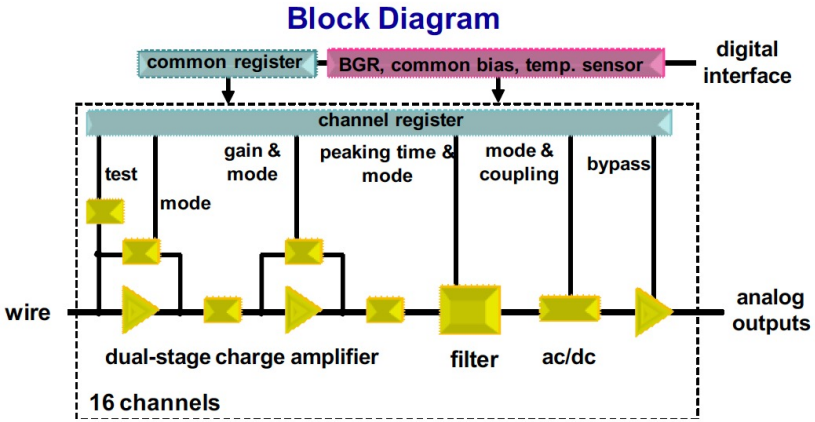
- The vertical drift charge readout plane anodes are being designed with the cold electronics developed for the APA-based horizontal drift TPC in mind.
- The printed circuit board hole size, board thickness, and the spacing between boards are chosen so that the induced currents will be similar to the currents induced in APA wires.

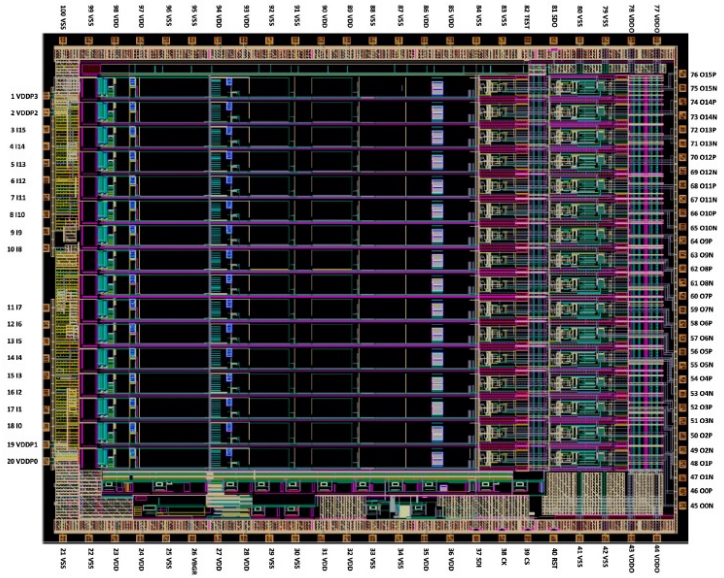
- Induced currents computed by Francesco Pietropaolo for one of the proposed 3-view anodes (show at last week's collaboration meeting)
- The electronics response used was LArASIC w/2 μs shaping time.



LArASIC_V5 (received May 2021)

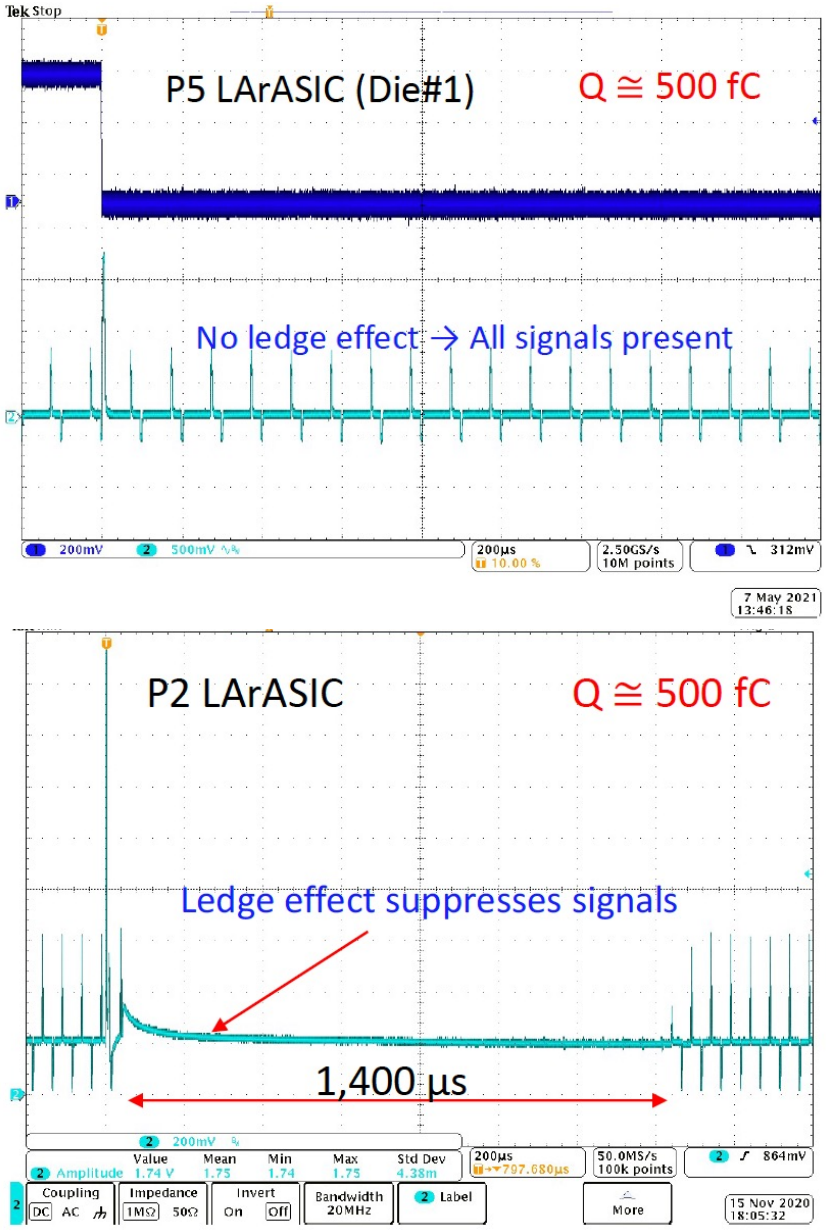
- LArASIC has been developed over a number of years and versions have been used successfully in MicroBooNE and ProtoDUNE-SP
- Changes since ProtoDUNE:
  - Eliminated “ledge” issue observed in ProtoDUNE.
  - Added a single ended to differential converter to allow optimal coupling to COLDADC.
  - Modified the band gap reference circuit to improve yield (~7% of LArASIC_P2 chips failed to start up at cryogenic temperature).
  - Modified the test charge injection pulser DAC to improve linearity for small signals while maintaining large dynamic range.





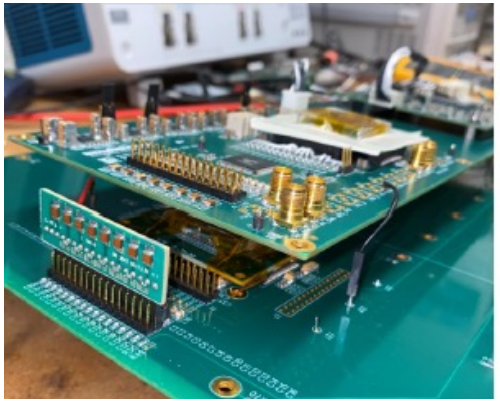
Ledge Effect

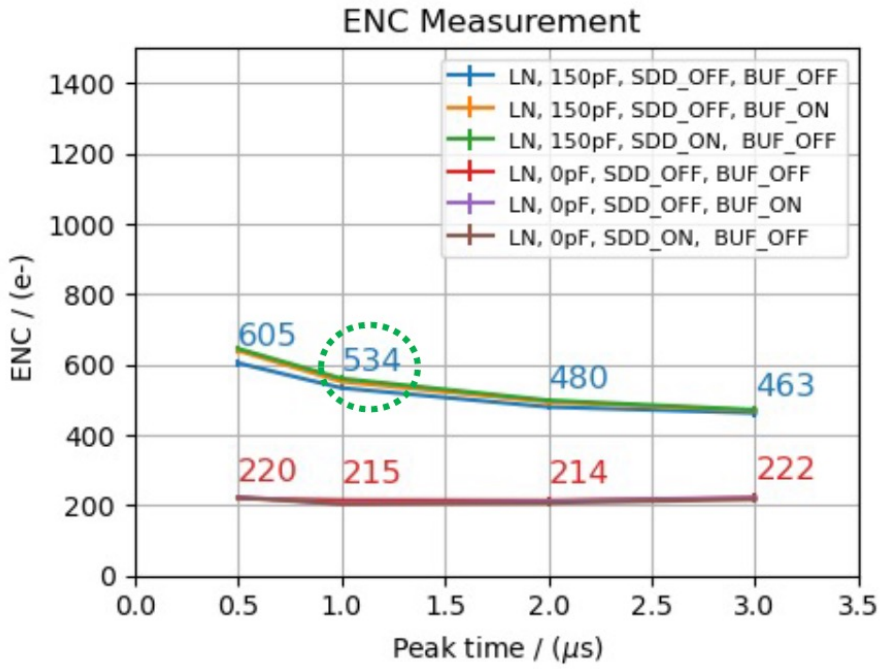
- Ledge Effect observed in ProtoDUNE-SP has been understood and eliminated.
- Test Method:
  - LArASIC internal calibration pulser is enabled (regular smaller amplitude signal)
  - Large charge pulse is injected into a normal input.



Single Ended to Differential Converter

- Tests using LArASIC_V5 and COLDADC_P2 have been performed.
- Good results obtained with both single ended and differential outputs.



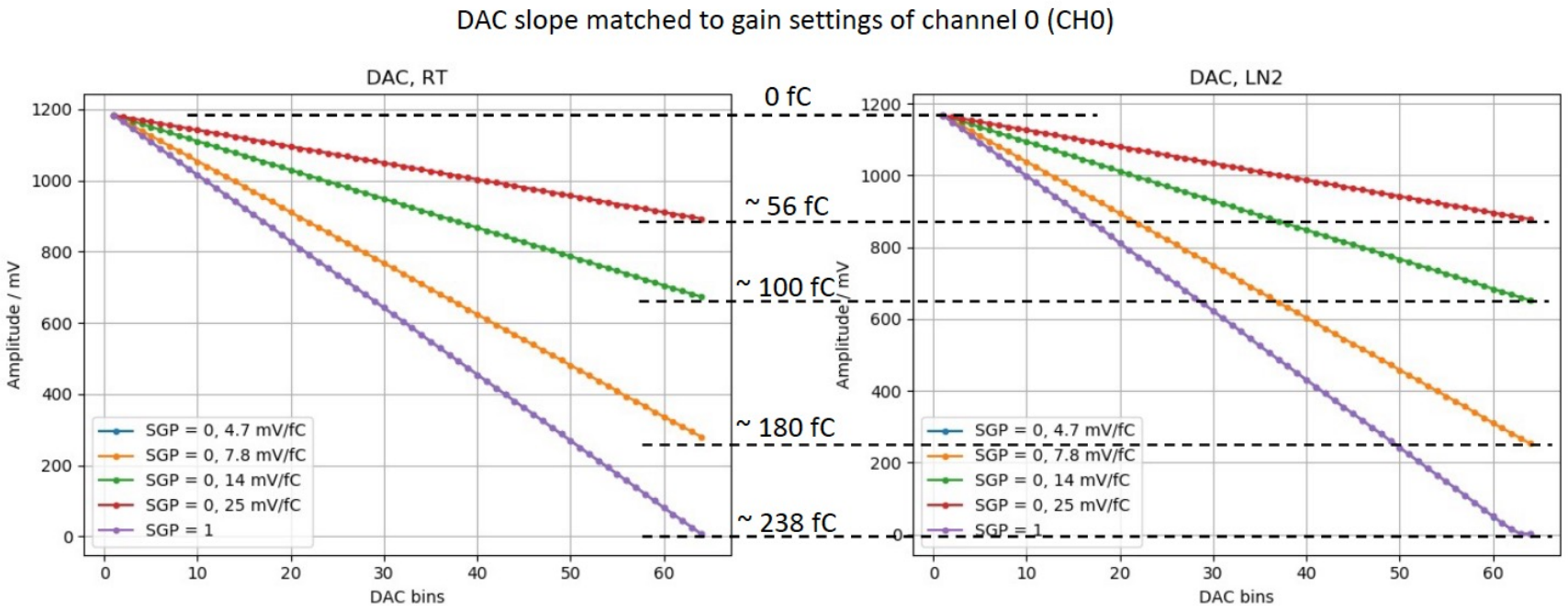


Band Gap Reference Circuit

- 7% of the LArASIC_P2 chips that were used in ProtoDUNE-SP and will be used in SBND fail QC because the band gap reference circuit fails to start when the chip is cold.
- The likely root cause of this failure was identified and corrected for LArASIC_V4.
- Validation of the fix will be possible later this year when ~150 packaged LArASIC_V5s will be tested before assembly on FEMBs.

Test Charge Injection Pulser DAC

Data from tests of LArASIC_V5



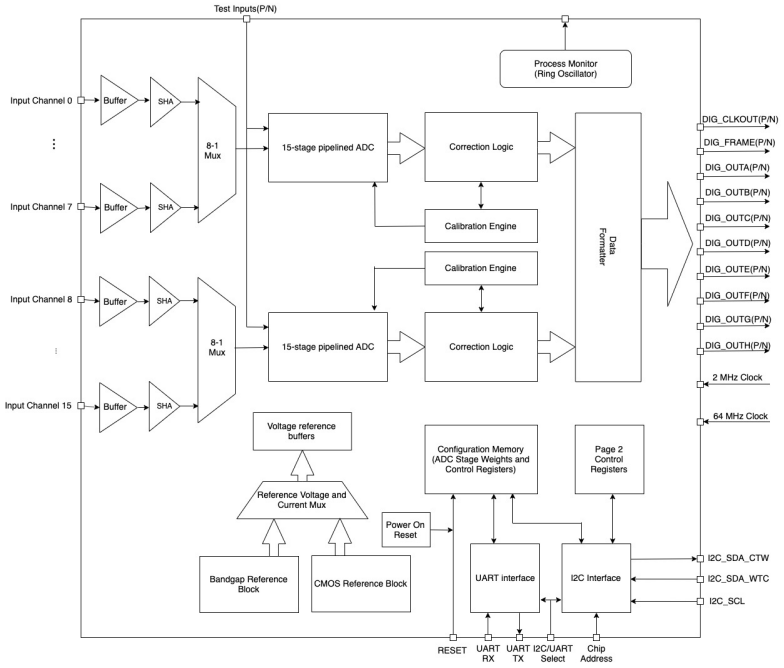
Monotonic and linear operation even for large charge injection

Summary

- LArASIC_V5 meets DUNE requirements for both HD & VD TPCs.

COLDADC_P2

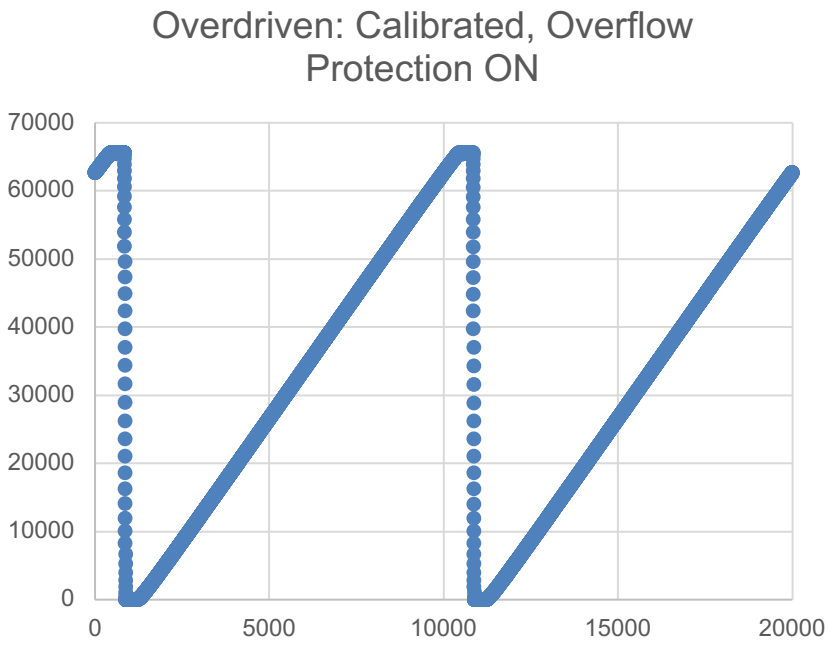
- First version of COLDADC was functional (& was used in the recent test of 3-ASIC FEMBs in ICEBERG), but a number of issues were addressed for COLDADC_P2:
  - Forgotten level shifters included in input buffer block
  - Power distribution improved & IR drop tool used in redesign
  - Bandgap reference Op Amp “flavor error” corrected
  - Automatic pipeline calibration logic fixed
  - Sample and hold multiplexer linearity improved
  - ADC data overflow detection & correction logic included
  - Power-on-reset added
  - Sampling clock control simplified

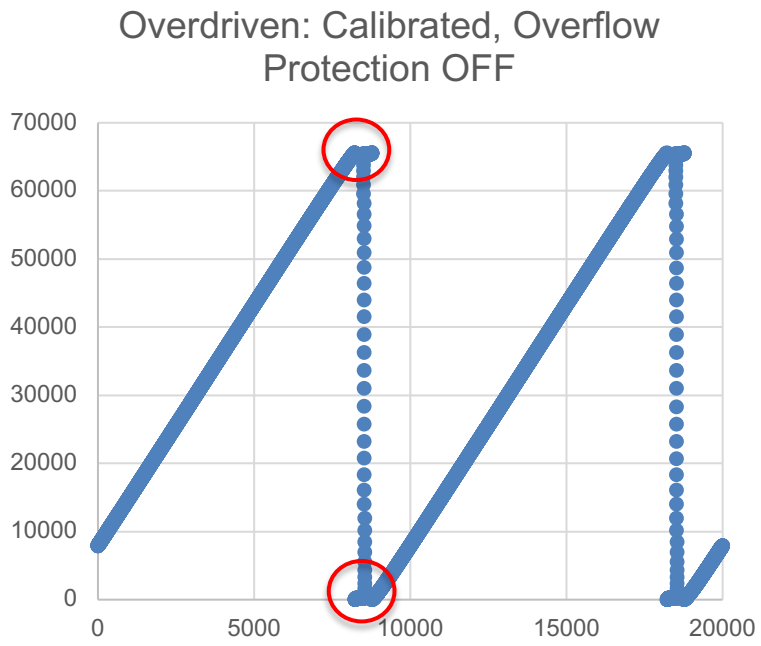


COLDADC_P2 Testing

- COLDADC_P2 operates as designed with nominal bias voltages (2.25V & 1.1V).
- Both CMOS and Bandgap reference blocks work as designed.
- Automatic pipeline calibration works.
- Small crosstalk associated with the sample and hold multiplexer has been reduced by more than a factor of 10.
  - crosstalk is now < 0.06%.
- All other design changes were successful.

Overflow Protection

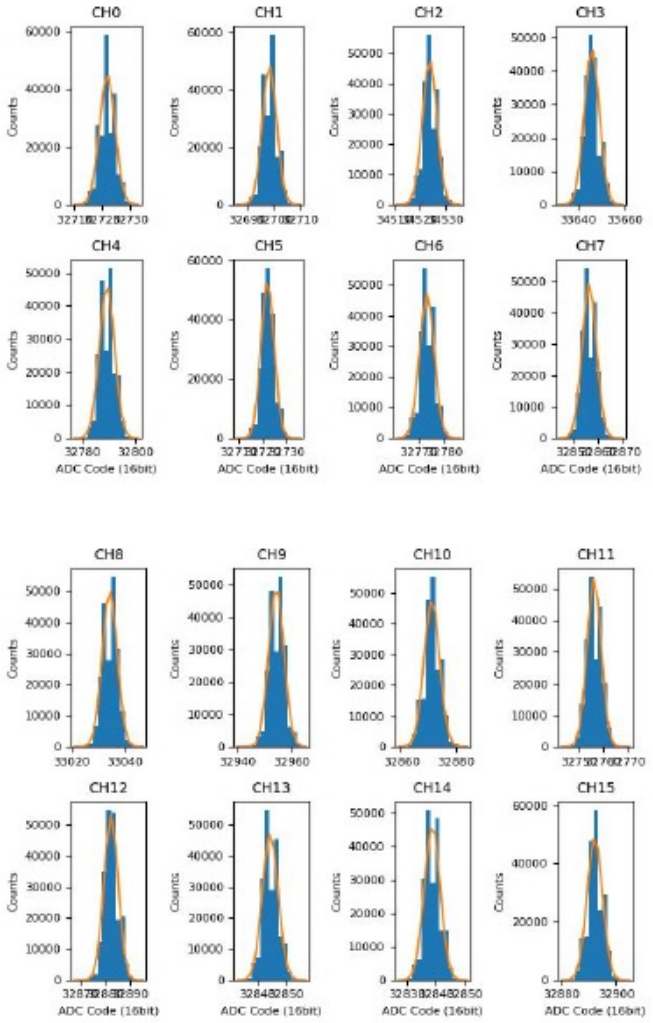




If the pipeline interstage gain is greater than 2, the output can exceed 16 bits. Correction logic is included to peg overflows at the maximum ADC value and underflows at the minimum ADC value.

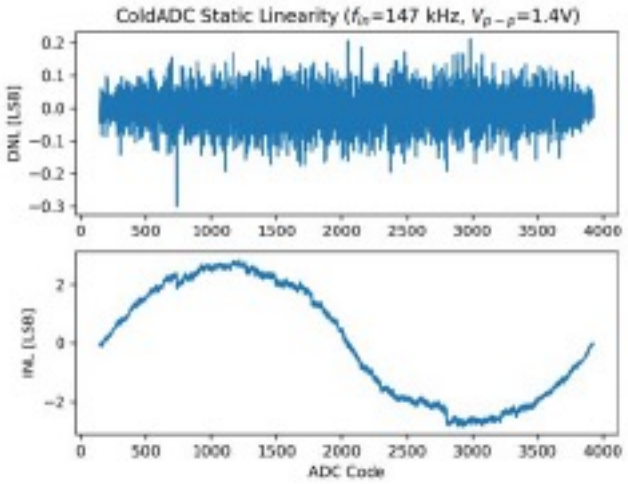
ADC Noise

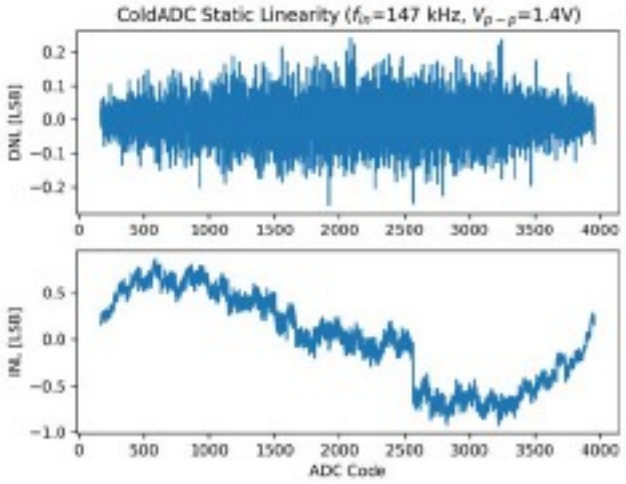
- COLDADC_P1 had very low noise.
- COLDADC_P2 also has very low noise.
- Measured noise with differential inputs at LN_2 temperature is ~ 130 μV rms (2.8 LSB 16-bit).



Static Linearity (DNL & INL)

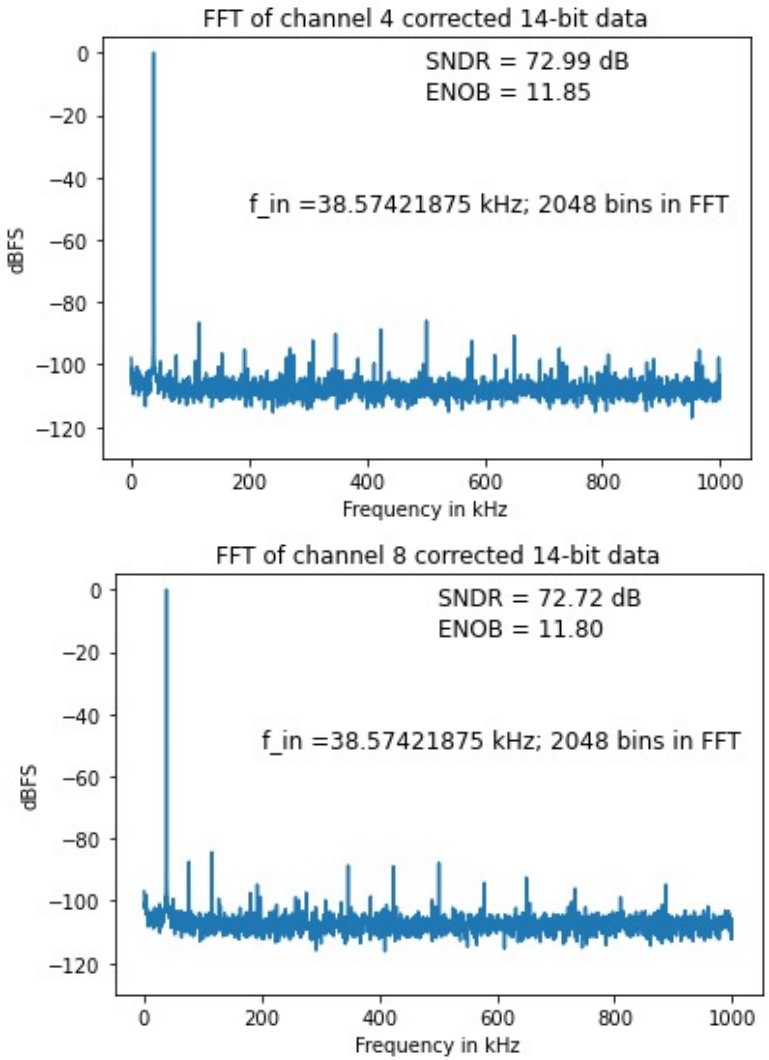
- Differential non-linearity is very good (typically less than +/- 0.2 LSB 12-bit; always much less than +/- 1 LSB)
- Integral non-linearity is not as good as expected.
- There are significant INL differences channel to channel.
- Chip to chip differences are smaller than channel to channel differences.
- Response is stable (doesn't change day to day or month to month).
- INL can be corrected with a simple polynomial fit.
- Source of non-linearity appears to be capacitor dielectric absorption.
  - See Carl Grace's slides.
- Since the non-linearity can be corrected, no redesign is planned.





Dynamic Linearity (SNDR/ENOB)

- After correction with a polynomial, dynamic linearity is very good, with little channel to channel variation.
- Our current measurements appear to be limited by our test setup and the linearity of our waveform generators.
- The measured ENOB is above 11 for input sinusoidal frequency up to 227 kHz

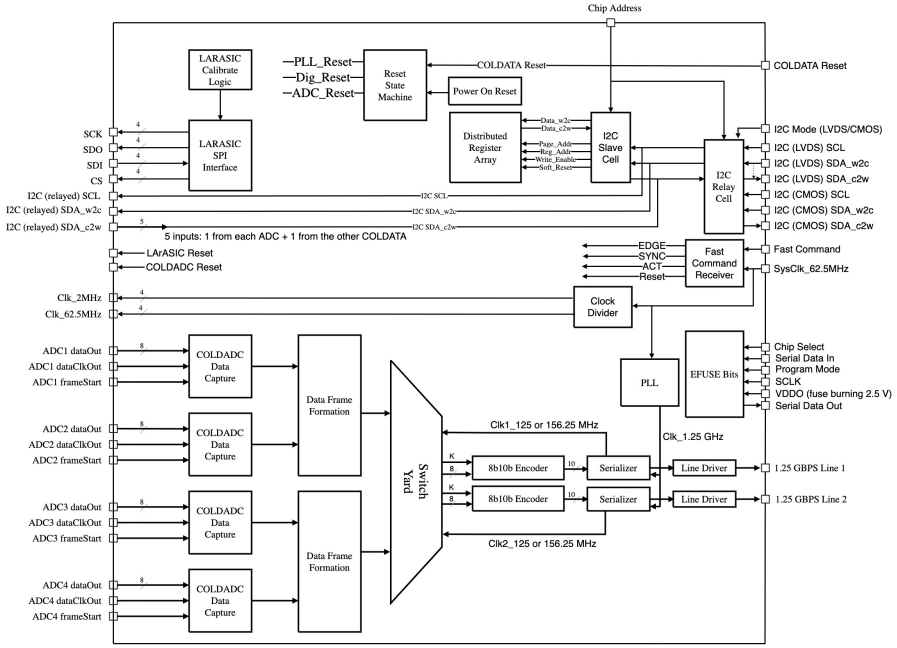


Summary

- COLDADC_P2 meets DUNE requirements for both HD & VD TPCs.

COLDATA Controller/Data Concentrator

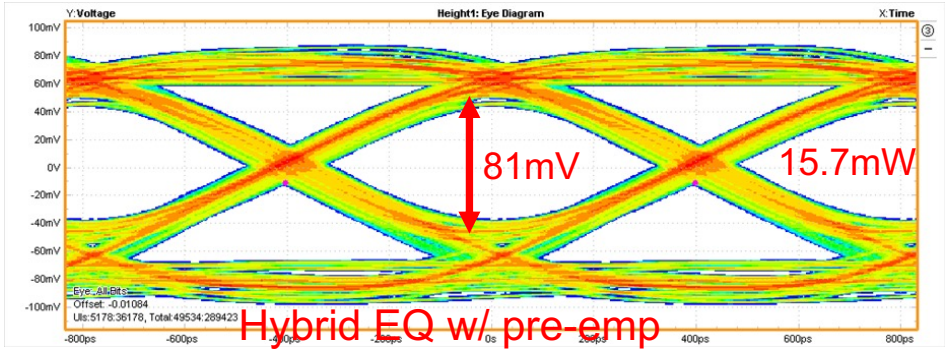
- The first full prototype of COLDATA (COLDATA_P2) was fully functional and is being used in systems tests.
- Minor bug fixes and a handful of new features were added for the current version.



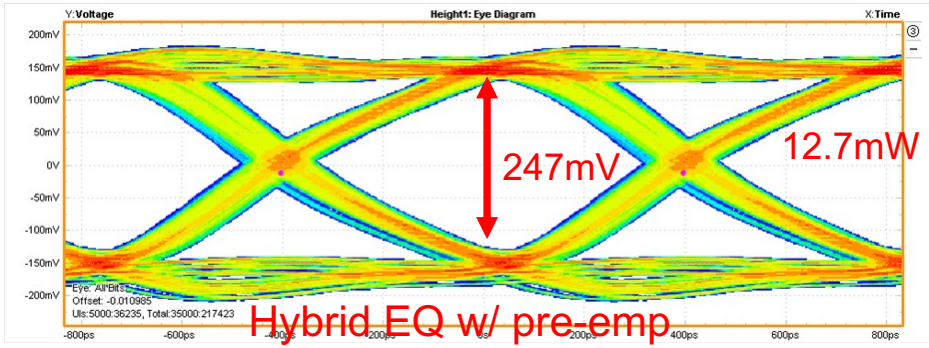
Ability to drive long cables

- The 1.25 Gbps hybrid-mode line driver is designed with current-mode transmitter equalization and voltage-mode pre-emphasis to drive 25-35 meter long twin-axial cables. The current-mode transmitter equalization circuit uses a finite impulse response (FIR) filter to distort the data pulse and compensate for the large frequency-dependent signal loss over a long twinax cable with low dynamic power consumption. The voltage-mode main driver and pre-emphasis circuit uses source-series-terminated (SST) output stages to provide a large output voltage swing and low static power consumption.
- The eye diagrams on the right were obtained from COLDATA_P2.

Warm 35m



Cold 35m



Eye diagrams for PRBS7

New for COLDATA_P3

- PLL
  - Now locks to 62.5 MHz system clock instead of dedicated 40 MHz clock.
  - 1st version failed to lock at room temp with 1.1V bias (required 1.17V at RT; locked at 1.1V when cold).
- I2C relay
  - 1st command to a new I2C address failed if it was a read
- Misc:
  - Timestamp now counts 62.5 MHz clock ticks and has been extended to 15 bits (16th bit used to indicate test pulse issued to LArASIC)
  - Registers used to control time between LArASIC pulse edges extended to 16 bits
- Additional functionality
  - Added a means to determine cable delay from WIB
  - Added 3 more general purpose I/O pads & made all 5 of these bits tri-stateable
- Procedure to read EFUSE registers made more user friendly
- Modified data frame structure to make WIB microcoding easier

COLDATA_P3 Testing

- PLL locks at nominal bias voltage both at room temp and cold.
- I2C bug was fixed.
- Almost all new features work as intended.
- Two minor bugs found:
  - All 5 general purpose I/O bits are shorted together
  - The LArASIC SPI clock is very asymmetric (still can program LArASICs)
  - These will be corrected before submission of engineering run

Summary

- COLDATA_P3 meets DUNE requirements for both HD & VD TPCs.
- The 5 general purpose I/O bits of COLDATA_P4 will allow more features to be included in the FEMB.

A Final Comment

- No change will be required to any of the ASICs in order for them to be used for the vertical drift detector.
- COLDATA can drive 35 m long twinax cables.
- The only thing we need to verify is that the signal integrity is maintained if a patch panel is included in the signal path.
  - Shanshan will discuss this in the next presentation.