BERKELEY LAB
Bringing Science Solutions to the World

U.S. DEPARTMENT OF ENERGY
Office of Science

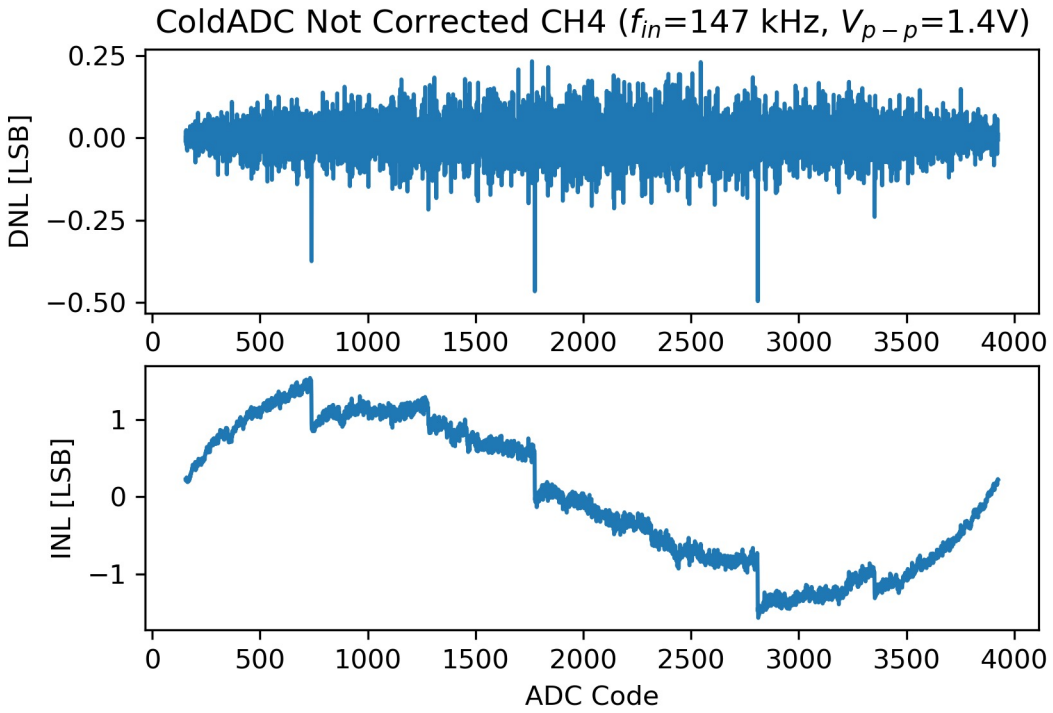
ColdADC Dielectric Absorption

C.Grace 11/23/2020

Lawrence Berkeley National Laboratory

Introduction

- While the raw linearity of ColdADC is good, it exhibits a marked structure



Results of tests are confusing and seem contradictory

Example:

- Increasing opamp and reference current doesn't help → not a settling issue
- Reducing temperature doesn't help → not a settling issue
- Slowing down the clock significantly helps performance → settling issue

- The 3rd-order characteristic appears to be distortion (supported by FFT)
- However, remedies to improve distortion don't help much (reducing reference voltages, increasing supply voltage)

Possible explanation consistent with observations → **capacitor dielectric absorption**
(also called dielectric relaxation and capacitor soakage in the literature)

EE Dielectric Absorption Literature

1550 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 25, NO. 6, DECEMBER 1990

The Effect of Dielectric Relaxation on Charge-Redistribution A/D Converters

JOHN W. FATTARUSO, MEMBER, IEEE, MICHIEL DE WIT, MEMBER, IEEE, GREG WARWAR, MEMBER, IEEE, KHEN-SANG TAN, MEMBER, IEEE, AND RICHARD K. HESTER, SENIOR MEMBER, IEEE

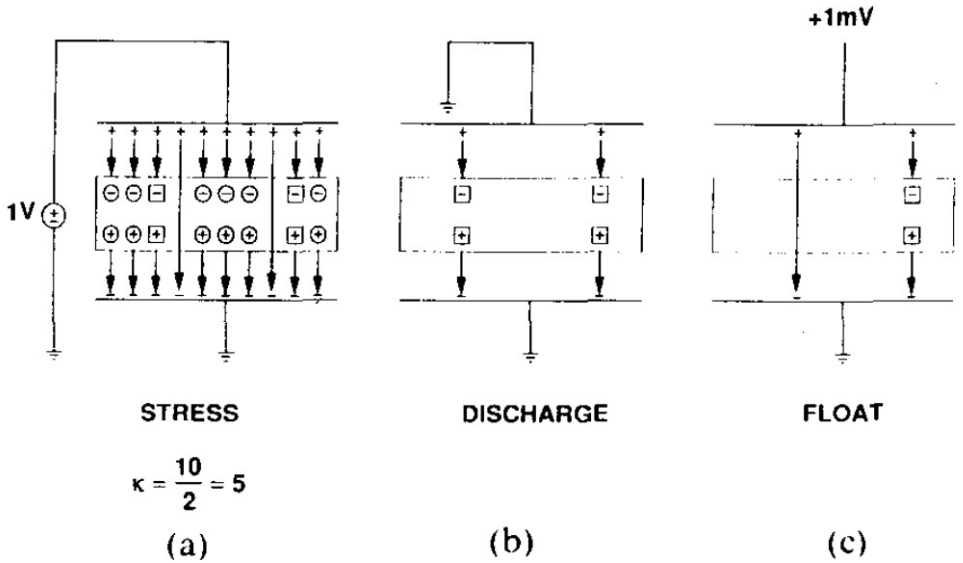


Fig. 1. Relaxation effect in practical dielectrics: (a) stress period, (b) discharge period, and (c) float period.

- In ideal capacitor, internal dipoles dissipate instantly when capacitor is reset
- In real capacitor, relaxation of dipoles takes time, and time required depends on the mechanism for charge displacement

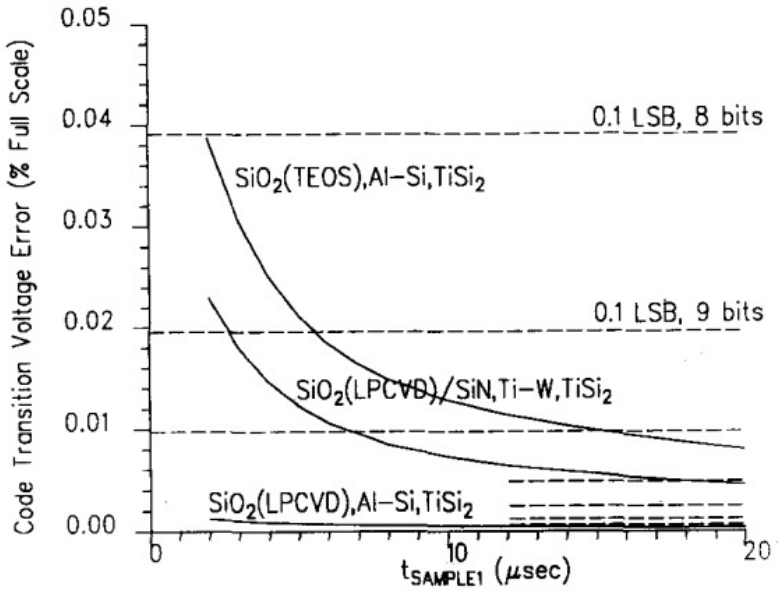


Fig. 10. Simulated code transition voltage error versus $t_{SAMPLE1}$ with three capacitor structures and $V_{IN0} = 0.001$ V, $t_{SAMPLE0} = \infty$, $V_{IN1} = 4.999$ V, $t_{BIT} = 330$ ns, and 10 b. Dashed lines correspond to 1/10 LSB errors for 8, 9, 10, 11, 12, 13, and 14 b.

Dielectric Absorption

*…some of the internal polarization may be due to physical charges accumulating on grain boundaries in a polycrystaline material, or to charges tunneling to surface states at a plate interface. The characteristic time constants associated with these dipoles may range from **nanoseconds** to minutes, or even longer.*

Fattaruso, et al., JSSC 12/90

- The MIMCAPs we used in ColdADC have very thin SiO_2 dielectrics included to save area, and so have a relatively large surface area-to-volume ratio, so likely have a lot of surface states.
- Higher density capacitors have thinner dielectric layers → more dielectric absorption
- Not modeled by the foundry for simulation

Dielectric Absorption

ANALOG DEVICES

AN-348
APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

Avoiding Passive-Component Pitfalls

The Wrong Passive Component Can Derail Even the Best Op Amp or Data Converter
Here Are Some Basic Traps to Watch for

by Doug Grant and Scott Wurcer

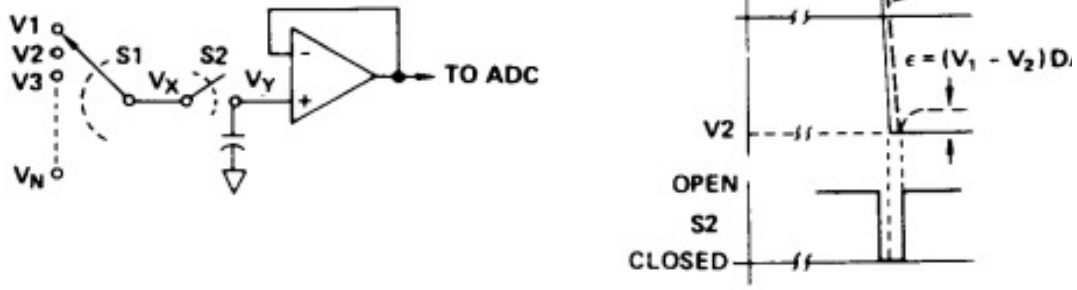


Figure 3. Dielectric absorption induces errors in sample-and-hold application.

Dielectric absorption can produce long tails in the transient response of fast-settling circuits, such as those found in high-pass active filters or ac amplifiers.

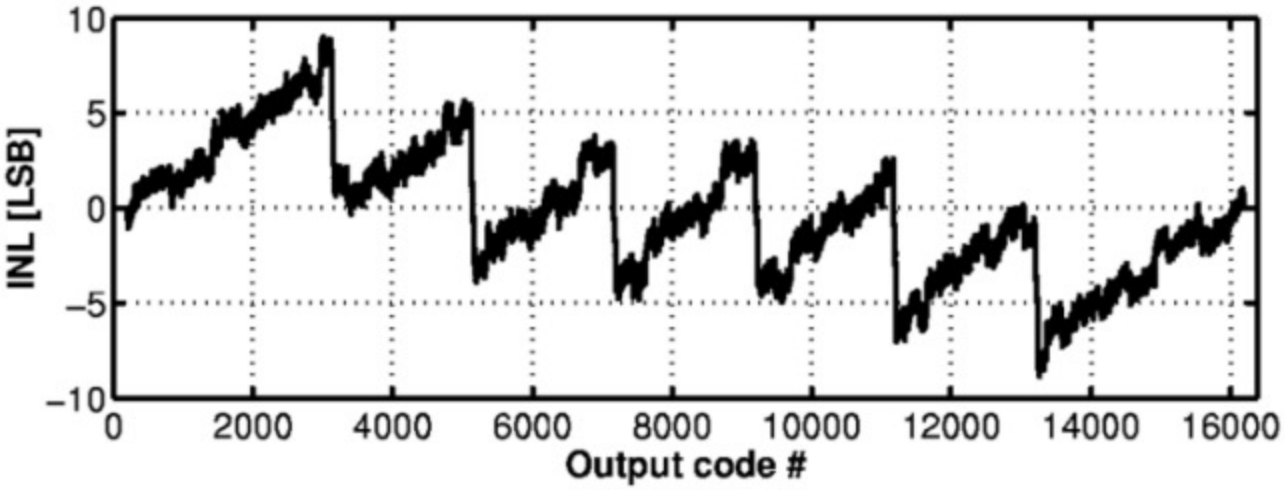
Dielectric Absorption

Has this been seen before?

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 38, NO. 12, DECEMBER 2003 2077

Impact of Capacitor Dielectric Relaxation on a 14-bit 70-MS/s Pipeline ADC in 3-V BiCMOS

Alfio Zanchi, *Member; IEEE*, Frank (Ching-Yuh) Tsay, *Senior Member; IEEE*, and Ioannis Papantonopoulos



Zanchi et al. used Si_3N_4 capacitors. They found dielectric absorption effect varied only weakly across temperature. Improved by moving to LPCVD SiO_2.

Zanchi et al. identified VCC as source of 2nd order tone (which we observe).

Dielectric Absorption

Has this been seen before?

US007498219B2

(12) **United States Patent**
Tian et al.

(10) **Patent No.: US 7,498,219 B2**
(45) **Date of Patent: Mar. 3, 2009**

(54) **METHODS FOR REDUCING CAPACITOR DIELECTRIC ABSORPTION AND VOLTAGE COEFFICIENT**

(75) Inventors: **Weidong Tian**, Dallas, TX (US); **Jozef Mitros**, Richardson, TX (US); **Victor Ivanov**, Richardson, TX (US)

(73) Assignee: **Texas Instruments Incorporated**, Dallas, TX (US)

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,877,751	A	10/1989	Teng et al.	
5,185,689	A *	2/1993	Maniar	361/313
5,192,703	A	3/1993	Lee et al.	
5,583,359	A *	12/1996	Ng et al.	257/306
5,808,335	A *	9/1998	Sung	257/306
5,877,533	A *	3/1999	Arai et al.	257/350
5,914,851	A *	6/1999	Saenger et al.	361/311
6,159,819	A	12/2000	Tsai et al.	

FIGS. **5**A and **5**B are plots illustrating integral linearity performance for 14 bit analog to digital converters having high dielectric absorption capacitors and low dielectric absorption capacitors, respectively;

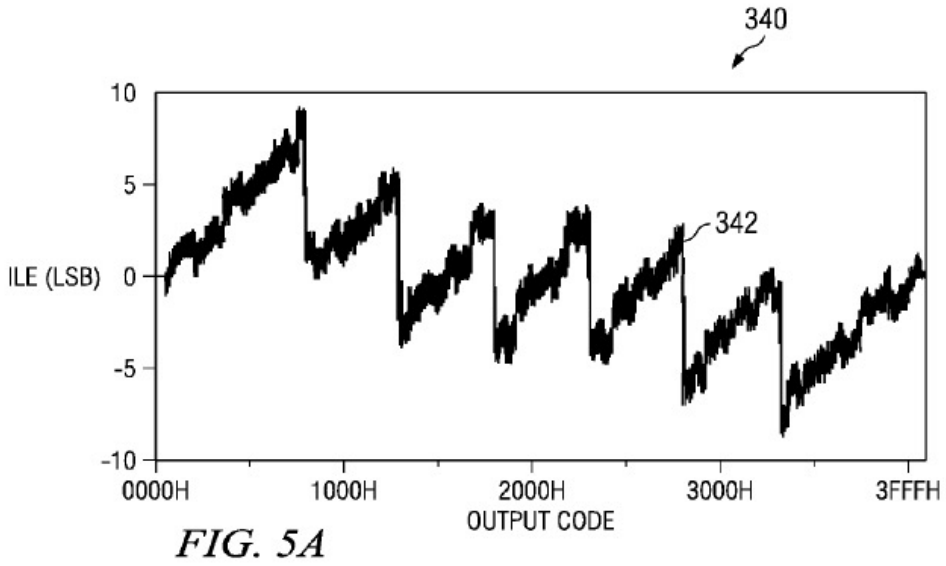


FIG. 5A

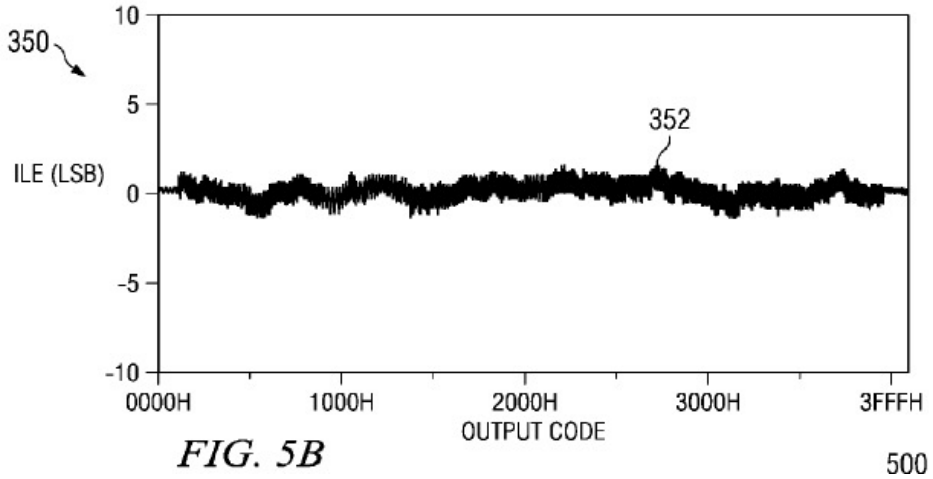
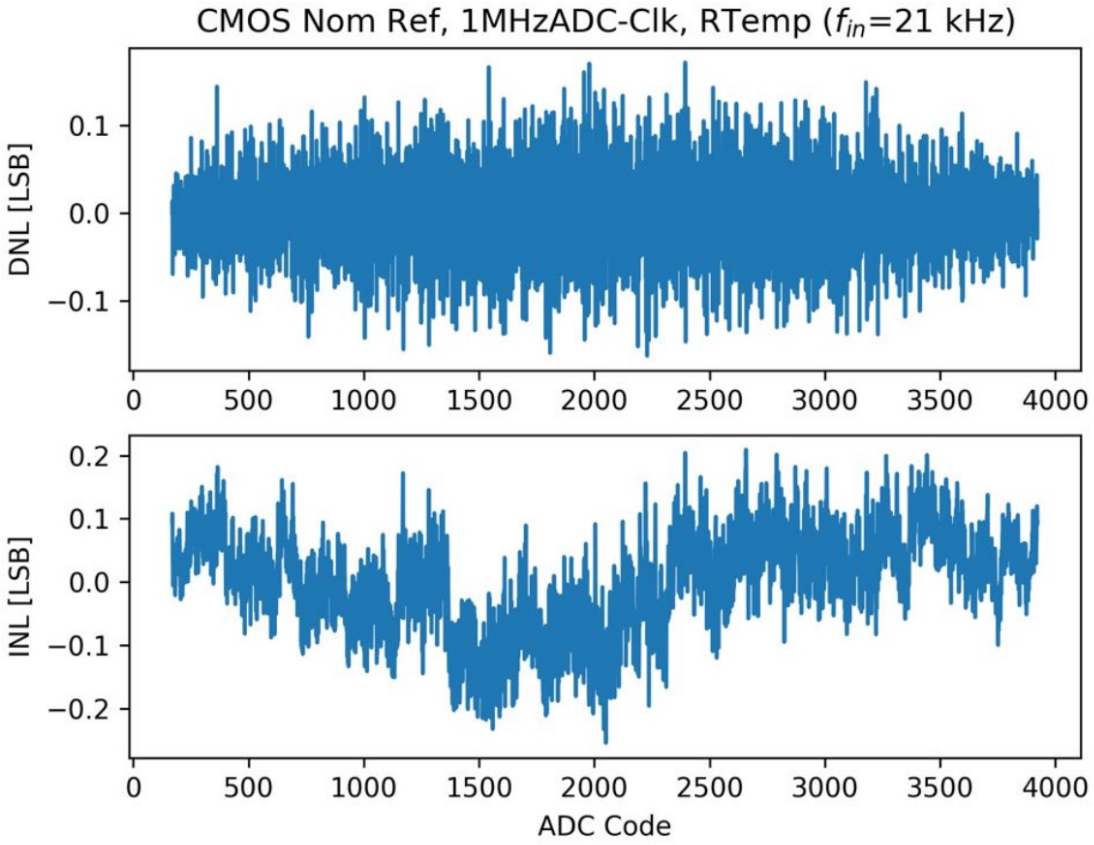


FIG. 5B

500

Dielectric Absorption Evidence



Measured result consistent with analog simulation

Reducing ADC sampling rate to 1 MS/s (16X slower). Third order structure removed.
Increasing bias current at fixed sampling rate does NOT have same effect

Dielectric Absorption

Why does slowing down the ADC help?

Understand capacitor soakage to optimize analog systems

Dielectric absorption can cause subtle errors in analog applications such as those employing S/H circuits, integrating ADCs and active filters. But knowing how to measure this soakage and compensate for it helps you minimize its effects.

Robert A Pease, National Semiconductor Corp

EDN OCTOBER 13, 1982

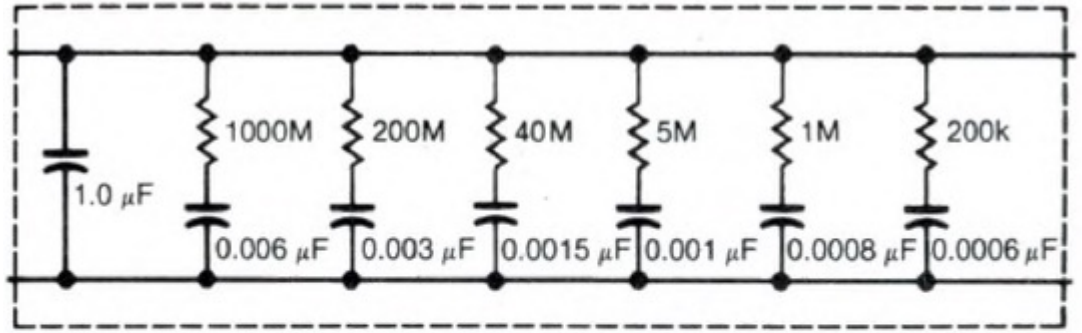


Fig 4—More precise than Fig 2's equivalent circuit, *a capacitor model employing several time constants proves valid for a wide range of charge and discharge times. This model approximates a Mylar capacitor.*

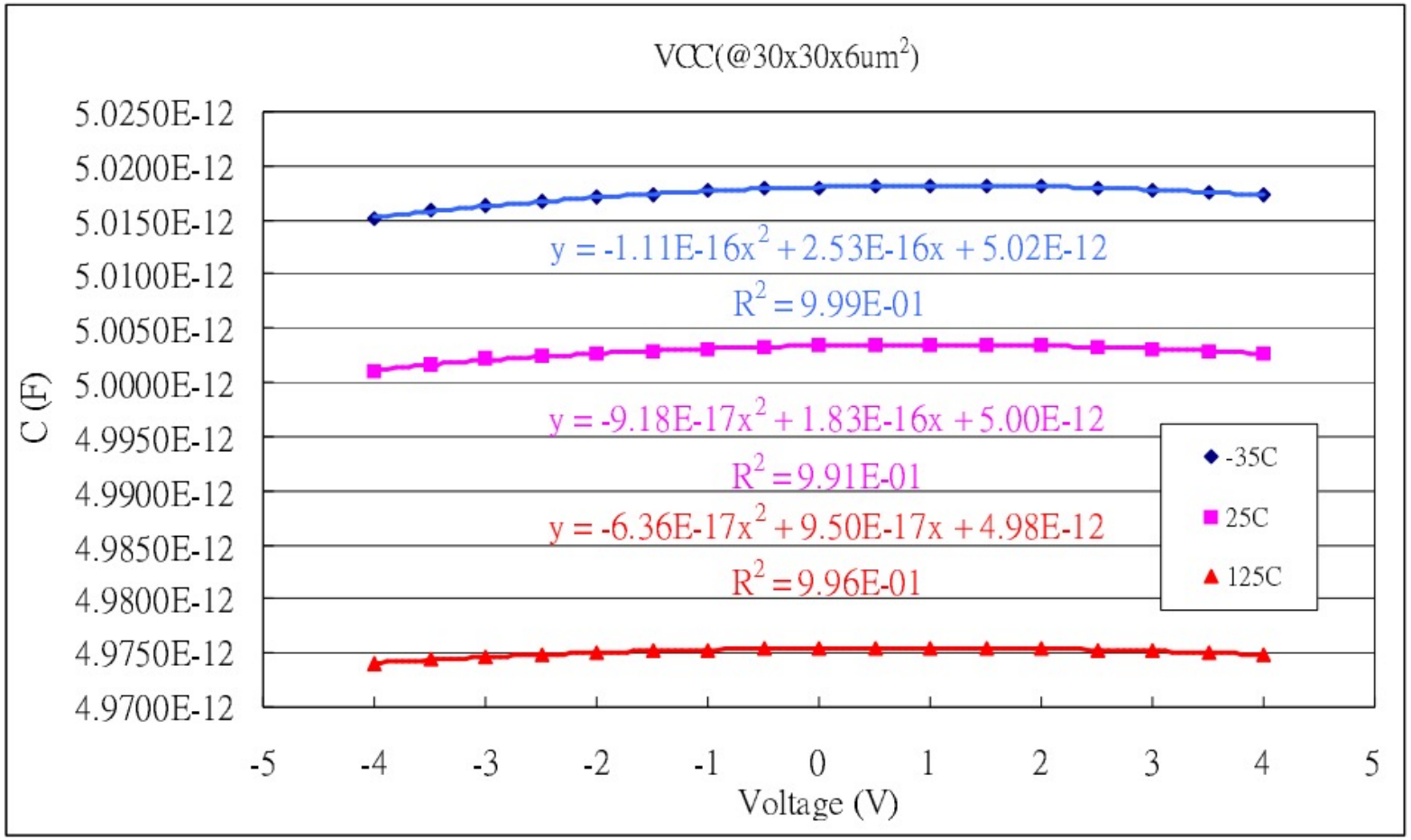
Capacitor has multiple time constants associated with discharge

Summary of Evidence for Dielectric Absorption

- Third-order structure INL consistent with Dielectric Absorption literature
- Structure cannot be removed by cooling chip, reducing reference voltage magnitudes or increasing bias currents → suggests not primarily a settling issue
- Structure can be removed by slowing down sampling rate (suggests not capacitor nonlinearity, besides, errors are too large)
- Structure largely stable on a channel-by-channel basis

Capacitor Voltage Coefficient

The value of a capacitor is a weak function of its bias level. This is called Voltage Coefficient of Capacitance (VCC) and is described with a polynomial.



Capacitor Voltage Coefficient

MDAC gain is: 1 + CS/CF

Decision level is worst case (with normalized capacitors):
CF sees 1V (nominal), CS sees 0.5V

- CF = 1 – 0.003% = 0.99997.
- CS = 1 – (0.003%/4) = 1 – 0.00075% = 0.9999925.

Therefore, maximum stage gain error at is:

- Gain = 1 + (0.9999925 / 0.99997) = 2.0000225

This is an error of 0.001%.
One LSB at 12-bits is 0.02% so this is a negligible error at the 12-bit level

This result is consistent with the literature.

Capacitor Voltage Coefficient

Similar to ColdADC expectations

A 200 mW, 1 Msample/s, 16-b Pipelined A/D Converter with On-Chip 32-b Microcontroller

Michael K. Mayes, *Member, IEEE*, and Sing W. Chin

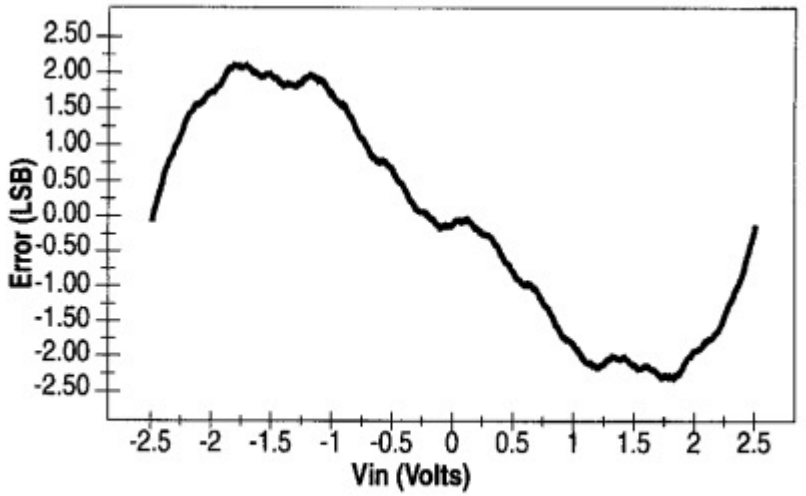


Fig. 20. INL errors due to second order capacitor voltage coefficient.

Takeaways

- Observations suggest dielectric absorption likely source of structured residual nonlinearity in ColdADC
- Effects not consistent with polynomial capacitor voltage nonlinearity
- Effect is highly dependent on particular material system and deposition process used to fabricate the capacitors (haven’t found our exact capacitors in the literature)
- Because dielectric absorption is an inherent property of the materials and methods used to implement the capacitors, so corrections should be stable once channel has been fabricated
- While fixing this requires redesign: lower density MiMcaps or (better) MOMcaps, it probably won’t be worth the (large) effort. Either accepting the INL or post-correcting it is likely good enough.