Bottom Electronics CDR

FEMB Design Status

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BROOKHAVEN NATIONAL LABORATORY

DUNE

Content

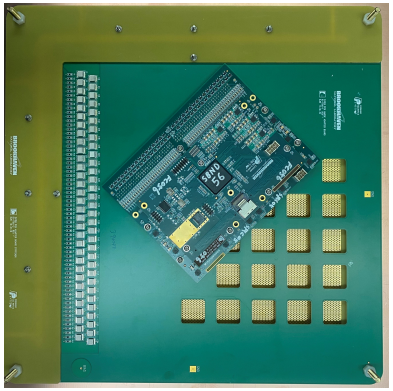
- FEMB Design for both HD and VD single-phase LArTPC
- FEMB Roadmap
- Integration Tests
- Consideration of the EMI shielding box for FEMB
- Consideration of Cabling
- FEMB QC Plan
- Summary

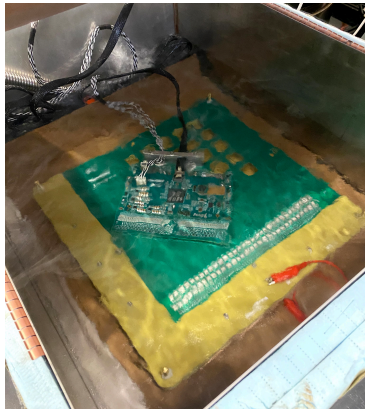
Using the horizontal drift electronics for the bottom CRUs

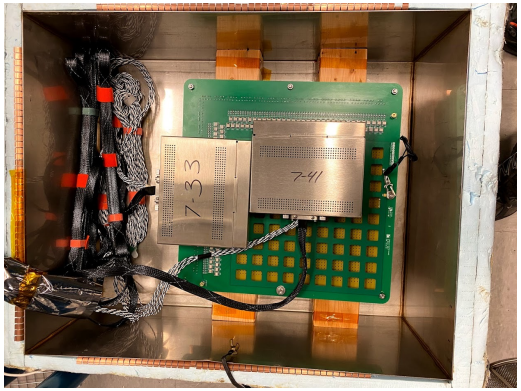
- Electronics designed to be immersed in LAr, installed very close to the pickup electrodes, transmit digitized signals on long cold cables (9-22 m for the horizontal drift)
  - **Minimize noise / space required on feedthroughs**
- SBND FEMBs used to read out prototype in the CERN 50L prototype
  - Promising performance with both 2-view and 3-view anode PCB prototype
- The design of the FEMBs, WIBs, WIECs, services on top of the cryostat inherit from the horizontal drift detector (no change or minor revision)
  - Production of detector components for the vertical drift detector will follow that of components for the horizontal drift detector
- Heat generated by electronics is negligible
  - Tests have been made at BNL with cryostat with LAr under pressure. At 14 m depth, no bubbles are released from heating elements with power density up to 4W/cm^2 $\rightarrow$ no bubble formation (gas boils bubbles collapse immediately under hydrostatic pressure)

Using the horizontal drift electronics for the bottom CRUs

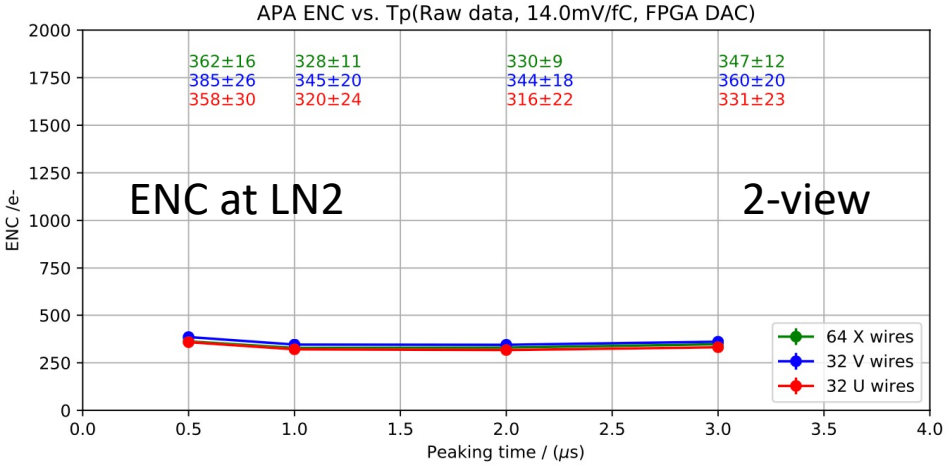
- SBND FEMBs used to read out 2-view and 3-view anode PCB prototype
  - Anode PCB, adapter board and CE were thoroughly verified at BNL in LN2
  - 2-view and 3-view anode PCB prototypes with integrated CEs have been working excellently at 50L setup
    - Serhan Tufanli. Vertical drift anode PCB demonstrators with integrated bottom electronics. DUNE collaboration meeting, May 20, 2021



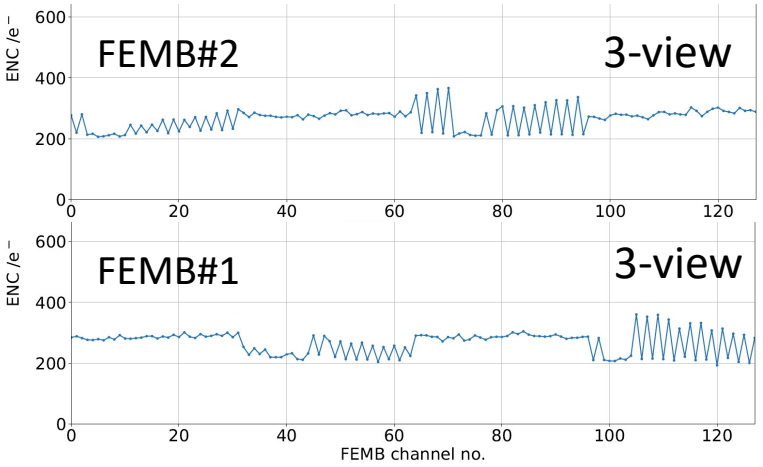




2-view anode PCB tested at BNL



3-view anode PCB with CE tested at BNL

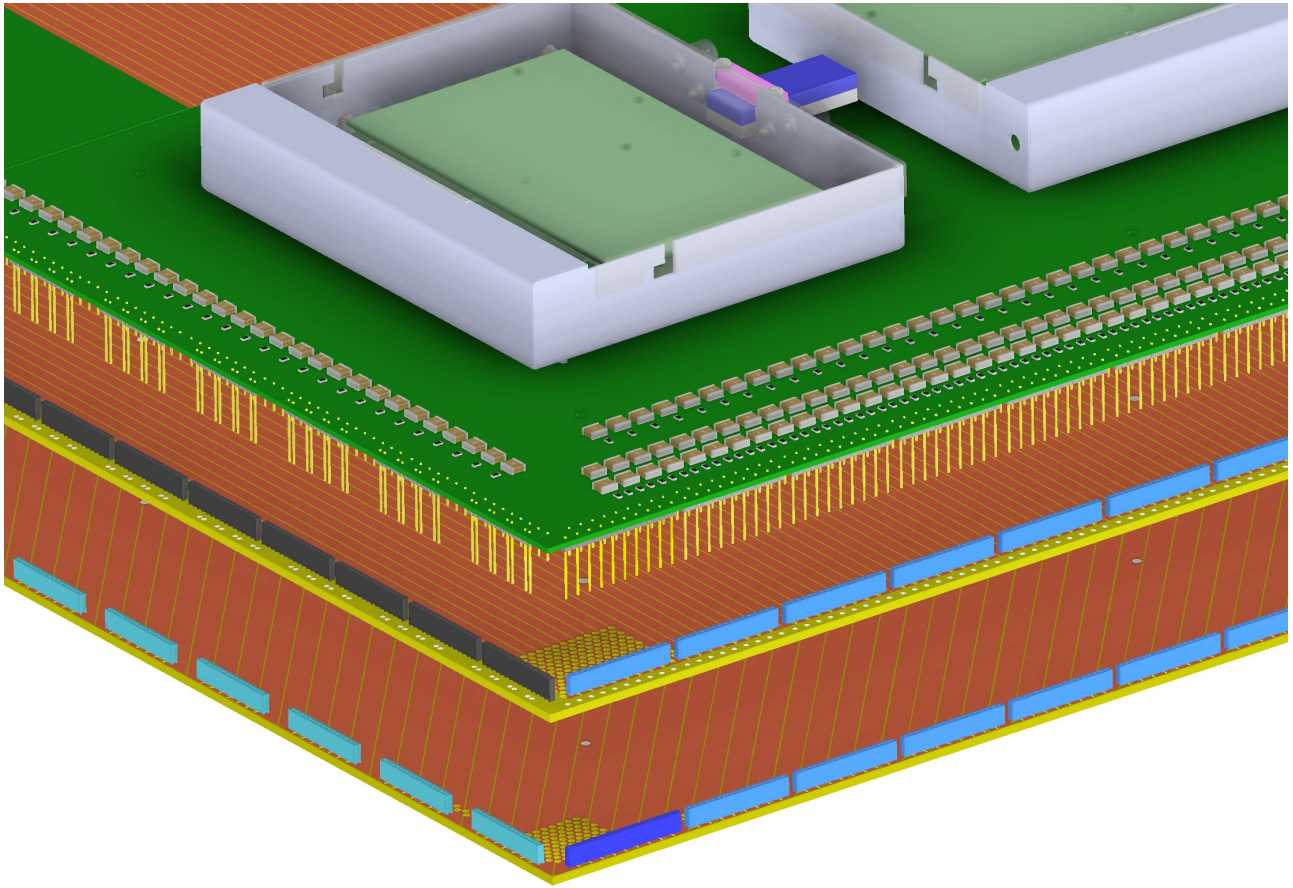


1st Cold Box 3-View Design : Bottom CRU Assembly Details

Slide from Yu Bo in DUNE collaboration meeting

8 unique CE adapter boards carries 13 CE modules, in addition to the high voltage coupling capacitors and current limiting resistors.

2 of the 13 modules on the CRU use 96 of the total of 128 channels.



Initial evaluation of the 50L 3-view setup at BNL showed noise pickup when the FEMBs are not enclosed the metal boxes.

To ensure good noise performance in the cold box test, the adapter boards, and composite frame holding the CRUs are designed to accommodate the CE boxes.

In the meantime, the CE boxes are being redesigned to be thinner, shorter, and lighter for the monolithic FEMBs.

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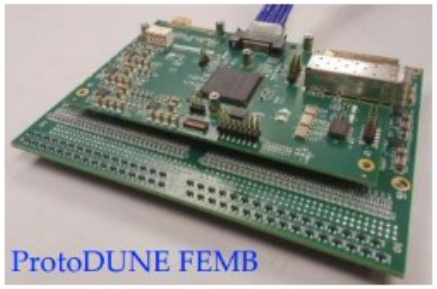
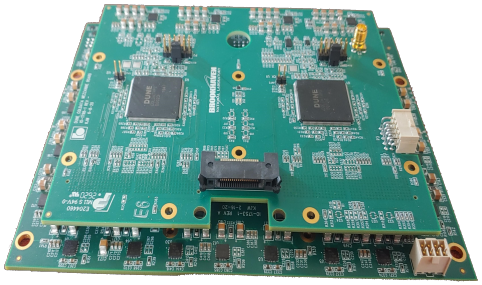
FEMB Roadmap

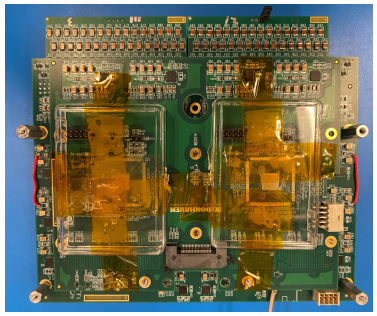
FEMB	FE amplifier	ADC	Serializer	Status
ProtoDUNE	8 * LArASIC p2	8 * P1 ADC (obsolete)	1 * cold FPGA	Used in ProtoDUNE
SBND	8 * LArASIC p2	128 * COTS ADC	1 * cold FPGA	Tested in 40% APA
Dual FPGA FEMB	8 * LArASIC p2 / p3	8 * ColdADC p1	2 * cold FPGA	Tested in 40% APA
COLDATA FEMB			2 * COLDATA P2	Tested in 40% APA, ICEBERG
Monolithic FEMB	8 * LArASIC p4 / p5	8 * ColdADC p2	2 * COLDATA p3 / p4	Ready for assembly

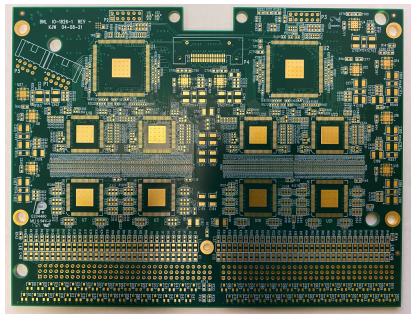

ProtoDUNE FEMB


SBND Top FEMB


Dual-FPGA FEMB


COLDATA FEMB (R0)


COLDATA FEMB (R1)

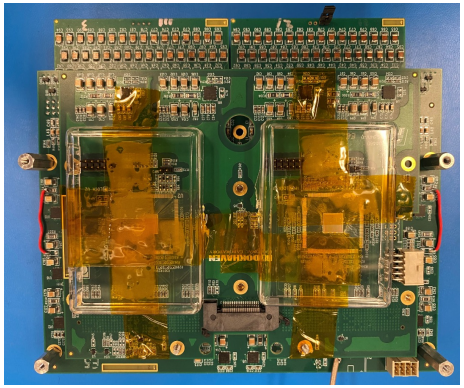

Monolithic FEMB (Final)

One final design iteration on the monolithic FEMB

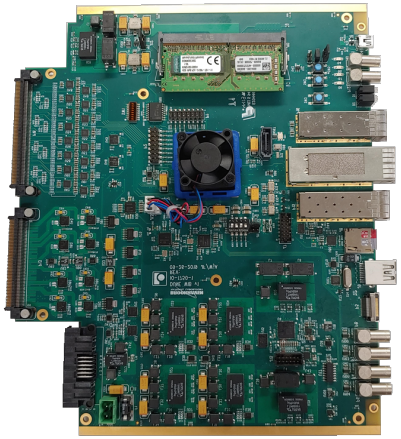
- **minor revision, design changes do not present any risk**
- **Reduce the cable plant between the FEMB and the CE flange**
  - Necessary for FD1-HD
  - Reduction in the number of connections per FEMB is useful also for FD2-VD
- Enhanced analog monitoring feature(requires COLDATA P4)
  - 8x LArASIC: each channel output, bandgap reference, and temperature
  - 1x ColdADC: Voltage references can be monitored
    - Share the same path with LArASIC monitoring by the analog switch
- Incorporate lessons learned from the first monolithic FEMB
  - Possible layout optimization for better performance
  - Mechanical optimization for assembly installation
    - Locations of connectors, assembly holes, and etc.
- FD1-HD to FD2-VD
  - If patch panel and mini-SAS cable are chosen
    - Minor revision to replace Samtec data connector to mini-SAS connector
  - If CE box is removed
    - New cable relief scheme should be considered

Latest Mezzanine 3-ASIC FEMB Characterization

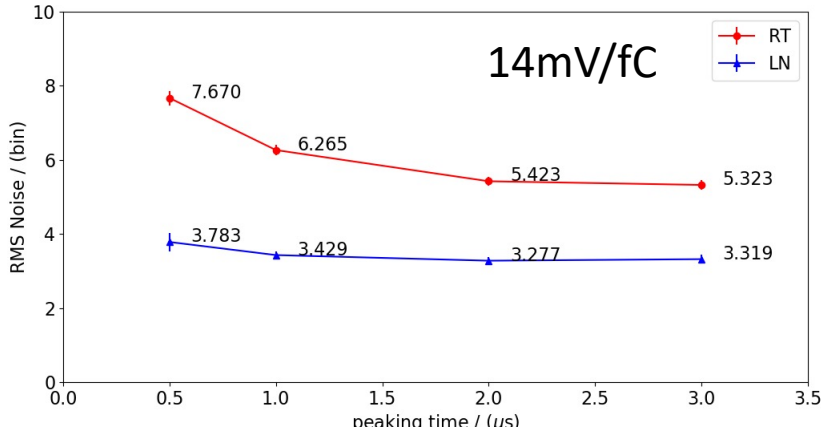
- Reported in the DUNE CE consortium meeting on 04/26/2021
  - The latest Mezzanine 3-ASIC FEMB (intermediate FEMB towards the monolithic FEMB design) shows promising performance with the bench-top test stand at BNL

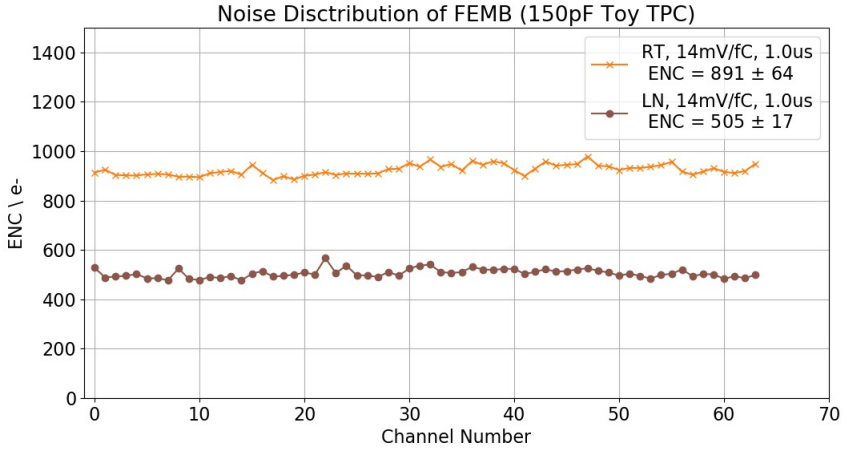


Mezzanine 3-ASIC FEMB (R1)



Zynq+ WIB





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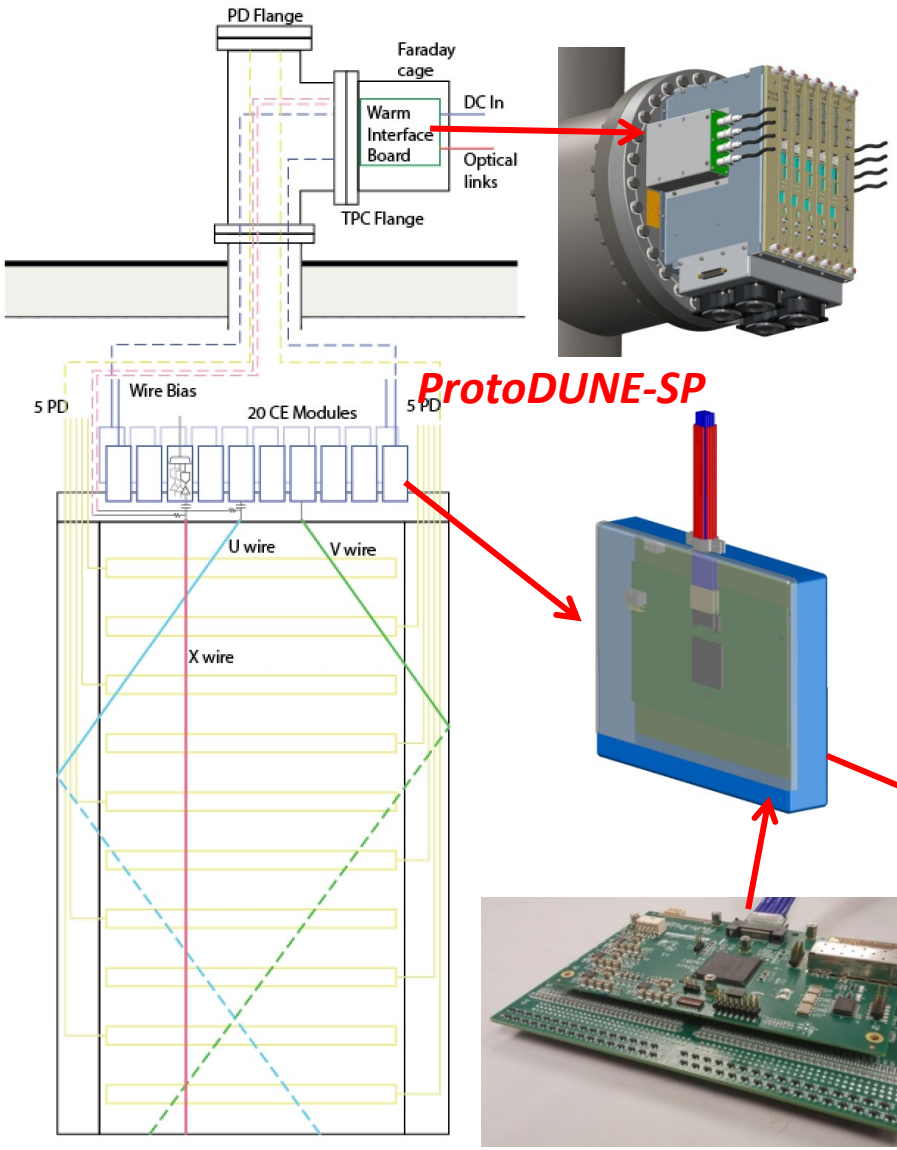
Integral System Design Concept



ProtoDUNE-SP

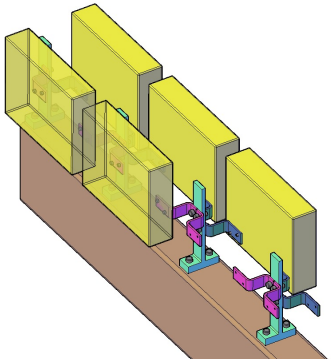
A necessary (but not sufficient!) condition to achieve a good performance, **the integral design concept** of APA + CE + Feed-through, plus Warm Interface Electronics with **local diagnostics** and strict isolation and **grounding rules** will have to be followed

HD

- BNL: 40% APA test stand (LN_2)
- CERN: Cold box test stand (Cold N_2 gas)
- Fermilab: ICEBERG test stand (LAr)

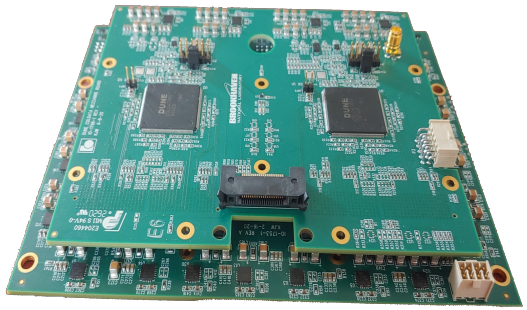
VD

- **BNL: CRP cold box (LN2) under construction**
- **CERN: 50L for small prototype**
- **CERN: CRP cold box (LAr)**

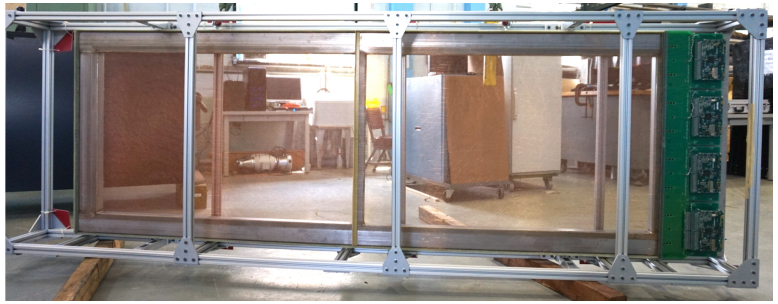


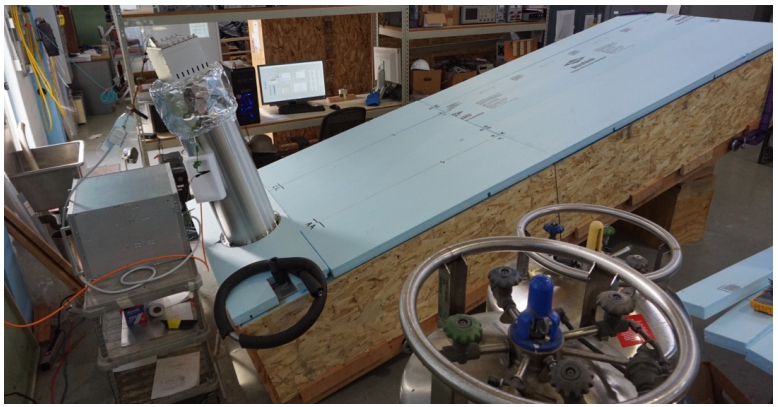
Cold electronics module and its attachment to the APA frame

40% APA Integration Test Stand at BNL

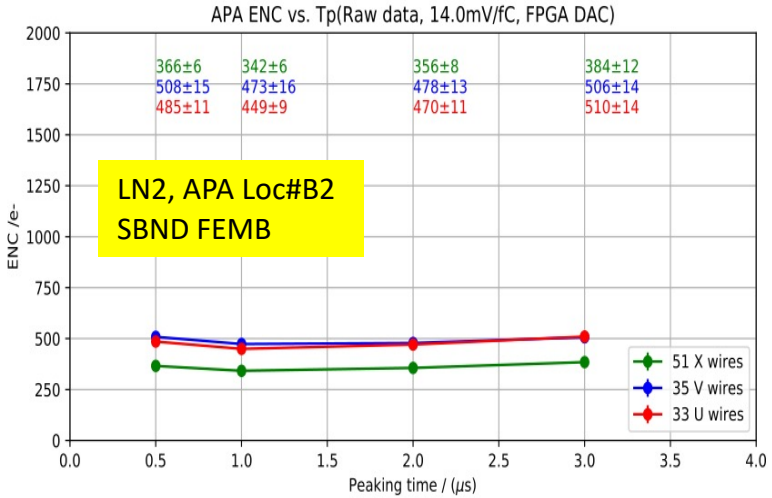


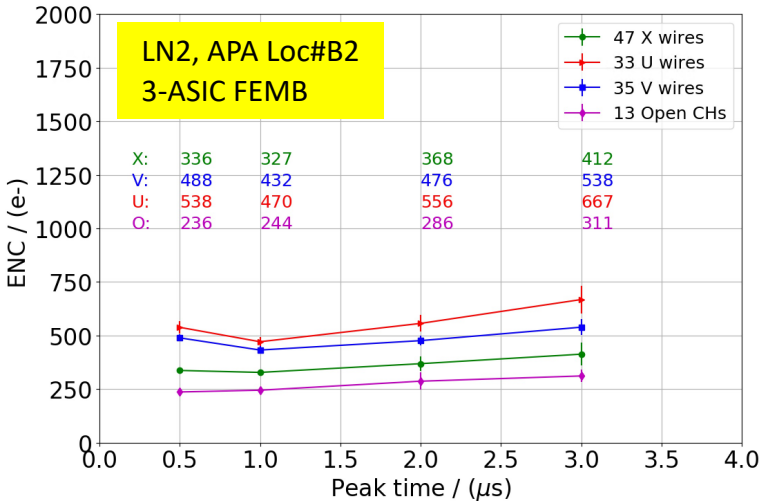
3-ASIC FEMB Prototype





40% APA Integration Test at BNL

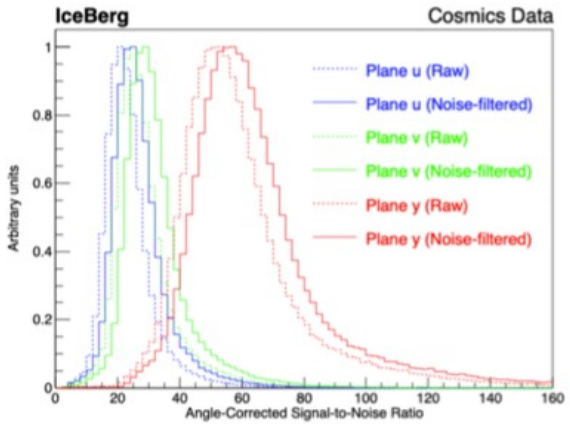




Consistent with previous measurements with ProtoDUNE or SBND FEMB

ICEBERG Test Result

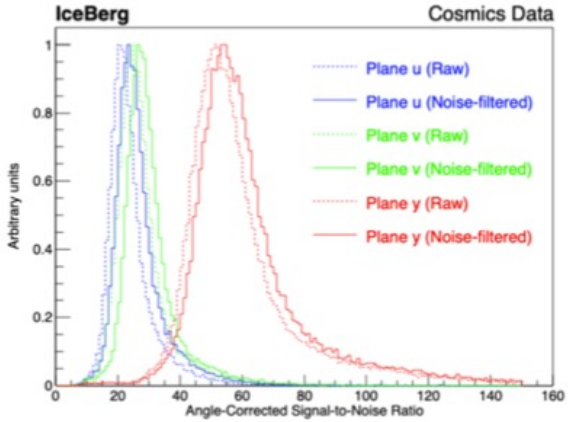
Run4 (COTS ADC) 7080-7210



Plane	Most probable value	
	Raw data	Noise-filtered
Induction U	21.2 ± 0.0	24.2 ± 0.0
Induction V	24.8 ± 0.0	28.3 ± 0.1
Collection Y	51.9 ± 0.1	56.7 ± 0.1

Plane	Average	
	Raw data	Noise-filtered
Induction U	23.8 ± 0.0	27.2 ± 0.0
Induction V	28.6 ± 0.0	32.8 ± 0.0
Collection Y	59.5 ± 0.0	64.8 ± 0.0

Run5 (3-ASIC) 8898-8947



Plane	Most probable value	
	Raw data	Noise-filtered
Induction U	21.4 ± 0.1	23.9 ± 0.1
Induction V	24.8 ± 0.1	27.3 ± 0.1
Collection Y	51.9 ± 0.1	54.7 ± 0.1

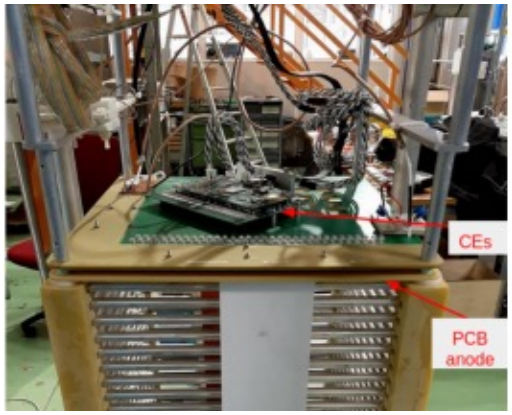
Plane	Average	
	Raw data	Noise-filtered
Induction U	24.3 ± 0.1	27.1 ± 0.1
Induction V	27.6 ± 0.0	30.6 ± 0.1
Collection Y	59.6 ± 0.1	62.4 ± 0.1

3-ASIC FEMB has the similar level of noise compared to ProtoDUNE FEMBs, few % higher than SBND FEMBs based on the commercial off the shelf ADC.

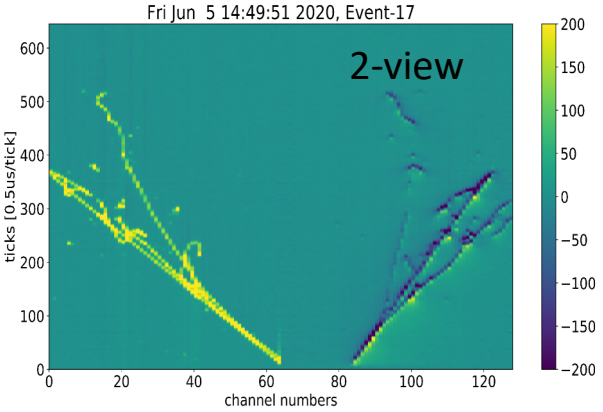
CERN 50L Setup

See Serhan and Filippo's talk

- Vertical drift anode PCB demonstrators with integrated bottom electronics
  - Serhan Tufanli. DUNE collaboration meeting, May 20, 2021



2-view: FEMB without CE box

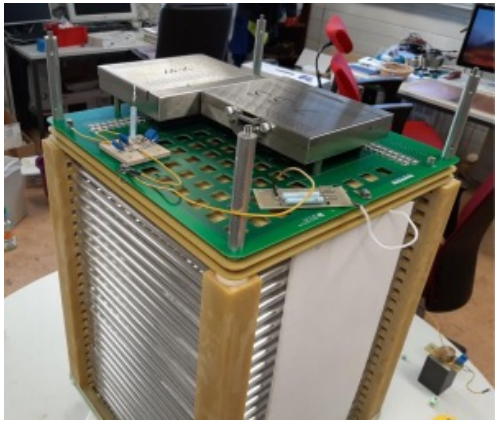


ENC of 2-view at LAr

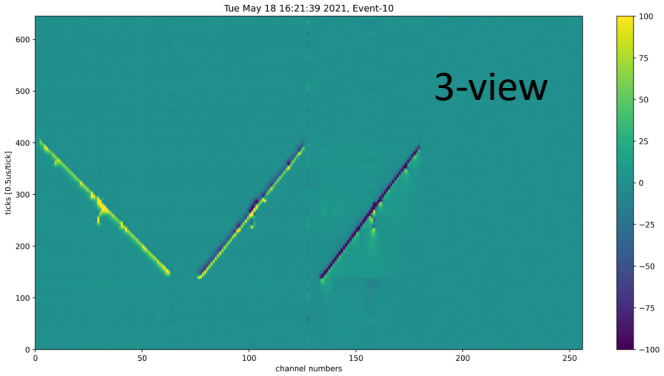
- C = ~ 320 e
- I = ~355 e

After coherent noise removal

- ~300 e for both C and I



3-view: FEMB without CE box



- Noise levels (MPV) with coherent noise:
  - Induction 1: ~500e
  - Induction 2: ~310e
  - Collection: ~310e
- Noise levels (MPV) after coherent noise removal
  - Induction 1: ~290e
  - Induction 2: ~280e
  - Collection: ~280e

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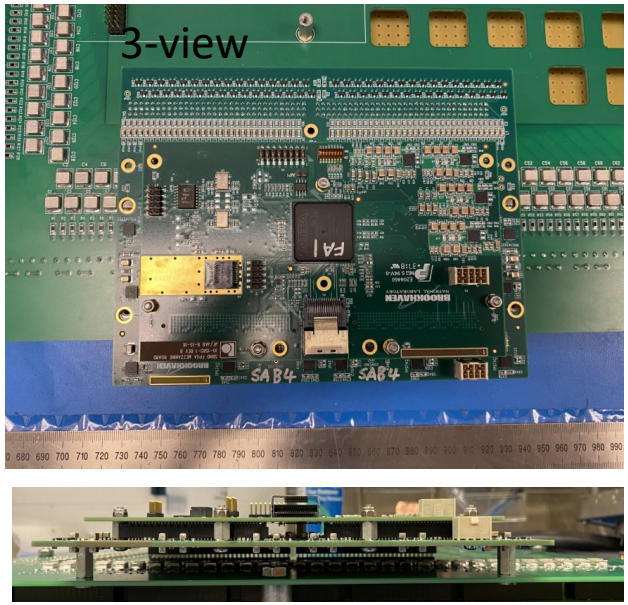
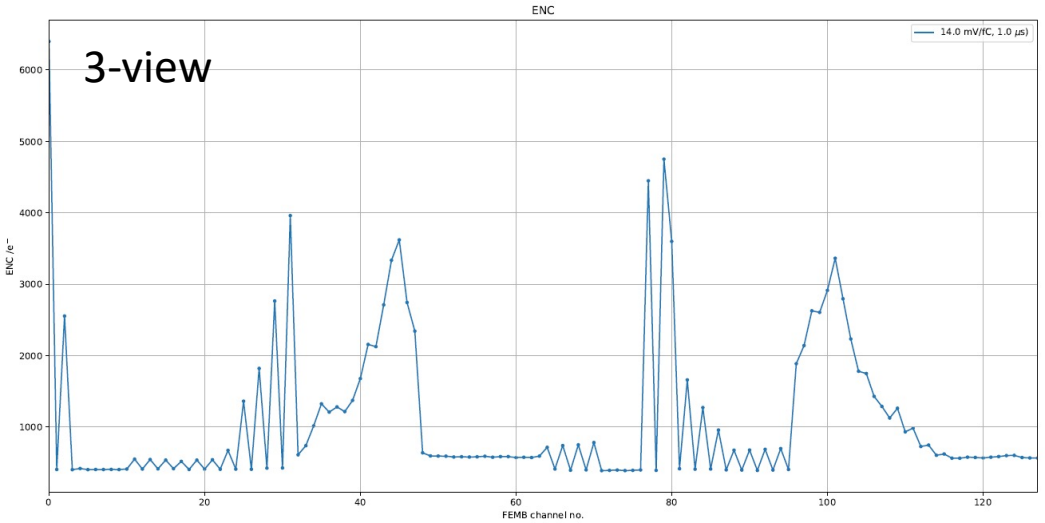
CE Box for 3-View Prototype

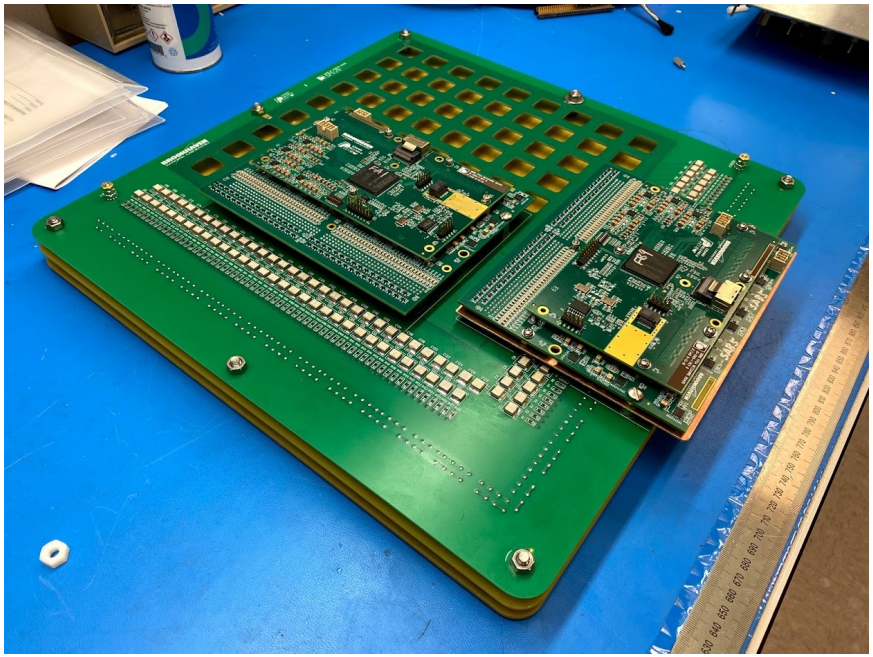
- 2-View Anode PCB
  - The adapter board between FEMB and anode PCB has an entire copper plane to common ground, which provide good EMI shielding
  - No trace or HV capacitor on the adapter board right under the FEMB
- 3-View Anode PCB
  - The adapter board between two FEMBs and anode PCB has limited copper plane area
  - Many traces and HV capacitors right under one FEMB, digitization (ADCs) emits noise to them.
    - The placement of the FEMB module in this picture was due to space constraints inside the 50L cryostat. On the large CRPs, the FEMB are not placed directly above the fan-in traces



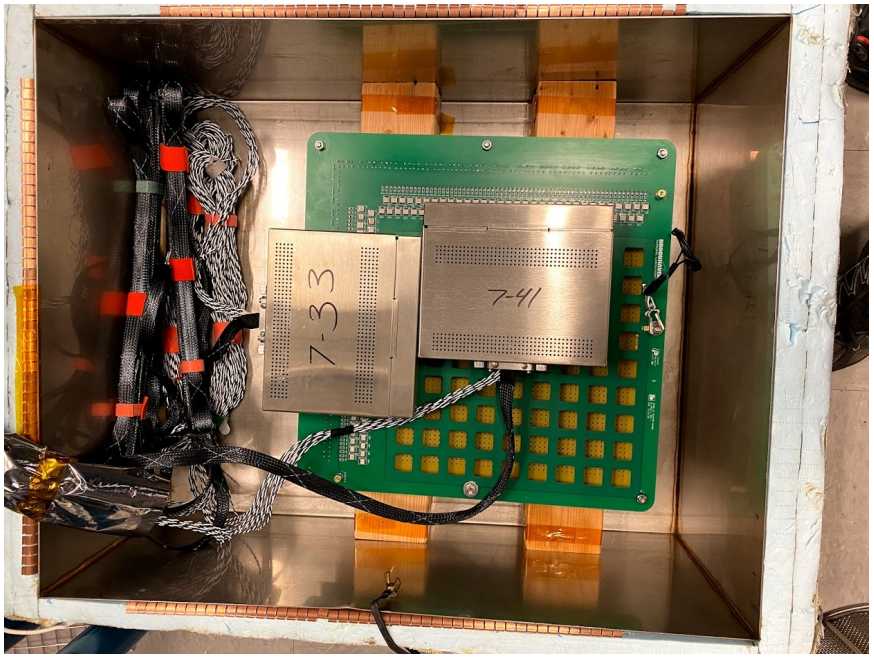


Higher than expected noise even at RT shows with the channels having traces on the adapter board under FEMB

CE Box for 3-View Prototype



Adding a copper shielding plane between FEMB and the adapter board helps mitigate extra pick-up noise

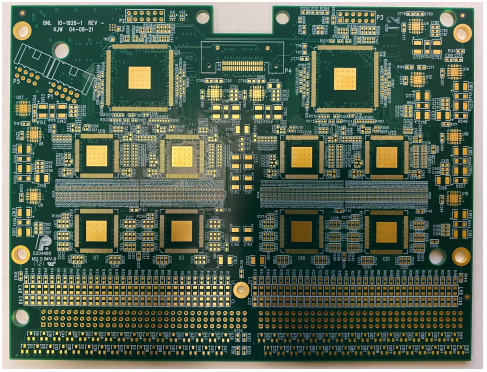


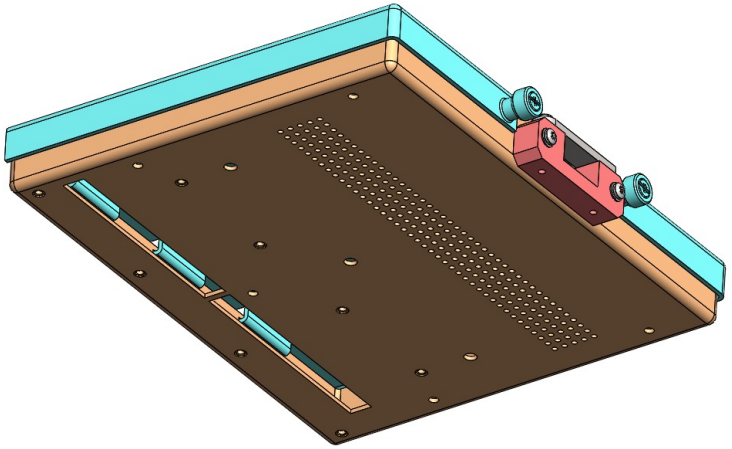
CE boxes are added to provide sufficient shielding

- The shielding plane under FEMBs can mitigate pick-up noise significantly at RT
- At cryogenic temperatures, the shielding plane under FEMBs can mitigate the pick-up noise to an acceptable level but not optimal
  - Digital devices (ADC, FPGA, COLDATA) on FEMB could be noise sources
  - CE box is recommended since potential noise path in full-size CRU could be hard to control

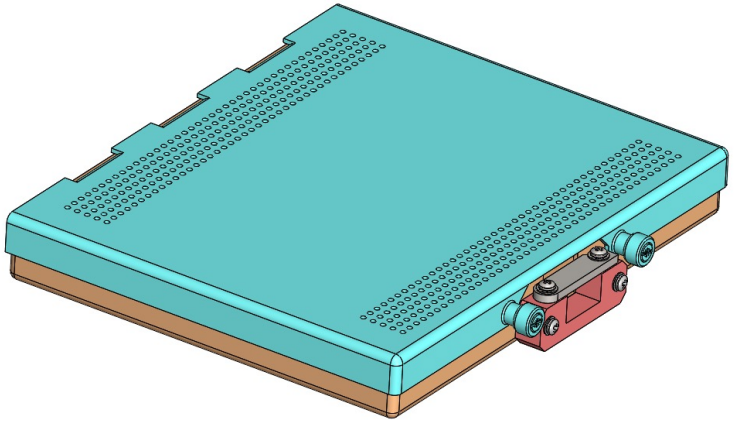
Thinner and lighter CE box in Aluminum

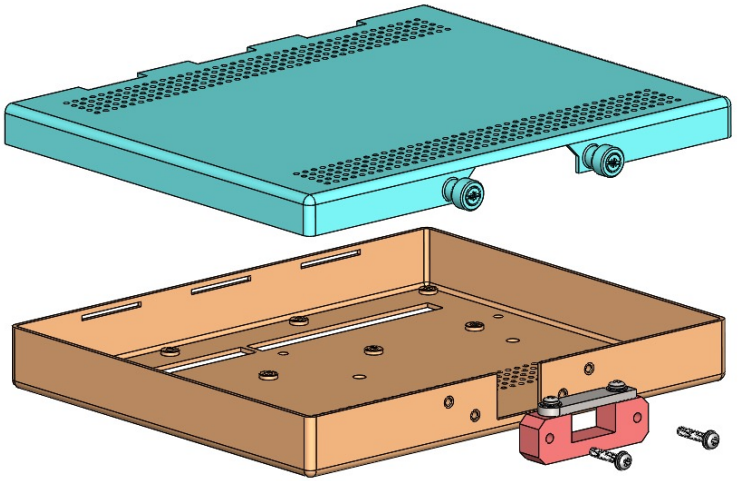
See Manhong's talk





CE box is designed for the monolithic FEMB





The weight of CE box (without FEMB) is reduced from 767g to 394g

FEMB w/wo CE box for the CRP

- FEMB with CE box
  - Better EMI shielding to avoid anode PCB picking up noise from FEMB
  - Easy for strain relief design
    - Strain relief is on the CE box
  - More freedom of CR adapter design and FEMB placement on the CRP
- FEMB without CE box
  - Much lighter, easy the requirement of the suspension design
  - Redesign strain relief for cold cables attached to the FEMBs
  - A shielding layer (entire copper plane) of the CR adapter board between FEMB and Anode PCB is necessary
- NP02 cold box test can help make the decision
  - Preliminary plan for a CRP testing in NP02 cold box
    - FEMBs enclosed in CE boxes will be populated one CRU
    - The other CRU will have FEMBs w/o CE boxes

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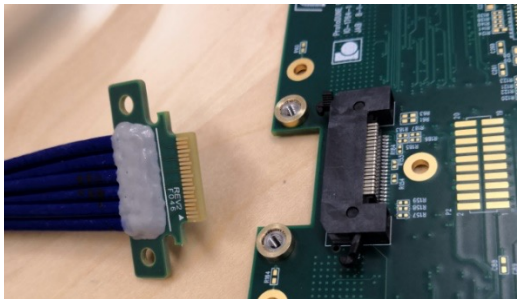
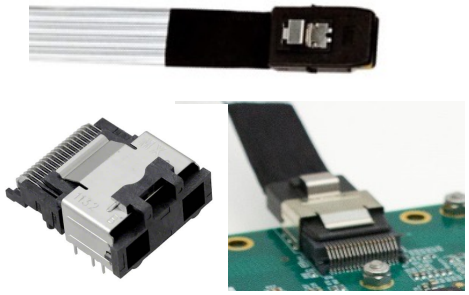
Cabling

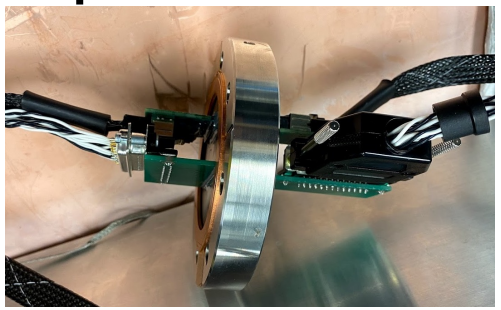
- COLDATA support high-speed link over 35m Samtec cable
- Possible minor revision of FEMB from FD1 to FD2
  - FD1: a signal cable from the CE flange to the FEMB
  - **FD2: 1) same single cable as FD1 (but longer, from 22m to 26m)**
  - **2) a patch panel is also considered as an option**



Samtec cable and connector



Mini-SAS cable and connector used in SBND

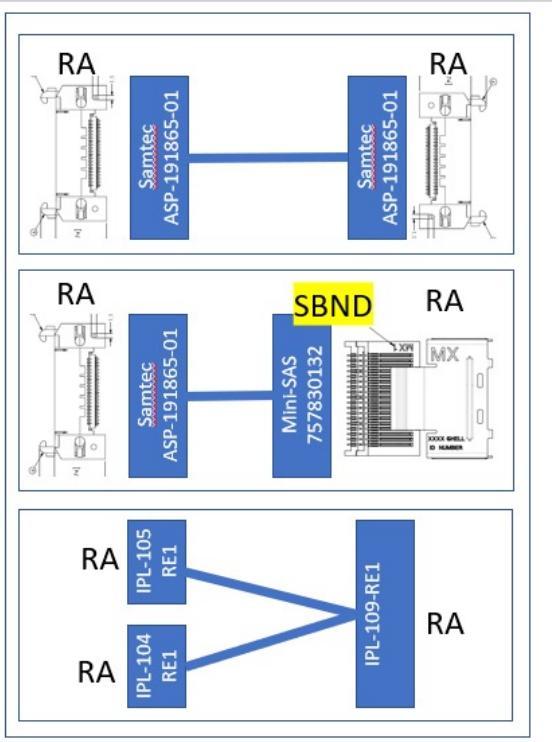


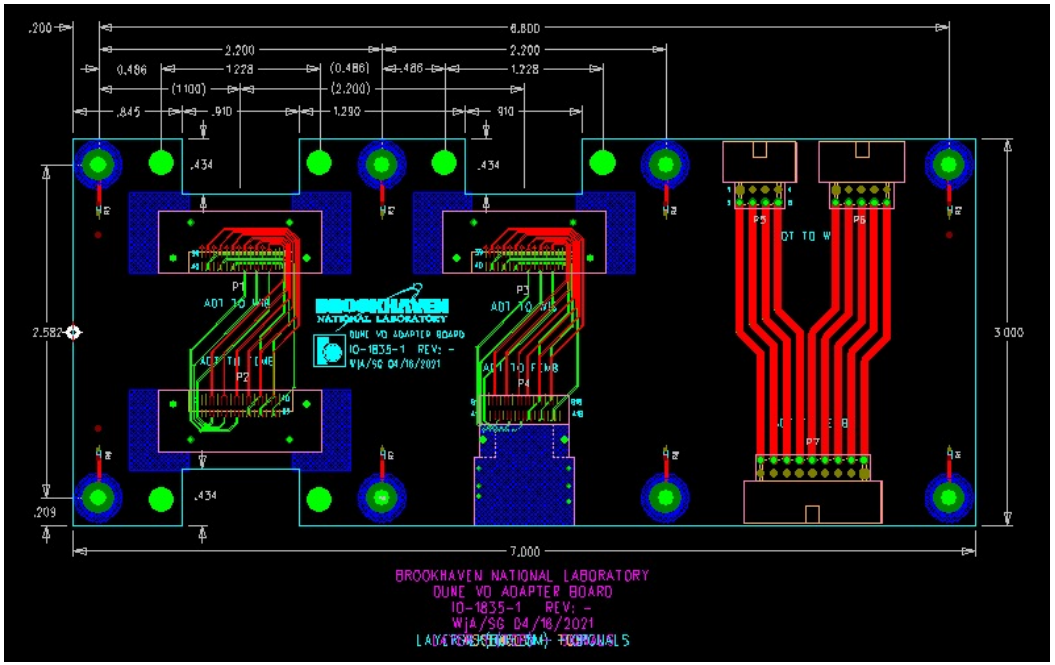
Verified 2 x 7m mini-SAS cables and an adapter board on flange for 50L setup

- The patch panel can simplify the installation
- Both short Samtec cable and mini-SAS cable will be evaluated
  - A prototype adapter board is designed to test the data transmission of COLDATA, and verify that the readout signals are not degraded by the insertion of the connector
- Drawback: one extra connection increase the chance of point of failure

A prototype cable adapter is being fabricated

- The prototype cable adapter
  - To verify the feasibility of the patch panel
  - Option 1: DUNE Samtec connector to DUNE Samtec connector
  - Option 2: DUNE Samtec connector to mini-SAS connector (SBND)
  - Option 3: Adapter for power distribution if power cable goes to the patch panel





Measurement to be done in the coming month

Content

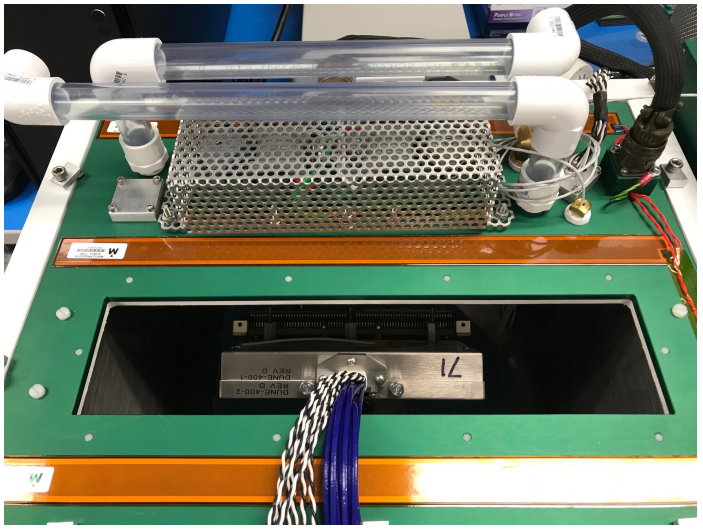
- FEMB Design for both HD and VD single-phase LArTPC
- FEMB Roadmap
- Integration Tests
- Consideration of the EMI shielding box for FEMB
- Consideration of Cabling
- FEMB QC Plan
- Summary

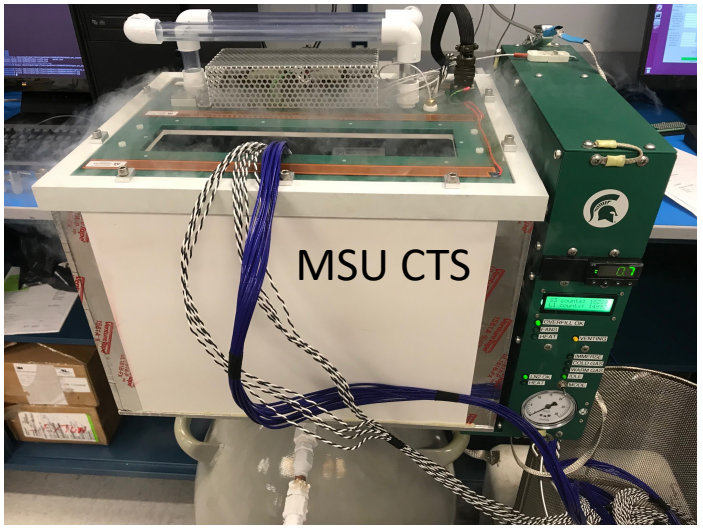
FEMB QC Plan

- A comprehensive set of QA/QC tests carried out for all components to ensure reliable operation of FEMB
  - DUNE FEMB QC plan is still under discussion
- Lessons learned from ProtoDUNE-SP and SBND CE
  - FEMB QA/QC procedures
    - Post-assembly screening test before installation in CE box
      - Get rid of defective FEMB assemblies
    - Characterization both at RT and LN2 after assembly
      - A whole assembly includes FEMB, CE box, cold power cable and data cable
    - Reception checkout test (RT) is recommended
    - Cold box integration test can further assure correct and reliable connection
- Challenge for DUNE FEMB QC
  - Ensure that QC procedures are applied uniformly at different test sites
  - Online database for logging
- **ASICs/FEMBs task force was formed on 04/05/2021**
  - Weekly meeting since 04/19/2021

Example of ProtoDUNE FEMB QC Test

- Power cycle test
  - Power to FEMB cycled and simple baseline measurement performed
  - 5 iterations
- Gain/ENC measurements
  - 17 separate gain/ENC measurements performed with different combinations of configurations
    - Gain: 14mV/fC, 25mV/fC
    - Shaping time: 0.5us, 1.0us, 2.0us, 3.0us
    - Both FPGA-DAC and ASIC-DAC calibration
    - One check of internal ADC clocks using nominal FE settings
- Power / current monitoring
  - Reads back FEMB voltages/currents measured on WIB
- Summary PDF of test results created as part of the test automatically





Summary

- No issues with using the FD-1 cold electronics for the readout of the bottom CRUs in the vertical drift detector (FD-2)
  - Identical to FD-1 HD FEMB design (See Cheng-Ju's talk)
    - Minor revision if the patch panel is presented
  - 3-ASIC FEMB solution meets all the DUNE needs
    - See Dave's talk
  - Production of CE components for the vertical drift detector will follow that of components for the horizontal drift detector
    - ASICs/FEMBs task force was formed
- Continuous effort should be made for the integration test
  - The integral system design concept is crucial
  - 50L setup shows the promising result (See Serhan and Filippo's talk)
  - Confidence of FEMB design is expected to be gained from the CERN cold box testing