# Top Electronics Digital Frontend

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FD2-VD CDR Review

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# Overview

Digital electronics is outside of the cryostat at warm near each SFT

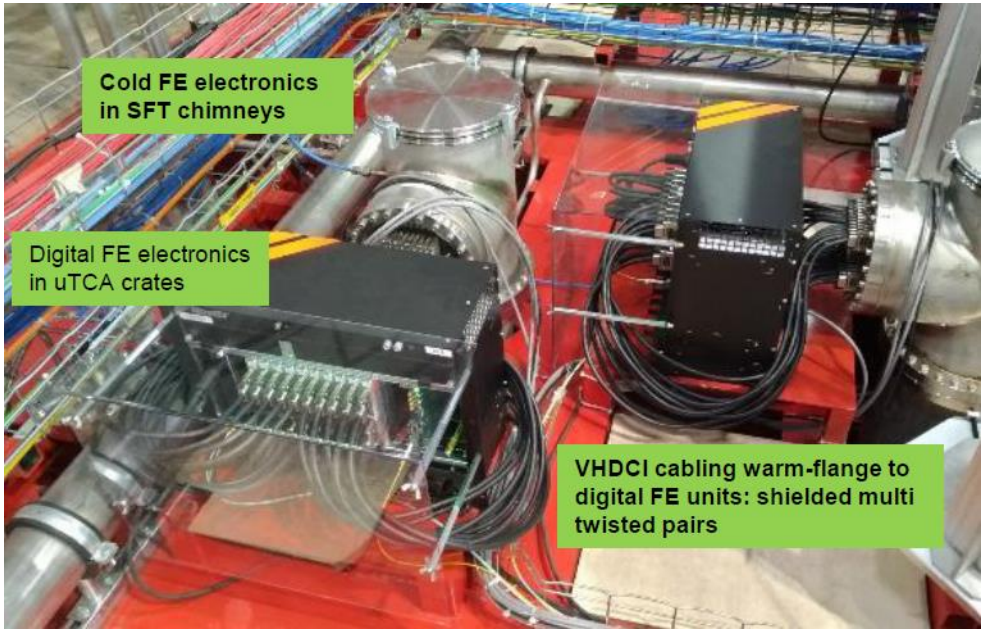
- No particular environmental requirements (e.g., stability / survivability at cold)
- Built with commercial components

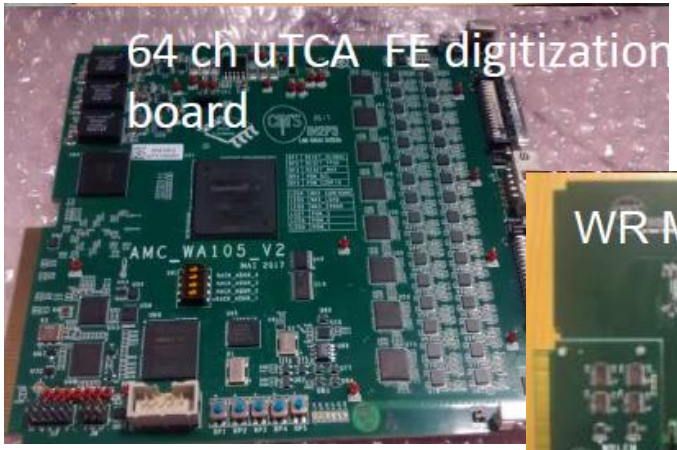
Advanced Mezzanine Card (AMC) are hosted in uTCA crates (up to 12 per crate)

Data from / to AMCs propagate through crate backplane and are routed via a uTCA central hub (switch) MCH

Each crate also contains a WR timing card (WR-MCH) :

- Keeps AMCs synchronized to the common clock
- In ProtoDUNE-DP also used for triggered readout whe WR-MCH receives a dedicated packet with timestamp of a trigger



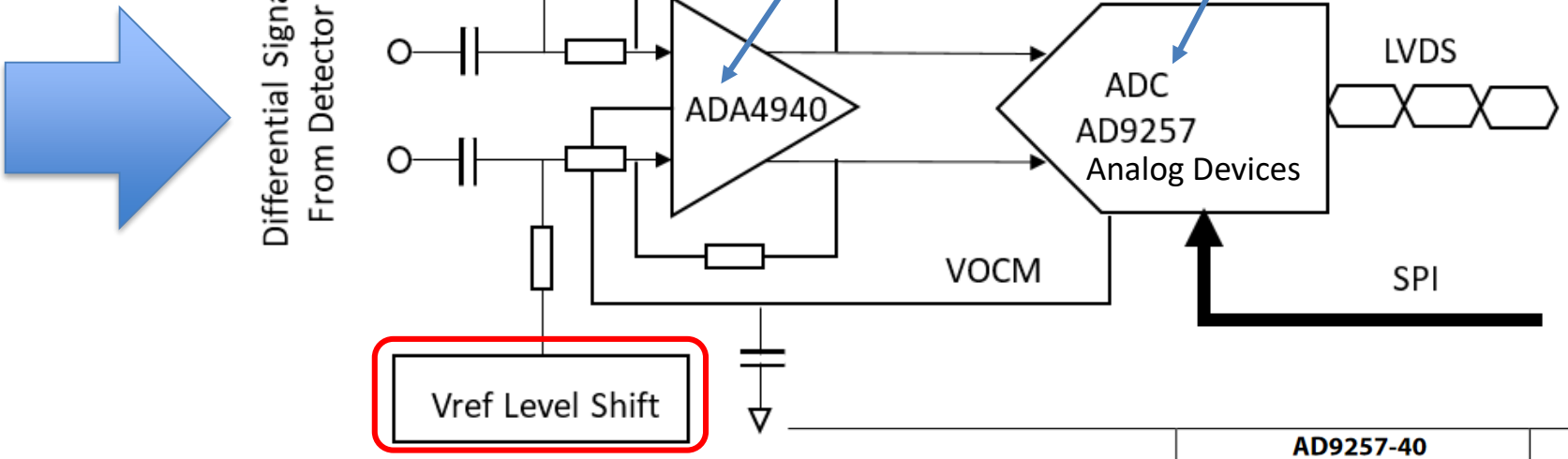

# Some Numbers: Channel Count

- Each AMC digitizes 64 channels matching one FE cryogenic analog card
  - Take differential input from analog cards via two 68wire VHDCI cables (32 ch per cable)
- uTCA crate can host up to 12 AMCs
  - 5 crates per chimney with 10 AMCs each to read 1 CRP (4 x ¼ CRP segments)
  - Two spare slots
- 4000 AMCs & 400 uTCA crates for 3-view FD2-VD baseline

| Item | Three-view |
|---|---|
| 1.5 m x 1.7 m CRUs in the top drift | 320 |
| Anode channels per CRP | 3200 |
| Channels per FE card or AMC card | 64 |
| FE cards or AMC cards per CRP | 50 |
| Number of SFT | 105 |
| FE card slots per SFT | 50 |
| Installed FE cards per SFT | 50 |
| $\mu$TCA crates | 400 |
| AMC cards per crate | 10 |
| WR-MCH | 400 |
| 40 Gb/s data links | 400 |
| Anode channels in the top drift | 256,000 |

# AMC Digitalization Stage

Differential analog signal from FE amplifier cards connected via AC coupling capacitors



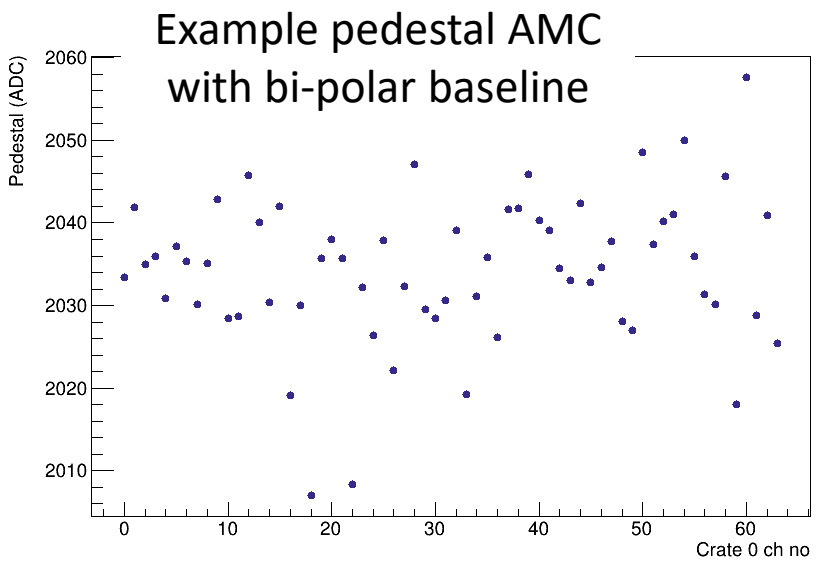

Level shift common to all 64 channels on the card

- For unipolar operation a VSHIFT is applied to negative branch to get maximal dynamic range between 0 – 2 V
- For bi-polar baseline (mid. dynamic range) VSHIFT = 0

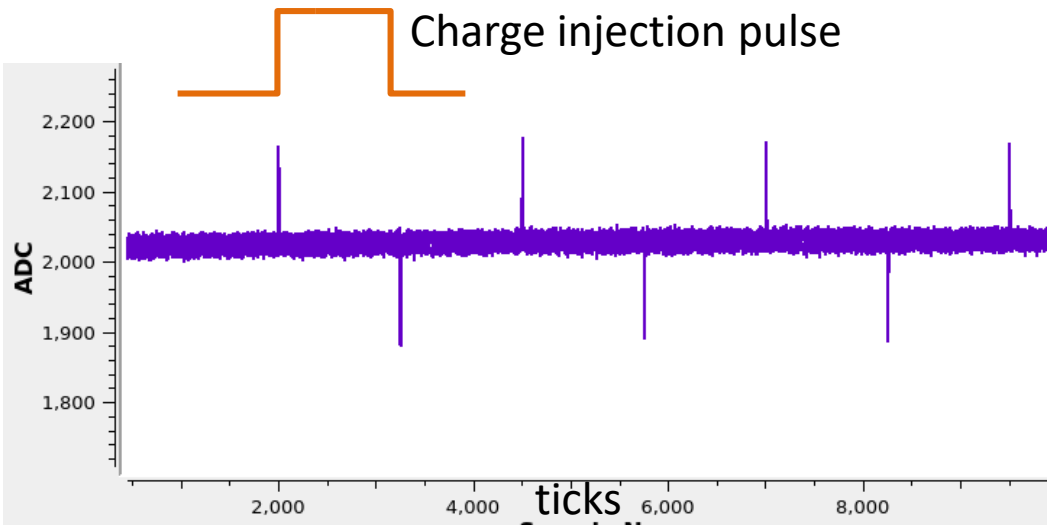
| | AD9257-40 | | | |
|---|---|---|---|---|
| **Parameter[1]** | **Min** | **Typ** | **Max** | **Unit** |
| RESOLUTION | 14 | | | Bits |
| ACCURACY | | | | |
| No Missing Codes | | Guaranteed | | |
| Offset Error | −0.6 | −0.3 | +0.1 | % FSR |
| Offset Matching | 0 | 0.2 | 0.6 | % FSR |
| Gain Error | −6.0 | −2.1 | 2.0 | % FSR |
| Gain Matching | −1.0 | +1.7 | +5.0 | % FSR |
| Differential Nonlinearity (DNL) | −1.0 | −0.5/+0.8 | +1.7 | LSB |
| Integral Nonlinearity (INL) | −3.1 | ±1.1 | +3.1 | LSB |

# AMC with bi-polar baseline

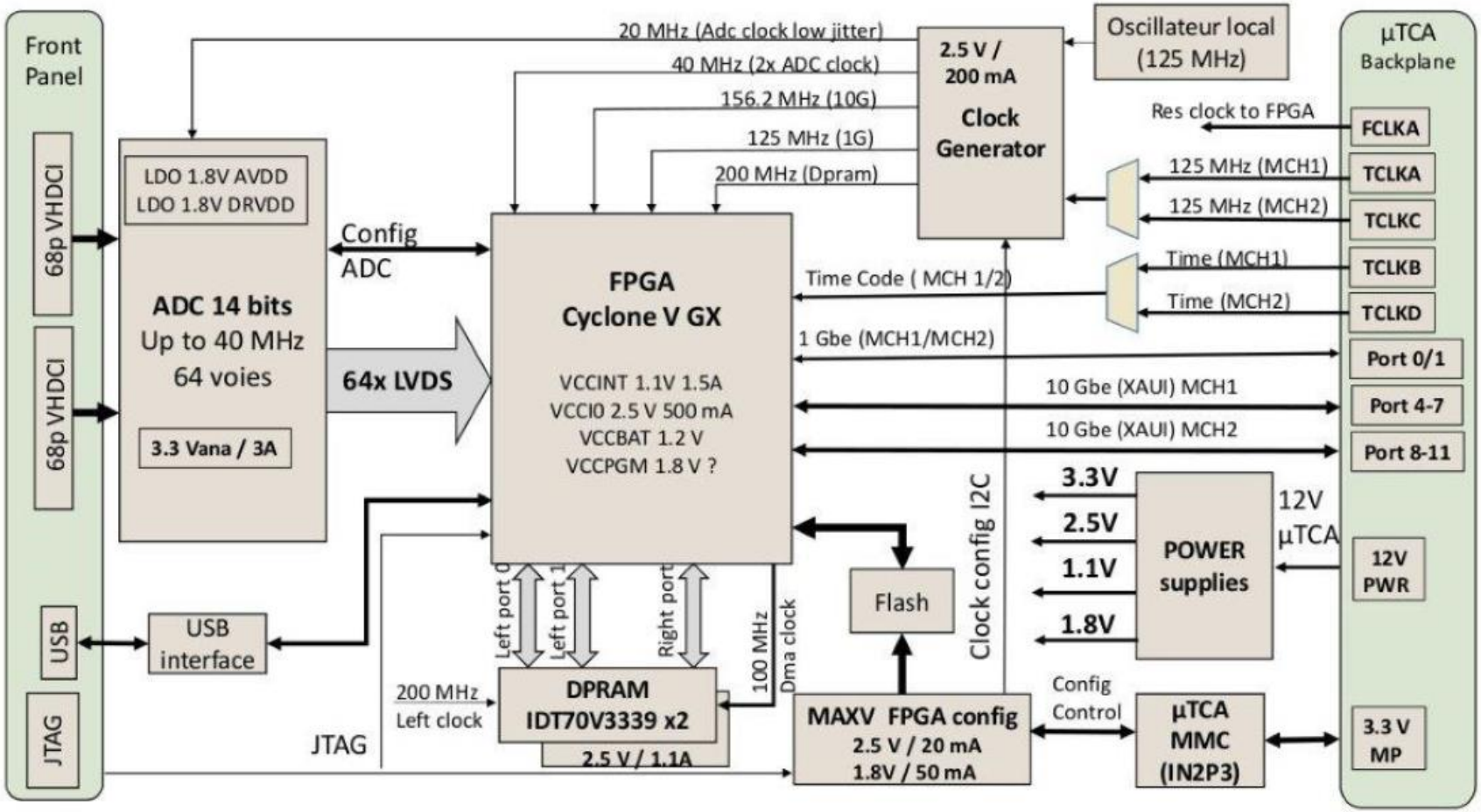
- In NP02 CRPs anode had two views which were collection type → unipolar signals
- Channel baseline in AMCs was set to give the maximal dynamic range for unipolar signals
  - DP expected dynamics was larger than in VD operation. Channel baseline in AMCs set ~100 ADC counts to optimize the maximal dynamic range for unipolar signals, up to max 4095 ADC



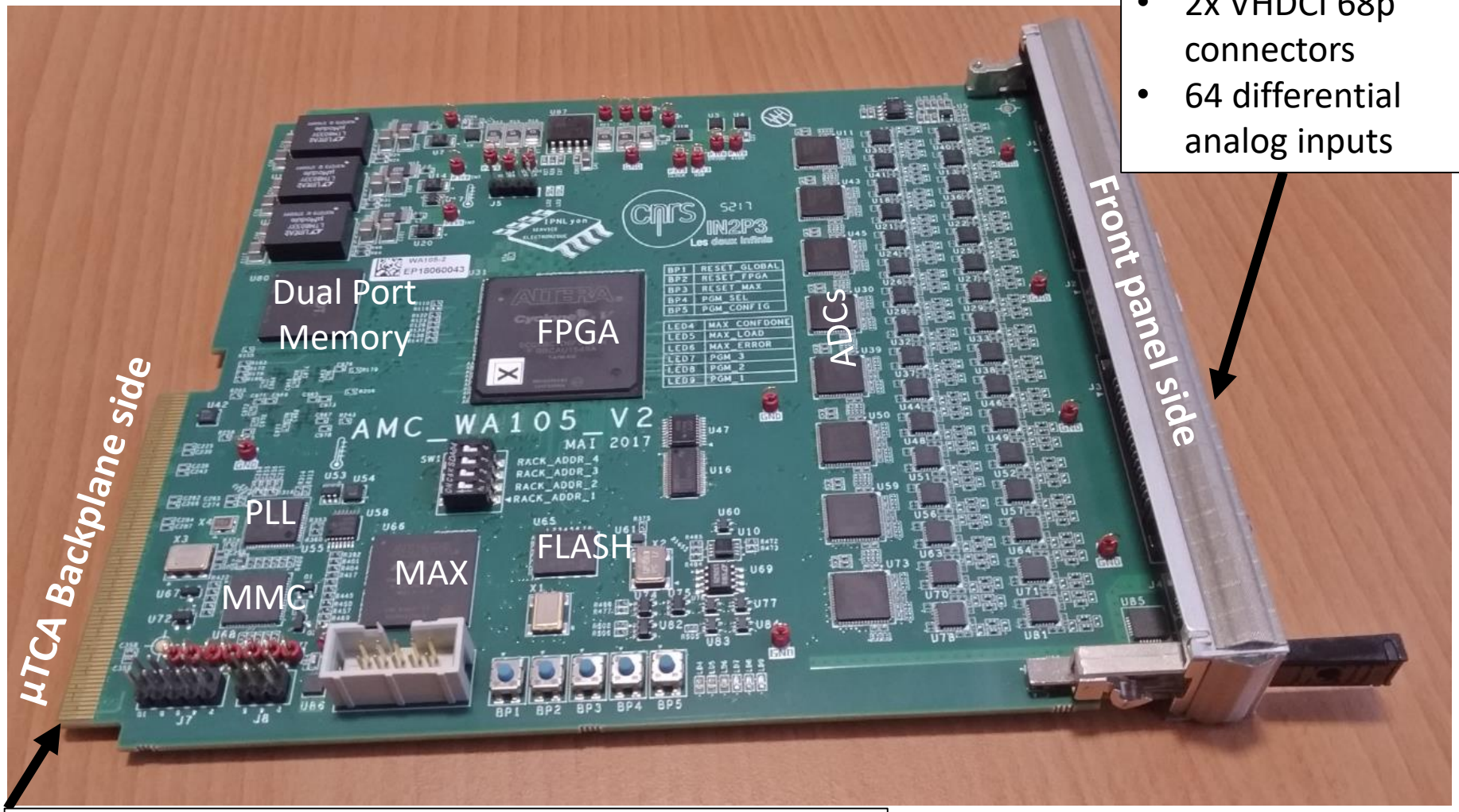

- Top electronics works with differential signals (+ve, -ve polarity); for bi-polar operation the ADC baseline needs to be set to ~middle of dynamic range



# NP02 AMC BLOCK DIAGRAM




- FPGA control / configure can be done via IPMI
- Base FW (“factory”) allows updating FW remotely over network




- 2x VHDCI 68p connectors
- 64 differential analog inputs

- 10 Gbe XAUI
- 1 Gbe
- IPMI for control and FPGA configuration
- 125 MHz White Rabbit clock
- White Rabbit network also used to transmit trigger timestamps data

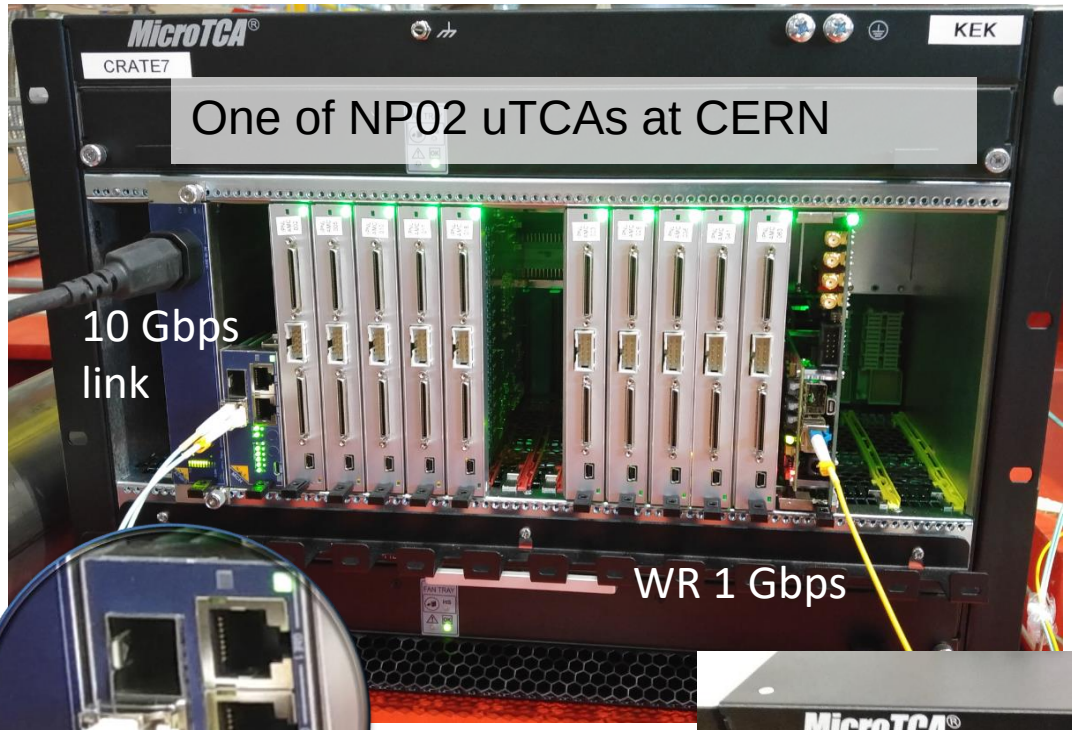
# FPGA Digital Data Processing

- FPGA has a virtual processor NIOS II that forms the core of the digital data processing and transmission
- For ProtoDUNE-DP configuration :
  - Input ADC data stream down-sampled to 2.5 MSPS and only 12 MSBs retained
  - Latency FIFO to guarantee that the first sample of event is always present independent of the delays of receiving trigger timestamp at AMCs
    - When WR timestamp trigger packet is received and decoded the latency FIFO is read until the sample corresponding to the real trigger time is found. The following samples corresponding to the desired drift window are then stored in memory to form appropriate UDP data packets for transmission
  - Optionally Huffman compression can be performed in real-time
- Flexibility in configuration for the final AMC output data resolution (digital data are available at much higher sampling rate)
  - AMC firmware can be flashed via the crate network connection
- Generating trigger primitives in AMCs is also a possibility

# Crate Bandwidth

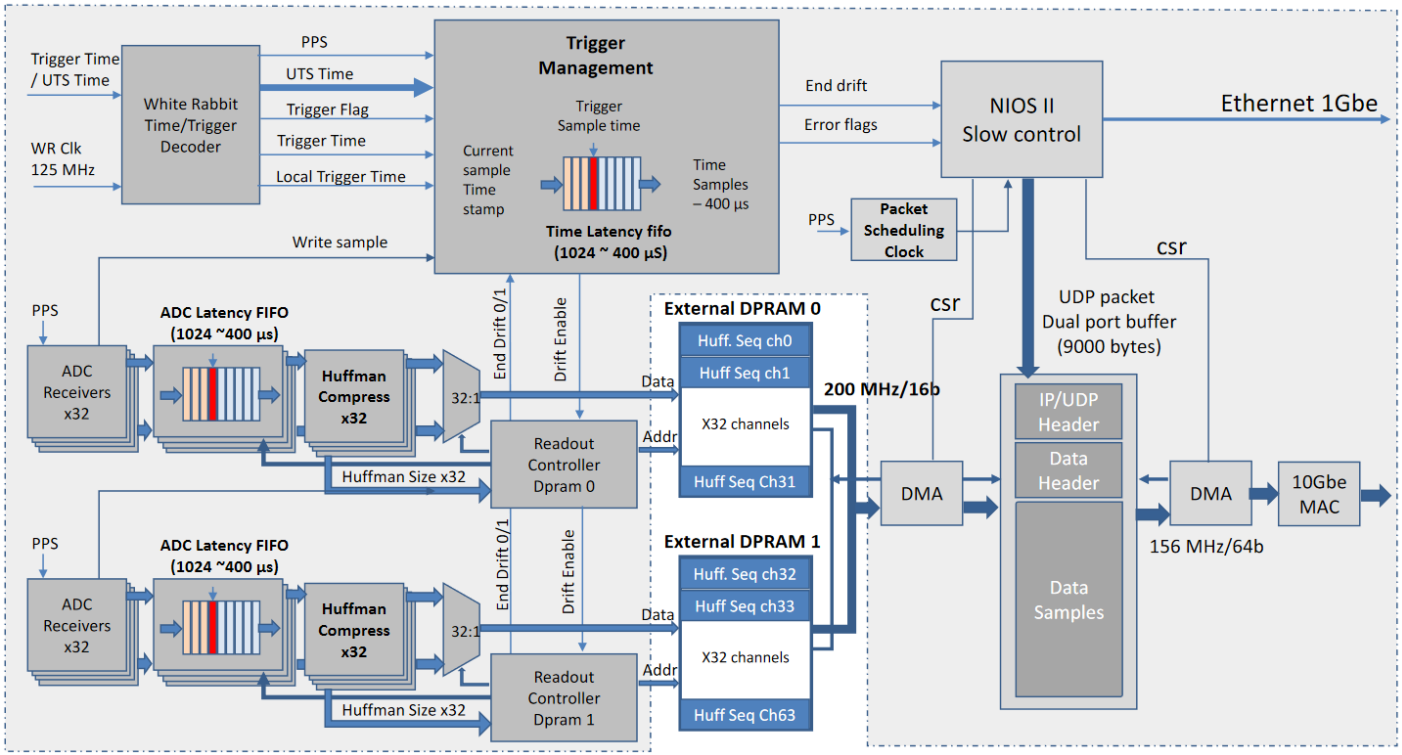
- In continuous streaming of 12 bit data at 2 MSPS each AMC generates **1.5 Gbit/s**
- For each uTCA crate (x10 AMCs) : **15 Gbit/s**
- In ProtoDUNE – DP uTCA MCH had a bandwidth of 10 Gbit/s
  - Data losslessly compressed with Huffman algorithm in real-time in AMCs
  - Minimally only a modest compression factor of ~2 needed
- Now uTCA with MCH bandwidth of 40 Gbit/s are available at no extra cost → no compression needed

- For FD2-VD the baseline is uTCA with 40 Gbit/s MCH




40 Gbps crate at IP2I Lyon
(MCH-40G-XAUI)

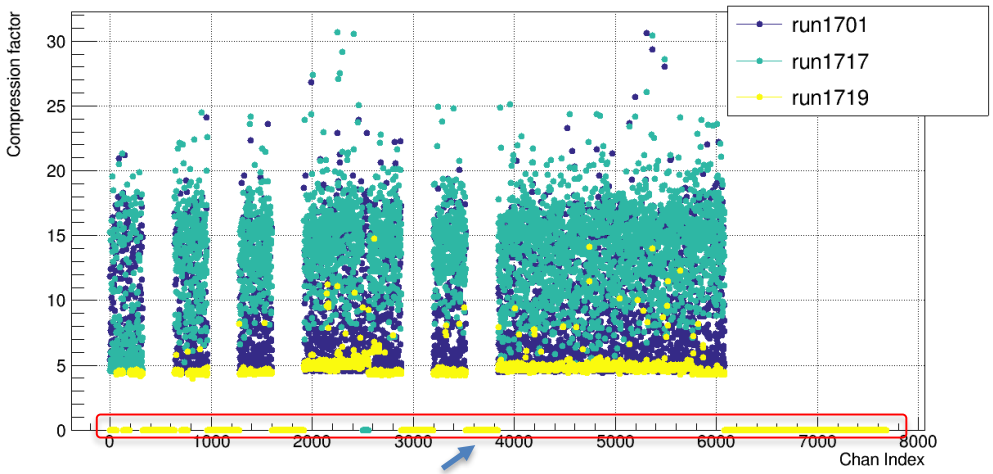
# Huffman Compression FW



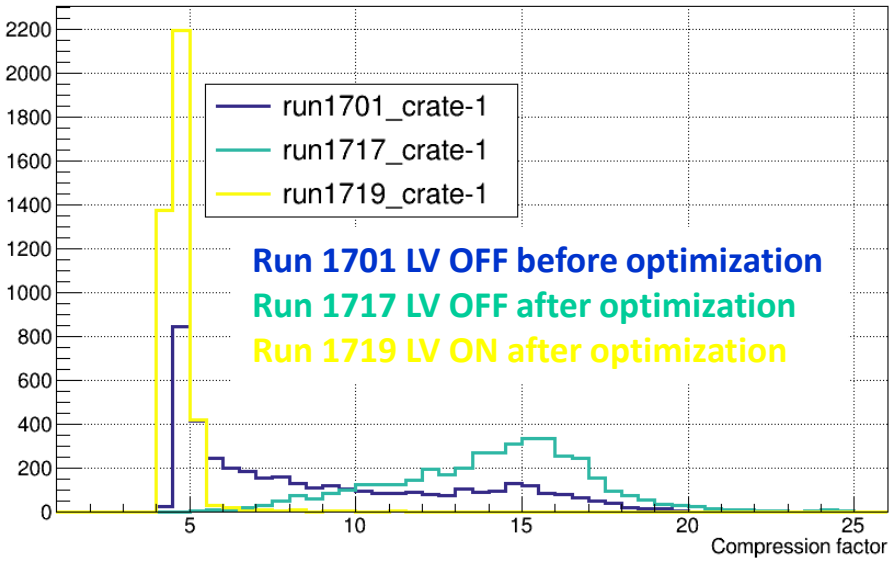

- Data compressor runs in real-time on AMCs (a compressor block per each channel)
- Tested with a decompressor receiving data on Stratix V FPGA bittware board
- Decompression FW and search for trigger primitives in real-time using Bittware with Arria 10 FPGA board (Q. David, DUNE GM)

# AMC Compression FW at NP02

- At the end of NP02 run (in August 2020) deployed AMC firmware with Huffman compression
- Procedure to maximize compression factor by moving channel baseline closer to an ADC code (ADC offset adjustment) → less codes to compress
  - Average compression factors ~14
- With analog front-ends powered (additional noise from detector), average compression factor ~5




Non instrumented CRP channels



# Slow control

In addition to MCH, uTCA crate contains a PS and two cooling units

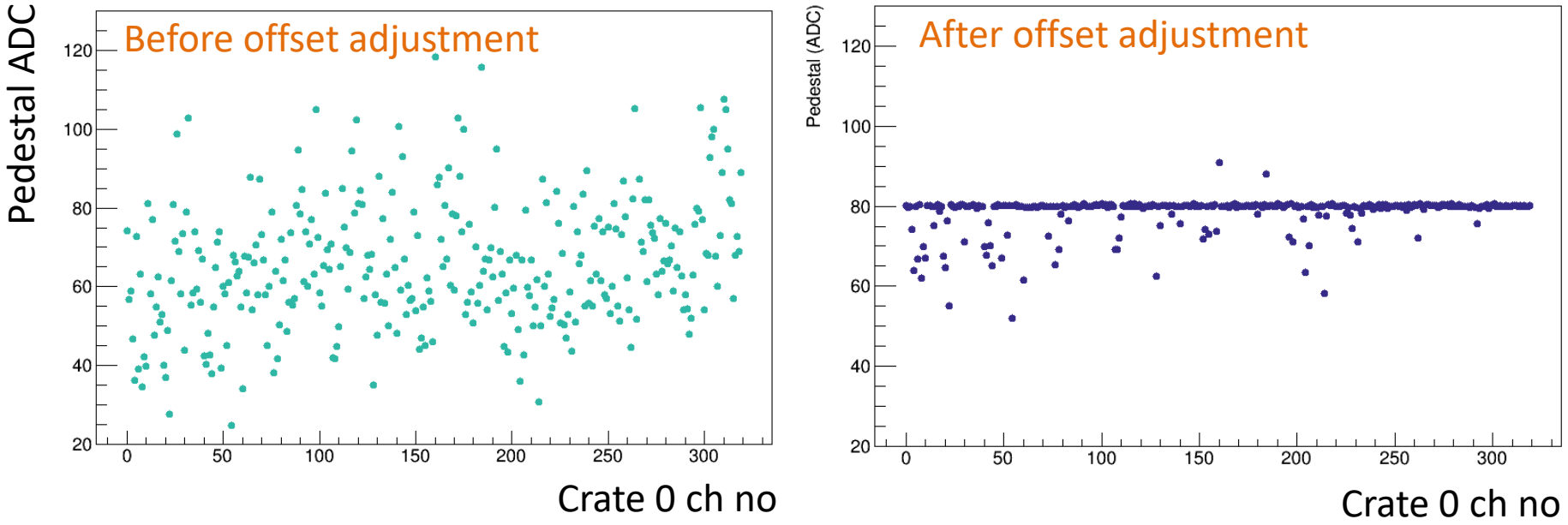
```
nat> show_pm
-------------------------------------------------------------
PM1: - online, primary(fru 50)     : budget 50.0 A (alloc 49.0 A avail 1.0 A)
PM2: - unknown
PM3: - unknown
PM4: - unknown
|-----------------------------------------------------------|
|chan  FRU FruId  primPM  secPM  PS1  POn  ENA   MP  PP  Amps |
|-----------------------------------------------------------|
  1   MCH1     3   1       -      y    y    y     y   y   4.0
  2  AMC13    30   1       -      y    -    y     y   y   6.0
  3    CU1    40   1       -      y    -    y     y   y   7.0
  4    CU2    41   1       -      y    -    y     y   y   7.0
  5   AMC1     5   1       -      y    -    y     y   y   2.5
  6   AMC2     6   1       -      y    -    y     y   y   2.5
  7   AMC3     7   1       -      y    -    y     y   y   2.5
  8   AMC4     8   1       -      y    -    y     y   y   2.5
  9   AMC5     9   1       -      y    -    y     y   y   2.5
 10   AMC6    10   1       -      y    -    y     y   y   2.5
 11   AMC7    11   1       -      y    -    y     y   y   2.5
 12   AMC8    12   1       -      y    -    y     y   y   2.5
 13   AMC9    13   1       -      y    -    y     y   y   2.5
 14  AMC10    14   1       -      y    -    y     y   y   2.5
 15  AMC11    15   1       -      -    -    -     -   -
 16  AMC12    16   1       -      -    -    -     -   -
|-----------------------------------------------------------|
```

```
nat>
nat> show_sensorinfo 61
Sensor Information for FRU 61 / HUB1
=============================================================================
  #   SDRType  Sensor Entity Inst  Value    State     Name
-----------------------------------------------------------------------------
  -   MDevLoc          0xc2  0x64                    HUB-MCH-40G
  1   Full     Voltage 0xc2  0x64  0.988 V    ok      1.0V
  2   Full     Voltage 0xc2  0x64  1.118 V    ok      1.0V-AVS
  3   Full     Voltage 0xc2  0x64  1.092 V    ok      1.1V
  4   Full     Voltage 0xc2  0x64  1.196 V    ok      1.2V
  5   Full     Voltage 0xc2  0x64  1.807 V    ok      1.8V
  6   Full     Voltage 0xc2  0x64  3.381 V    ok      3.3V
  7   Full     Voltage 0xc2  0x64  12.40 V    ok      12V
```

- uTCA MCH switch runs a basic operating system, which allows to monitor and control crate functionality
- Accessible remotely (ssh / telnet / ipmi)
- Extensive functionality:
  - Reboot crate or power cycle each AMC individually
  - Check temperatures, power consumption, etc.
  - Show status of links / ports
  - More administrative functions (e.g., network configuration)
  - …
- Crates are connected on DAQ network
  - In NP02 needed to tunnel through the L1 machine to access the crates

# ADC Pedestal Adjustment

*Pedestal offset adjustment with ADC adjustment control in NP02*




- The pedestals have a ch-to-ch dispersion on the order of 10 ADC RMS
- AD9257 allows to program an offset (-128 → 127 in 14bit resolution) to each channel independently that can be done by slow control

# DUNE AMC version

- AMC components obsolescence monitoring → PCB layout updated
- Minor changes for obsolescence:
  - Replacement of firmware flash memory with equivalent chip
- In addition:
  - Redefinition of ADC level for bi-polar signal dynamics
  - Removal of some minor unused components and small simplifications/optimizations in view of large production
  - Considering replacement of IDT/FPGA with models of same series with slightly different performance depending on further optimization cost opportunities

# Conclusions

- FD2-VD top digital electronics is at room temperature on the roof of the cryostat completely accessible
- Used extensively in NP02 and also 3x1x1 LArTPC DP prototype
- Flexibility in FPGA configuration: firmware can be flashed over network to all (or some selected) AMCs in a crate
- Minor adaptations of exiting AMC board layout: take into account component obsolescence and additional improvements

# Extra

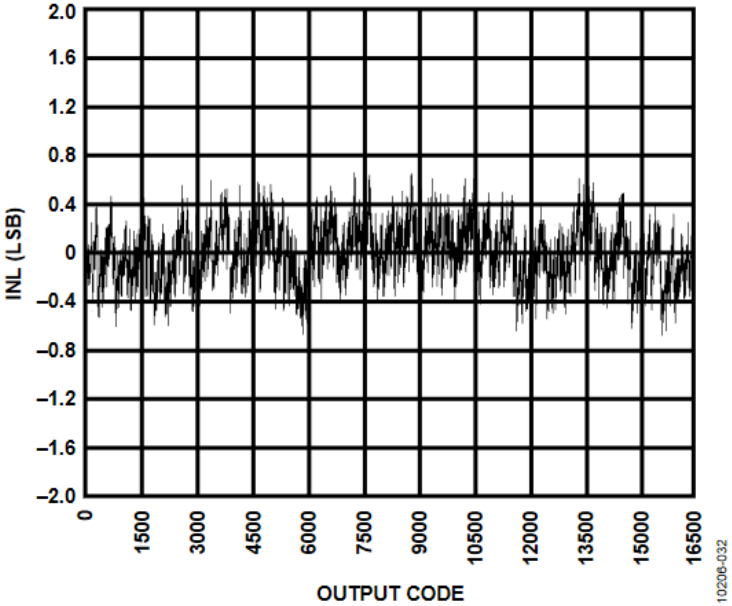



Figure 33. INL, $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 40 MSPS

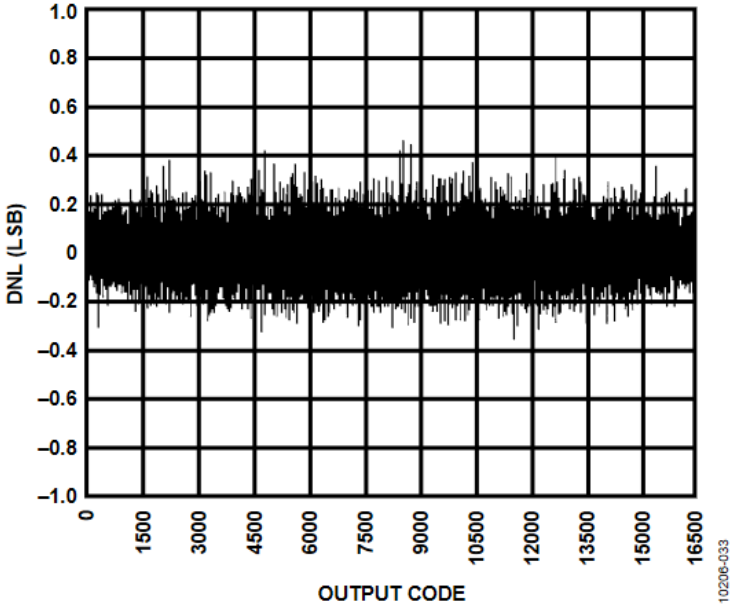



Figure 34. DNL, $f_{IN}$ = 9.7 MHz, $f_{SAMPLE}$ = 40 MSPS