Top Electronics Production & QC

Vyacheslav Galymov (IP2I Lyon)

FD2-VD CDR Review

June 4, 2021

Top Electronics Production

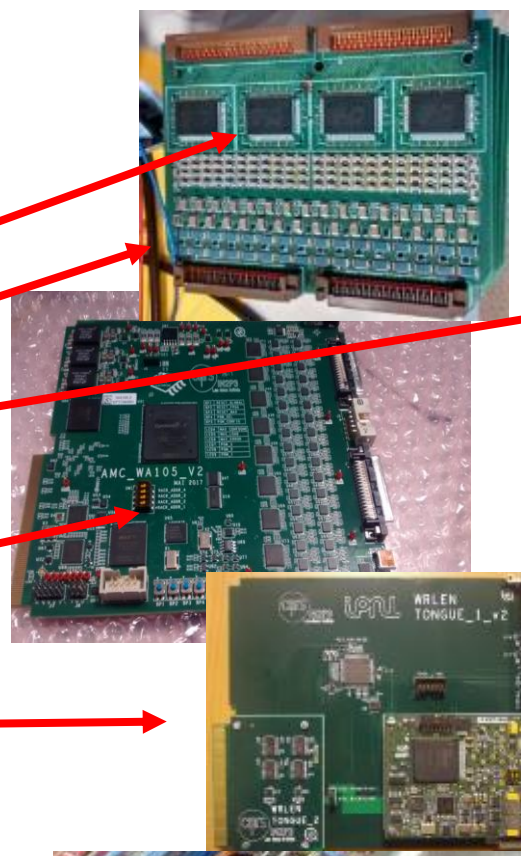
Total number of channels to read: **256k**

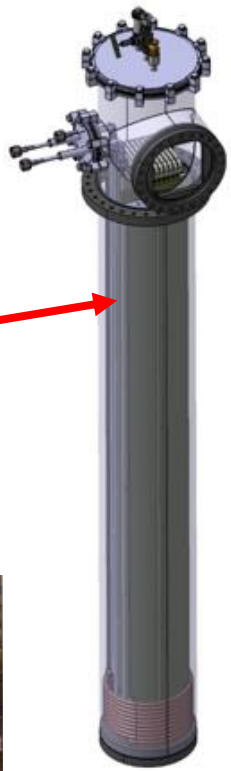
Analog:

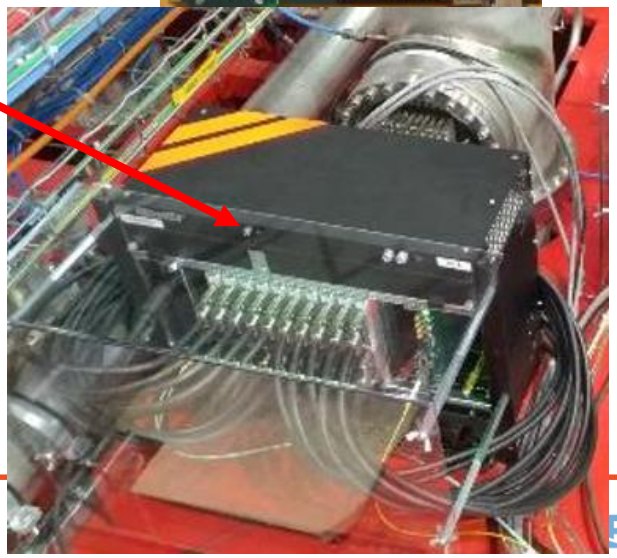
- Cryogenic ASICs (16 ch): 16000
- Cryogenic FE cards (64 ch): **4000**
- 50 Cards Chimneys: **105**

Digital:

- AMC cards (64 ch): **4000**
- uTCA White Rabbit MCH: 400
- uTCA crates (including MCH,PU,FU): **400**
- 40 Gbe optical links to backend: 400







The top-drift CRPs electronics is based on **two main elements** with **64 ch modularity**:

- **The analog cryogenic FE cards** accessible via the chimneys → **4000 units**
- **The AMC digitization cards** in the uTCA crates → **4000 units**

Production assumptions

- Production of different items: FE cryogenic cards, AMC cards, uTCA crates, cables and chimneys **can be completely parallelized**
- Minimal technical **production** + tests **time for all items is of the order of one year**
- Productions will be anticipated and spread between 2023-2026 in order to have an **even time profile and safety margins**
- **QC tests are pipelined with production** (in batches) with a delay of 1-2 months

Production timeline

- **PRR Sep-Oct 2023 → Productions can be started**
- **Ready for installation milestone (3 months before installation) → Jul 2026**
- **Periods for production with pipelined QC (2023-2026):**

• AMC digitization cards:	Dec 23 - Jun 25
• Cryogenic ASICs & FE cards:	May 24 - Dec 25
• Timing end-nodes:	Jul 24 – Jan 25
• uTCA crates:	Jul 24 - Jun 25
• Chimneys:	Jan 25 – Feb 26
• Cabling:	Oct 24 – Mar 26

Electronics Production QC

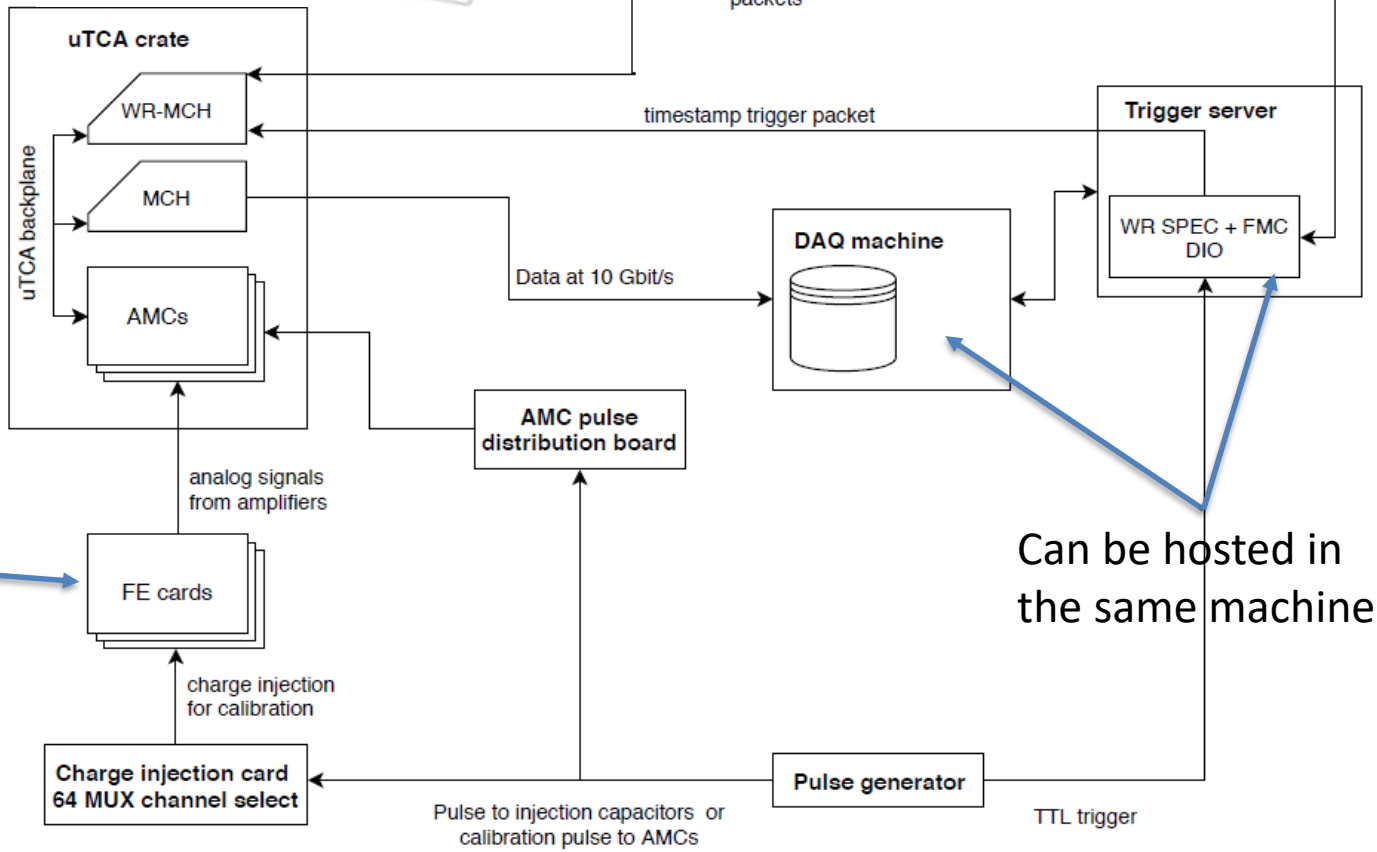
- Well-defined QC scheme based on the experience from NP02 production
  - For NP02 120 analog FE cards + 120 AMCs were tested at IP2I Lyon
  - Also used to validate small FE analog card production for cold-box test
- QC tests are foreseen to mainly happen in France with possible external contributions from Japanese and US groups
- Equipping a site to carry out QC tests requires an investment of <30 kEuro (k$) for equipment

Electronics test bench scheme

From DP-TDR

Meinberg LANTIME

Seven Solutions
White Rabbit switch

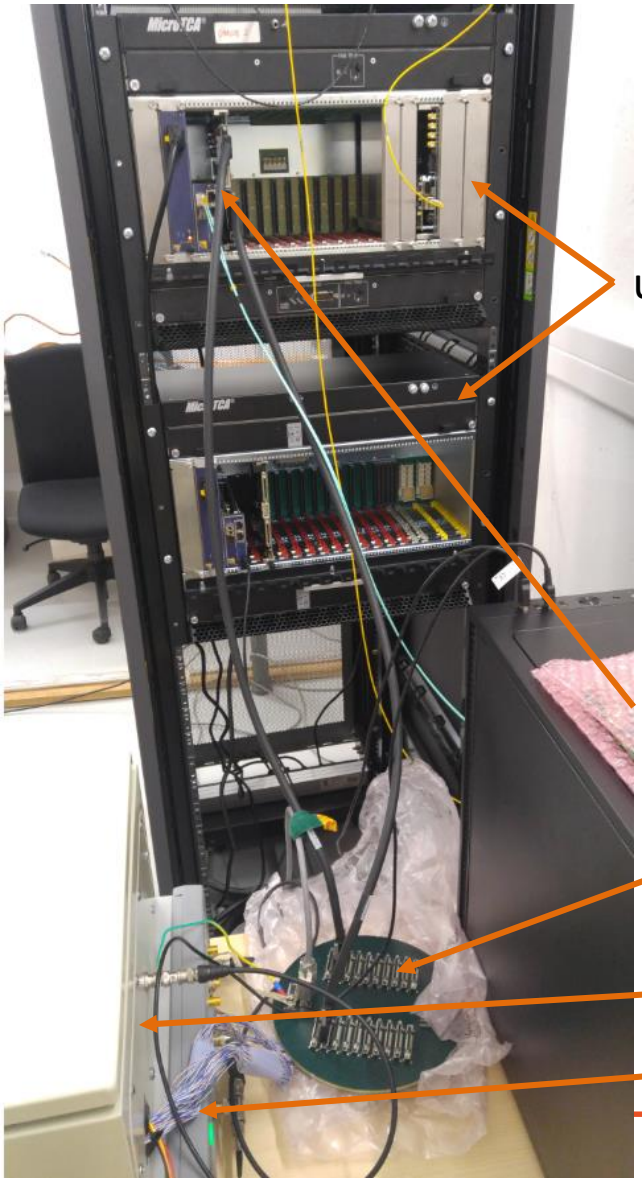


+LV system to power the FE cards

Can be hosted in the same machine

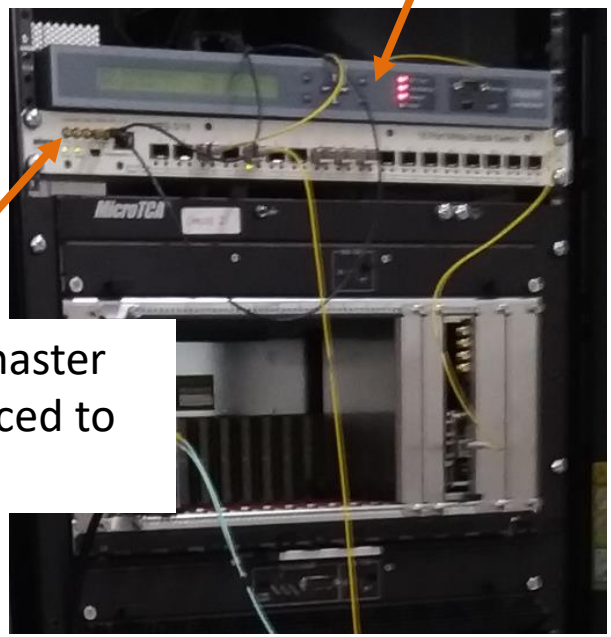
Electronics test bench

Current set-up at IP2I Lyon



uTCA crates

GPSDO (Meinberg LANTIME M600) clock reference



WR switch grandmaster keeps all units synced to the same clock

AMC with VHDCI cables connected to warm flange

Warm flange PCB

Analog FE & calibration cards in a shielding box

Pulse generator (Keysight 81150A)

Electronics test bench

Current set-up at IP2I Lyon

Analog card with pre-amplifier card

Charge injection card :

- 32 inj capactiors mechanically tunable
- MUX switch controllable via SPI to distribute the pulse signals from generator

Parts of flat cable are still exposed (normally inside the chimneys)

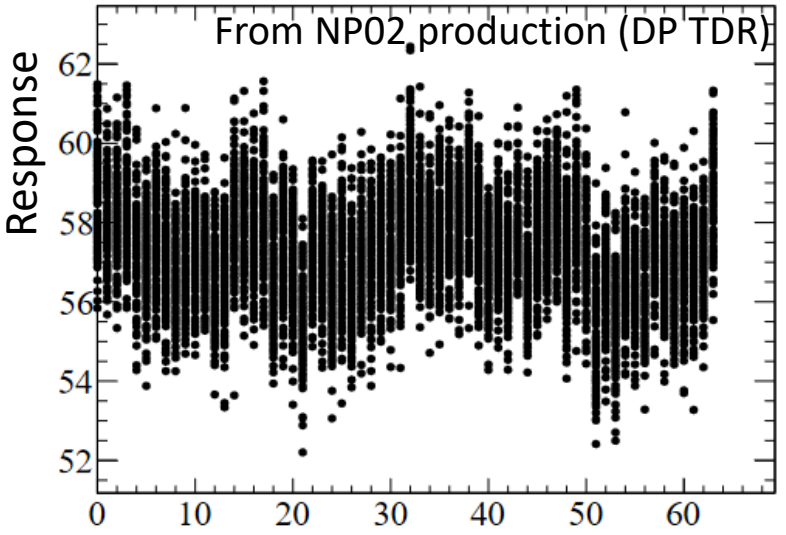
All equipment is connected to a common building ground (noisy)

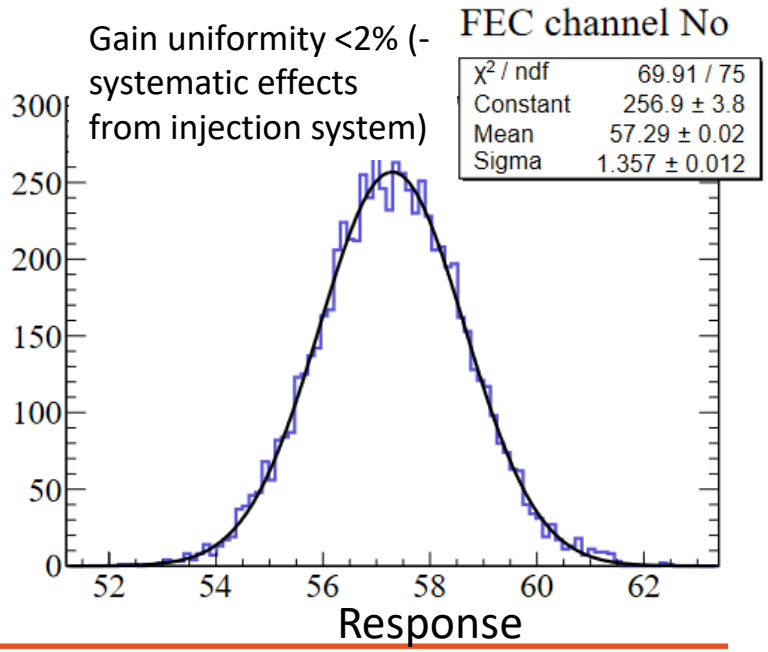
➔ Add insulation transform

Not an optimal low noise environment, but workable

QC for analog pre-amplifier cards

- Simple boards that require only check of signal continuity
- Inject charge via external calibration board (like the one shown on the previous page)
  - Check signal continuity
  - Check the dispersion between channels
- In NP02 production helped identified all poorly mounted components (the manufacturer had poor quality control)
- No issues with manufacturer with the cards produced for cold box tests





AMC commissioning & QC chain

1. Loading MMC firmware (enables power negotiation for each card)
   - Takes 15 min / AMC
   - Start monitoring of power consumption

Need physical access to a JTAG interface on each AMC
➔ To be done (once) at a given test site after card reception

AMC commissioning & QC chain

1. Loading MMC firmware (enables power negotiation for each card)
   - Takes 15 min / AMC
   - Start monitoring of power consumption
2. Programming of the operation firmware into flash
   - Takes 20 min / crate (parallelized for 10 cards)

Need physical access to a JTAG interface to load a base “factory” version on each FPGA (this is very fast O(20s) per card) in order to allow loading of firmware (factory & operation) into flash via XAUI link (network)

➔ To be done only once

Once a version of a factory firmware had been programmed into flash can do updates remotely via network

```
1 Gigabit Ethernet interface:   static IP-address 10.73.32.1
Server IP address  10.73.32.129
10 Gigabit Ethernet interface    static IP-address 10.73.32.1
PHY RESET Done  : PCS control register = 1140
PCS status register = ad
.Arp reply from 10.73.32.129
Destination MAC is 3c:fd:fe:c9:2f:f0
*******************************************
*  WA105 6x6x6 CYCLONE V AMC  IPNL        *
*  NIOS2 software Release 11/02/2019      *
*    - Drift = 10000 (IDT)                *
*    - 9000 bytes Jumbo Frames            *
*    - Packet Sync Period                 *
*    - Cache bypass on ip_header memory   *
*    - Server Address based on shelf number  *
*******************************************
*  Firmware Configuration:
*  [10Gb Eth Link XAUI]
*  [CERN_SERVER_IP]  (10.73.32.129)
*  [LARGUI_DAQ]
*  [JUMBO_FRAMES]
*****************************************
SG-DMA openned successfully !
Descriptor memory allocation succesfull !
tx_frame_max_lenght = 9026
rx_frame_max_lenght = 9026
RX 10G macaddr0 = eda2010d
RX 10G macaddr1 = 7
Verifying ADCs ...
Read ADC Chip Id(0x1):                  [OK]
Read ADC Speed Grade(0x2):              [OK]
Read ADC Sample Rate (0x100):           [OK]
Read ADC Serial Control (0x21):         [OK]
Read ADC Output Mode(0x14) :            [OK]
Data Aligned Reg 0 = ffffffff
Data Aligned Reg 1 = ffffffff
Read ADC Data Aligned_0 Status:         [OK]
Read ADC Data Aligned_1 Status:         [OK]
Read ADC Test Mode(0x0D):               [OK]
Verifying timing status ...
Read WRLEN BitSlip :                    [OK]
Read WRLEN Amc_Tm_Time_Valid :          [OK]
 (retry=0)ADC Board initialized !
```

- After DUNE FW is loaded, the card can be booted
- During boot cards run basic diagnostics. This can be monitored via a serial port

AMC commissioning & QC chain

1. Loading MMC firmware (enables power negotiation for each card)
   - Takes 15 min / AMC
   - Start monitoring of power consumption
2. Programming of the operation firmware into flash
   - Takes 20 min / crate (parallelized for 10 cards)
3. Pedestal acquisition
   - Fast checks of basic functionality
   - Allowed to identify all problematic AMCs in production for NP02
4. Calibration of ADC buffer

Conclusions

- Production of components can be completely parallelized
- From experience with NP02 the requirements for QC procedure are well-defined
- Tests can be carried at multiple sites with some very modest investment for the required equipment and are pipelined with the production