SLDO Irradiation

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RD53B testing meeting

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SLDO irradiation procedure

• Started irradiating a V1.1 chip in shunt LDO mode
• During irradiation:
  • Read ring oscillators
  • Monitor all of the voltages on the analog monitoring card
  • Monitor from MUX: Vina, Vind, Voff, Vdda, Vddd, IGND, Iana_I, lana_S, Idig_I, Idig_S, Iref, VrefADC, GND
• SLDO measurements every 10 Mrad:
  • VI curves → powercycling at each step
  • Use low power config for VMUX reading → check that chip configures
• Once a day:
  • Power-up @ low temperature (-20 C)
  • Check under-shunt protection
First look at SLDO curves

• Irradiation up to ~300 Mrad so far
• Slopes of Vin stay very consistent
• Start-up behaviour is changes slightly
• Chip is not configured → VDDA/VDDD in these curves is not trimmed

→ Increase in VDDA and VDDD
First look at SLDO curves

- Other chip voltages also increase with irradiation
- In particular VrefADC should explain the increase in VDDA and VDDD
- Also monitored temperature during startup

![Graphs of VrefADC, VDD_PRE, Temperature, VrefA, VrefD](image-url)
Cold start-up test

- In the irradiation setup, cool down the chip to -20 C (unpowered) and take VI curve
- Powercycle at each step and let cool down to -20 before each measurement point
- Nothing concerning visible yet
Conclusions

- Irradiation of ITkPixV1.1 in SLDO mode ongoing, collected 300 Mrad of dose
- No operational issues and no striking features observed in the VI curves so far
- Analysis of data ongoing – lots more data to analyse (monitoring of voltages/currents during irradiation, ring oscillators, under-shunt protection with irradiation)
- Will keep going until at least 500 Mrad (though there’s currently no time constraints on the use of the X-ray system, so possible to keep going until 1 Grad)
Thank you!

Questions?
Additional Slides