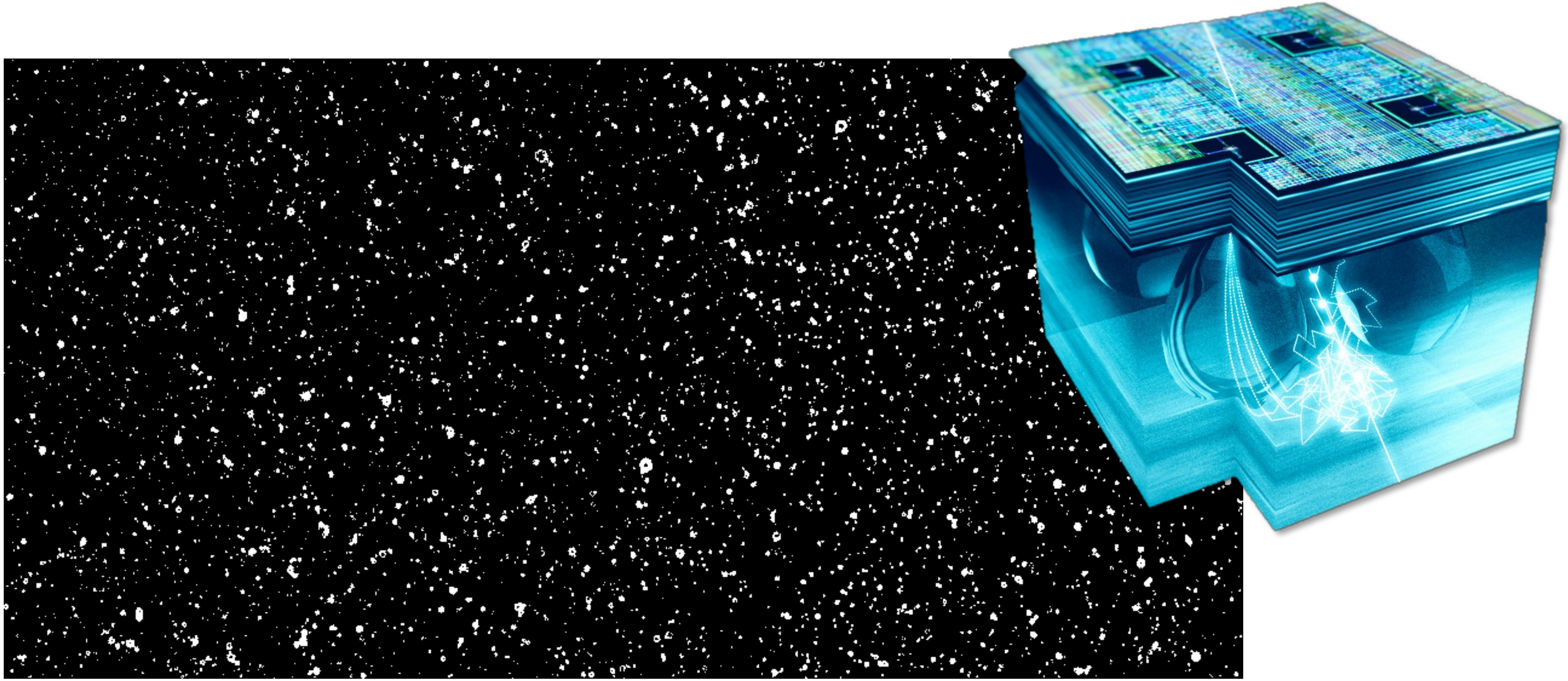
CMOS detectors for FCCee trackers



ALPIDE prototype: 200 MeV protons at PSI

W. Snoeys

Geneva, Switzerland

Fostering Swiss collaboration towards a future circular collider September 7th, 2021

Acknowledgements

- The workshop organizers
- T. Kugathasan, G. Aglieri, E. Buschmann, M. Campbell, T. Kugathasan, M. Muenker, K. Dort, J. Hasenbichler, L. Musa, H. Pernegger, P. Riedler, N. Guerrini, C. Hu, P. Giubilato, D. Dannheim, T. Hirono, I. Peric, A. Schoening
- S. Parker, C. Kenney, J. Plummer, J. Segal
- G. Anelli, F. Anghinolfi, P. Aspell, R. Ballabriga, S. Bonacini, M. Campbell, J. Christiansen, R. De Oliveira, F. Faccio, P. Farthouat, E. Heijne, P. Jarron, J. Kaplon, K. Kloukinas, A. Kluge, T. Kugathashan, X. Llopart, A. Marchioro, S. Michelis, P. Moreira, F. Vasey, K. Wyllie, M. Mager, M. Keil, D. Kim, A. Dorokhov, A. Collu, C. Gao, P. Yang, X. Sun, H. Hillemanns, S. Hristozkov, A. Junique, M. Kofarago, M. Keil, A. Lattuca, M. Lupi, C. Marin Tobon, D. Marras, M. Mager, P. Martinengo, S. Mattiazzo, G. Mazza, H. Mugnier, H. Pham, F. Piro, L. Cecconi, W. Deng, G. H. Hong, J. De Melo, J. Rousset, F. Reidt, P. Riedler, J. Van Hoorne, P. Yang, D. Gajanana, A. Sharma, B. Blochet, C. Sbarra, C. Solans Sanchez, C. Riegel, C. Buttar, D. Michael Schaefer, D. Maneuski, I. Berdalovic, K. Moustakas, M. Dalla, N. Wermes, N. Egidos Plaja, R. Bates, R. Cardella, T. Wang, T. Hemperek, C. Bespin, T. Hirono, W. Wong, G. Iacobucci, M. Barbero, P. Pangaud, A. Habib, S. Bhat, S. Grinstein, Y. Degerli, F. Guilloux, P. Schwemling, W. Riegler, E. Schioppa, V. Dao, L. Flores, M. Dyndal, C. Colledani, M. Winter, A. Dorokhov, S. Bugiel, S. Mathew, I. Sedgwick, C. Reckleben, K. Hansen, V. Gromov, D. Gajanana, R. Kluit, Y. Kwon, …

and other colleagues from CERN, the ALICE ITS upgrade, ATLAS Itk, WP1.2 …

walter.snoeys@cern.ch

CMOS Monolithic Active Pixel Sensors revolutionized the imaging world

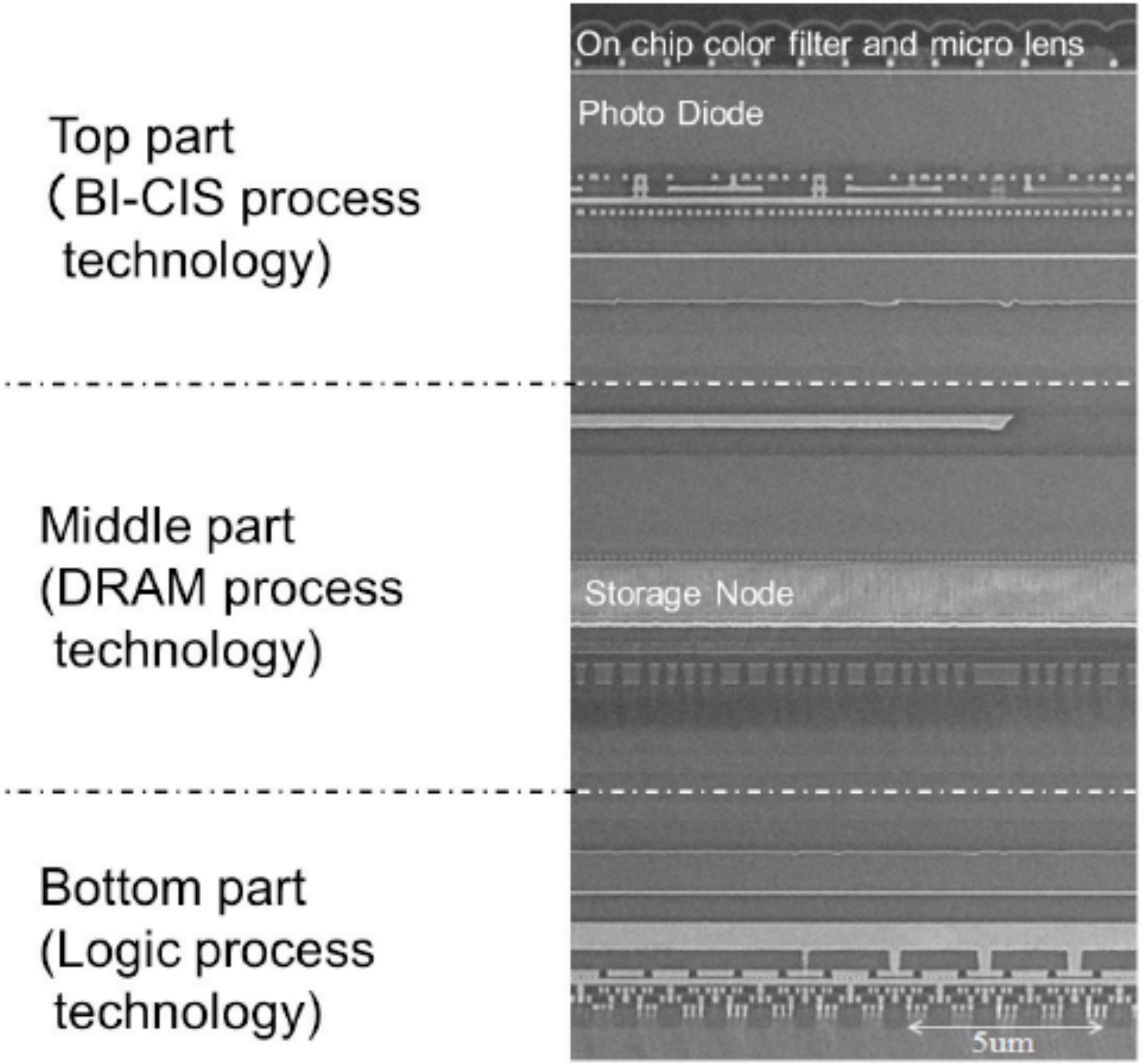
reaching:

- less than 1 e^- noise
- > 40 Mpixels
- Wafer scale integration
- Wafer stacking
- …

Silicon has become the standard in tracking applications both for sensor and readout

… and now CMOS MAPS make their way in High Energy Physics !

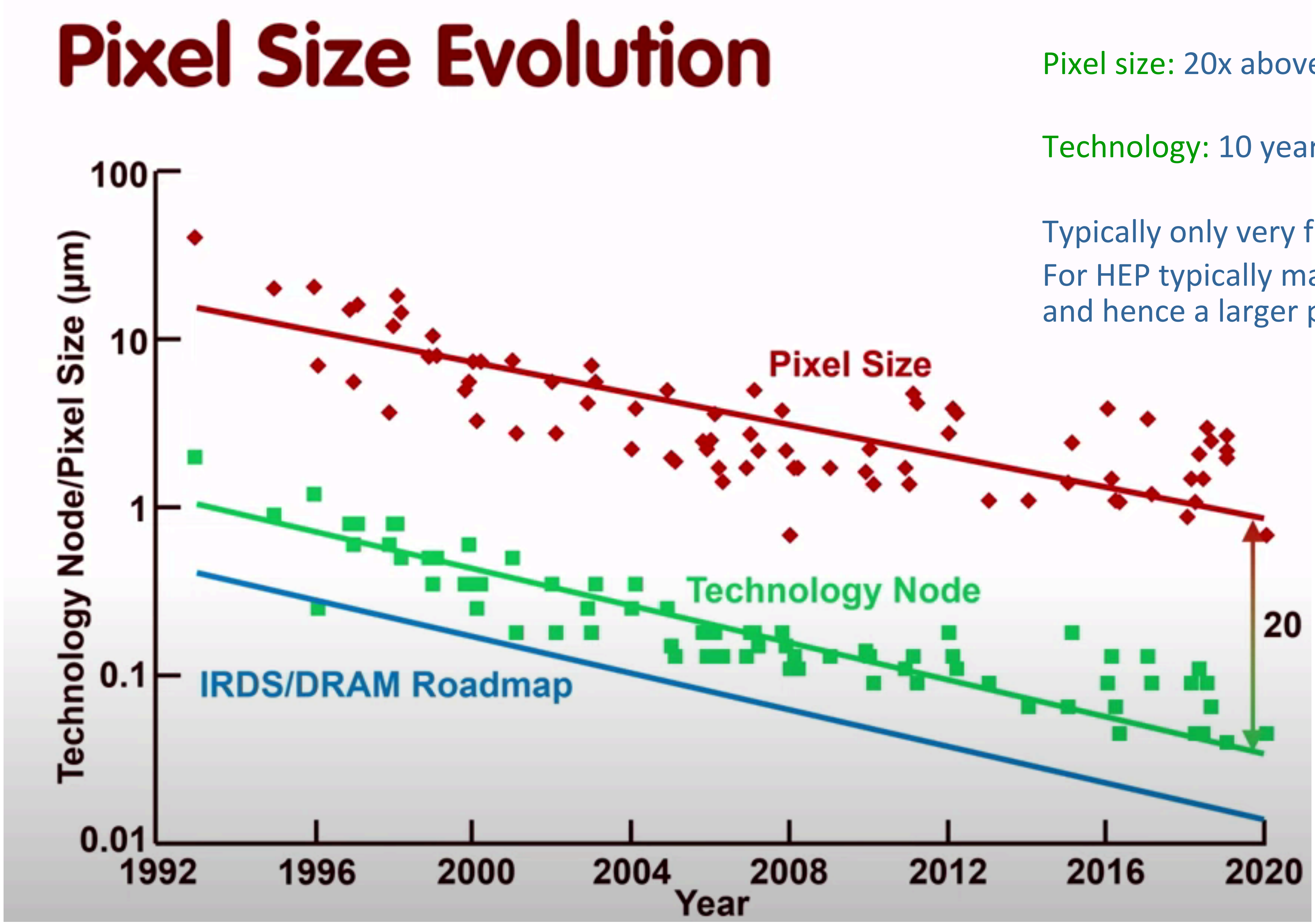
Hybrid still in majority in presently installed systems



Sony, ISSCC 2017

New technologies (TSV’s, microbumps, wafer stacking…) make the distinction more vague.

Evolution of pixel size and technology node for visible:



Pixel size: 20x above technology feature size

Technology: 10 years behind DRAM technology

Typically only very few (1-4) transistors per pixel,
For HEP typically many more transistors per pixel,
and hence a larger pixel.

Albert Theuwissen, ISSCC 2021

Requirements for High Energy Physics

	Dose (Mgy)	Fluence (10^{16} 1MeVn_{eq}/cm^2)
ALICE ITS	0.01	10^{-3}
LHC	1	0.1…0.3
HL-LHC 3ab^{-1}	5	1.5
FCC	10-350	3-100

Radiation tolerance

- CMOS circuit typically more sensitive to ionizing radiation
- Sensor to non-ionizing radiation (displacement damage)

Single particle hits instead of continuously collected signal in visible imaging

- Sparse images < or << 1% pixels hit per event
- Near 100% efficiency, full CMOS in-pixel needed, often circuit (much) more complex

Position resolution (~µm)

Low power consumption is the key for low mass

- Now tens of mW/cm^2 for silicon trackers and hundreds of mW/cm^2 for pixels
- Despite enhanced detector functionality for upgrades, material penalty limits power consumption increase

More bandwidth

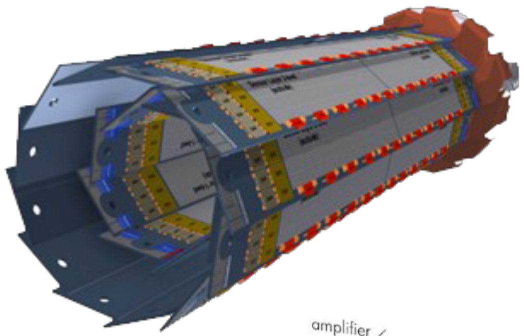
Time resolution

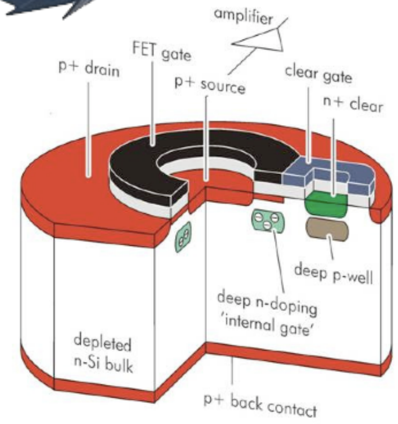
- Time stamping ~ 25 ns or even lower, ... much lower (10s of ps)

Larger and larger areas

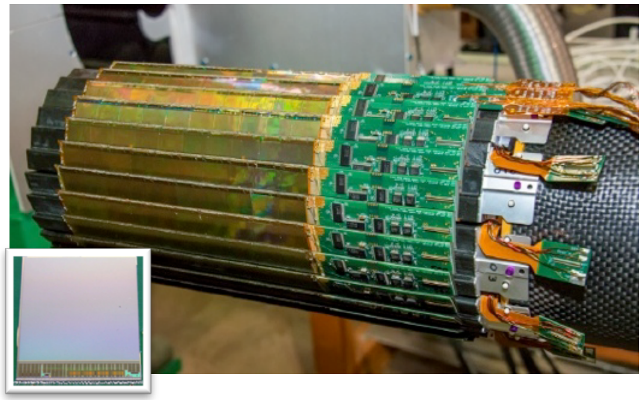
- ALICE ITS2 10 m^2, discussions on hundreds to even thousands square m^2,
- Interest for versatile sensors programmable for different applications (P. Allport CERN EP seminar 2020)

Monolithic sensors in HEP move into mainstream technology





DEPFET in Belle



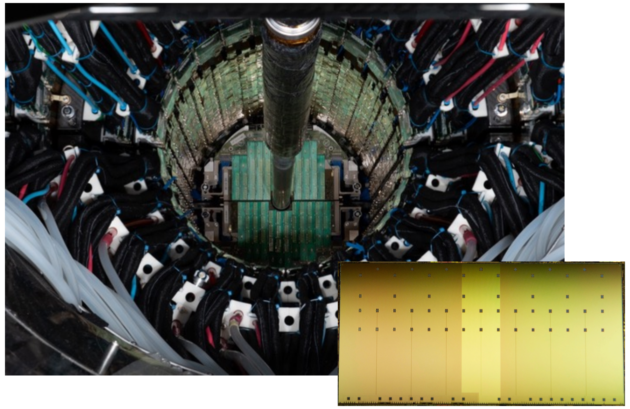
MIMOSA28 (ULTIMATE) in STAR

IPHC Strasbourg

First MAPS system in HEP

Twin well 0.35 µm CMOS

- Integration time 190 µs
- No reverse bias -> NIEL few 10^{12} 1 MeV n_{eq}/cm^2
- Rolling shutter readout



ALPIDE in ALICE

First MAPS in HEP with sparse readout similar to hybrid sensors

Quadruple well 0.18 µm CMOS

- Integration time <10 µs
- Reverse bias but no full depletion -> NIEL ~10^{14} 1 MeV n_{eq}/cm^2

DEPLETED MAPS for better time resolution and radiation tolerance

Large collection electrode

LF Monopix, MuPix,…

Extreme radiation tolerance and timing uniformity, but large capacitance

Small collection electrode

ARCADIA LF, TJ Malta, TJ Monopix, Fastpix, CLICTD, …

- Sub-ns timing
- NIEL >10^{15} 1 MeV n_{eq}/cm^2 and beyond

Commercial deep submicron CMOS technology evolved "naturally" towards

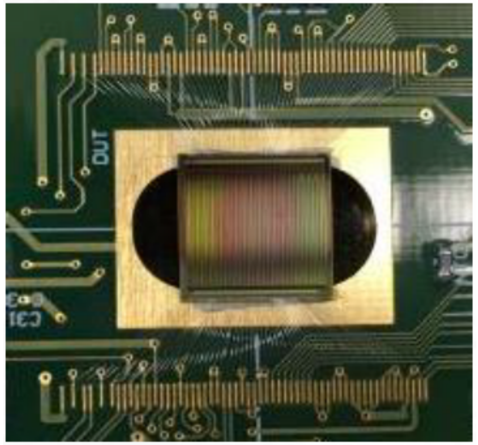
- Very high tolerance to ionizing radiation (some caveats, cfr G. Borghello, F. Faccio et al.)
- SEU protection by triplication and majority voting
- Availability of substrates compatible with particle detection
- Imaging technology not absolutely required, but some flexibility/features very beneficial for sensor optimization, both for small and large collection electrode structures.

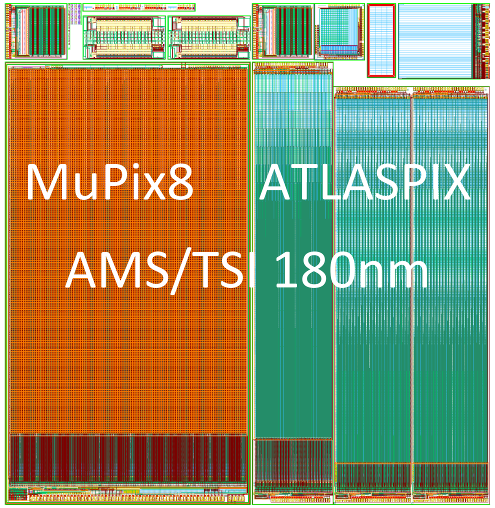
Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but larger C (100fF or more)


MONOPIX

50 x 250 µm^2 pixel

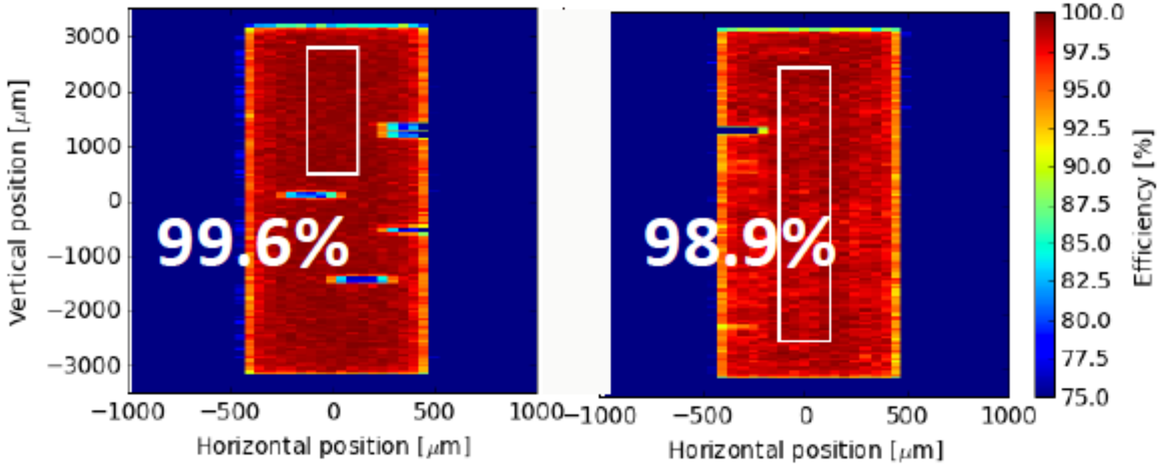
Lfoundry 150 nm



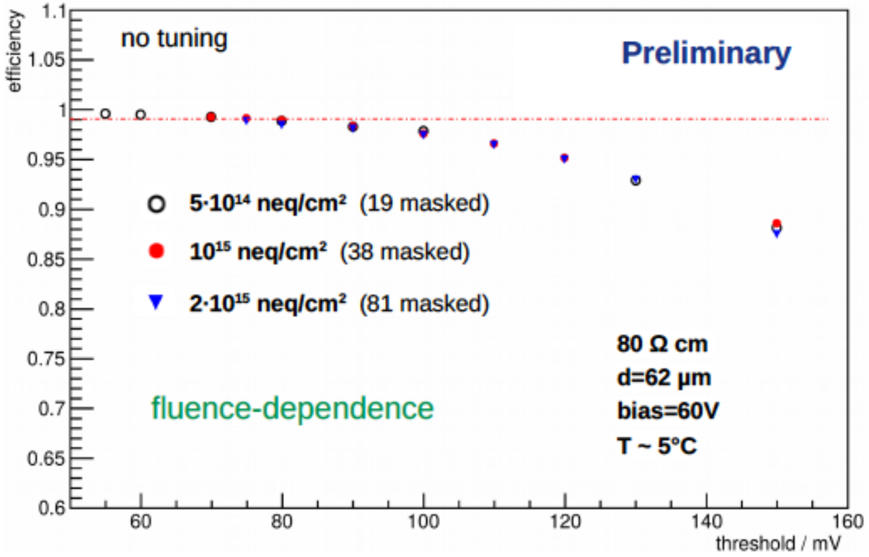

MuPix8 ATLASPIX

AMS/TSI 180nm

Efficiency non-irradiated **after 1.14 E15 n_{eq}/cm^2**



T. Hirono et al., https://doi.org/10.1016/j.nima.2018.10.059



Courtesy I.Peric and A. Schoening

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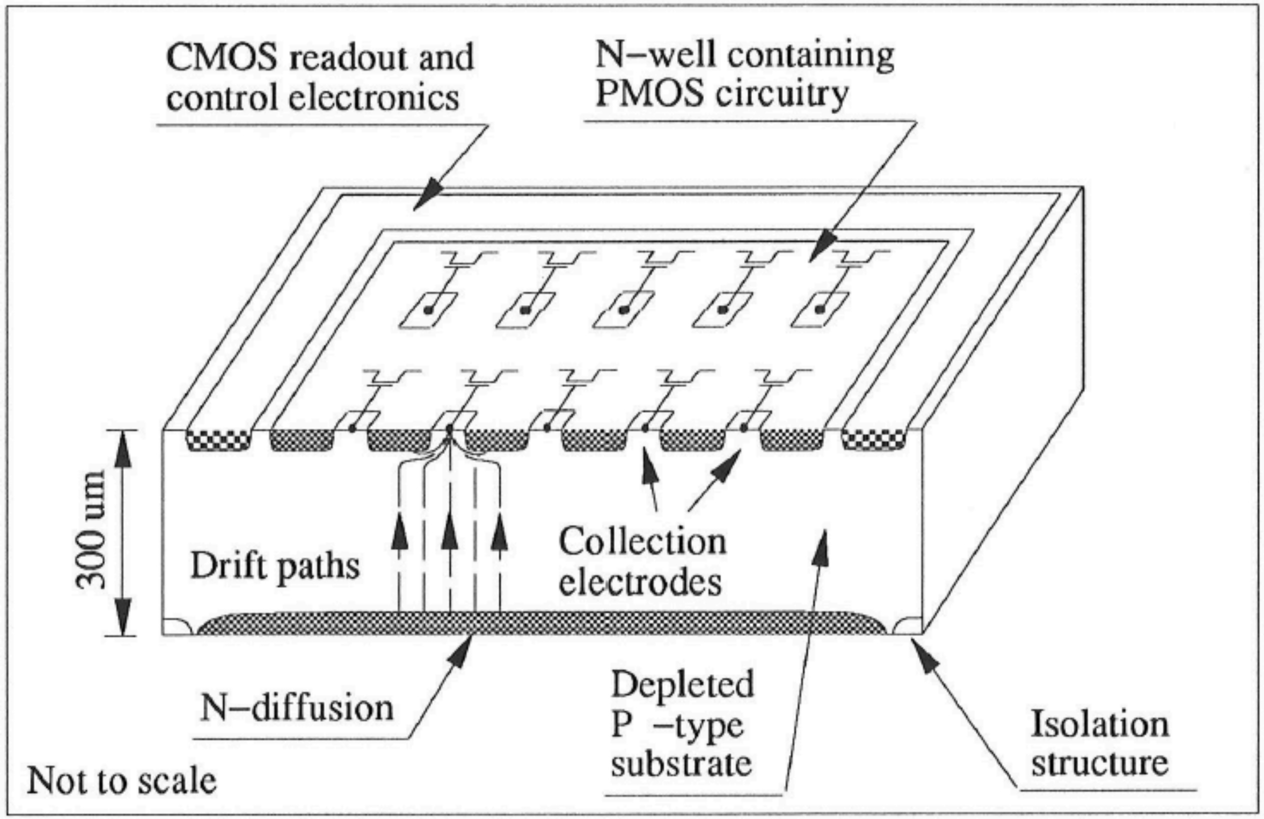
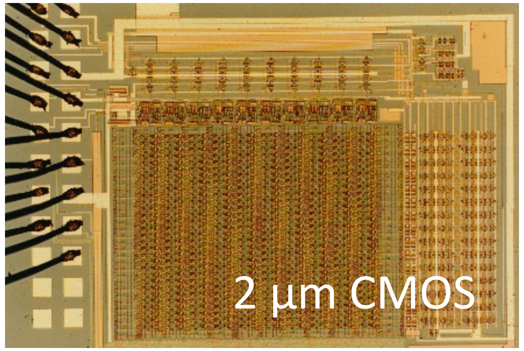
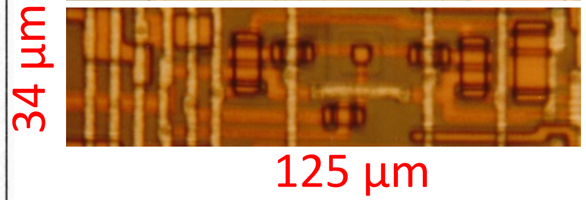
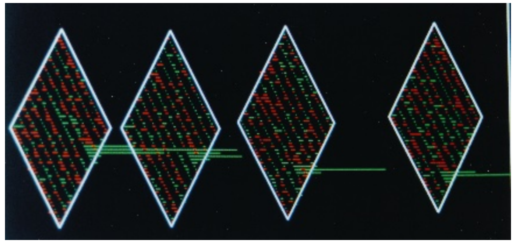
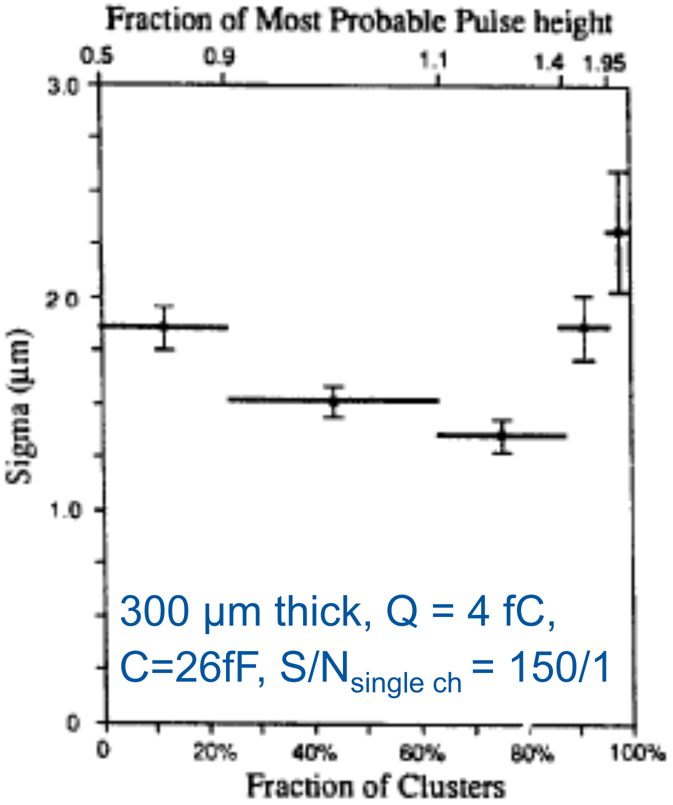
Towards standard technology, but double-sided processing





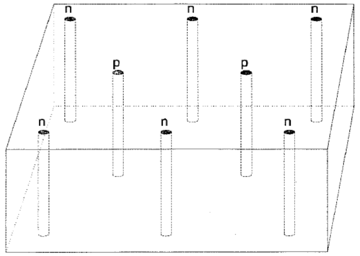






300 µm thick, Q = 4 fC, C=26fF, $S/N_{\text{single ch}}$ = 150/1

- Separation of junction from collection electrode
- Better than 2 µm position resolution even at large pitch due to good S/N
- Improved back side isolation with trenches lead to sensors with 3D electrodes (S.Parker) →

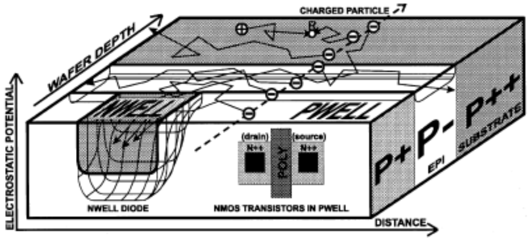


C. Kenney, S. Parker, J. Plummer, J. Segal, W. Snoeys et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

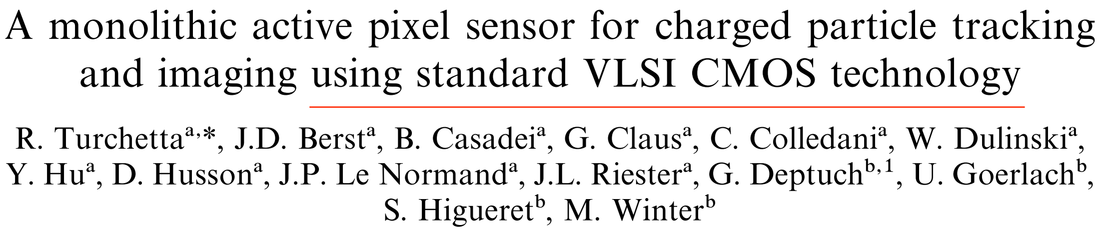
Other examples: ~ 1 µm resolution: SOI sensor, pitch 13.75 µm *M. Battaglia et al. NIM A 654 (2011) 258-265, NIM A 676 (2012) 50-53*

Position resolution: good S/N for interpolation Junction separation and back side processing: see below

Mimosa series – IPHC Strasbourg

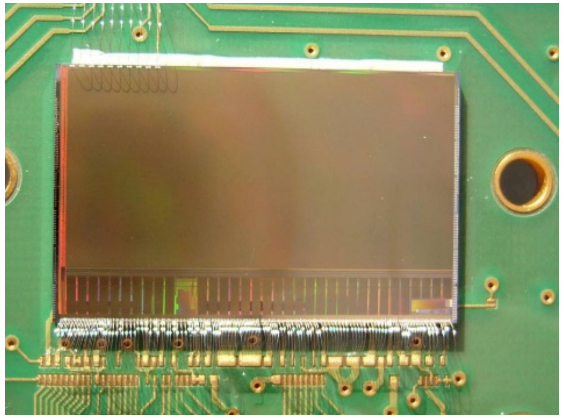


NIM A 458 (2001) 677-689



A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]



Rolling shutter readout

Mimosa26 – 2008

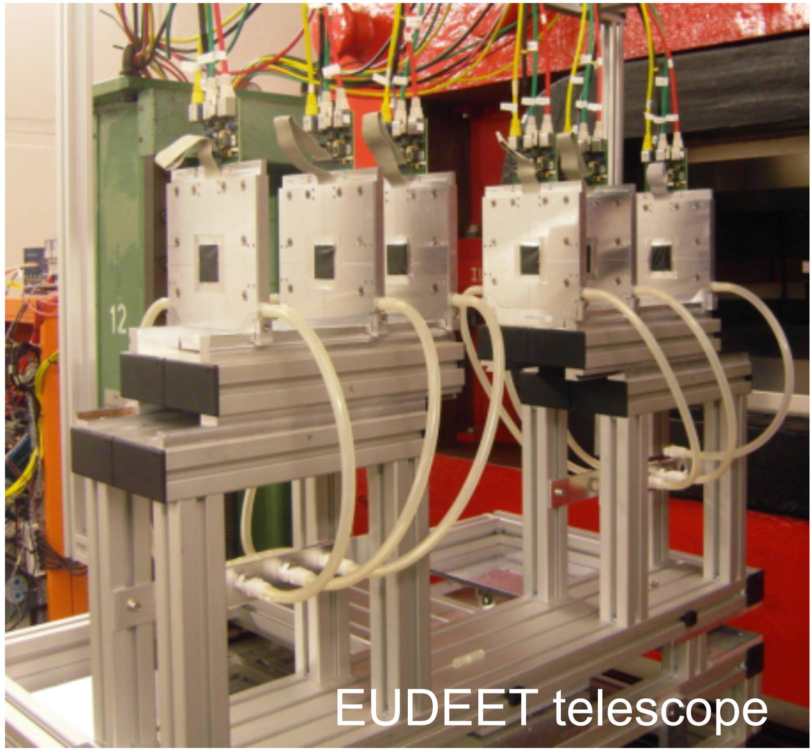
AMS 0.35 µm

18.4 µm pixel pitch 576x1152 pixels

First MAPS with integrated zero-suppressed readout

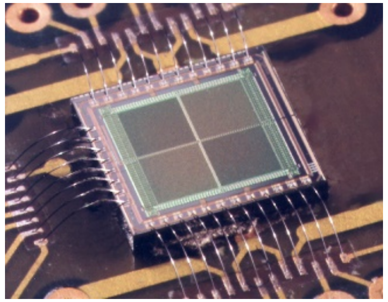
First MAPS used for several applications, also for EUDEET telescope

Courtesy of C. Hu IPHC Strasbourg



EUDEET telescope

Mimosa1 – 1999
AMS 0.6 µm

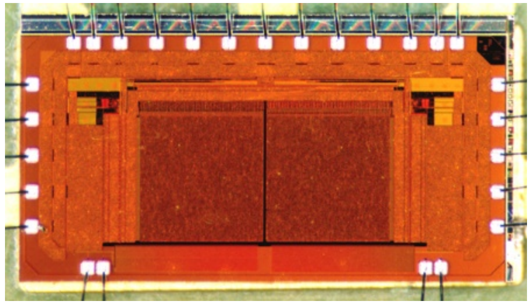


20µm pixel

Mimosa2 – 2000
MIETEC 0.35 µm

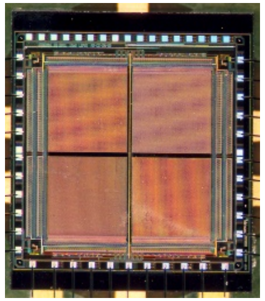
20µm pixel

Mimosa3 – 2001
IBM 0.25 µm



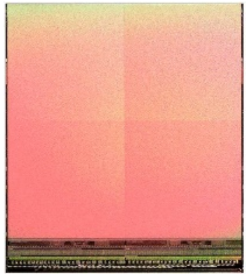
8µm pixel

Mimosa4 – 2001
AMS 0.35 µm



20 µm pixel

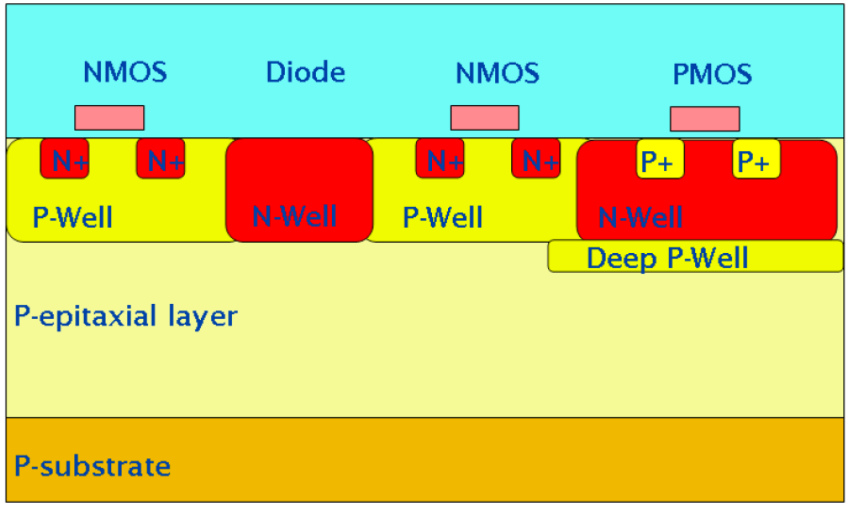
Mimosa5 – 2001
AMS 0.6 µm



17 µm pixel

....

The INMAPS process: quadruple well for full CMOS in the pixel



STFC development, in collaboration with TowerJazz

Additional deep P-well implant allows complex in-pixel CMOS and 100 % fill-factor

New generation of CMOS sensors for scientific applications (TowerJazz CIS 180nm

Also 5Gb/s transmitter in development

Sensors 2008 (8) 5336, DOI:10.3390/s8095336

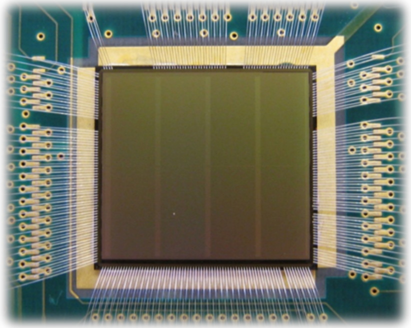
https://iopscience.iop.org/article/10.1088/1748-0221/7/08/C08001/meta

https://iopscience.iop.org/article/10.1088/1748-0221/14/01/C01006/meta

http://pimms.chem.ox.ac.uk/publications.php …

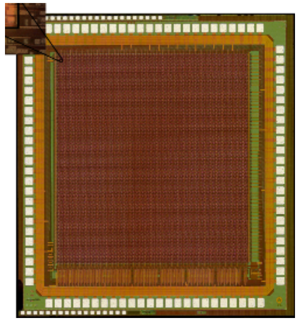
courtesy of N. Guerrini, STFC

TPAC
ILC ECAL (CALICE)



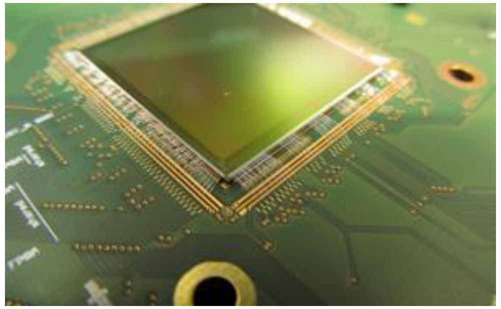
50μm pixel

DECAL
Calorimetry



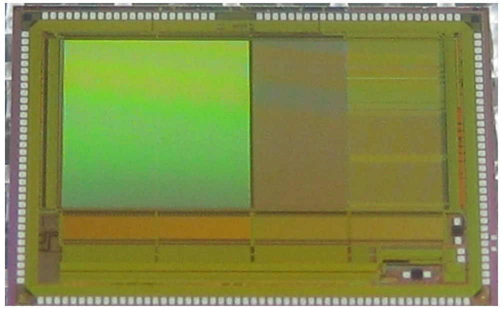
50μm pixel

PIMMS
TOF mass spectroscopy

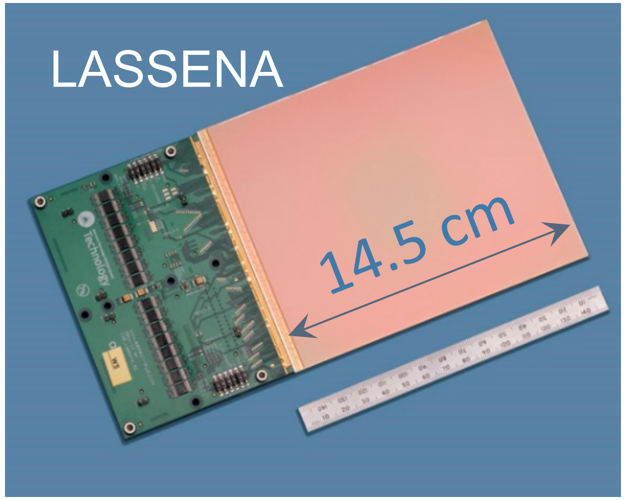


70μm pixel

CHERWELL
Calorimetry/Tracking



48 μm x 96 μm pixel

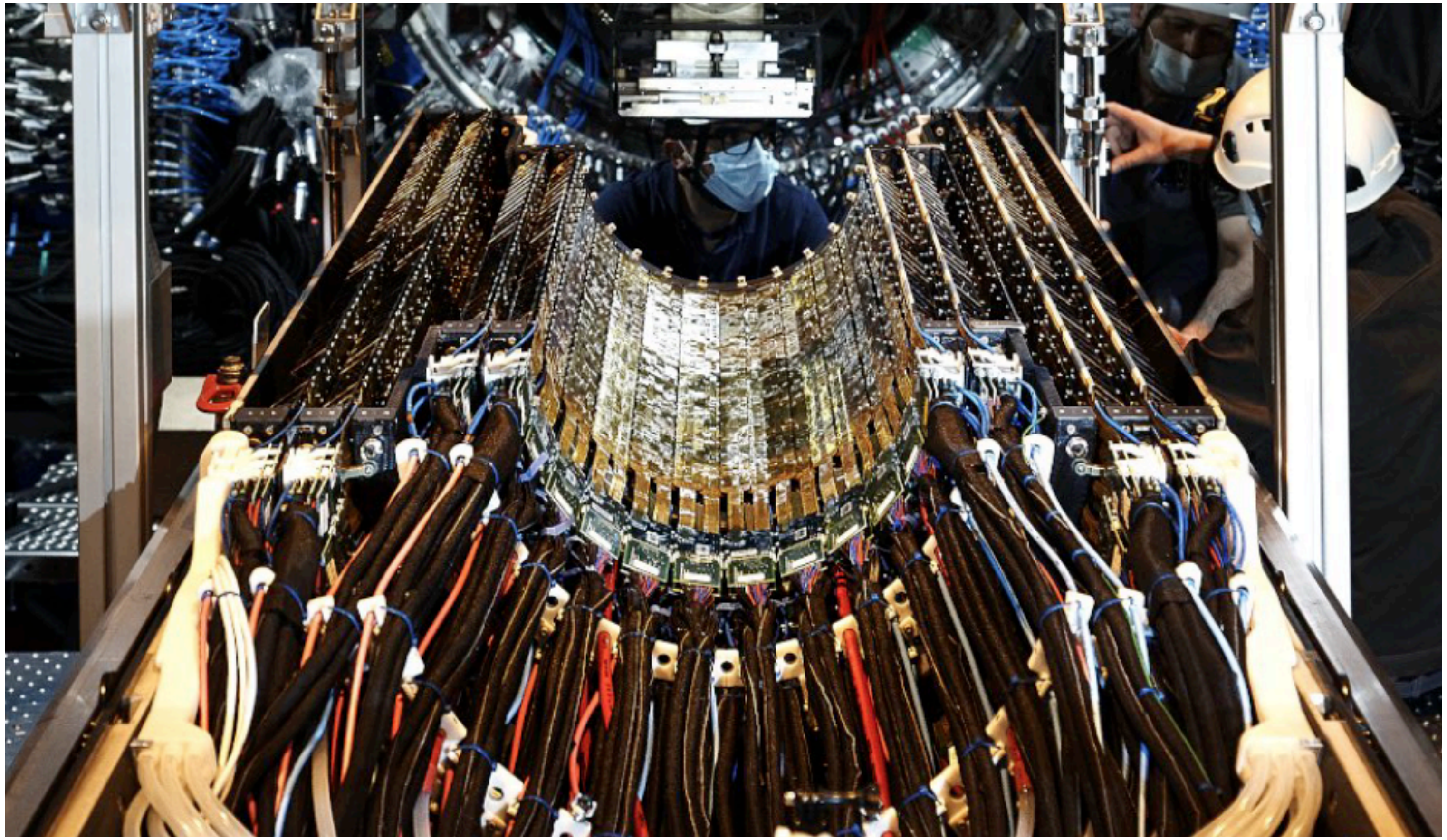


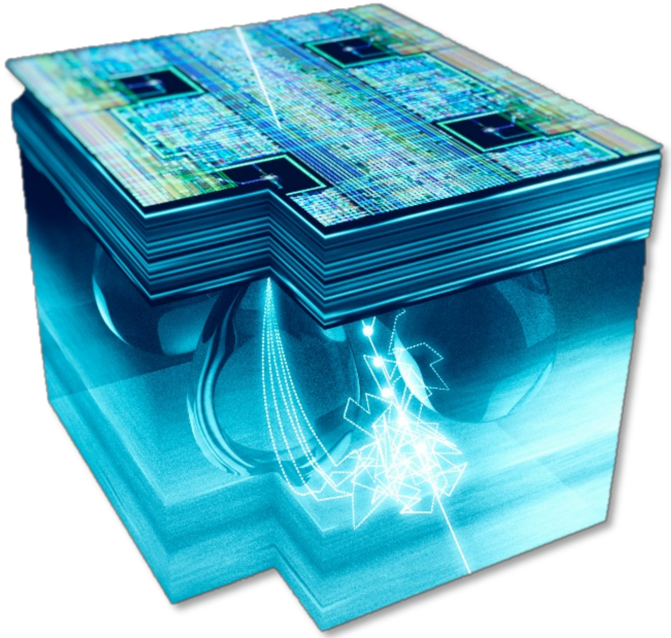
50μm pixel, waferscale

Standard INMAPS process also used for the ALPIDE (27 μm x 29 μm pixel) and MIMOSIS (CBM)

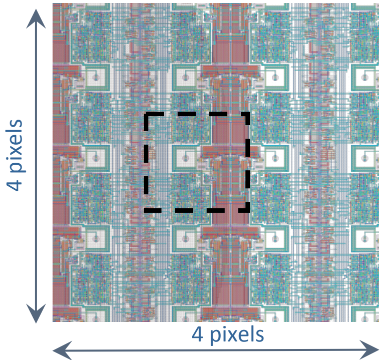
walter.snoeys@cern.ch

State of the art: ITS2 and ALPIDE: 10 m^2, 12.5 Gpixels

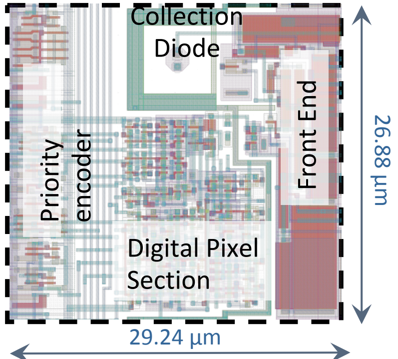


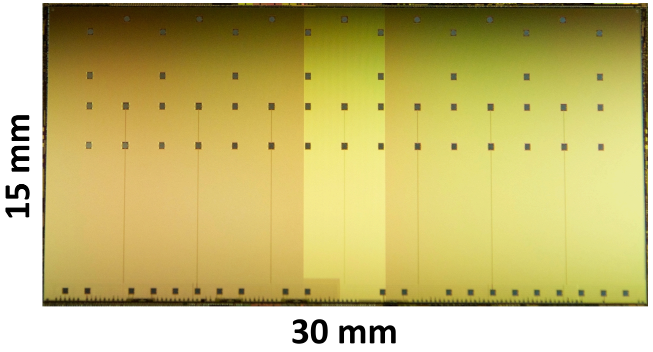


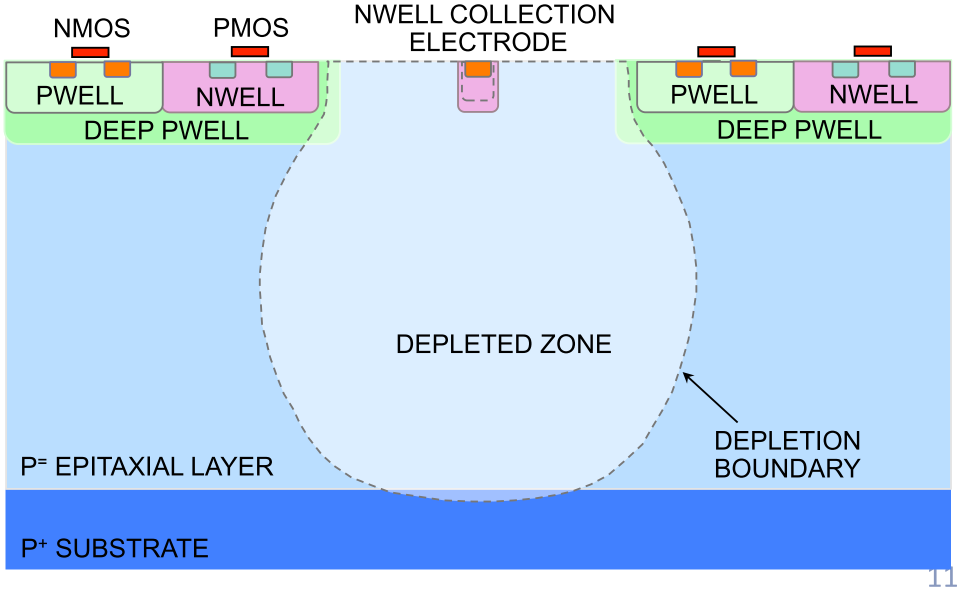
Matrix layout



Pixel layout



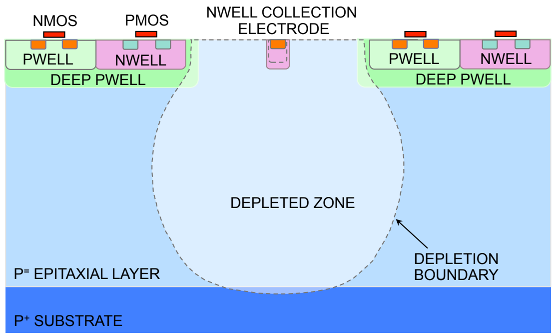




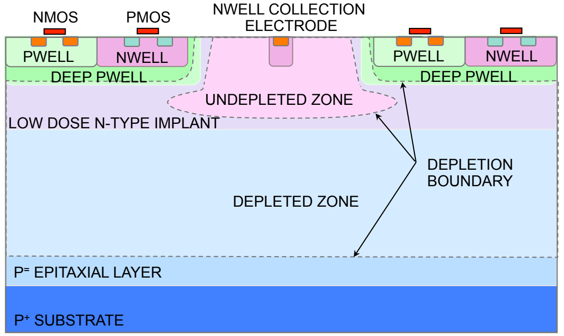
Sensor optimization: Moving the junction away from the collection electrode

for full depletion, better time resolution and radiation hardness… and better efficiency, especially for thin sensors

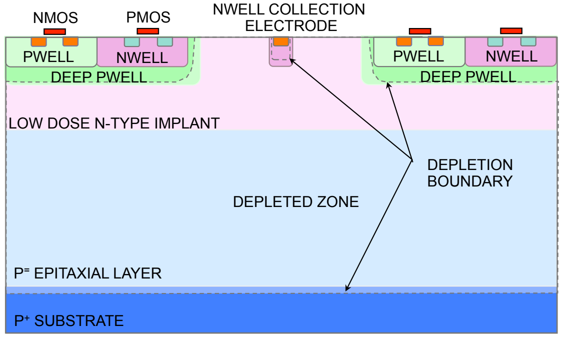
Main damage mechanism: displacement damage (Non-Ionizing Energy Loss or NIEL)
Collect signal charge FAST before it gets trapped => depletion and large electric field…



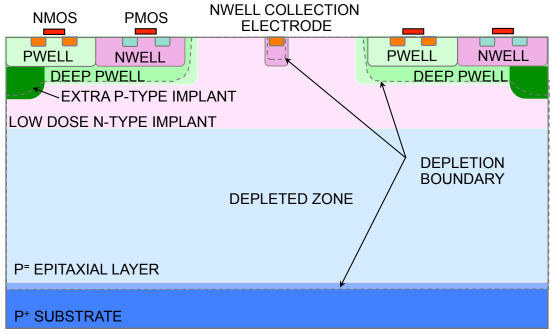
Standard, not fully depleted (ALPIDE)



Not fully depleted at low reverse bias



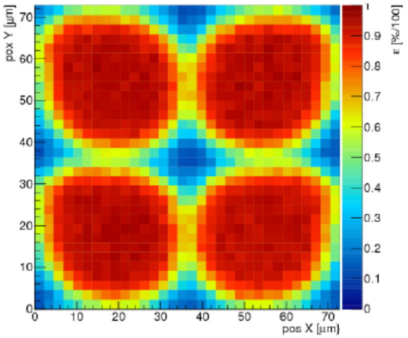
Depletion at higher reverse bias
(MALTA1, MONOPIX)



Further improvements by
influencing the lateral field

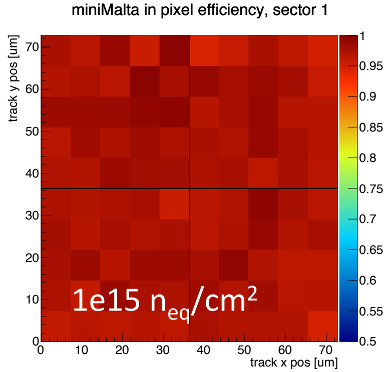
Additional implant for full depletion
=> order of magnitude improvement
Side development of ALICE for ALPIDE
NIMA 871 (2017) pp. 90-96
Triggered development in ATLAS
H. Pernegger et al, 2017 JINST 12 P06008

Efficiency drop at pixel edges
after irradiation
for 36.4 x 36.4 μm^2 pixel
needs improvement
E. Schioppa et al, VCI 2019



3D TCAD simulation
M. Munker et al. PIXEL2018

Significant improvement verified
Also encouraging results with Cz
H. Pernegger et al., Hiroshima 2019
M. Dyndal et al., arXiv:1909.11987



Other similar developments for fast charge collection and depletion:

T.G. Etoh et al., Sensors 17(3) (2017) 483, https://doi.org/10.3390/s17030483
H. Kamehama et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027…
S. Kawahito et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027
L. Pancheri et al., PIXEL 2018, https://doi.org/10.3390/s18010027
C. Kenney et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

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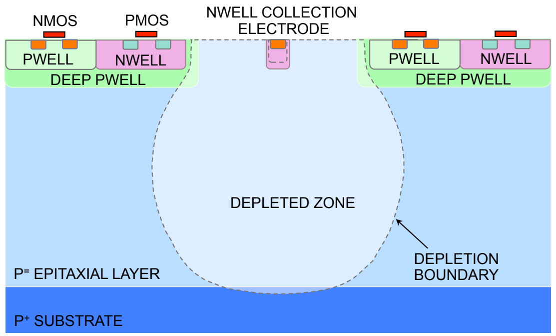
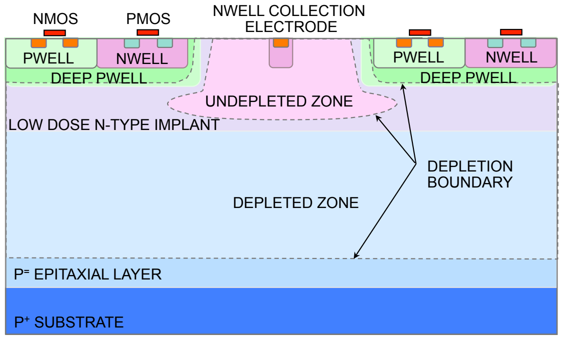
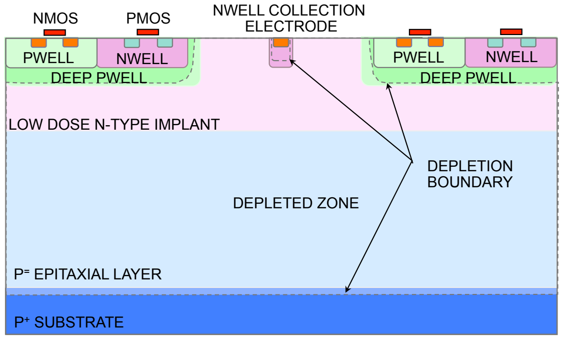


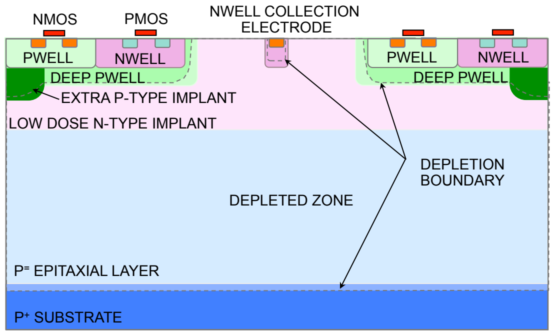
Standard, not fully depleted (ALPIDE)



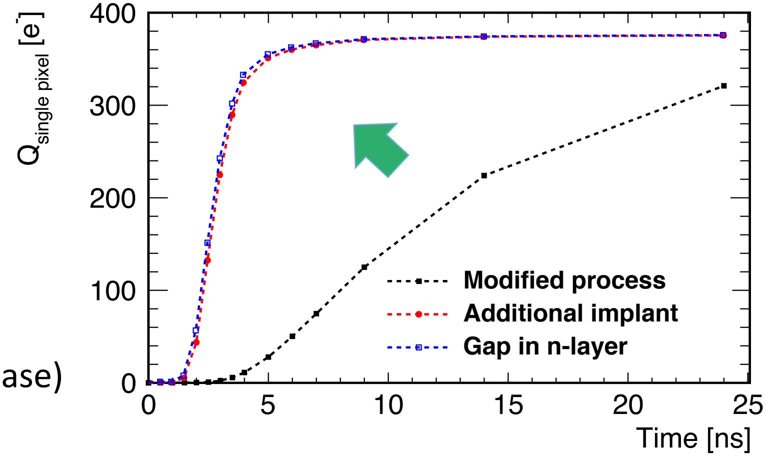
Not fully depleted at low reverse bias



Depletion at higher reverse bias (MALTA1, MONOPIX)



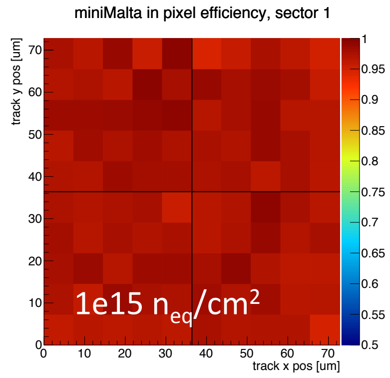
Further improvements by influencing the lateral field



Hit in the pixel corner (= worst case)

3D TCAD simulation
M. Munker et al. PIXEL2018

Significant improvement verified
Also encouraging results with Cz
H. Pernegger et al., Hiroshima 2019
M. Dyndal et al., arXiv:1909.11987

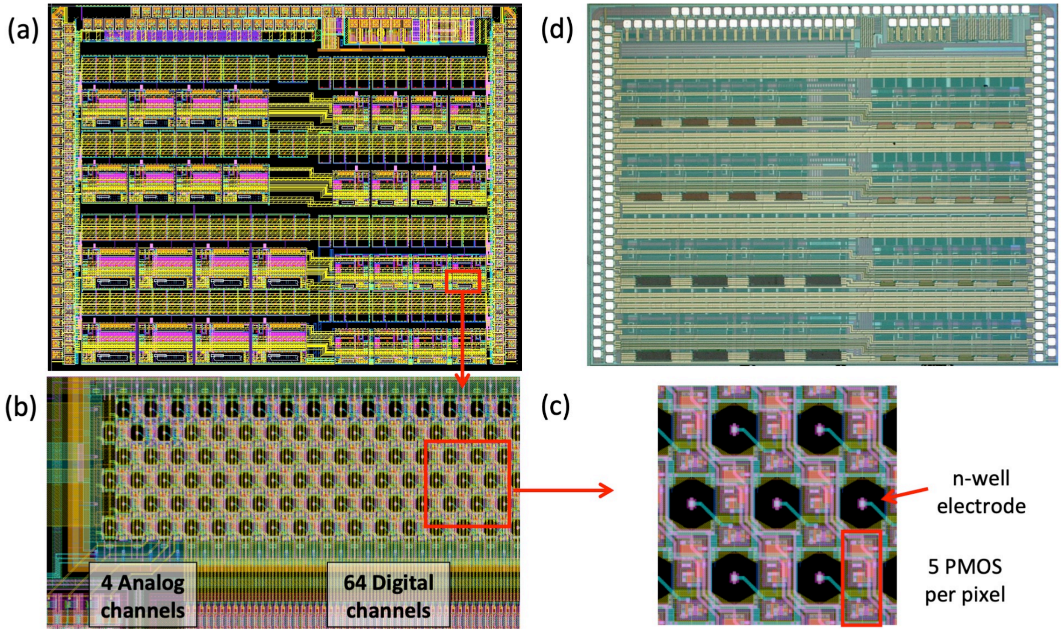


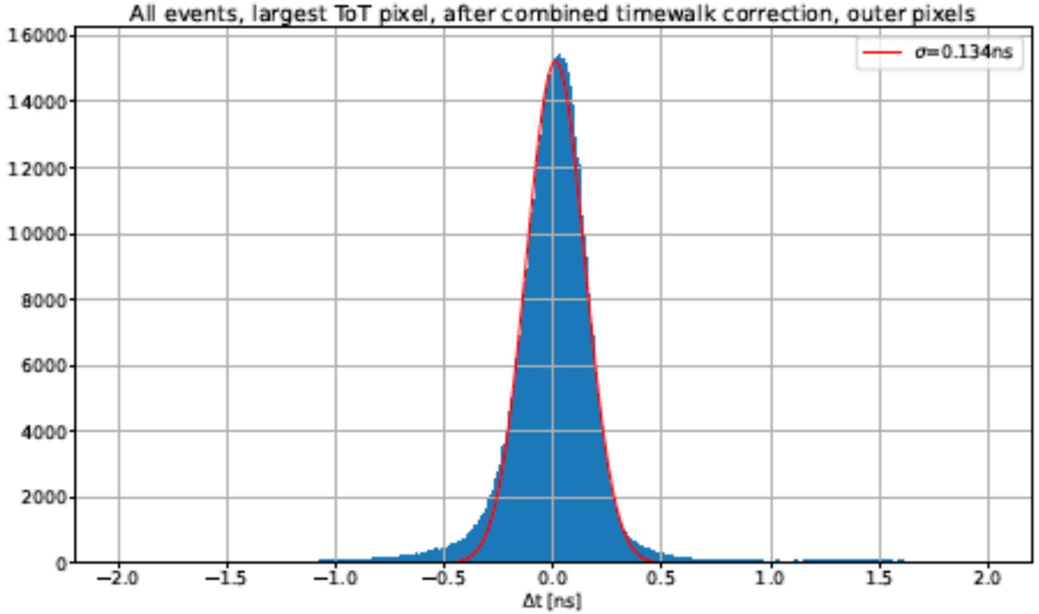
Other similar developments for fast charge collection and depletion:

T.G. Etoh et al., Sensors 17(3) (2017) 483, https://doi.org/10.3390/s17030483
S. Kawahito et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027
L. Pancheri et al., PIXEL 2018, https://doi.org/10.3390/s18010027
C. Kenney et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999))

FASTPIX ATTRACT project

EP R&D





σ = 134 ps, 20 µm pitch

E. Buschmann, K. Dort, J. Braach, D. Dannheim et al.
12th Workshop on pico-second timing detectors for high energy physics,
Zurich 9-11 September 2021

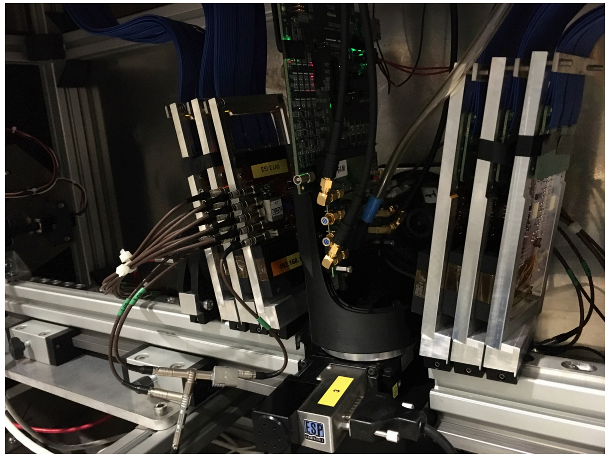
T. Kugathasan et al., https://doi.org/10.1016/j.nima.2020.164461 (ATTRACT: INFN, Ritsumeikan University and CERN)

Direct relation between charge collection and process variant (TowerJazz 180nm)

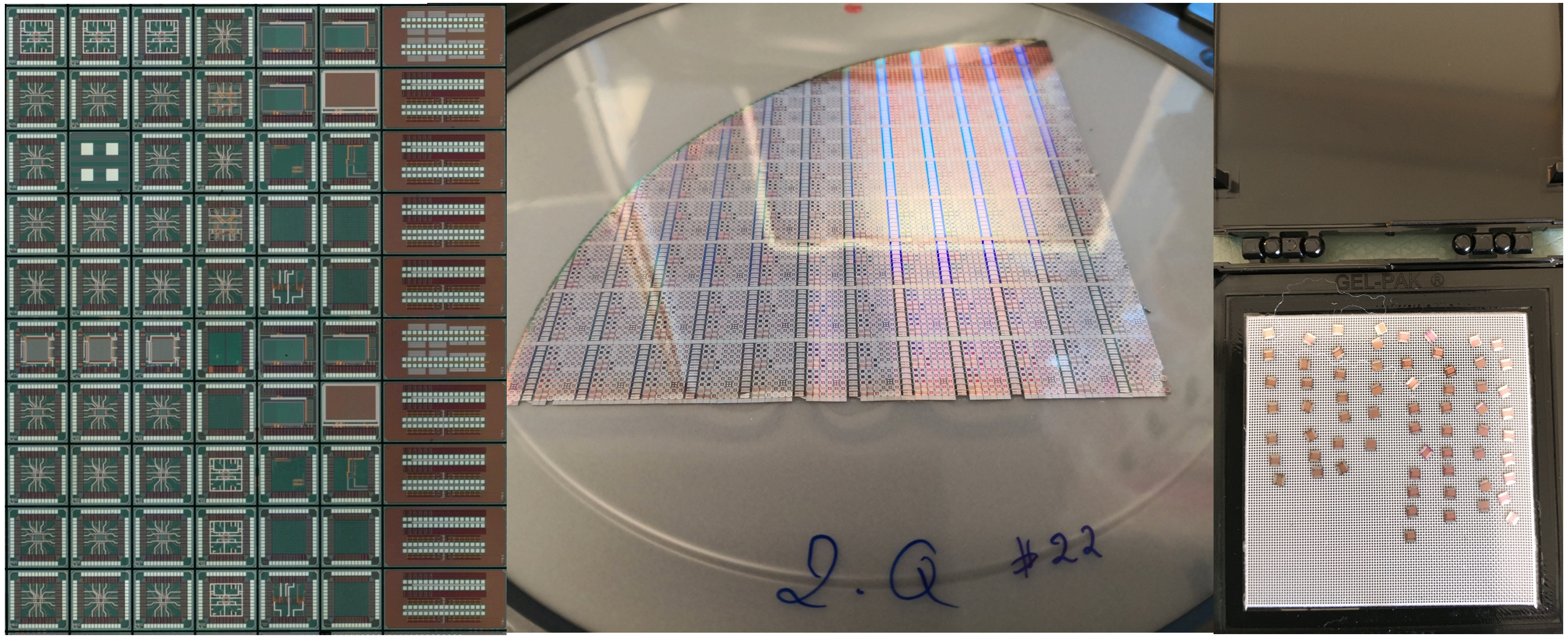
Significant impact even at very small pixel pitch

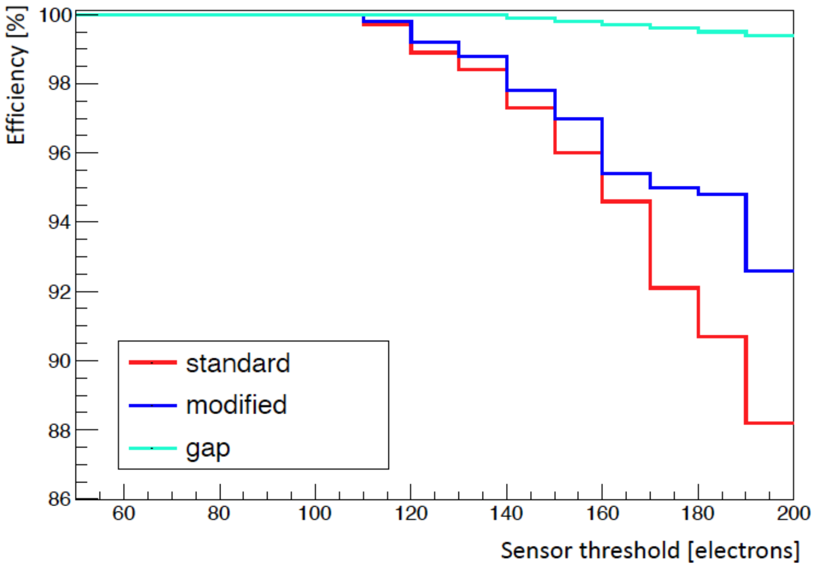
Hexagonal pixels

- better approximation of a circle
- charge sharing in the corners between 3 pixels instead of 4 -> more margin
- collection electrodes on hexagonal grid, circuit remains on Manhattan layout



EP-RD WP1.2 TPSCo 65 nm




Efficiency vs. sensor threshold from TCAD + MC(Garfield++):

Jan Hasenbichler

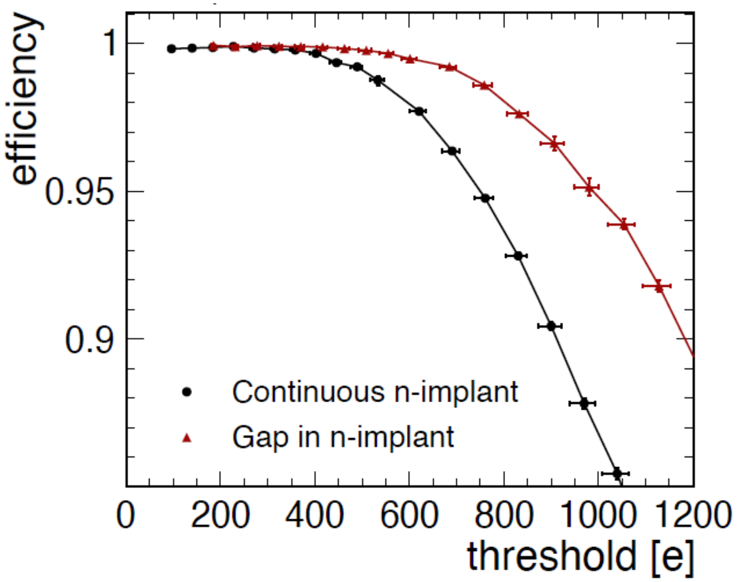
- IPHC: rolling shutter larger matrices, DESY: pixel test structure (using charge amplifier with Krummenacher feedback, RAL: LVDS/CML receiver/driver, NIKHEF: bandgap, T-sensor, VCO, CPPM: ring-oscillators, Yonsei: amplifier structures
- Significant effort from participating institutes
- Transistor test structures, analog pixel (4x4 matrix) test matrices in several versions (in collaboration with IPHC with special amplifier), digital pixel test matrix (DPTS) (32x32), pad structure for assembly testing.
- Process modifications even more needed due to thinner epitaxial layer, hopefully in a similar position as on 180nm process
- Measurements in progress now

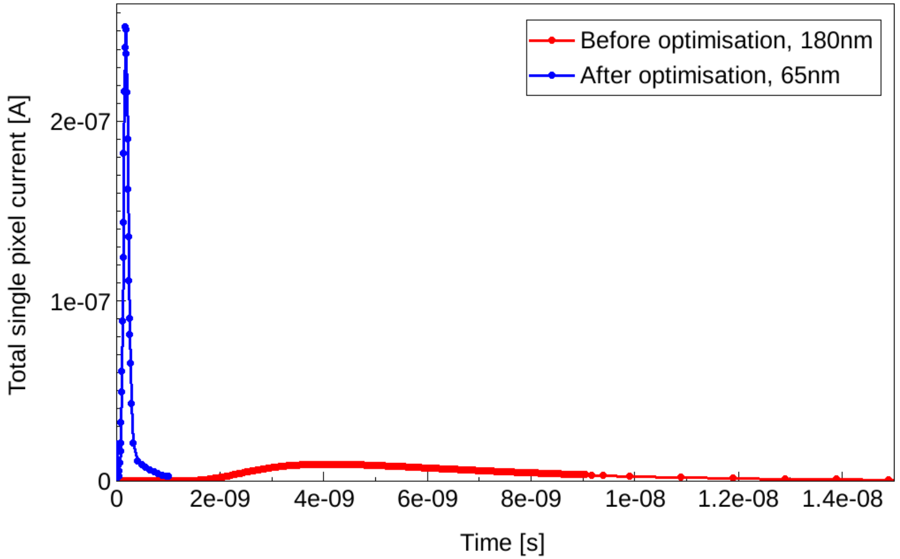
Process optimizations for small collection electrode

Efficiency vs. threshold:

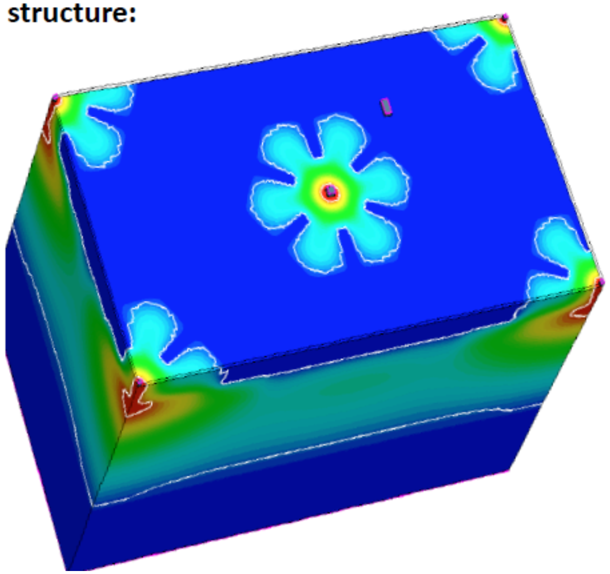
arXiv:2102.04025

~ K. Dort ~





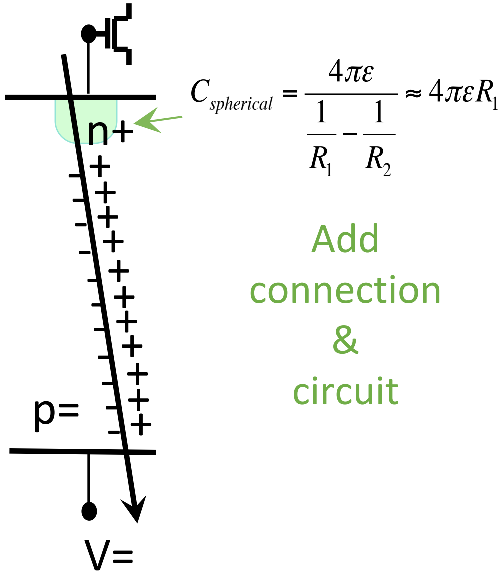
Example of complex 3D TCAD structure:



- Efficiency improvement is not only simulated but also measured, even before irradiation (see top left: efficient operating window is almost doubled)
- The optimization over different pixel pitches and flavors, and technologies has improved the timing by several orders of magnitude. Simulations of even more complex structures bring peak-to-peak variations in the order of 50 ps at the moment
- These techniques have now been applied to several chips, and technologies and are generally applicable.

See M. Muenker’s CERN EP detector seminar

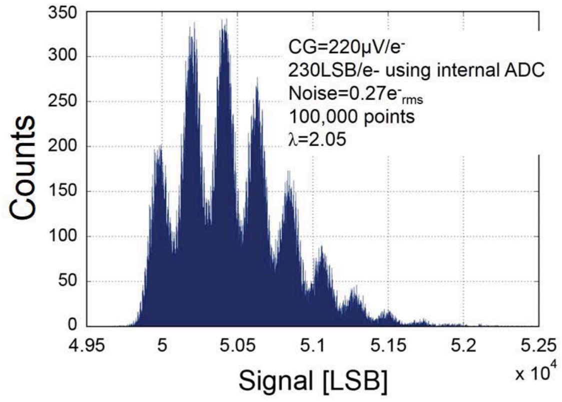
Analog power consumption ~ $(Q/C)^{-2}$ (NIM A 731 (2013) 125)



$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

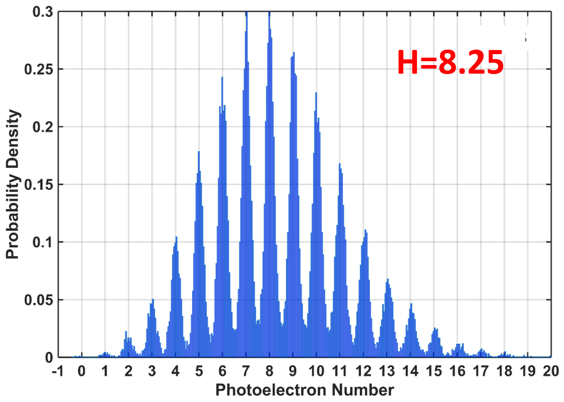
Add
connection
&
circuit

M.W. Seo and S. Kawahito EDL 2015



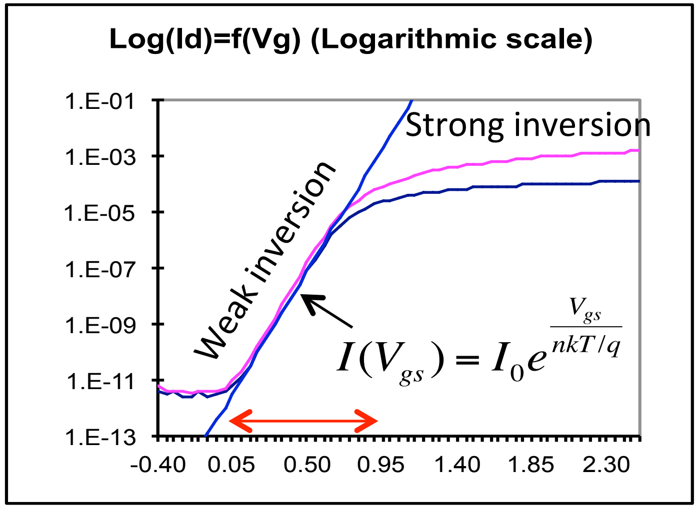
220 µV/e- in 0.11 µm, C=0.73 fF

Ma, Masoodian, Wang, Fossum 2017



350 µV/e- in 45 nm, C=0.46 fF

Non-linearity in weak inversion



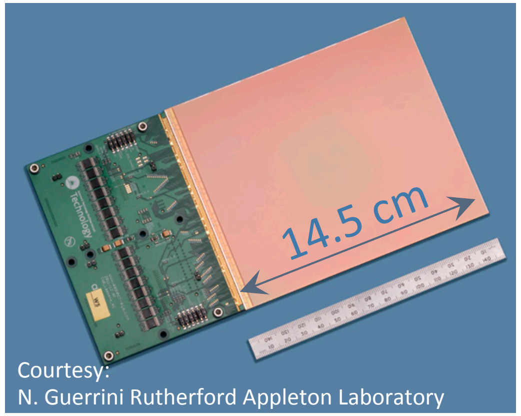
$$I(V_{gs}) = I_0 e^{\frac{V_{gs}}{nkT/q}}$$

Analog power often dominant !

- Q/C several 10's of mV in 180 nm
- "Conventional" approach
  - ITS3 estimate ~ 10-15 nW front end for about 10 mW/cm² (ALPIDE in 180nm ~ 40 nW), 5x area reduction
  - Increase power and speed for better timing, µW for < 1 ns F. Piro
- Reduce capacitance further, using:
  - tricks from imaging technology, at present not yet explored?
    - now very conventional nwell collection electrode…
    - Still need to extract signal charge from underneath the readout circuit !
  - deeper submicron: 2500 e- to switch inverter in 65 nm, 850 e- in 28 nm, 100 e- in 5 nm A. Marchioro 2019 CERN EP seminar
- Gain layers in the sensor
- Holy Grail: For Q/C > 400 mV, analog power consumption goes to zero.

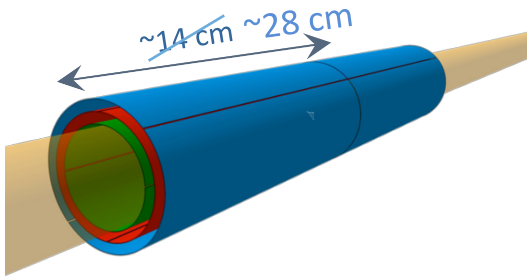
Stitching for better integration, lower mass and constructing larger areas

Exploiting flexible nature of thin silicon and stitching

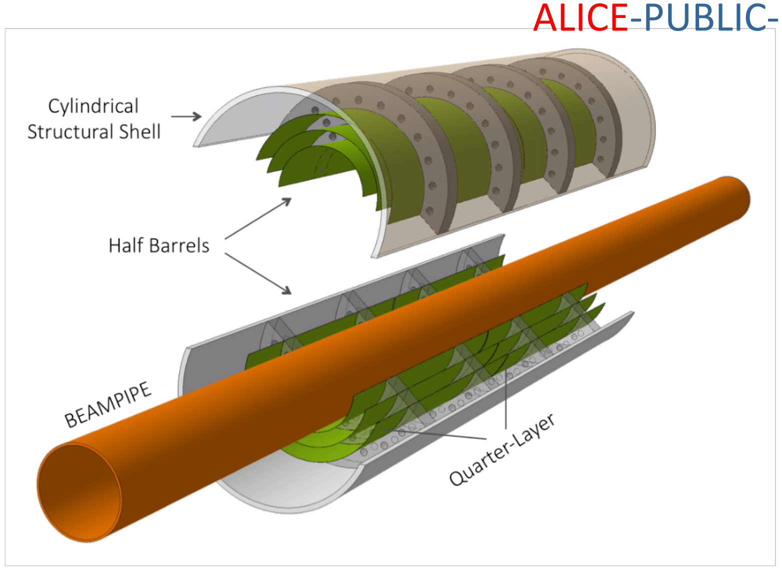


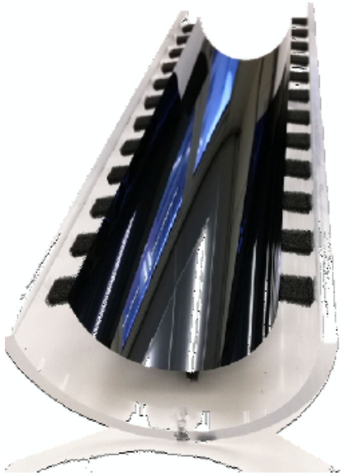
Courtesy:
N. Guerrini Rutherford Appleton Laboratory

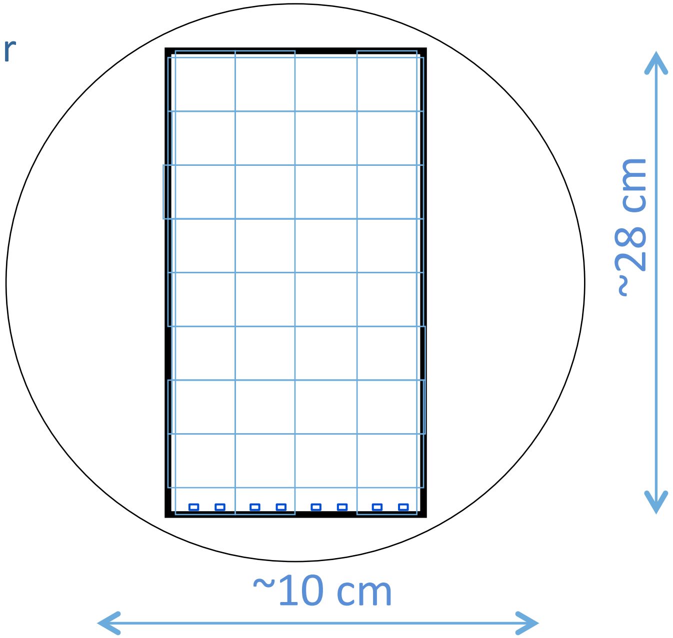
20 µm thick wafer
(Silicon Genesis)



Truly cylindrical vertex detector
New ultra light barrel in LS3 0.05% X/X0 per layer
ALICE-PUBLIC-2018-013





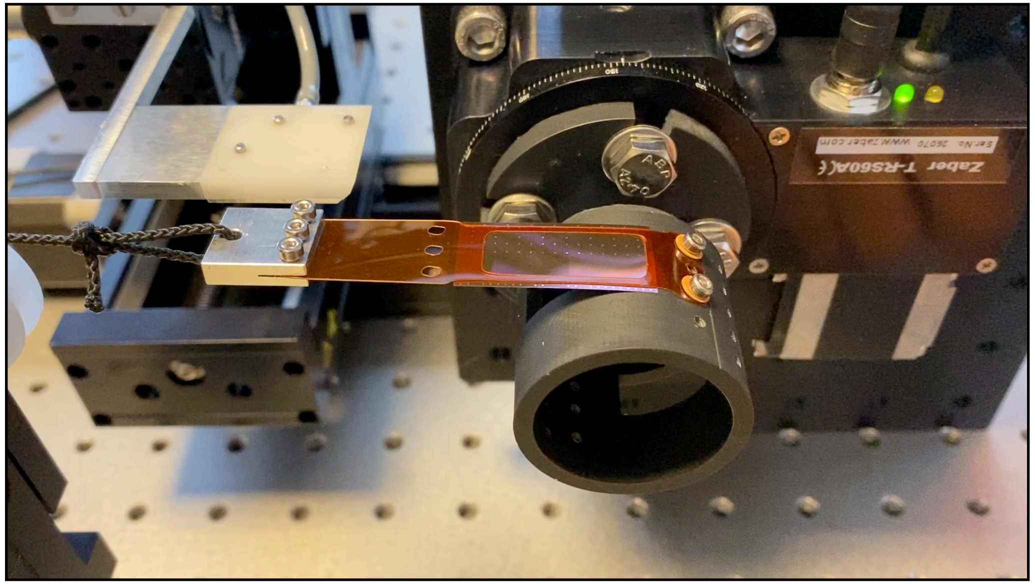


Motivated by lower material budget

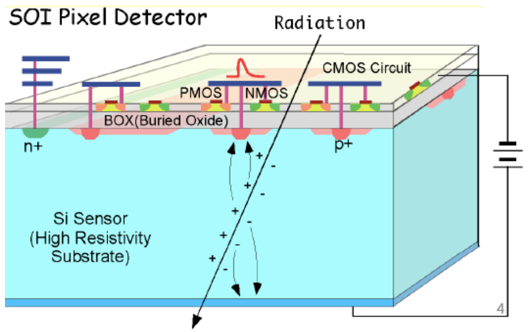
Bent chips just continue to work !
https://arxiv.org/abs/2105.13000v2

Stitching and bending of general interest to
cover large areas with new geometries

Significant challenges in design and verification,
power consumption and distribution, yield,
signal transmission for such a large chip



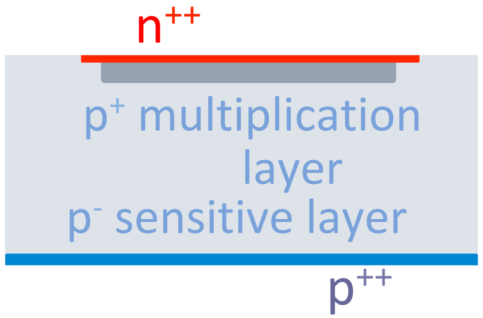
Other developments



SOI sensors

LAPIS 0.2 µm Y. Arai et al.

- Impressive technology development with excellent Q/C
- Large user base
- Some freedom on sensor material
- BOX causes reduced radiation tolerance, several measures for improvement



Low gain Avalanche Diodes (LGAD)

N. Cartiglia et al.

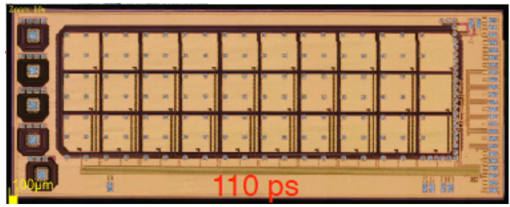
- Charge gain in Si
- ps timing for thin sensors
- Radiation damage mitigation under study

NIM A730 (2013) 226-231, NIM A831 (2016) 18-23

NIM A796 (2015) 141-148, NIM A845 (2017) 47-51

W. Riegler & G. Aglieri: 2017 JINST 12 P11017 "Time resolution of Si detectors"

See also other presentations

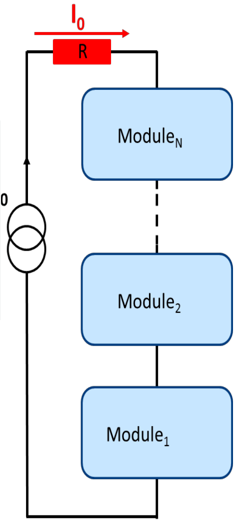


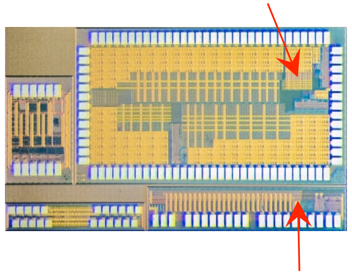
TT-PET

G. Iacobucci et al.

- SiGe readout + TDC
- Down to 50 ps
- Picosecond avalanche detector to do even better

arxiv:1908.09709
JINST 14 (2019) P02009,
JINST 14 (2019) P07013
JINST 13 (2017) P02015,
JINST 11 (2016) P03011,
arxiv:1812.00788
arxiv:1811.12381





Regulator

Charge Pump

Serial power

M. Karagounis et al. for hybrid sensors

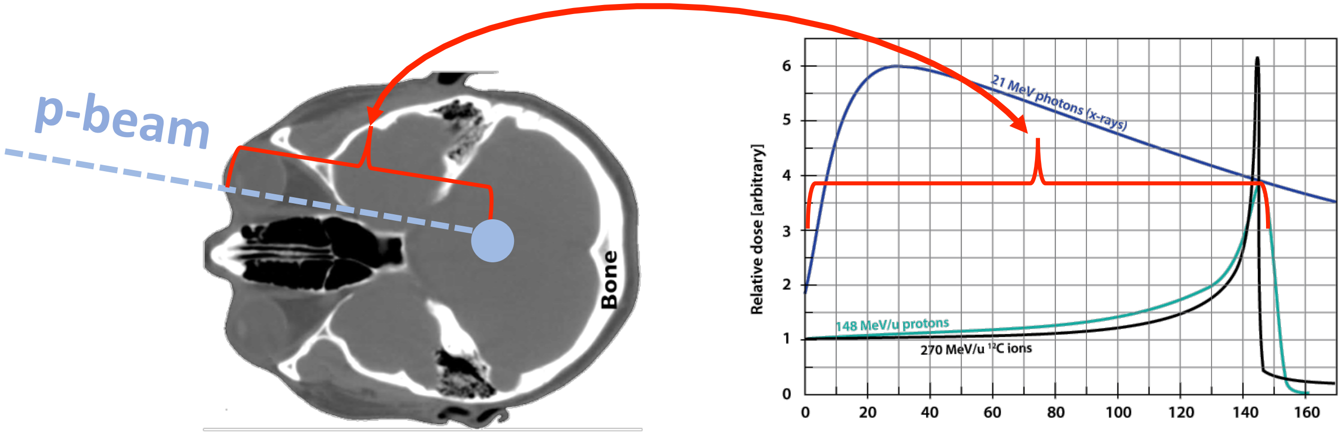
- Connecting sensors in series saves power cabling
- Requires regulation
- Charge pump for sensor bias

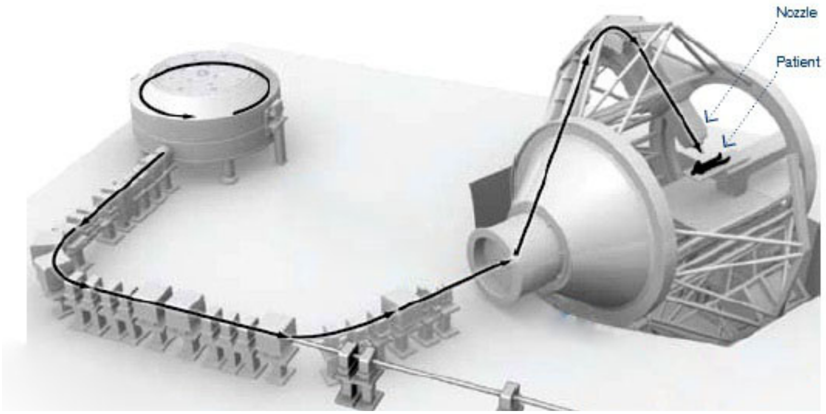
S. Bhat, A. Habib et al PIXEL 2018 (for CMOS sensors)

walter.snoeys@cern.ch

From medical imaging to medical tracking: Proton therapy and proton CT

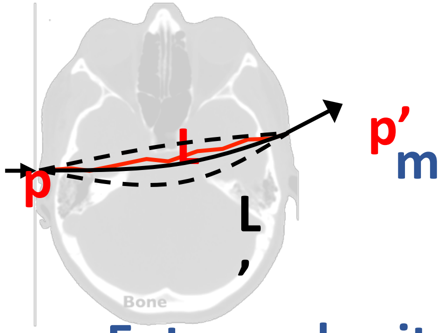
Energy tuning proton beam better than 0.5 % requires proton CT rather than X-ray CT (too poor tissue density resolution)





courtesy of P.Giubilato

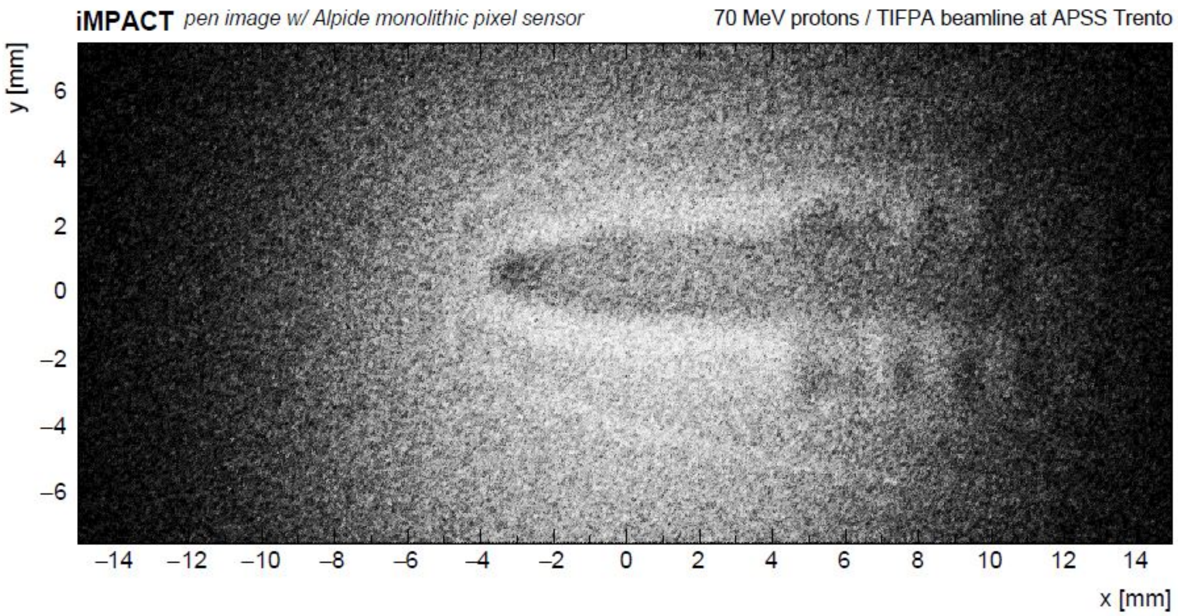
Proton true trajectory



Energy measurement

Entry and exit points + angle

Most Likely Path calculation



Demonstration with ALPIDE chip

Need at least 10^9 proton tracks (entry and exit + most likely path) and 10s of minutes with state of the art detectors.

Gaining time requires detectors which do not yet exist

walter.snoeys@cern.ch

Concluding remarks

After years of R&D monolithic sensors for HEP move to CMOS MAPS in mainstream CMOS technology, but requirements for HEP are not completely identical to those for visible light imaging, and some technology flexibility can still be beneficial.

Circuit radiation tolerance as for standard CMOS, which naturally evolved towards significant tolerance with some caveats.

Sensor radiation tolerance, precision timing and improved efficiency can be obtained from optimization for fast charge collection using techniques based on general principles applicable to different technologies. Large collection electrode sensors provide extreme radiation tolerance and more uniform sensor timing but exhibit large input capacitance.

Decreasing technology feature size or special imaging sensor features can increase the voltage excursion on a small collection electrode and ultimately reduce analog front end power to zero and allow precision timing.

Hybrid vs Monolithic distinction is becoming more vague:
2D integration combined with stitching will bring us a long way. 3D could help for the most challenging applications.

Feasibility studies on stitched devices will determine the size of the sensors we will design in the future and whether and to what extent we can profit from unbeatable wafer-scale integration. (production volume is in the outer layers, we need to be prepared for volume test/acceptance/monitoring)

Concluding remarks

Large area pixel sensors are enabling devices for many cutting edge research fields and practical applications like tracking in HEP as in FCC, medical imaging, space-borne instruments, etc, illustrated by the interest in chips like ALPIDE and others but also by other successful developments like Medipix/Timepix

MAPS are one of the few areas where production volume even within HEP would not be negligible, but where our community can have an impact not only on the quality of its own measurements, but also on society in general, and which we should try to exploit to enable access to the most advanced technologies.

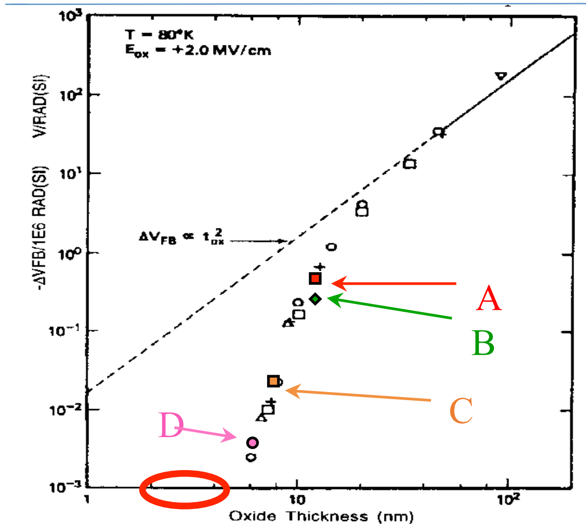
Concluding remarks

Large area pixel sensors are enabling devices for many cutting edge research fields and practical applications like tracking in HEP, medical imaging, space-borne instruments, etc, illustrated by the interest in chips like ALPIDE and others but also by other successful developments like Medipix/Timepix

MAPS are one of the few areas where production volume even within HEP would not be negligible, but where our community can have an impact not only on the quality of its own measurements, but also on society in general, and which we should try to exploit to enable access to the most advanced technologies.

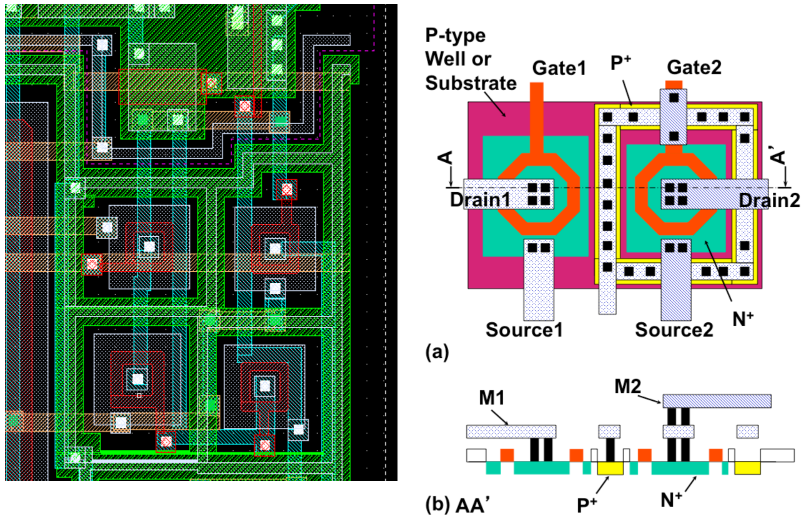
THANK YOU !

Circuit radiation tolerance: like standard CMOS

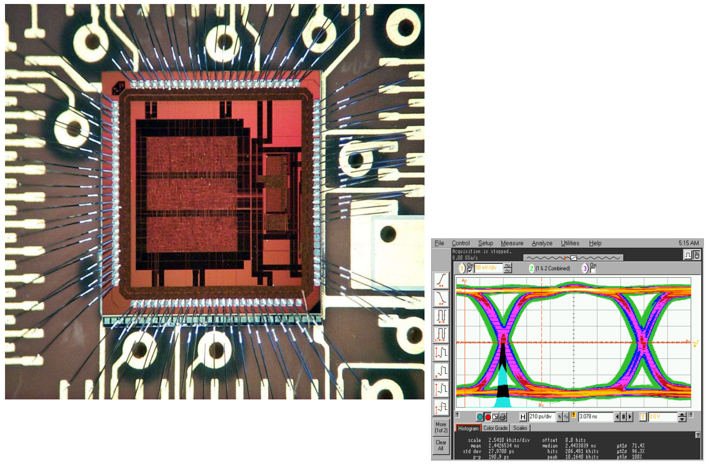


Now here

After N.S. Saks et al, IEEE TNS, Vol. NS-31 (1984) 1249



G. Anelli et al., IEEE TNS-46 (6) (1999) 1690



P. Moreira et al.
http://proj-gol.web.cern.ch/proj-gol/

Total ionizing dose:

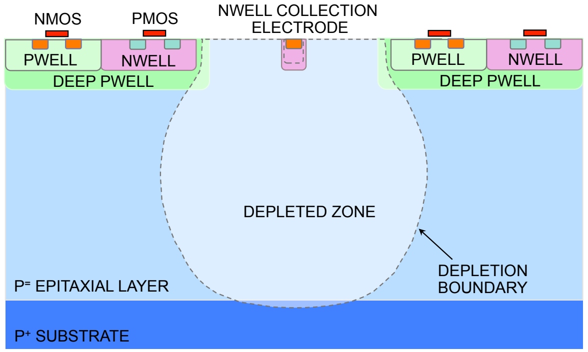
- Intrinsic transistor has become more and more radiation tolerant due to thinner gate oxide
- In LHC enclosed NMOS transistors and guard rings in 0.25 µm CMOS to avoid large leakage current
- In deeper submicron enclosed geometry usually no longer necessary for leakage, but for small dimensions parasitic effects dominate e.g. from spacers, new gate dielectrics, **requires extensive measurement campaigns**

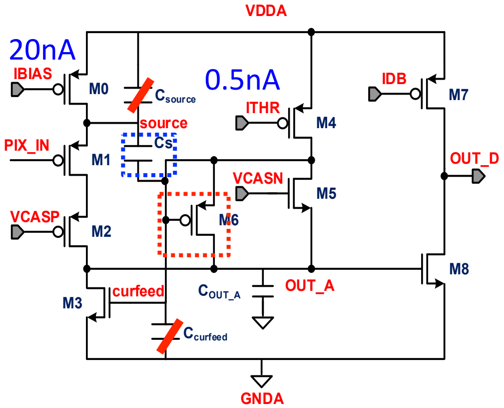
F. Faccio et al. IEEE TNS-65 (1) 164, 2018

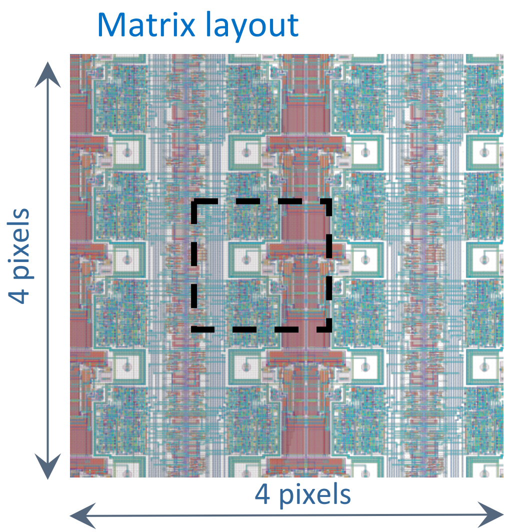
Single event effects:

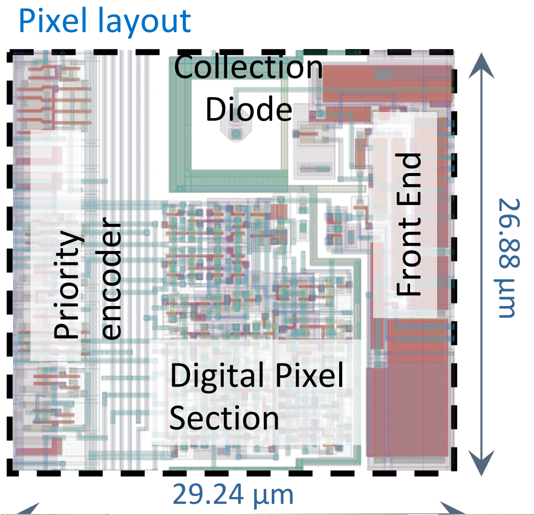
- Single Event Upset : triple redundancy with majority voting (now special scripts S. Kulis)
- Latch-up not observed so far in LHC, but observed on MAPs at STAR, and in new technologies => **need attention in the design**

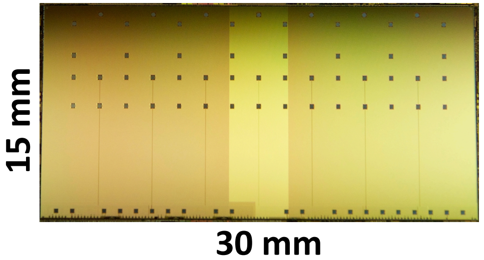
ALPIDE chip in ALICE ITS2

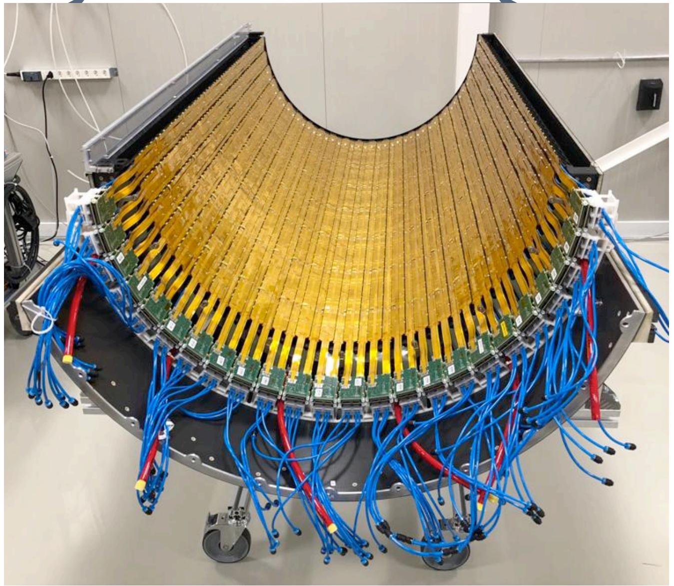






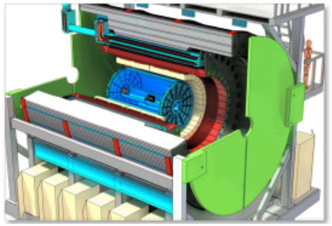




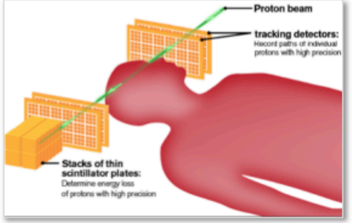


Half outer barrel (layer 6)
~ 2.47 Gpixels covering ~ 2 m² sensitive area

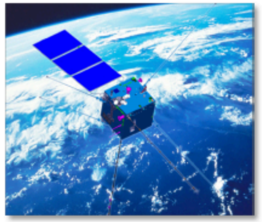
- TJ CMOS 180 nm INMAPS imaging process (TJ) > 1kΩ cm p-type epitaxial layer
- Small 2 μm n-well diode and reverse bias for low capacitance C(sensor+circuit) < 5 fF
- 40 nW continuously active front end D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042
- Q_{in}/C ~ 50 mV, analog power ~ $(Q/C)^{-2}$ NIM A 731 (2013) 125
- Zero-suppressed readout, no hits no digital power G. Aglieri et al. NIM A 845 (2017) 583-587
- Ratio between 15 x 30 mm² and 10 m² in the experiment not ideal -> stitching -> P. Riedler's presentation
- ALPIDE (ALICE Pixel Detector) to be used for several other physics experiments, in space and for medical applications



sPHENIX



Proton CT (tracking)

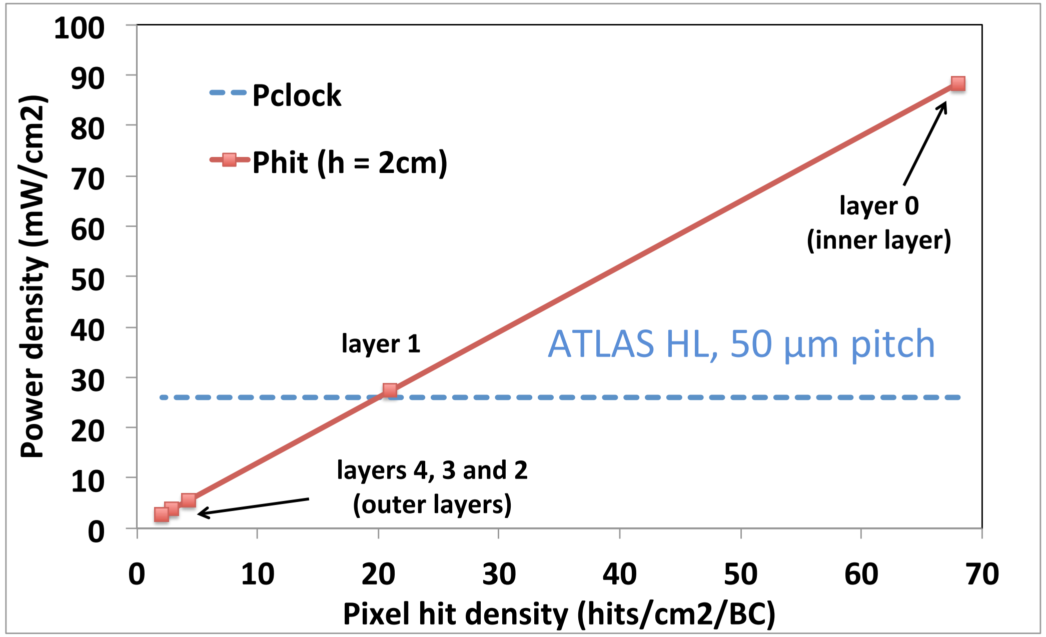


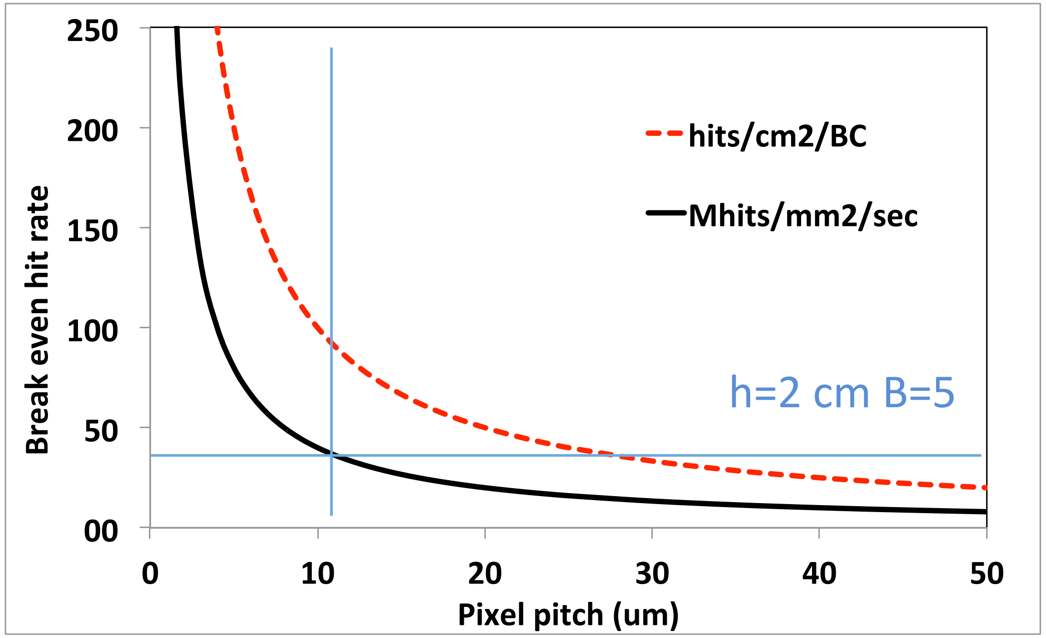
CSES − HEPD2

Design team: G. Aglieri, C. Cavicchioli, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, S. Lee, M. Lupi, D. Marras, C.A. Marin Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, A. Dorokhov, H. Pham, P. Yang, W. Snoeys (Institutes: CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC) and comparable team for test

1 MPW run and 5 engineering runs 2012-2016, production 2017-2018

Digital power consumption





Energy to transfer 1 bit to the periphery (assume line toggle, not step):

1 cm line at 1.8 V = CV^2 = 2 pF x $(1.8\ V)^2$ = **6.5 pJ** Lower VDD in deep submicron = 2 pF x $(1\ V)^2$ = **2 pJ**

Caveat: 2pF/cm can increase depending on line load…

- Defines break-even hit hit rate, where power for the clock = power to transfer hits to the periphery (h is column height, p is pixel pitch, B is number of bits transmitted/hit): $R_{/BC} = (hpB)^{-1}$
- At pitches < 12-13 µm should not distribute the clock over the pixel matrix, even at HL-LHC ATLAS inner pixel
- Break-even decreases with column height but very often rate is lower as well

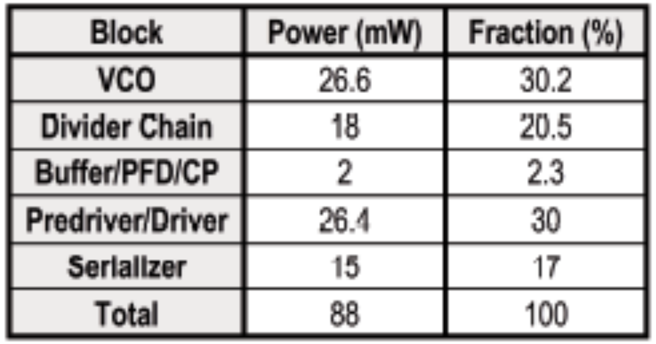
Off-detector transmission:

ISSCC 2013 / SESSION 2 / ULTRA-HIGH-SPEE

2.6 A 32-to-48Gb/s Serializing Transmitter Using Multiphase Sampling in 65nm CMOS

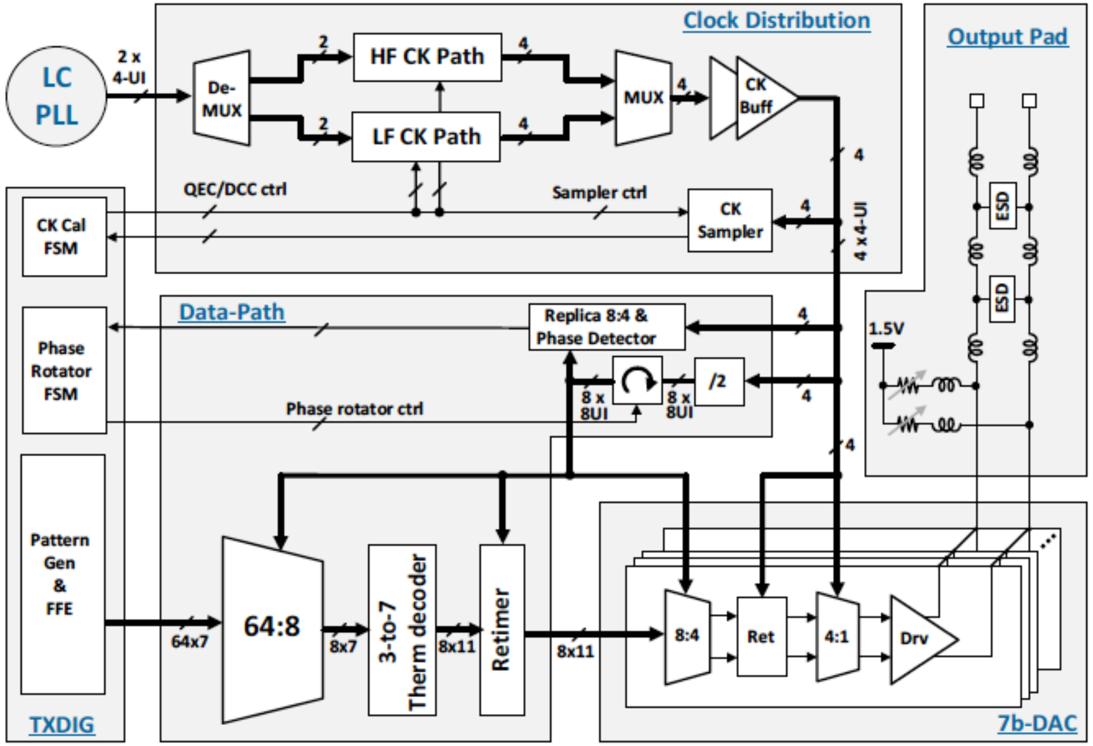
Amr Amin Hafez, Ming-Shuan Chen, Chih-Kong Ken Yang

University of California, Los Angeles, CA



Block	Power (mW)	Fraction (%)
VCO	26.6	30.2
Divider Chain	18	20.5
Buffer/PFD/CP	2	2.3
Predriver/Driver	26.4	30
Serializer	15	17
Total	88	100

INTEL, ISSCC2021, 224Gbps, PAM-4, 1.7 pJ/bit, 10 nm technology



State of the art: a few mW/Gbps, already earlier but also now at much higher bandwidths

Significant circuit complexity

For HEP important penalty for SEU robustness due to triplication/larger devices…

Important: data concentration, physical volume for material budget, and technology

Stitched sensor: challenges

Power consumption: only considering the matrix, pixel size 200 µm^2 (~ 15 µm pixel pitch on a hexagonal grid) 1nA/pixel = 0.5 mW/cm^2

Dynamic hit-rate related power density proportional to column height (28 cm, on average 14 cm x CV^2) and hit rate

- First simulations (parasitic extraction) encouraging dynamic power consumption and possible hit rates:
  most optimistic values (not on finalized design !!!!) around 25 mW/cm^2 @ 100 Mhit/cm^2/sec
- Avoid distribution of a clock over the matrix (150 − 200 mW/cm^2 for 40 MHz, unless extensive clock gating)

Static leakage not negligible at all, analog power determined by sensor Q/C (slow front end ~10-20 nA)

Power distribution:

- Additional thick metal(s) for power distribution to contain voltage drop, otherwise 10’s of mV/mW/cm^2
- Power regulation for uniformity
- Beyond 50 mW/cm^2 :
  - Power pads no longer only at the bottom, or
  - on-chip serial powering,
    interesting even for lower hit rates, for a single point connection of power/data/slow control
    1mW/cm^2 corresponds to 280 mA…

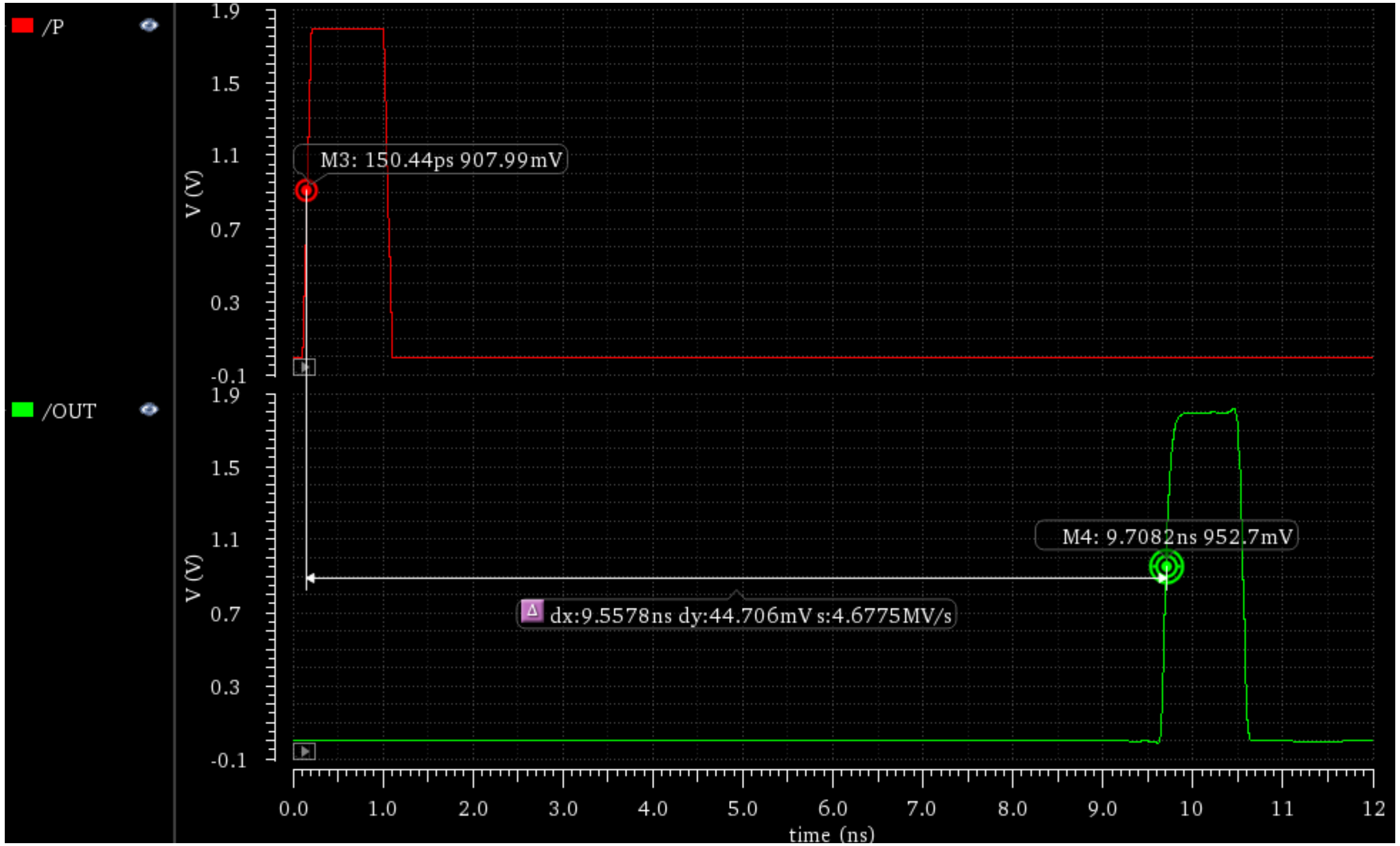
Yield:

- Conservative stitching rules represent a significant area penalty, need to find ways to regain density
- Power regulation for uniformity but also segmented with current limitation to protect against shorts

Very large chip:

- One column ~ 2^{14} pixels, extract hit info with limited number of lines
- Need digital on-top design and verification

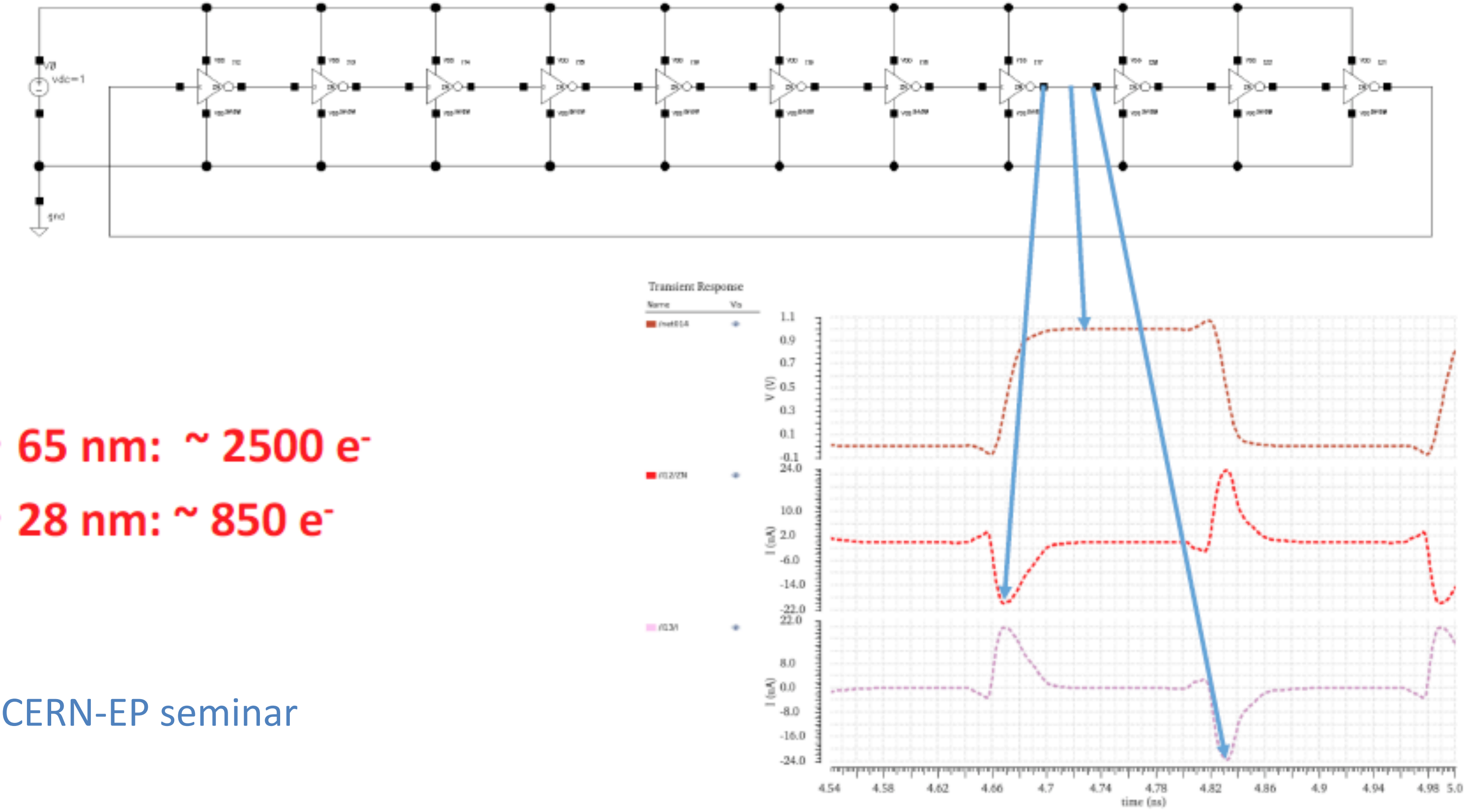
Stitched sensor challenges: timing and data bandwidth



- Monte Carlo simulation of 90 buffer stages
- Timing information maintained:
  - < 10 ps rms (mismatch) variation
  - jitter < 500 fs rms
- For very large matrix more than 90 buffer stages, ~3 x worse…
- Here 1ns pulse width, can decrease to 0.5 ns -> HUGE matrix bandwidth to be matched by periphery and off-chip data transmission
- Machinery to transmit timing information to the periphery available
- To be verified: process – power supply – temperature effects !

If these challenges can be overcome for a wafer-scale sensor with good yield, we prove we can build modules with single wafer-scale chips and unprecedented integration for large area detectors which would be a major step forward.

How many electrons are needed to switch a logic gate ?



- **65 nm: ~ 2500 e^-**
- **28 nm: ~ 850 e^-**

A. Marchioro, 2019 CERN-EP seminar