A hybrid architecture for a prompt momentum discriminating tracker for SHLC

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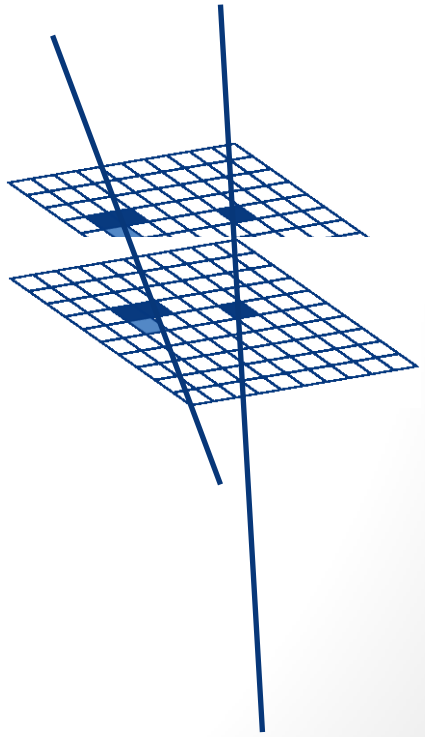


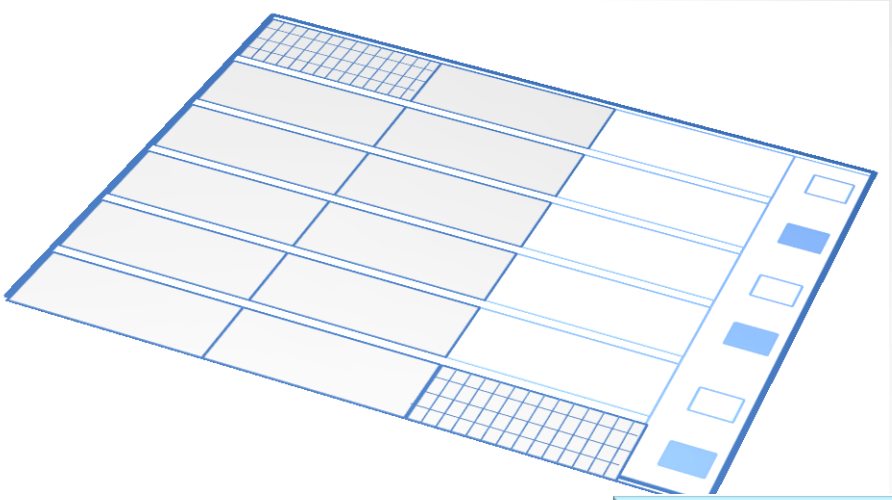
Acknowledgements

- Basic ideas of high pT discrimination based on two parallel layers of strips: R. Horisberger, circa 2009
- Finding high pT particles from stubs detailed by many authors, for a good review of the CMS ideas see presentation by M. Pesaresi, Vertex 2010
- Many details discussed an refined with D. Abbaneo
- Data on analog FE: J. Kaplon
- Detailed mechanical drawings: A. Conde

Outline

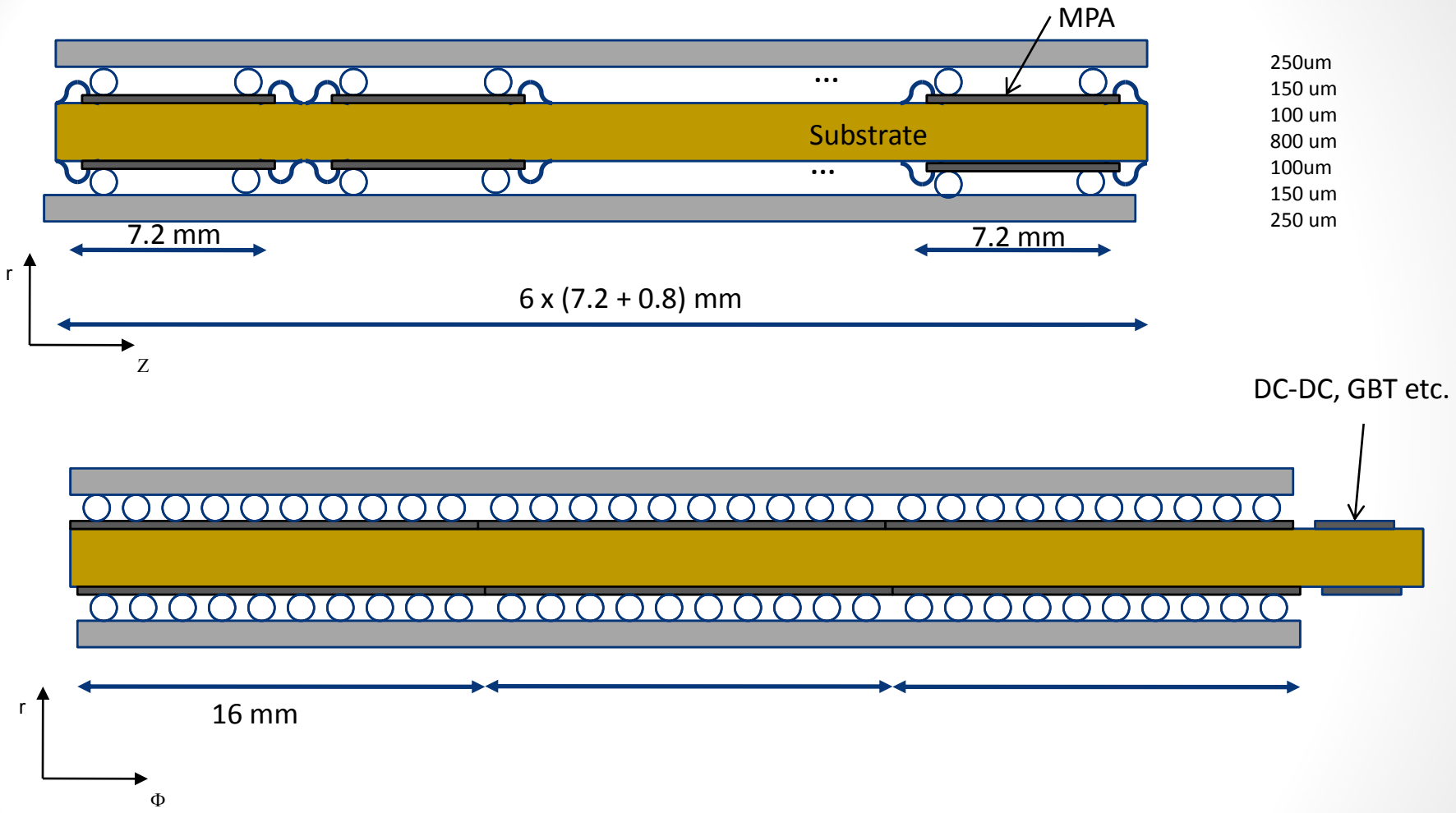
- Motivation and previous work
- Proposed architecture
  - Module details
    - Mechanics and connectivity
    - Pixel ASIC
- Modeling of data traffic
  - Requirement for trigger and data links
- Conclusions

Previous studies



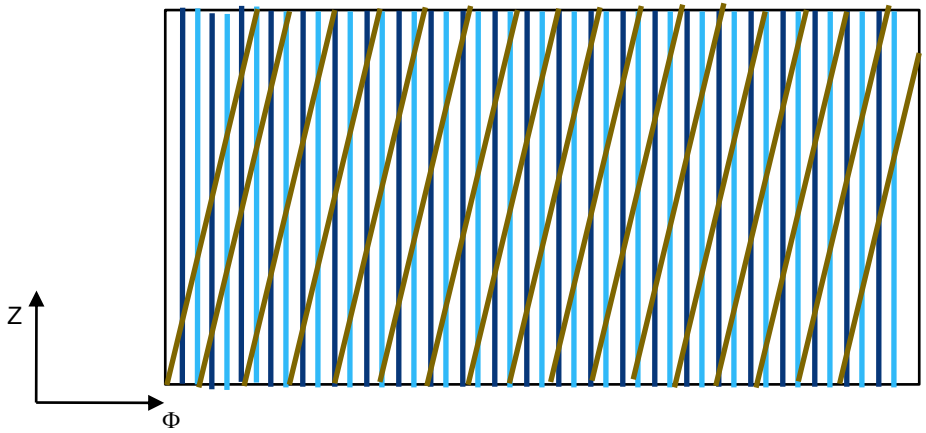
18 FE chips with
~ 160x4 pixels
of 100x2000 um

Assembly for dual pixel layers



Module size = [6 * 8] x [3 * 16 + 12] mm

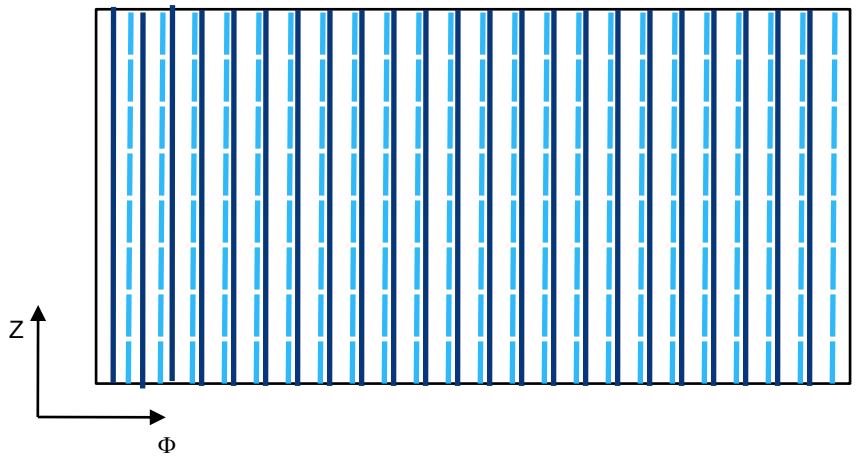
Z position with Triple Sensors Stereo Module



- Coincidence window with parallel strips gives pT cut
- Third layer of tilted (100 mrad) strips AND coincidence gives pT cut and Z coordinate
- Thickness: 3 sensors + hybrid sideways
- But it does not work even at relatively modest occupancy levels (one stereo strip covers ~ 25 parallel strips); could not work at low radius.

NEW ARCHITECTURE

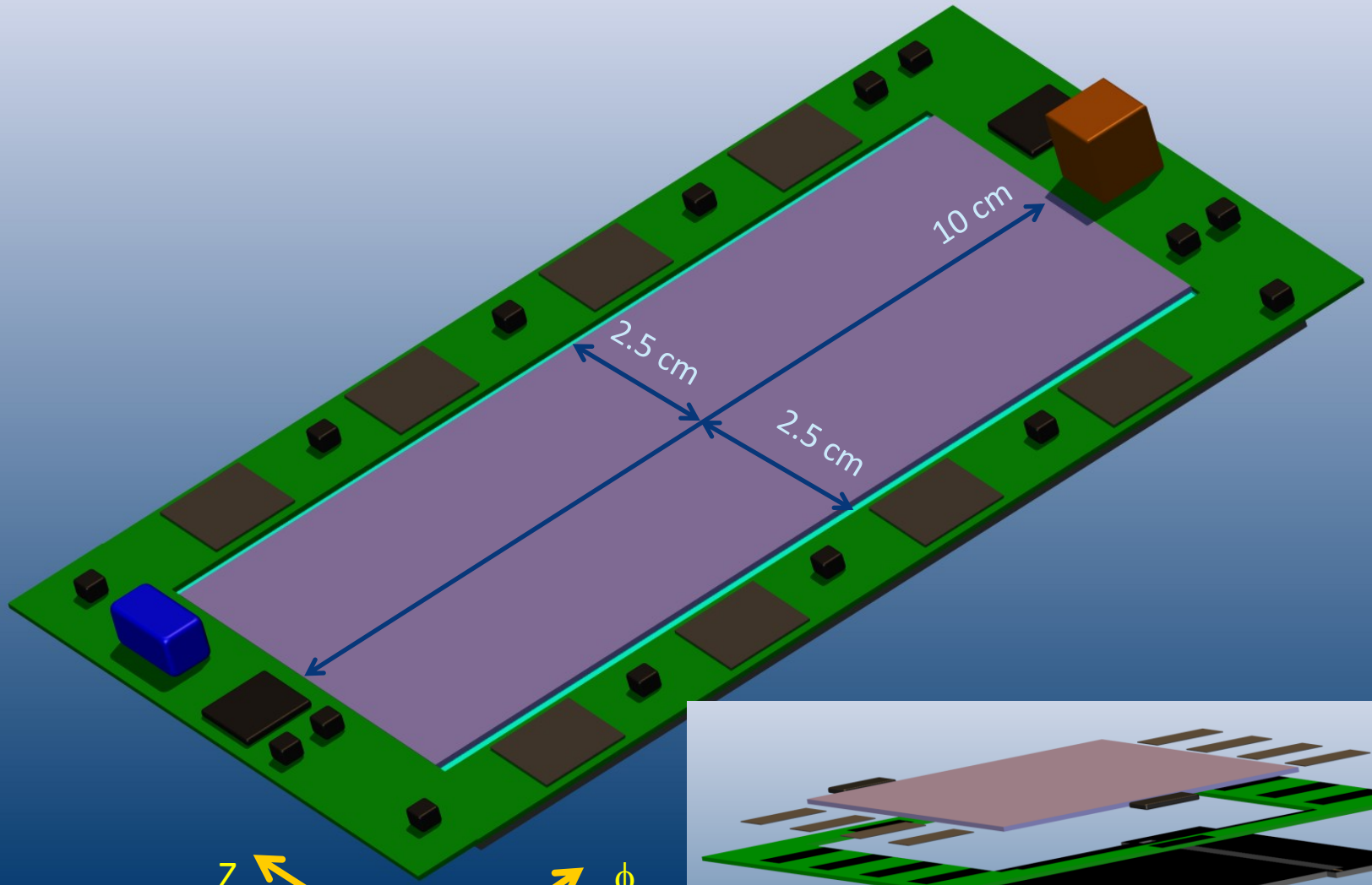
Hybrid strip-pixel Module



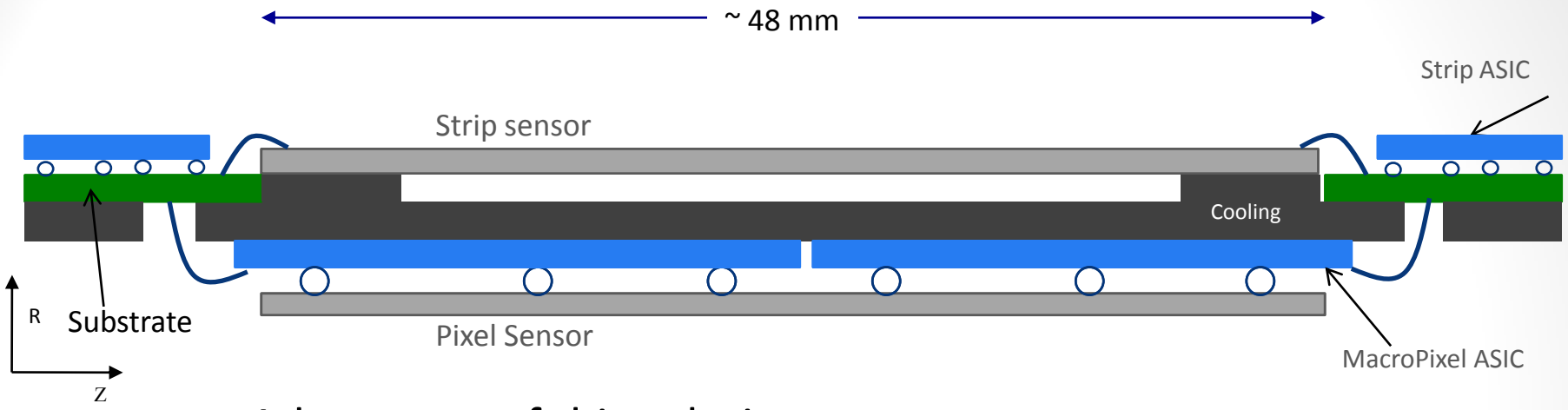
- Use one layer of short strip: ~24 mm
- And one pixelated layer of ~1.5 mm long pixels
- In the pixelated layer, perform the OR of the pixels in the Z direction and use it as single strip in Z
- *Coincidence of the two layers provides pT cut*
- *Pixel position provides Z coordinate*

- Thickness: two sensors + Pixel strip RO + some interposer + hybrid sideways

~5 x 10cm Hybrid Module, Top



Simplified cross-section



- Advantages of this solution:
  - Wire bonding and simple C4
  - All silicon stack (no substrate under Sensor)
    - Low mass (cooling) interposer
    - No substrate-Si CTE mismatch problem

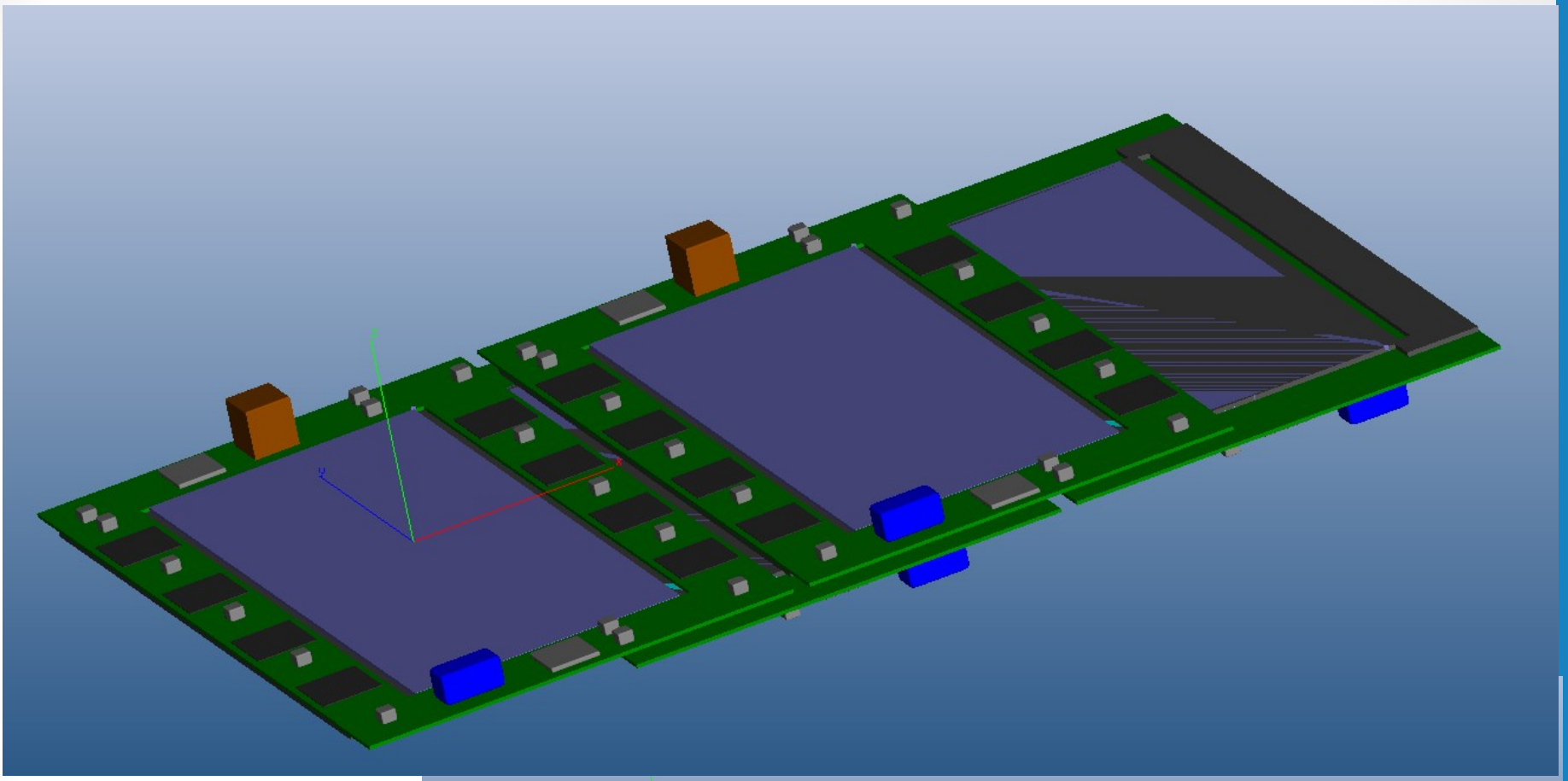
Pix Sensor 250um
C4 bumps 125 um
Pix chip 250 um
TPG+Carbon 600um

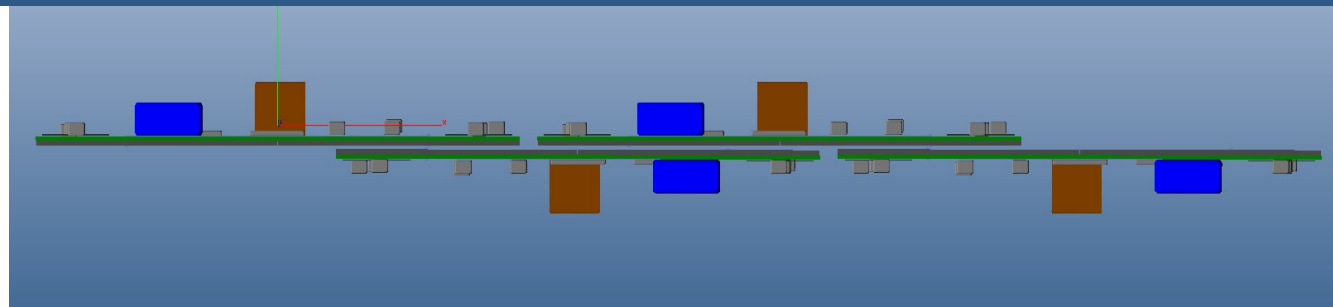
TPG / Substrate 900 um

Strip Sensor 250 um

Pixel ASIC on bumps (250 um)

Possible ROD assembly





Material Estimate (at $\eta = 0$)

Central sensitive area

Layer	*Material*	*Thickness [mm]*	*X0 [mm]*	*Contribution*
Pixel Sensor	Si	0.25	94	0.3%
C4 bumps	Sn	0.01	8.8	0.1%
MPA	Si	0.20	94	0.2%
TPG	C	0.80	280	0.3%
Strip Sensor	Si	0.25	94	0.3%
			Total	1.1%

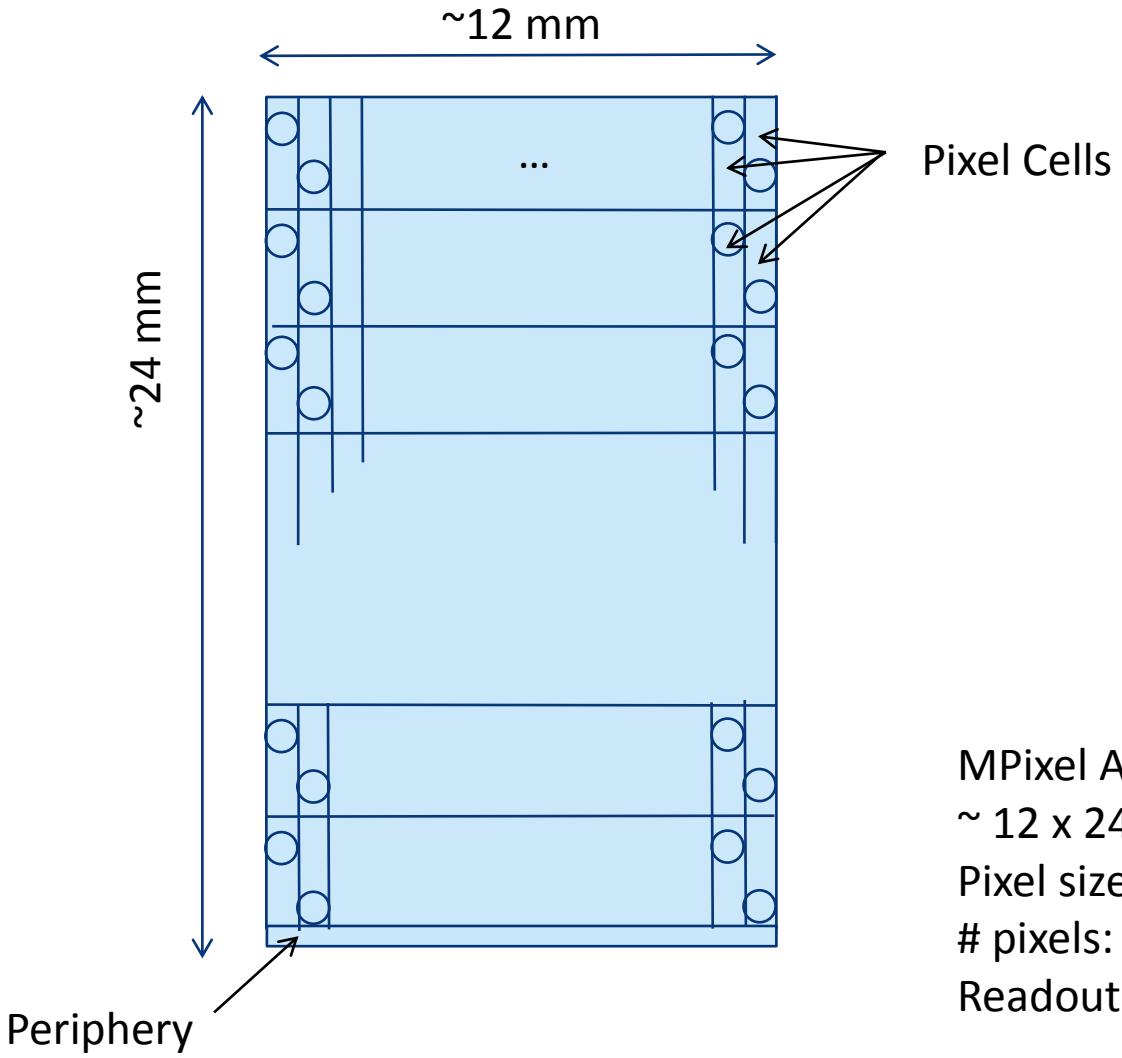
Peripheral "electronics" area

Layer	*Material*	*Thickness [mm]*	*X0 [mm]*	*Contribution*
SSA	Si	0.20	94	0.2%
C4 bumps	Sn	0.01	8.8	0.1%
FR4 PCB	Composite	0.80	185	0.4%
Cu on FR4	Cu	0.05	14.3	0.4%
TPG	C	0.50	280	0.2%
			Total	1.2%

- In the “electronics” area, the size of the SSA and C4 bumps have been exaggerated to the entire hybrid area but passive components not accounted for
- DC/DC and GBT not accounted for

ASICS

Macro-Pixel-ASIC global floorplan

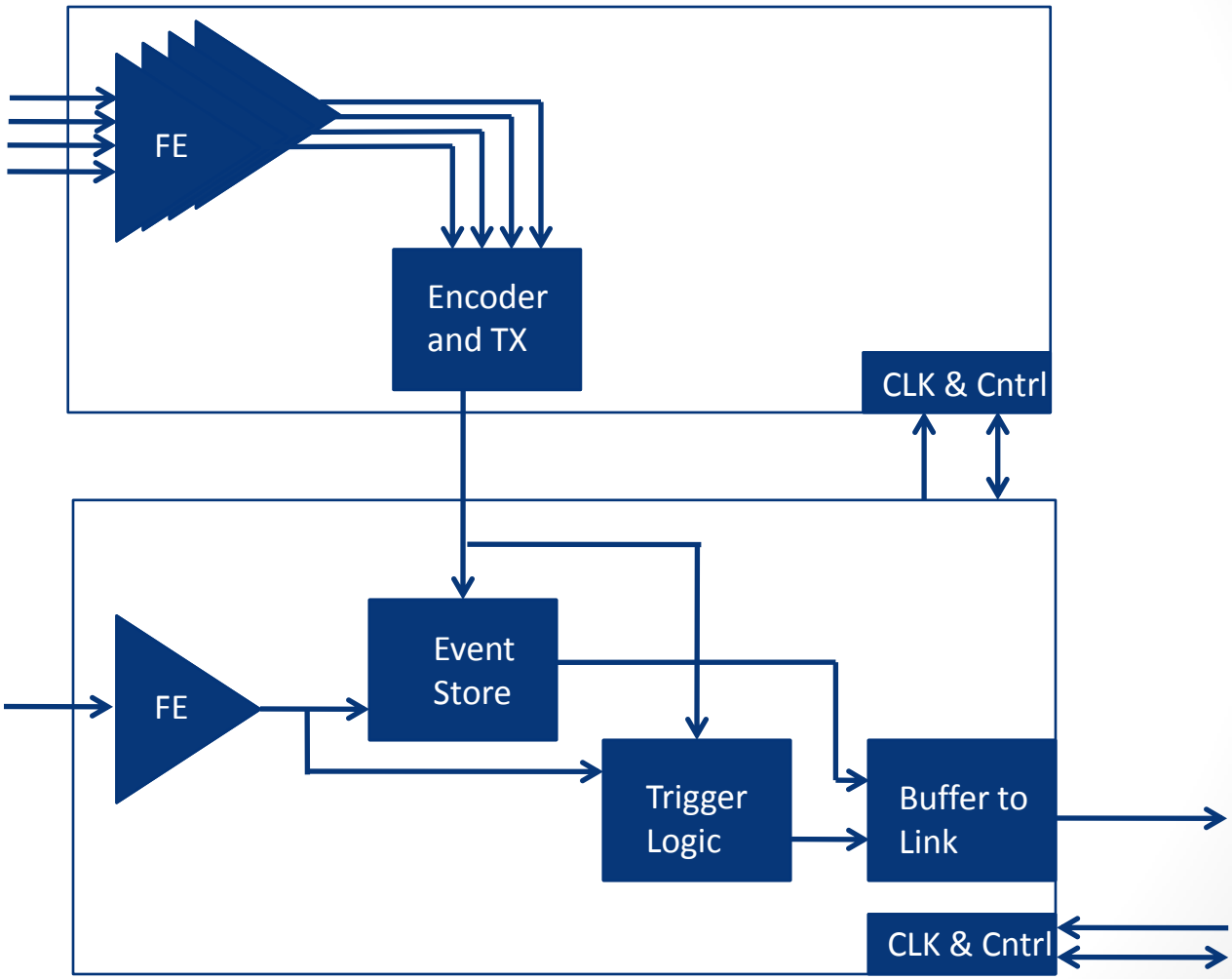


MPixel ASIC size:
~ 12 x 24 mm2
Pixel size: ~ 100 um x 1500um
pixels: 128 x 16 = 2048
Readout on one edge only

Module functional block diagram

Pixel Layer
MPA

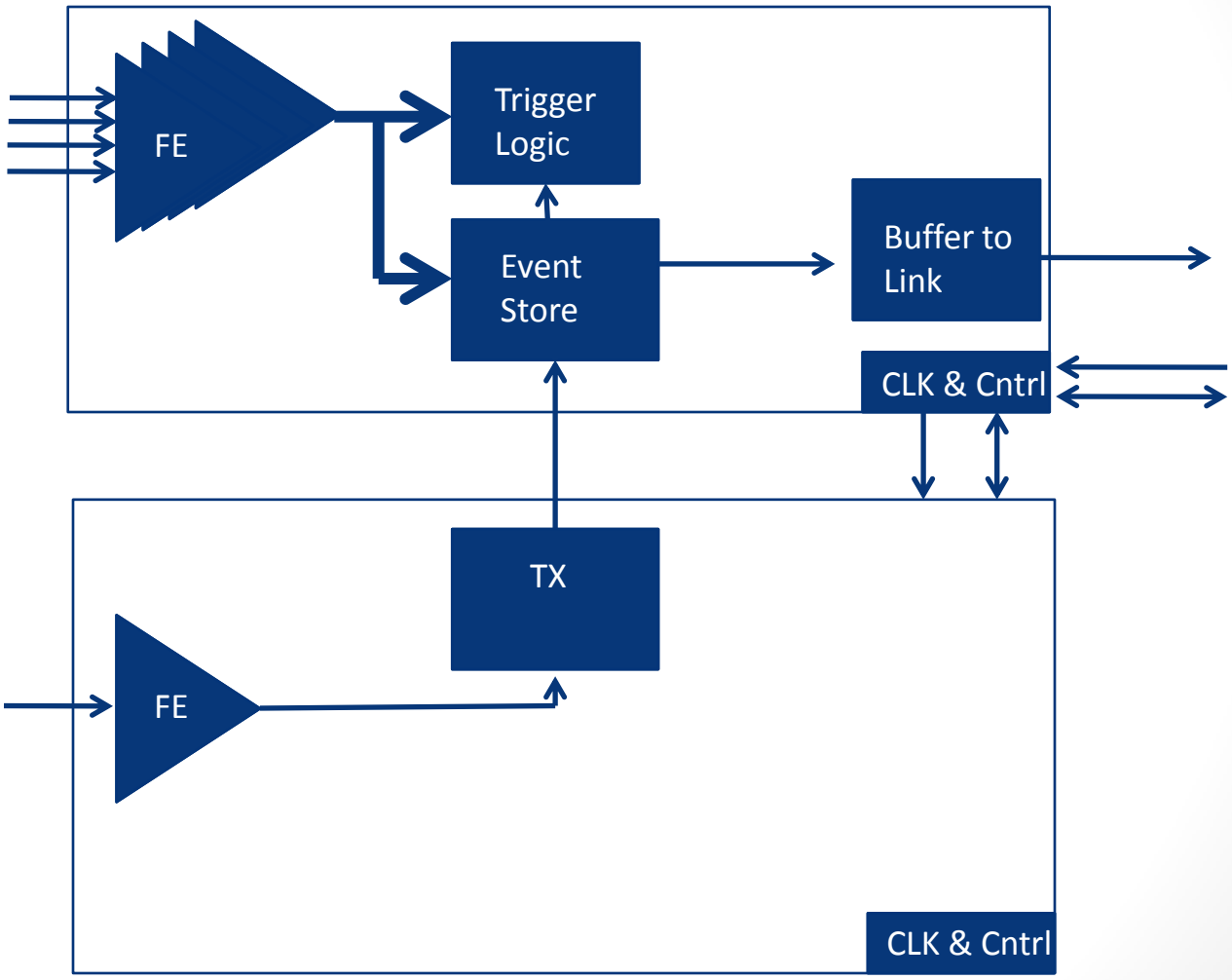
Strip Layer
SSA



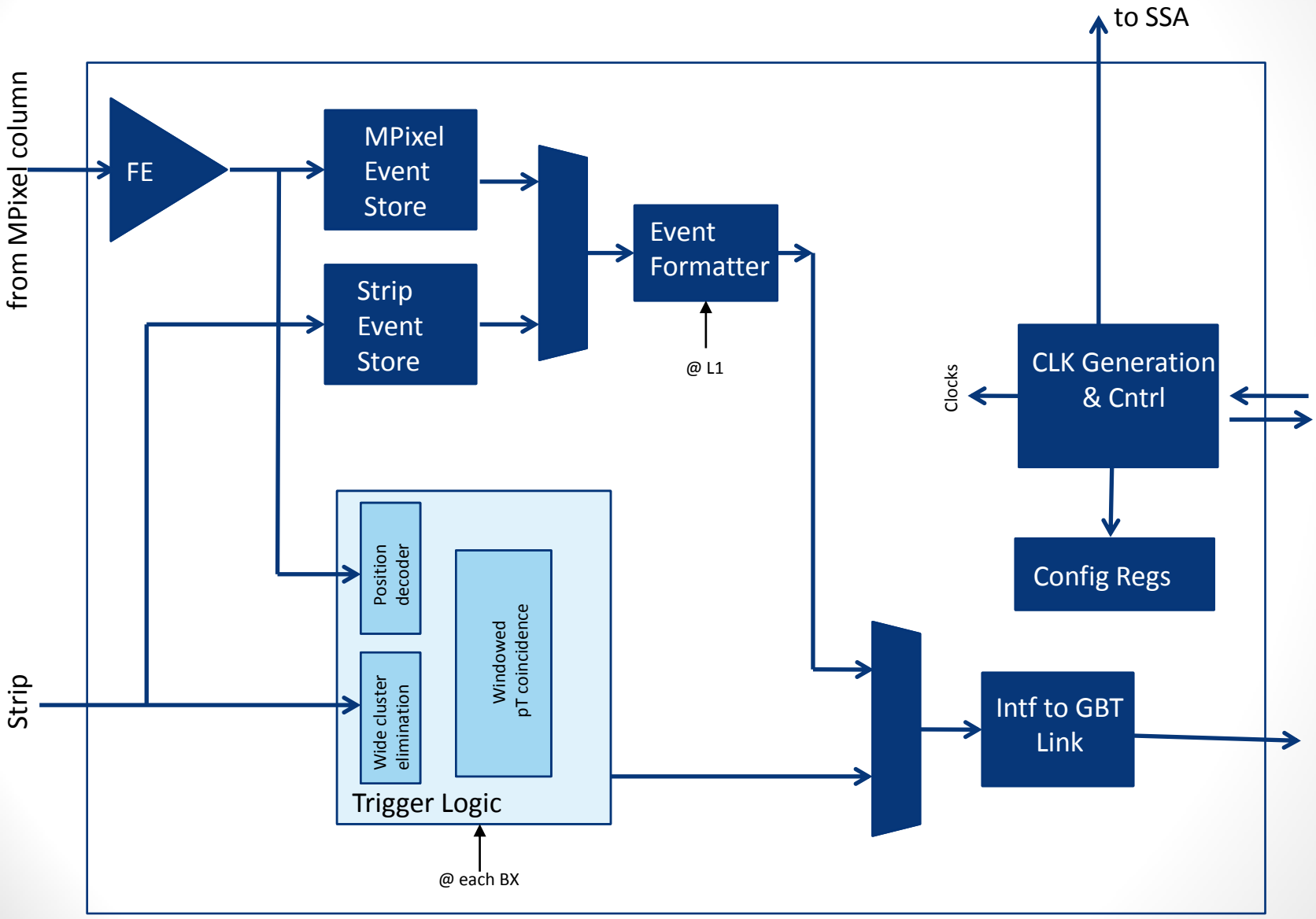
Better module functional block diagram

Pixel Layer
MPA

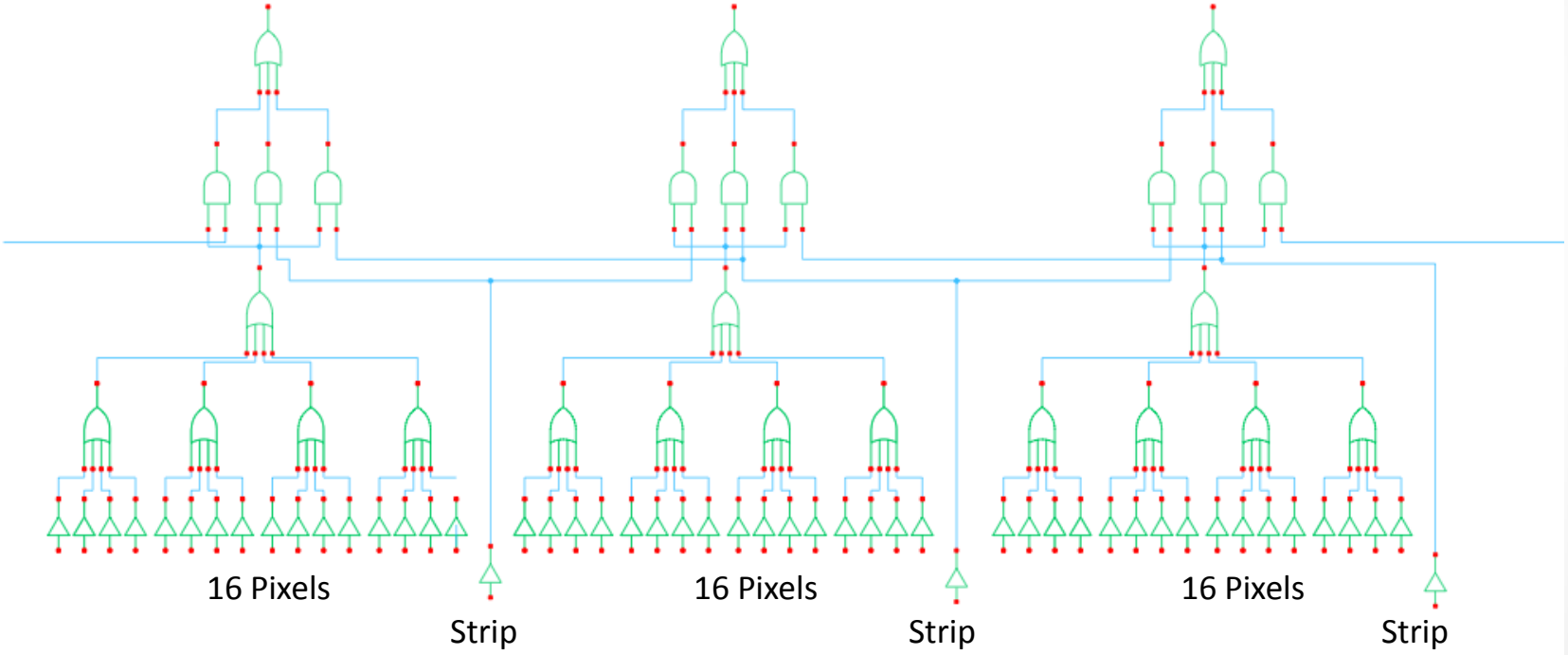
Strip Layer
SSA



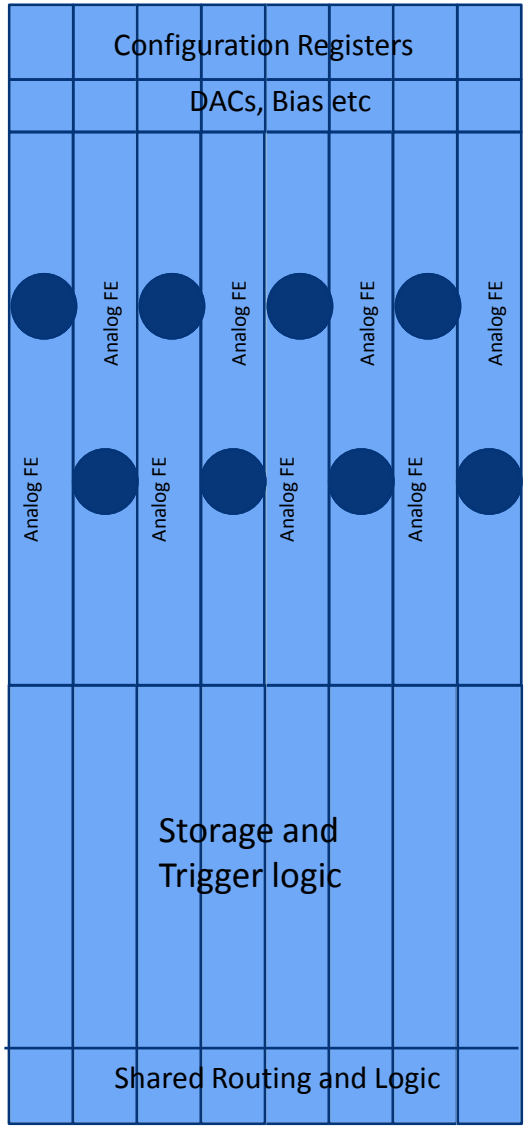
MPixel ASIC: more details



Simplified Stub finding logic



Macro-Pixel-Asic detailed floorplan



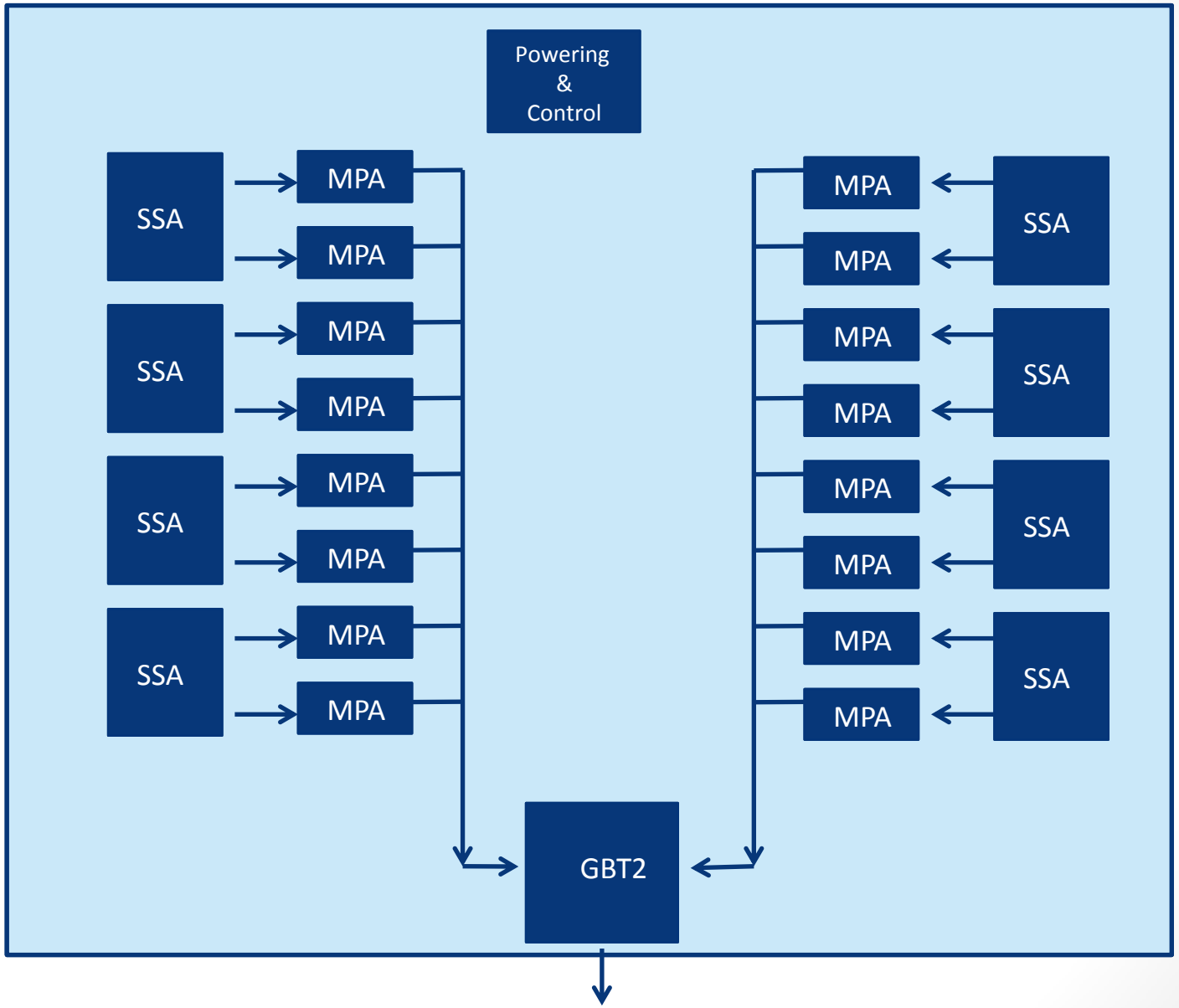
Single Pixel size: 100 x ~1400 μm^2

- Analog Pre+Shaper: 100 x 600 μm^2
- Bias, DACs etc: 100 x 50 μm^2
- Configuration Regs: 100 x 50 μm^2
- Storage & Trigger : 100 x 600 μm^2
- Routing & Interconnect: 100 x 100μm^2
- C4 Bump-bond pad: 90 x 90 $\mu m2$
  Pitch 200 μm in X, 300 in Y

Overall L1 memory requirement for
- Width :
  (5 [bit/16 pixel] + 1 [bit/strip]) * 128 = 768 bit

Size of RT SRAM		
	1 bit	**200 kbit**
130 nm	4.2 μm^2	910 x 910μm^2
65 nm	1.5 μm^2	550 x 550μm^2

Module Block Diagram



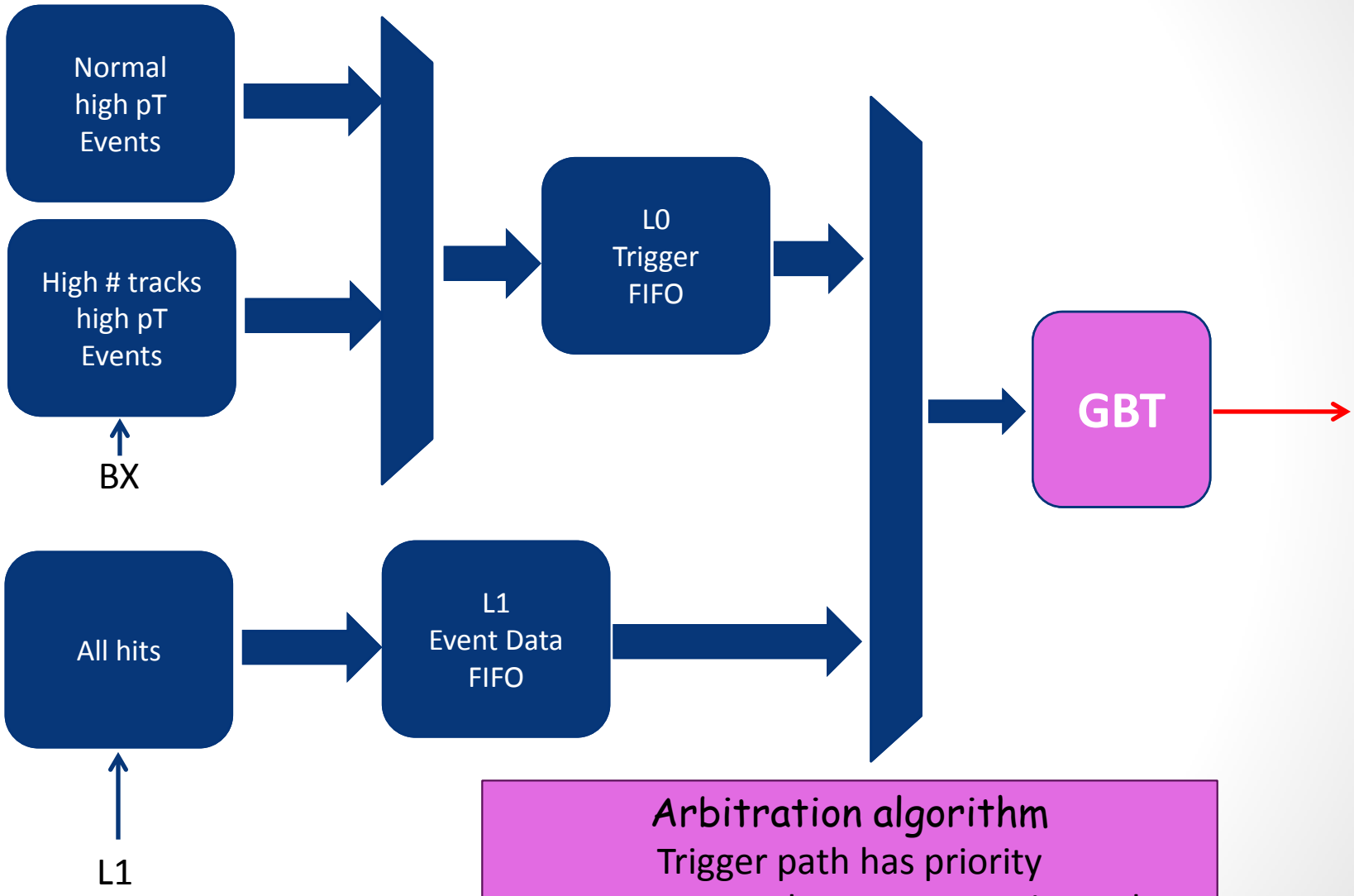
Hybrid Module Power estimate

	# elements	Pwr/element[mW]	Power [mW]
Pixel	2048 * 16	< 0.080	2,620
Strips	256 * 8	0.250	512
Trigger Logic @ 160MHz with α = 1%	10^6 * 16 * 160	0.000015	384
LP-GBT	1	500	500
DC-DC [η = 85%]	1	600	600
Total			~4,600

For a ~10 x 4.5 cm^2 module

DATA TRAFFIC

Trigger and L1 Data Data-Flow Model



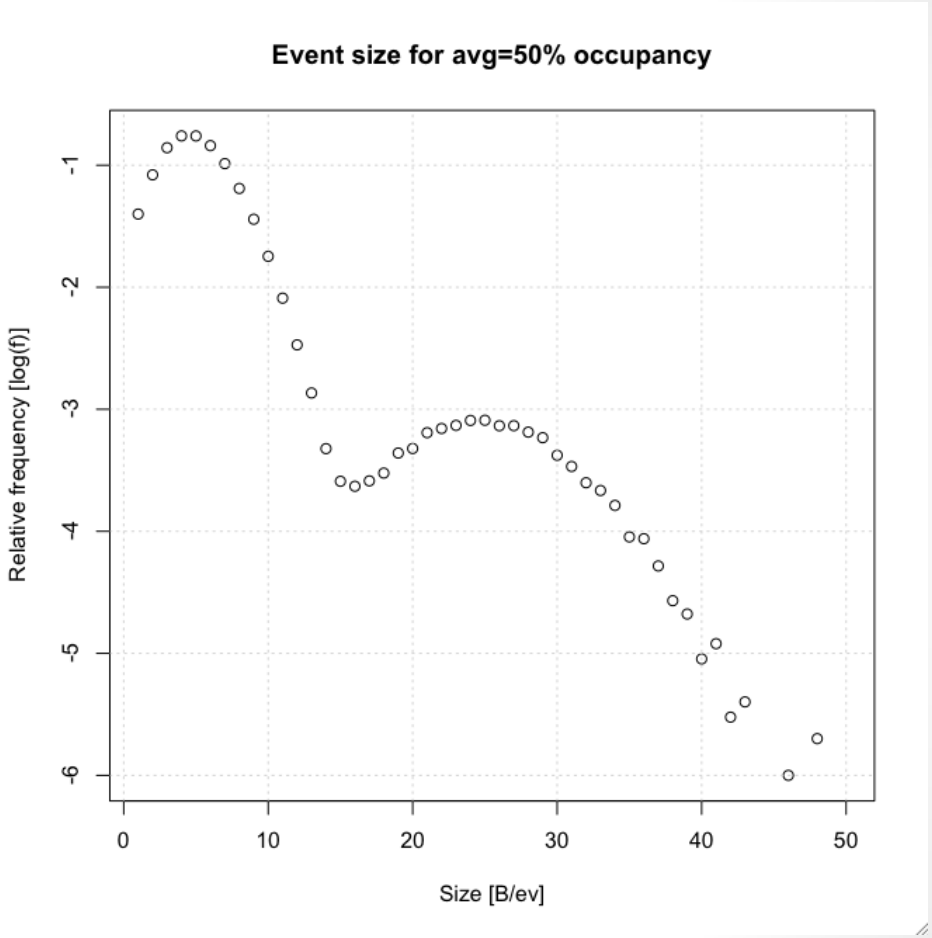
L1 Data volume with ZS (*)

- With 100KHz L1 and 8 bit to code one strip:
  - 1.5% hit probability($) (and 2 strips/hit):
    - On 256 channels SS strips: ~(0.015*256) * 8 = 32 [bit/10usec]
      + 3 bit chip number = 35 [bit/10usec]
    - 0n 128 channels MP pixel:
      ~(0.015*128) * (7 + 4) [bit/10usec] = 22 [bit/10usec]
      + 4 bit chip address = 26 [bit/10usec]
  - Total = $35_{SS} + 26_{MP}$ [bit/10usec]
  - Time tag: 8 bit
- Per module (with 16 MPA, i.e. 4 bit address + 8 SSA, i.e. 3 bit address chips):
  - 8 + 16*26 + 8*35 = 704bit/10usec ~ 70.4 Mb/sec

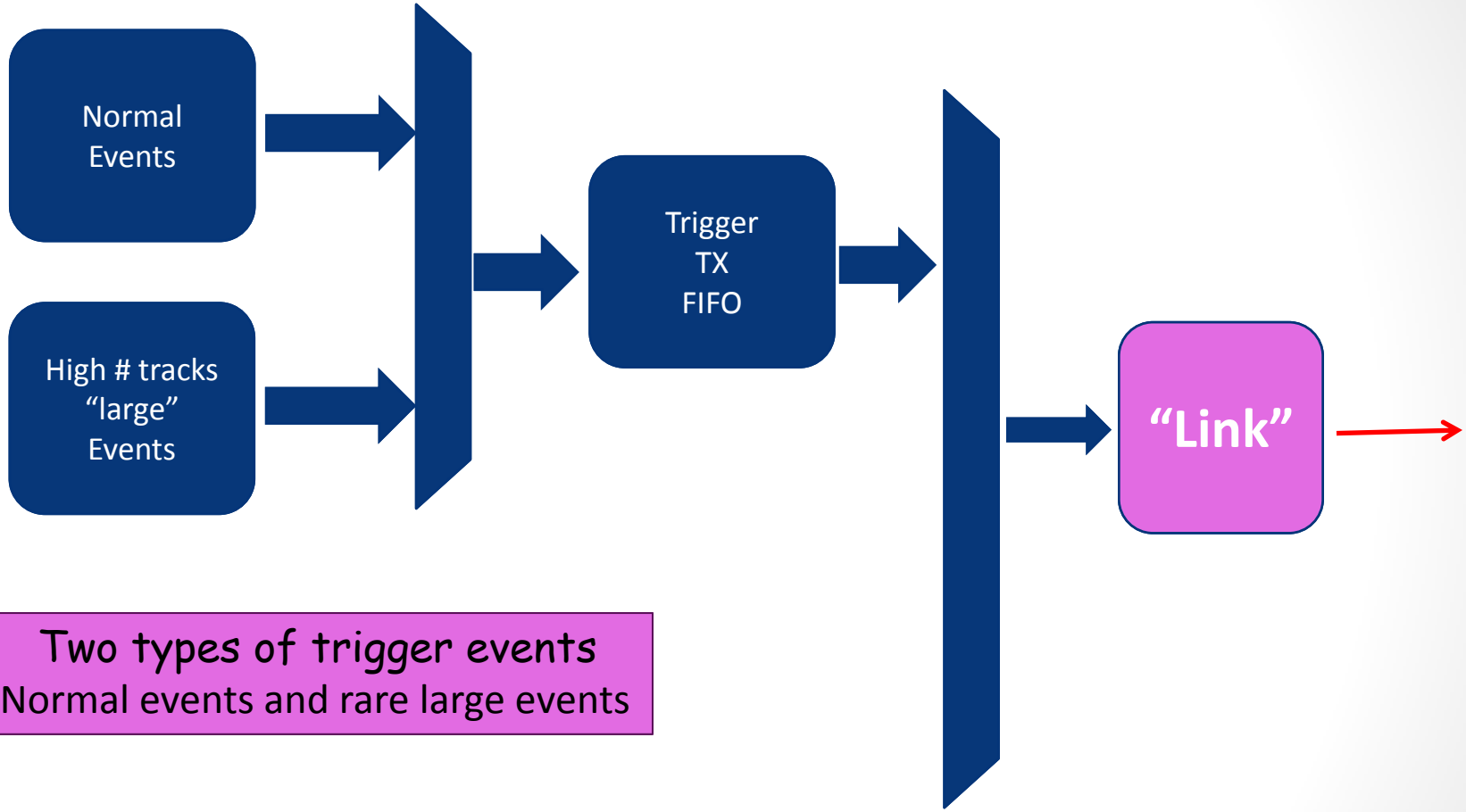
(*) Overhead of detailed packet format ignored
($) from M. Pesaresi's talk 22.03.11

L0 Trigger data volume

- Assume an optical link with a capacity of 10 [B/25ns], i.e. 3.2 Gbit/sec
- Assume that the average traffic generated uses 50% (40 to 70% actually modeled) of the total link capacity with two types of events
  - "Normal" events: at nominal capacity
  - Rare "large" events (with 1 to 10% probability)
    - Large events are 5x larger than normal ones

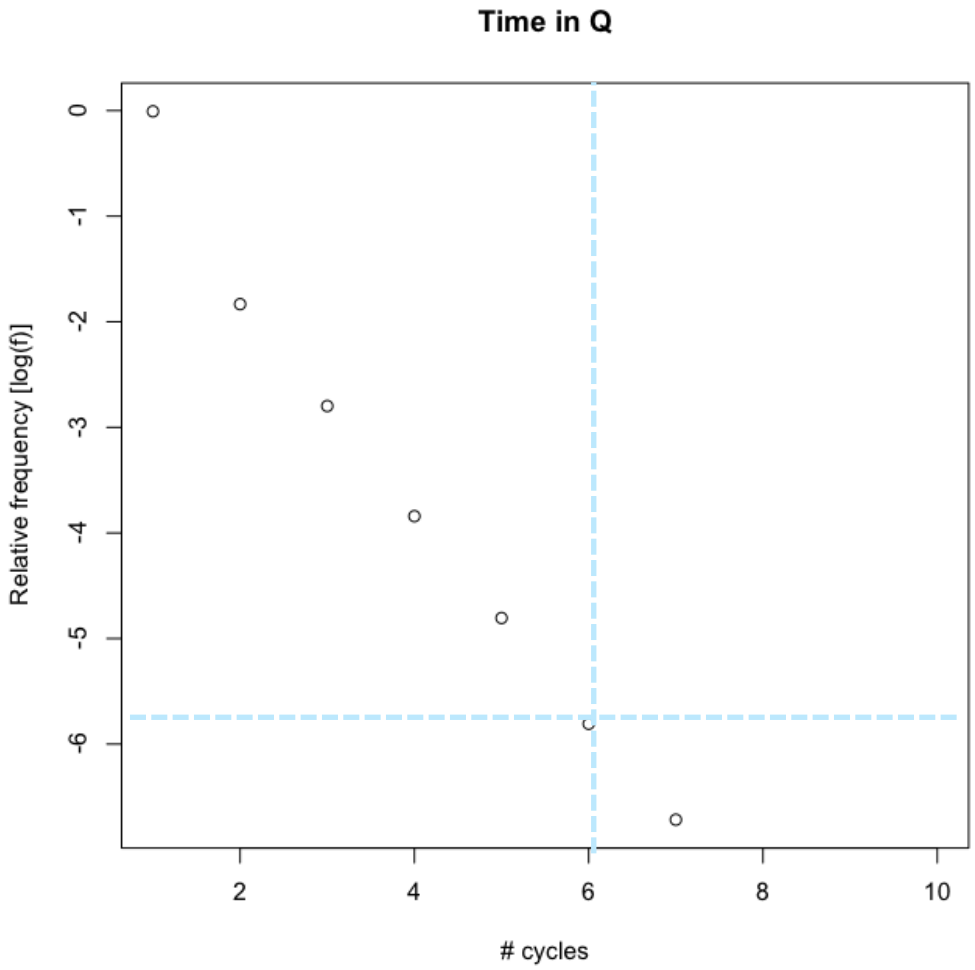


Trigger only Data-Flow Model



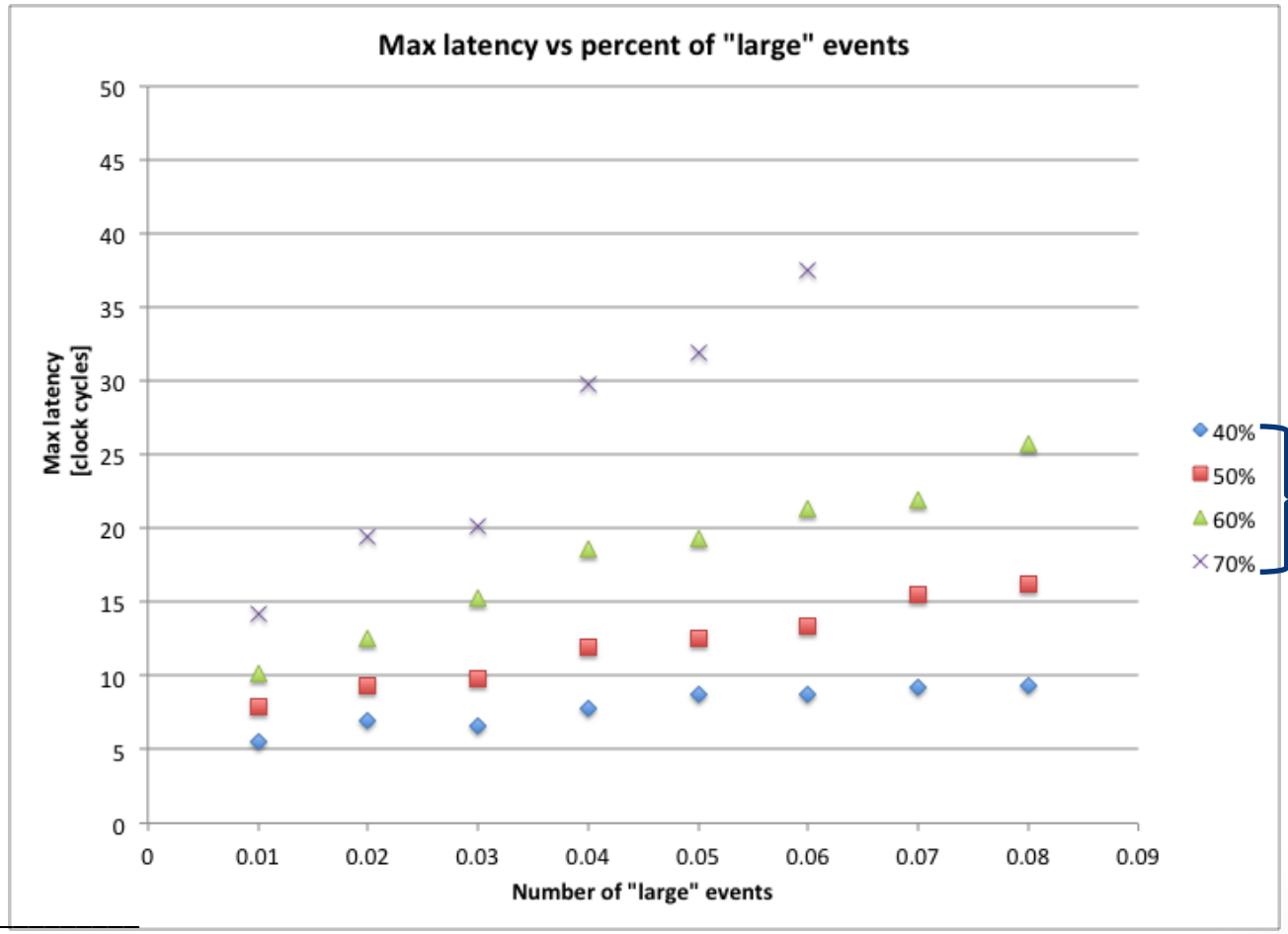
Two types of trigger events
Normal events and rare large events

Latency in Q at ½ link capacity (trigger only)



(40*10^6 events generated),
Frequency of large event is 1%

Link latency vs. percent of large events for different avg utilization (trigger only)



Avg link utilization

(40*10^6 events generated,
Worst case latency shown)

Acceptable max # of stubs

- At 50% link occupancy, i.e. allowing an average traffic of 5 [B/25ns], one has 40 bits/25ns available
- Each event has to be tagged with an 8 bit time stamp, and assuming 4 bits to code a hit in the pixel
- Number of permissible stubs:
  $(8 + 4) * n_{stubs} + 8 = 40 \rightarrow n_{stubs} = 2.7$ [stubs/25 ns*module]

CONCLUSIONS

Critical technologies

	Difficulty level (1 easy, 5 hard)	Comment
Analog Circuitry	3	Novelty required to reduce power, but is there any margin left?
Digital Circuitry	1	
ASIC Technology	4	Very large MPA, but testable
Local Interconnect	5	No risky technology involved, but sensors are bigger than commercial MCMs and little in-house (HEP) experience
Powering (DC-DC)	4	Reduce amount of material in passives
Links	5	Speed ok, power and size to be reduced

Summary

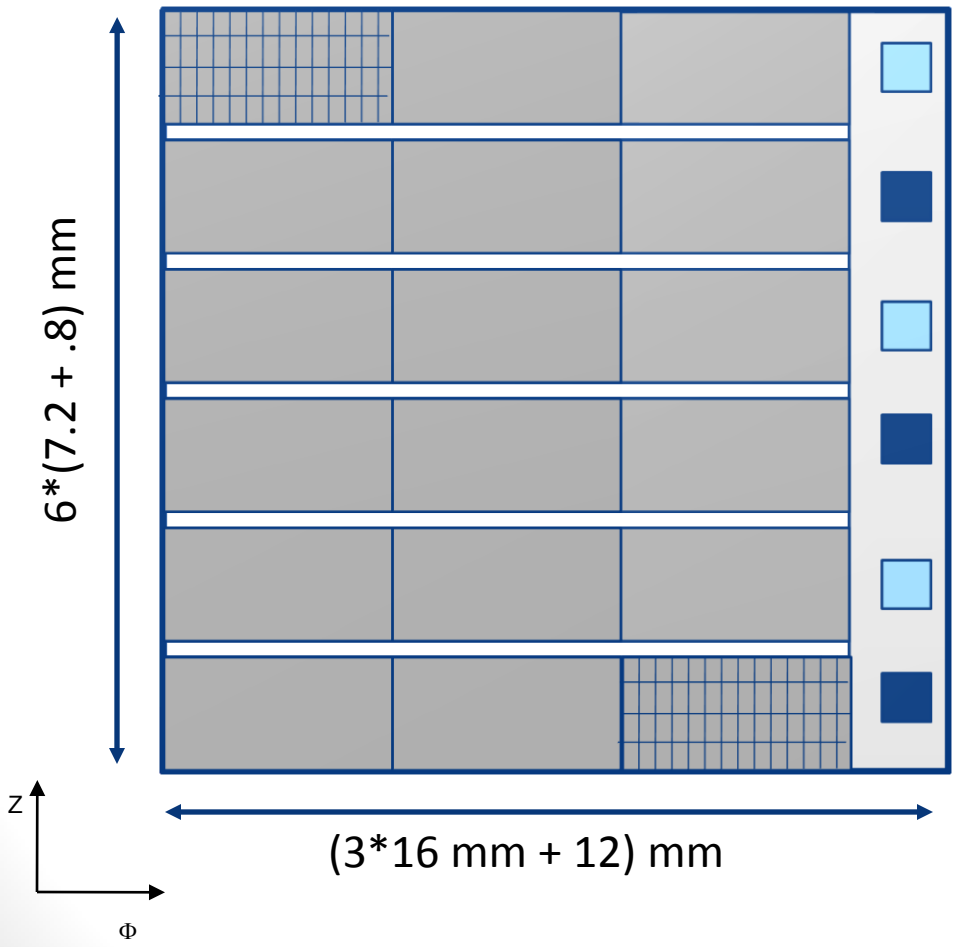
- Triggering on high pT particles requires detector to provide “primitives” and not just “points”
- Hybrid (pixel + strip) architecture could optimize several aspects:
  - Provide pT cut with required precision
  - Allow Z-measurement
  - Require less complex connectivity i,.e. retain advantage of the “à la Roland” minimal lateral connectivity
  - Affordable power
  - Can be realized with technologies very similar to today’s pixels (not too aggressive)

Spares

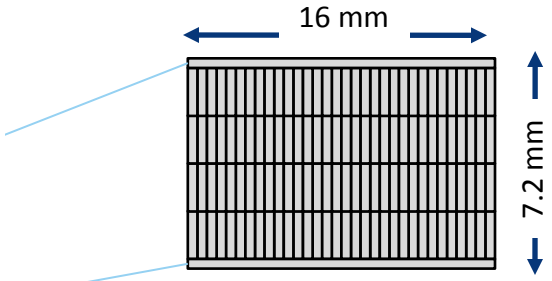
Comparison of architectures

	Z-info	Interconnect Complexity	Power	Material penalty
Dual strips	no	easy	low	low
Dual Pixel	yes	difficult	high	high
Hybrid	yes	moderate	moderate	moderate

2010 Module Layout

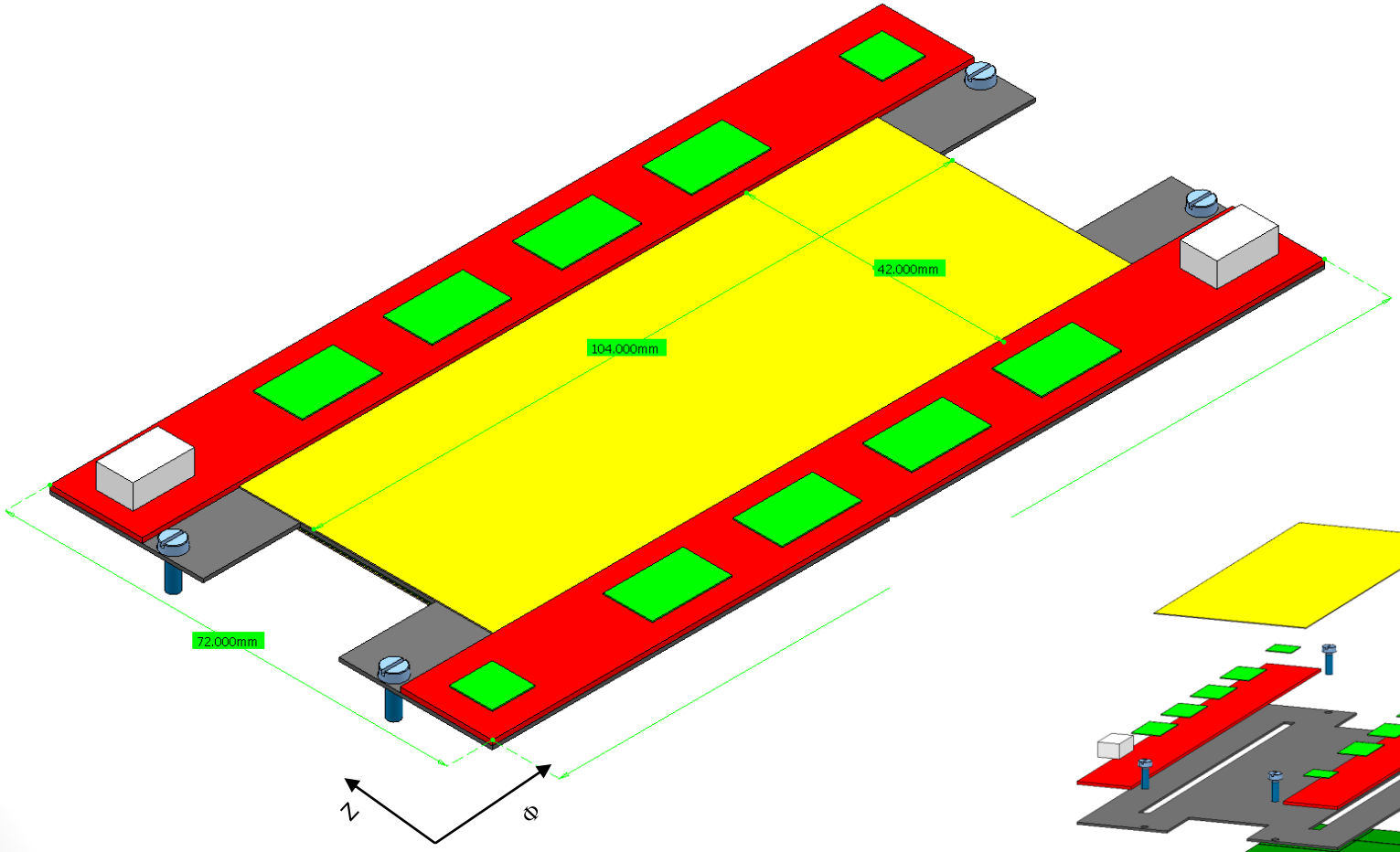


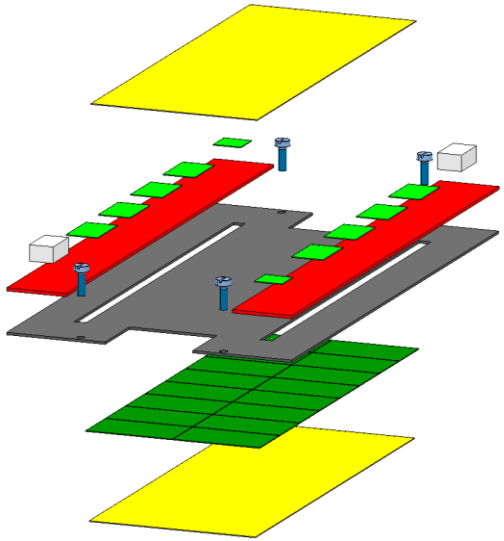
- Two sets of macro-pixels chips back-to-back on common interposer
- Allows both pT and Z measurement
- Very interconnect “dense”
- No “revolutionary” technology



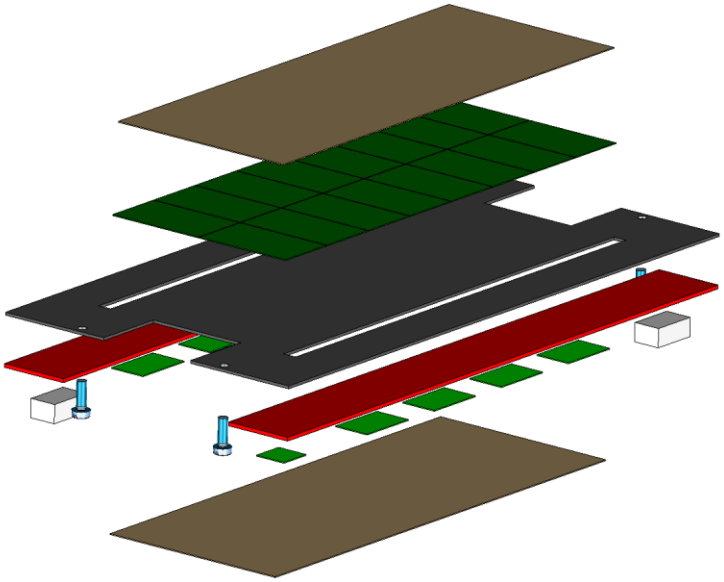
FE chip with
~ 160x4 pixels
of 100x2000 um

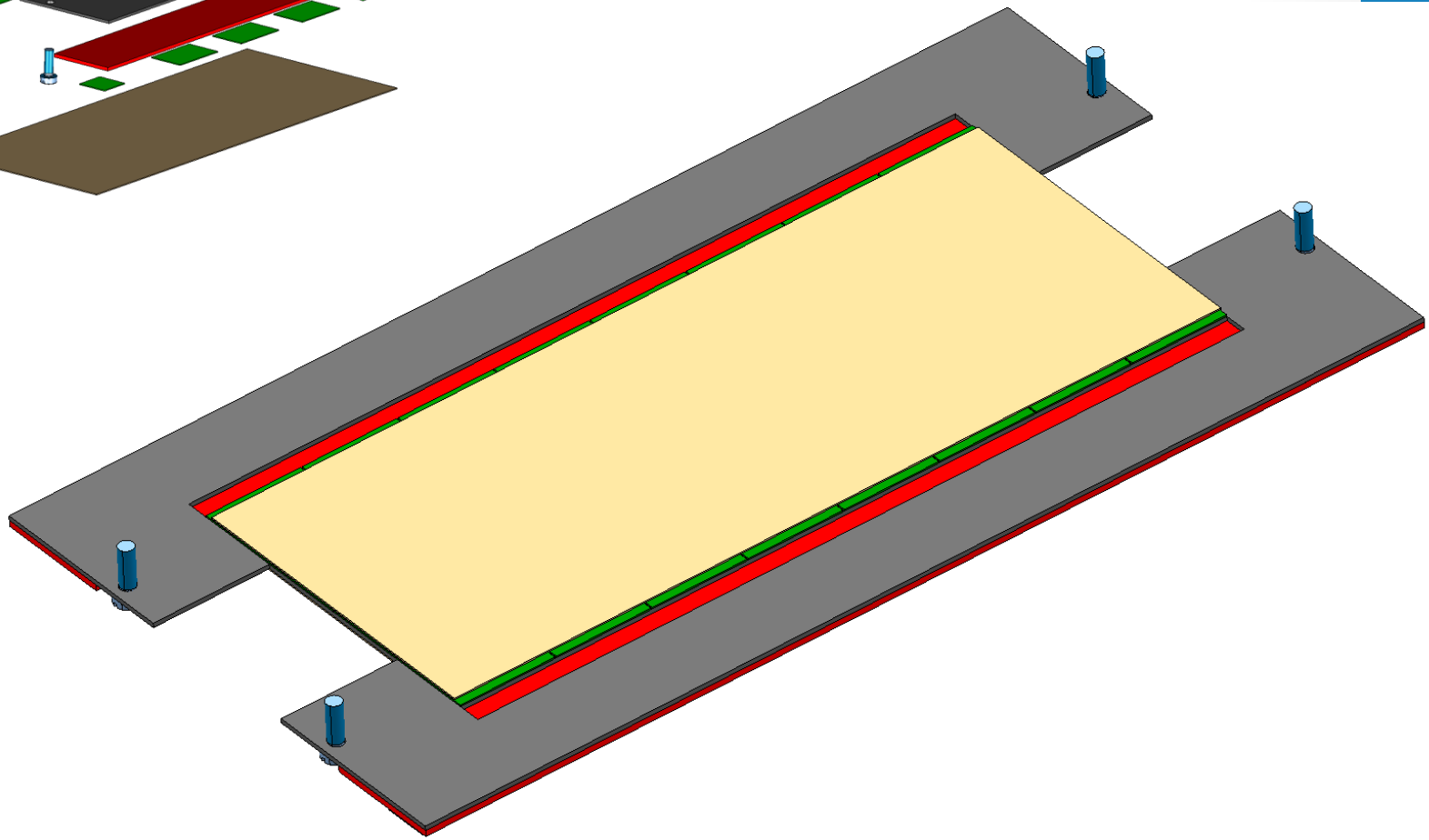
~5 x 10cm Hybrid Module, Top



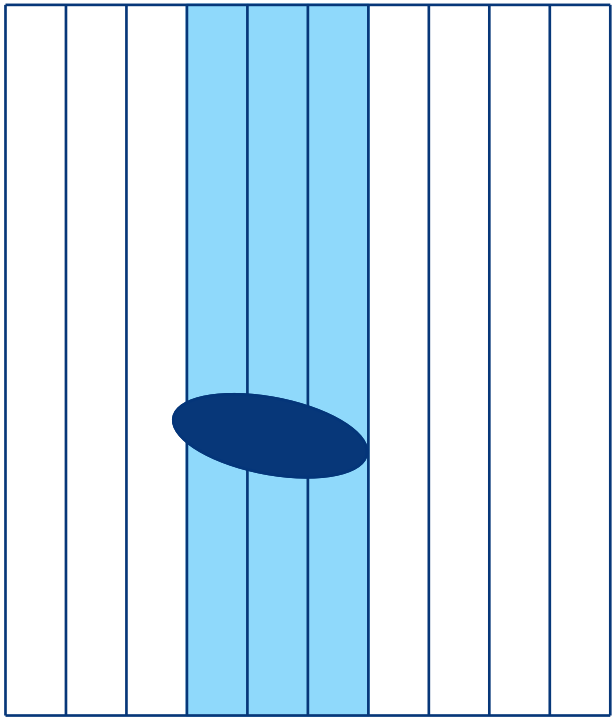


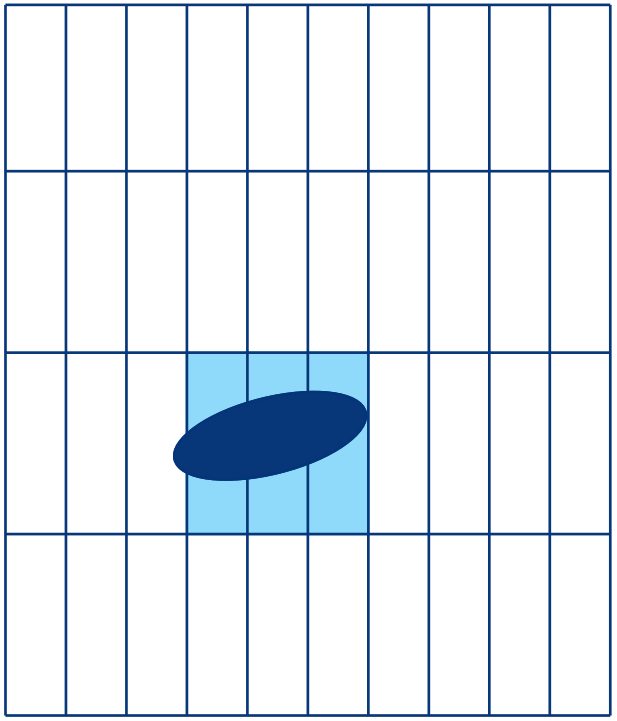
Bottom view





Cluster clean-up





- All these combinations (or larger) to be eliminated before attempting coincidences.
- Algorithm for clean-up:

  if any strip/pixel has more than one neighbor turned on in a ±1 vicinity,
  then all are turned off