



CMS Pixel Upgrade

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Pixel upgrade - why?

- The pixel detector was designed from the very beginning to be replaced during the lifetime of the LHC experiments (because of degradation of the sensors by hadronic irradiations)
- After 2017 LHC luminosities beyond the original design are likely – incapable by the present readout electronics
- Stay compatible with current system and installation procedure as much as possible

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An outline of the pixel upgrade (phase I)

- 1) Pixel tracking \bigcirc · From 3 hits/track to 4
- Material budget
 ✓ Keep it small (smaller!)
- 3) Performance 🗢 impact par., vertex, b-tag
- 4) LHC Luminosity \bigcirc · Ready to 2×10^{34} cm⁻²s⁻¹
- 5) Total Power demands 🗢 🔸 Kee
- Keep within pres. limits
 - use of LHC shutdowns

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6)

Scheduling

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Constraints for the pixel upgrade

- CMS must be physics-ready after each shutdown used for upgrade work
- minimize risk of damage, radiation exposure and accidents
- minimize start-up time and risk of compromised detector performance
- Consequently replacement impossible for power cables, readout fibers, pipes (from balcony to PP1)

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Pixel tracking: from 3 to 4 hits



Benefits of 4 pixel track points

Efficiency & resolution improvement for pixel-only tracks which are

- important for High Level Triggering
- seeds for full tracking \rightarrow resulting in
 - higher full track efficiency
 - lower fake track rate

important for primary & secondary vertexing
 (pile-up) (b-tagging)

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Material budget smaller !(?)

- Upgrade from 3 to 4 track points
 means 50-60% more modules!
- Expected mass ratio $R_m \equiv m_{2017}/m_{2008}$: - BPIX: $R_m \sim 0.57$ (n < 1.24) (~0.8 in %RL) 0.43* (n < 2.15)
 - FPIX: $R_m \sim 0.8 (n < 2.5) (\sim 0.5 in %RL)$ How is this possible ?

>cooling by 2-phase CO_2 instead C_6F_{14} >advanced mechanics + modified design

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* barrel part only

Mat. budget: "cool & mech"

 CO₂ cooling (total mass barrel layers): - 3 layers (2008): 3655g (1197g for cooling) - 4 layers (2017): 3029g (577g for cooling) - 4 layers (C_6F_{14}) : 4473g (2021g for cooling) other layer mat.: 2008(3L) 2017(4L) 224g - mechanics (w/o pipes) 1869 - modules 870g 828g - cables 159q 141g

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Cooling aspects

Present cooling using C_6F_{14} contributes a major fraction to the mat. budget.



Two-phase CO2 cooling requires only small diameter tubing, despite high pressure operation (up to 70bar).

Therefore changing the C_6F_{14} cooling system into a CO_2 system is rewarded by the largest fraction of material savings.

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CO2 cooling: pros and challenges

•Excellent thermodynamic properties:

- small viscosity
- high heat transfer
- high latent heat
- low liquid/vapor density ratio
- 🗢
- small pipes (1.6/1.8mm^ø) possible
- low mass (~half of C₆F₁₄)
 radiation hard
 cheap

• Challenges:

- Two-phase flow: predictions inaccurate; requires close cooperation between experimentalists and system designer.
- cooling plant design (~10kW @ -20°)
- primary cooling system
- pipe from plant \rightarrow PP1 (pressure!)
- channels from PP1 \rightarrow PPO (space!)
- control & monitoring
- validation of system operation
- warm start-up
- safety issues

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Prototype mechanics 1st layer



Weight Layer1 51g + 11g $CO_2 \rightarrow 40\%$ of old first layer

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Mat. budget: "shift & save"



Innermost section of supply tube contains :

AOHs, DOHs, PCBs, cables, connectors, fibers Total mass:

4 x 2289g

Mat. budget: "shift & save"

Supply tube 2017: First prototype made by S. Streuli

Sensor module connector board area (BPIX layer 3&4 outside, 1&2 inside)

Cable trench area (BPIX layer 3&4 outside, 1&2 inside)

> Z=1260 η=2.59

Z=800 η=2.17

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Mat. budget: "shift & save"

Supply tube 2017: Innermost section contains:

Z=800	Material	Weight
	Airex C70/55	83gr.
	Carbon fiber ribs	11gr.
	Carbon fiber tubes	27gr.
Z=0	Carbon fiber wheel support	7gr.
	Carbon fiber facets	180gr.
	Epoxy glue	100gr.
	Total weight	<u>408gr</u> .
	add:	
	CO2-pipes 38g	
	cables 280g	
	Total: 4 x 726g	
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Expected effect on mat. budget



Remark: the shown budget for the upgrade is probably somewhat pessimistic!

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BPIX layout

New layout: Full module type only! Layer 1



yer radius	# faces	# module	s # ROCs
* 39mm	16	128	2048
68mm	28	224	3584
109mm	44	352	5632
160mm	64	512	8192
* Clearance to	Total:	1216	19456
beam pipe 4mm			81M pixel

(~1.7x old BPIX)



If beam pipe r < 22.5 mm \rightarrow 1st Layer: 12 faces <R>=29.5mm (32 modules and 512 ROCs less \rightarrow 1184 / 18944) beam pipe clearance 2.25 mm (~79M pixel)

FPIX disk design





inner & outer ring for easier replacement

- 6 disk of 112 sensors each \rightarrow 672 modules
- one module size with 2x8 ROC / module

→ 10'752 ROC's ~ 44M pixel (2.5 x old FPIX)

Impact parameter

- Improvements by:
 - more hits / lower mass (see above)
 - smaller 1st layer radius (beam pipe radius?)
 - closer approach to beam pipe (difficult and a potential threat to CMS / LHC)
 - 🗢
 - direct "blind" insertion into CMS to risky
 - final adjustment system needed
 - test on mock-up

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Installation mock-up



BPIX dummy + Supp. Tube



Adjustable wheel set for BPIX



Precise BPIX shell adjustment



Improved Impact parameter

Barrel region



Beam pipe r<23mm : 16 faces to 12 faces \rightarrow reduce MS term by ~0.75 \rightarrow total 0.75x0.6 = 0.45

Forward region

Pixel Track seeding



b-tagging

ttbar 80 < pt < 120 GeV Combined Secondary Vertex Tagger

No pile up

Lumiosity = $1E34 \text{ cm}^{-2}\text{s}^{-1}$



ROC ready for the upgrade?

Present ROC :

Luminosity cm ⁻² s ⁻¹ 1 x 10 ³⁴	bx-spacing ns 25	Data loss (@ 1 st layer) 4%	Approx. 50% more ROCs in new pixel detector. Limited number of readout fibers © boost readout frequency	
	50	16% 🛶		
2 × 10 ³⁴	25	15%		
	50	~50% ←		
Clearly, the present ROC is not appropriate for luminosities expected in phase-1			This bx-mode was not foreseen in 1998 when ROC architecture has been designed	
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New ROC : Hit rate capability

Unchanged: front-end amplifier, threshold + trimming, column drain 0.25µm technology

 \rightarrow

Present ROC:

32 data buffer

12 timestamp buffer no readout buffer (8 ROC seq.)

New ROC:

- \rightarrow 80 data buffer
- \rightarrow 32 timestamp buffer
 - 64 x 24 bit static RAM as readout buffer space for 96 cells (set after simulation) readout buffer storage: simultaneous read/write (6 bit counters)

Design/simulation done;



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Buffered Readout

present ROC



- •Double columns with verified data stops → no more events accepted
- •Double columns have to wait for external token → long dead time
- •Sequential readout of of 8/16 ROCs → high token delay
- •DCol readout parallel in all ROCs after trigger → reduced waiting time
- •ROC readout buffer: read/write simultaneous; data with different time stamps
- •Easy implementation in separate buffer on ROC → keep present DCol logic

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new ROC

data bus

trigger

26 Double Columns

Readout Buffer & Logic

internal token

external token

Header

ROC : Readout bandwidth

Present ROC: 40 MHz analog (6 levels \cong 2.5 bits)

raising frequency risky because limited rise time!

Solution:

"GO DIGITAL"

$\Rightarrow \Rightarrow \Rightarrow \Rightarrow \Rightarrow$

on-chip 8-bit ADC, clock = 80 MHz ROC readout: 160 MHz TBM readout: 320 MHz

 μ twisted CCA pair (Copper-Cladded Aluminum)

1 m long link at 320 MHz from TBM to POH; chips done



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Digital ROC Readout



ROC: Other improvements

- Lower signal threshold (~3000e- >> ~150e- amp.noise)
 - chip internal X-talk (analog: identified, easy to solve \rightarrow layout digital: identified, more simulation req.)
- Linearity of pulse height (understood)
- Power-up behavior
- Removal of unused DACs
- Submission planned for Sept. 2011
- 2nd submission possible in 2012

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TBM (Token Bit Manager)

Staged development (Ed Bartz, Rutgers)

- 1. Step: keep analog data handling, replace digital TBM core *
 - correct minor impracticability's
 - install handling of PKAM events
- 2. Step: replace analog section by digital version (160MHz)
- 3. Step: shift ROC data to 400(320)MHz, 4/5 bit encoding

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Modification of Pixel-FED

- Keep single slot size
- Keep VME base board

New daughter board (instead of 3 ADC cards) including Zarlink receiver

Don't need to remove current ARx12 → allows easy swapping between old and new systems
Need new front panel in any case

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H. Steininger, M. Pernicka, HEPHY

Powering aspects

- LV power demands are based on present ROC data and up scaled
- up scaling existing power system leads to large cable losses (cable overheating !) and lack of power
- 🗢
- employ DCDC-converter close to detector and modify power supplies (A4603 from CAEN) to operate at higher voltage (→ less cable losses)

(for details of the converter see talk by Katja Klein)

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ROC/TBM submission & Pixel Testbeams



Some duties for LS1 (proposal)

- repair work if needed (BPIX, FPIX)
- install "Pilot system" on 3rd disk place
 - few blades with new FPIX design (2x8 mod.)
 - new HDI, new Al cables, new port card, POHs instead AOHs
 - test new electronics readout chain, DAQ handling (2014-2016)
- "pixel-cooling-insertion" device
 - full BPIX dummy, correct cooling loops, resistive loads
 - $\Rightarrow CO_2$ cooling test at TIF (2013-2016)
 - → mechanical insertion test into CMS (2013)
 - equip few ST-slots with DCDC-conv. test new power system (upgraded A4603 PS-modules + dummy ROCs) (P5 & TIF)

 final P5 cooling commissioning in 2017 just before insertion of new BPIX

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Summary

- Roots of the CMS pixel upgrade project:
 - limitations for high luminosity & non-stand. LHC modes
 - partial detector replacement (after ~150 fb⁻¹)
- Project has been detailed & enlarged:
 - 4 hit system (improve tracking seed, vertexing, track efficiency)
 - reduce material budget (improve impact parameter, b-tagging)
 - keep inefficiencies low (up to 2×10^{34} cm⁻²s⁻¹, also for >25ns mode)
- Mandatory constraints:
 - minimize impact on other CMS detectors (no new piping, cabling...)
 - minimize changes of DAQ, DCS and other CMS-global software
 - minimize radiation exposure of service personnel

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