The Silicon Pixel Tracker – beginning of a revolution?

Chris Damerell (RAL)

The SPT concept was first presented by Konstantin Stefanov at the International Linear Collider Workshop in Sendai, March 2008. Shortly afterwards, the UK 'ceased investment' in the LC, but internationally, interest in the SPT has grown, not only for the linear collider.

CONTENTS

- **Design concept**
- **Mechanical simulations**
- **Feasibility – new results with advanced CMOS pixels from:**
  Jim Janesick (California) working with Jazz Semiconductors and
  Dave Burt et al (e2V and Open U) working with Tower Semiconductors } *foundries now united*
- **Next steps**
- **Practical realization for LC and other applications (possibly including LHC)**

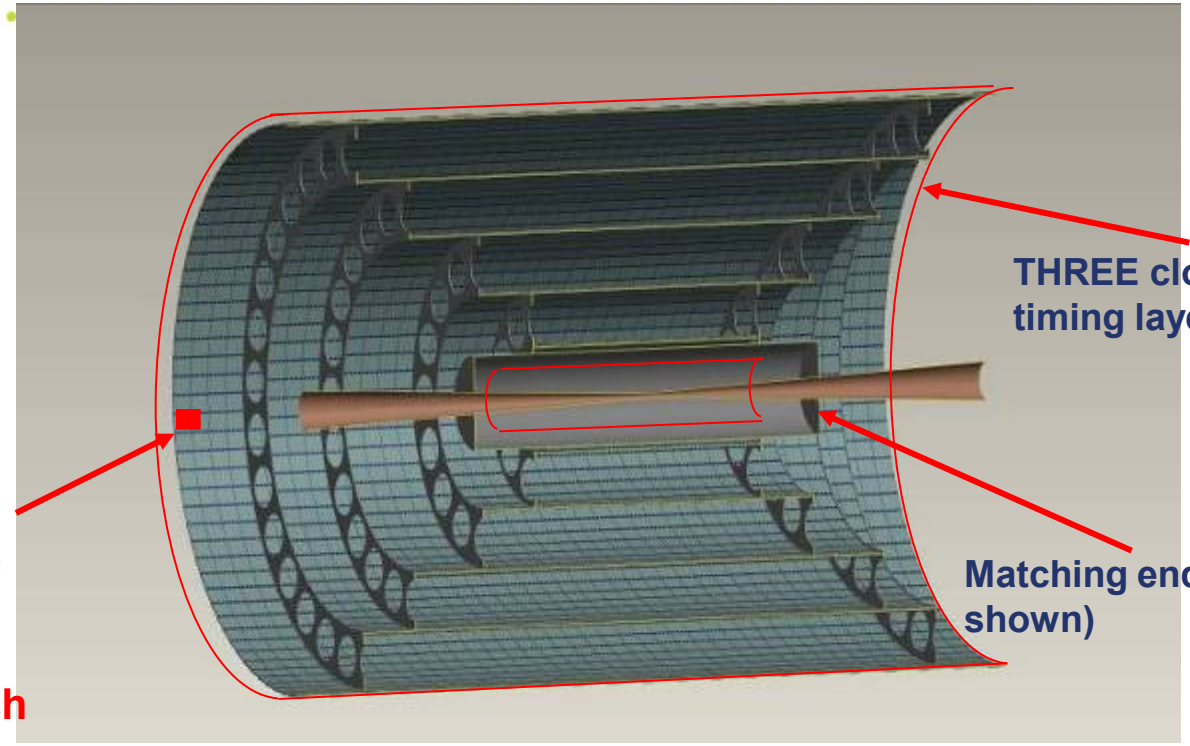
Design Concept – Linear Collider as one real-life example (1)

- **Goal is to devise a tracker design which significantly reduces the material budget wrt the currently projected leader, the SiD silicon microstrip tracker, which uses the same technology as the LHC GPD trackers**
- **Why push to minimise material in tracker?**
- **In general, we would like photons to convert in the ECAL not in the tracking system, clean tracking of electrons and minimal secondary interactions of hadrons**
- **Looking at previous tracking systems, they have all 'gone to hell in the forward region'**
- **This has diminished the physics output. Since we don't have any counter-examples, it's difficult to quantify**
- **The largest pixel tracking system in HEP (the SLD vertex detector with 307 Mpixels) used CCDs. Advanced CMOS pixels have evolved from this technology, achieving far higher functionality by in-pixel and chip-edge signal processing**

Design Concept – Linear Collider as one real-life example (2)

- **Basic SPT concept is a 'separated function' design – precision timing on every track *but not on every point on the track.* So we suggest an optimised mix of tracking layers and timing layers, the latter with single-bunch timing precision**
- **Key features are binary readout and on-sensor data sparsification**
- **Thin monolithic *charge-coupled CMOS pixels* offer a different 'separated function' feature – evading the link between charge collection and charge sensing given by the *'capacitance matching theorem',* with great advantages in terms of power dissipation and noise performance**
- **By working with a *monolithic planar architecture* (CMOS technology) the systems will be scalable by 2020 to the level of ~40 Gpixels**
- **This design has evolved within the international SiLC collaboration led by Aurore Savoy-Navarro – whose interest and support is much appreciated**

Possible layout for the linear collider

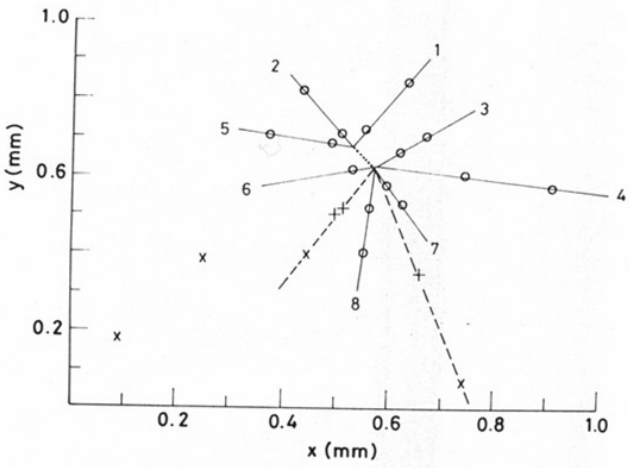


- Derived from SiD 5-layer microstrip tracker
- **Barrels:** SiC foam ladders
  - **Tracking layers:** 5 cylinders, ~0.6% X_0 per layer, 3.0% X_0 total, over full polar angle range ~50 μm square pixels
  - **Timing layers:** 3 cylinders as an envelope, ~1.5% X_0 per layer if evaporative CO_2 cooling ~150 μm square pixels
- **Endcap:** 5 tracking and 3 timing layers, closing off the nested barrels

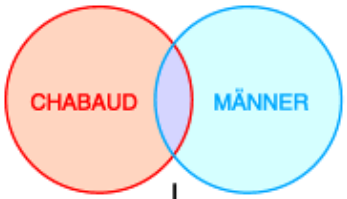
Track reconstruction

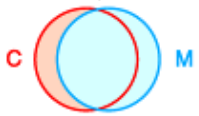
- Start with mini-vectors from on-time tracks found in the triplet of timing layers, together with an approximate IP constraint. 3 timing layers provide sufficient redundancy
- Work inwards through each successive tracking layer, refining the track parameters as points are added
- Background levels (~7000 out-of-time tracks at CLIC at 3 TeV) appear daunting at first sight, but pixel systems can absorb a very high density of background without loss of performance
- General principle, established in vertex detectors in ACCMOR (1980s) and SLD (1990s): fine granularity can to a great extent compensate for coarse timing. Precision time stamping costs power, hence layer thickness, whereas fine granularity need not
- Back-of-envelope calculations look promising (LCWS Warsaw 2008); hoping for some real simulations in near future
- 'Special methods' are envisaged for low momentum tracks, K-shorts, lambdas and photon conversions

Pixel detectors – advantages for track reconstruction



6 microstrip planes





2 CCDs added

ACCMOR 1984
Fred Wickens

A life-changing experience …

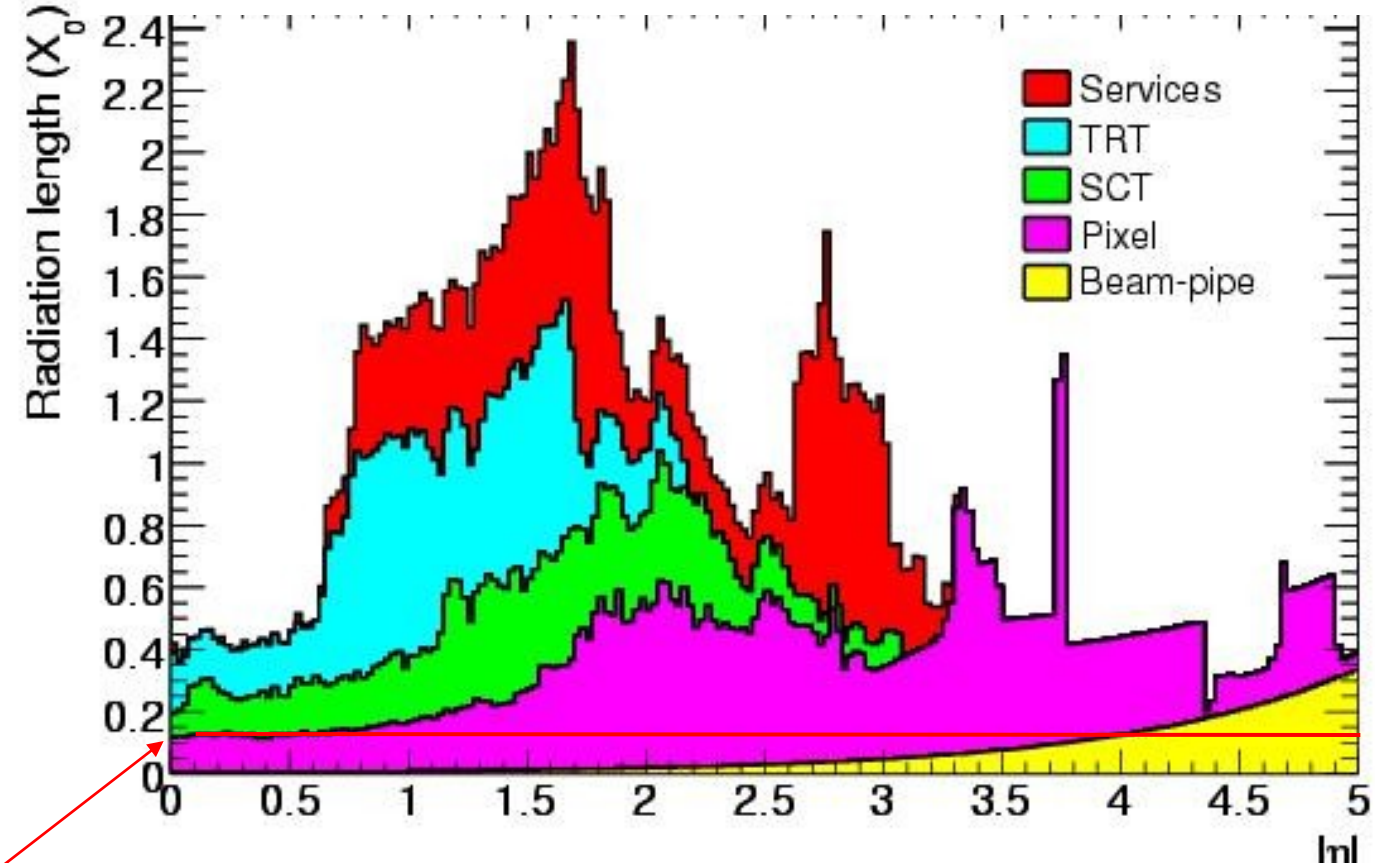
- **Unfortunate to assume that 'the better is the enemy of the good', when time is available for the necessary detector R&D**

Main challenges

- **Mechanical design – can such large and lightweight structures be made sufficiently stable?**
- **Overall scale - 33 Gpixels for tracking layers, 5 Gpixels for timing layers**
- **Need excellent and prompt charge collection efficiency, non-trivial for these relatively large pixels, which should be fully depleted through epi layer**
- **Need good noise performance, due to small signals from thin layers. Achievable with extremely low power, due to recent advances in charge-coupled CMOS pixels – a fast-moving technology**

- **Let's consider these issues in turn …**

Material budget - a major challenge



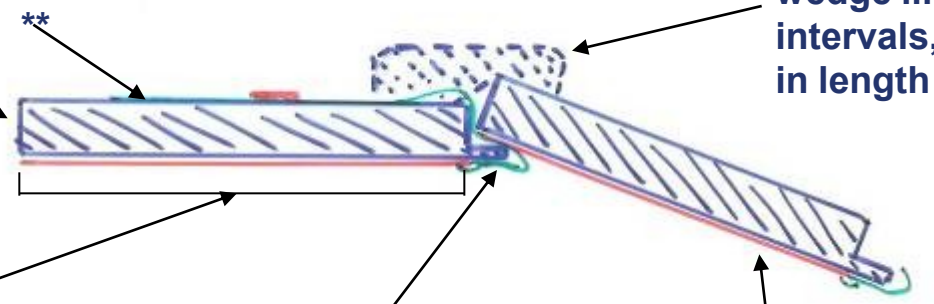
ATLAS tracking system

10% X_0, a frequently-suggested goal for the LC tracking systems (recently abandoned by LCTPC collab, but still the goal for SiD)

Our goal is <1% (vertex detector) plus ~3% (main tracker) ie ~4% total, followed by outer timing layers which may add ~5% [plus the inevitable obliquity factors]

End view of two barrel ladders ('spiral' geometry)

Adhesive-bonded *non-demountable* structure is 'daring' but justified by experience with gas-cooled systems using monolithic detectors (SLD, astronomy)



** Cu/kapton stripline runs length of ladder, plus tabs (~5 mm wide) which contact each sensor

Similar stripline runs round the end of each barrel, servicing all ladders of that barrel.

Sparsified data transmitted out of detector on optical fibres (1 or 2 fibres per end), continuously between bunch trains

Continuous (not pulsed) power for tracking layers, so minimal cross-section of power lines

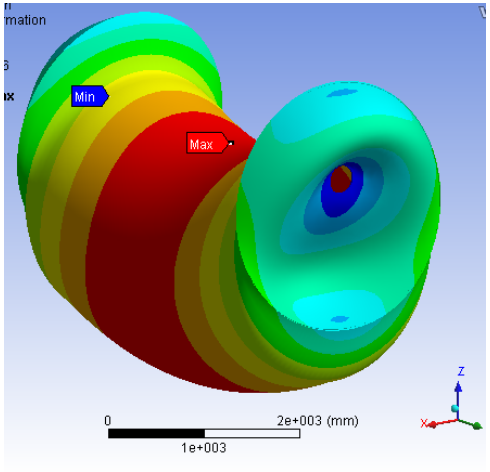
Tracking layers cooled by a gentle flow of nitrogen or air, hence no cooling pipes within tracking volume.

Timing layers need pulsed power, and possibly evaporative CO_2 cooling

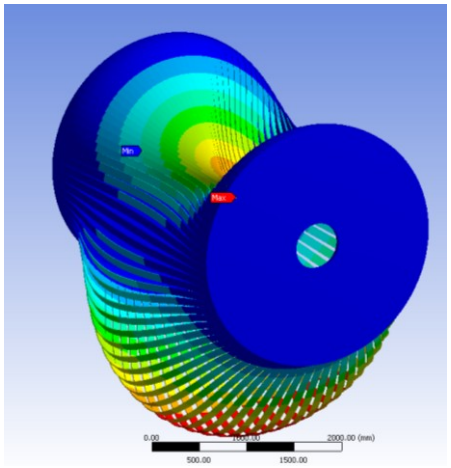
Mechanical structure

- SiC foam favoured wrt 'conventional' CFC sandwich, due to:
  - Homogeneous material, ultra-stable wrt temp fluctuations
  - Accurate match of expansion coefficient to Si, so bonding of large flexible thinned devices to substrate works well
- But what about the lower elastic modulus of SiC? A structure made of discrete ladders supported at ends would sag unacceptably under gravity
- Small foam links between ladders, both in the endcaps and in the barrels
- These spectacularly improve the shape stability, almost to the level of a continuous cylinder
- System is assembled layer by layer as pairs of closed half-barrels, sequentially onto the beampipe after the vertex detector
- After assembly, the vertex plus tracking system, mounted on the inner beampipe, is assembled into the overall detector, off the beamline, as part of the ILC push-pull approach for two detectors. Overall weight of this system is only ~200 kg

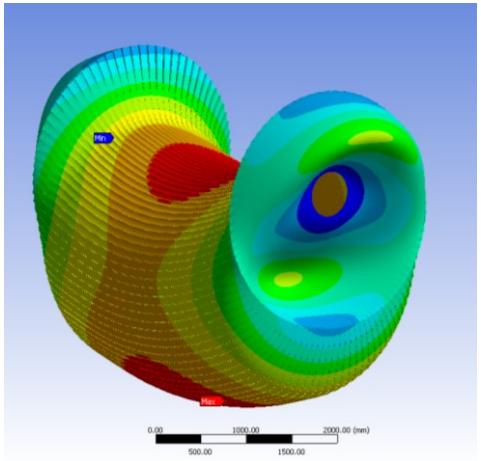
ANSYS simulation of Layer 5



- Continuous foam cylinder
- Max deflection 10 μm



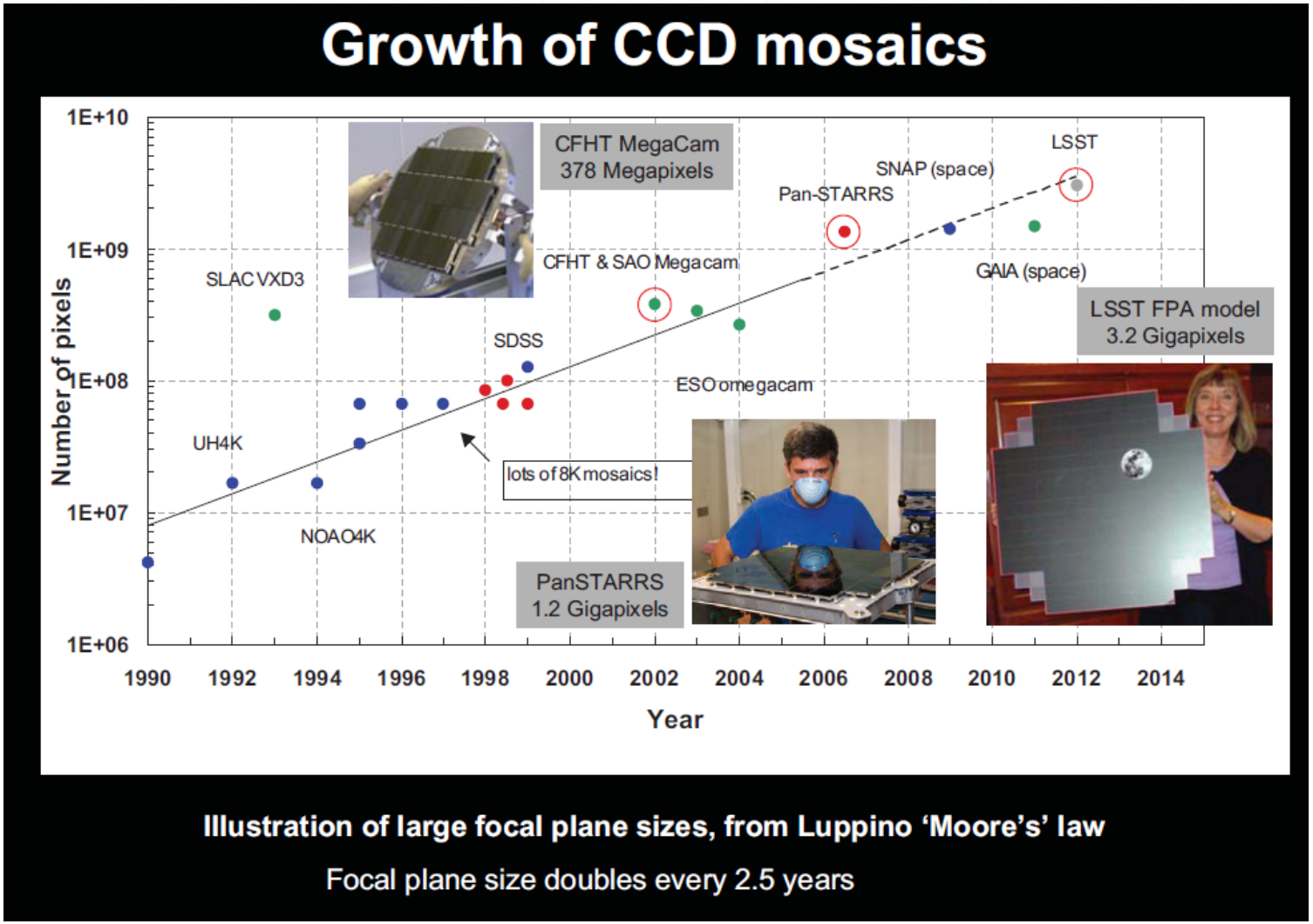
- Separate foam ladders
- Max deflection 20.5 mm



- Ladders joined by small foam piece every 40 cm
- Max deflection 20 μm

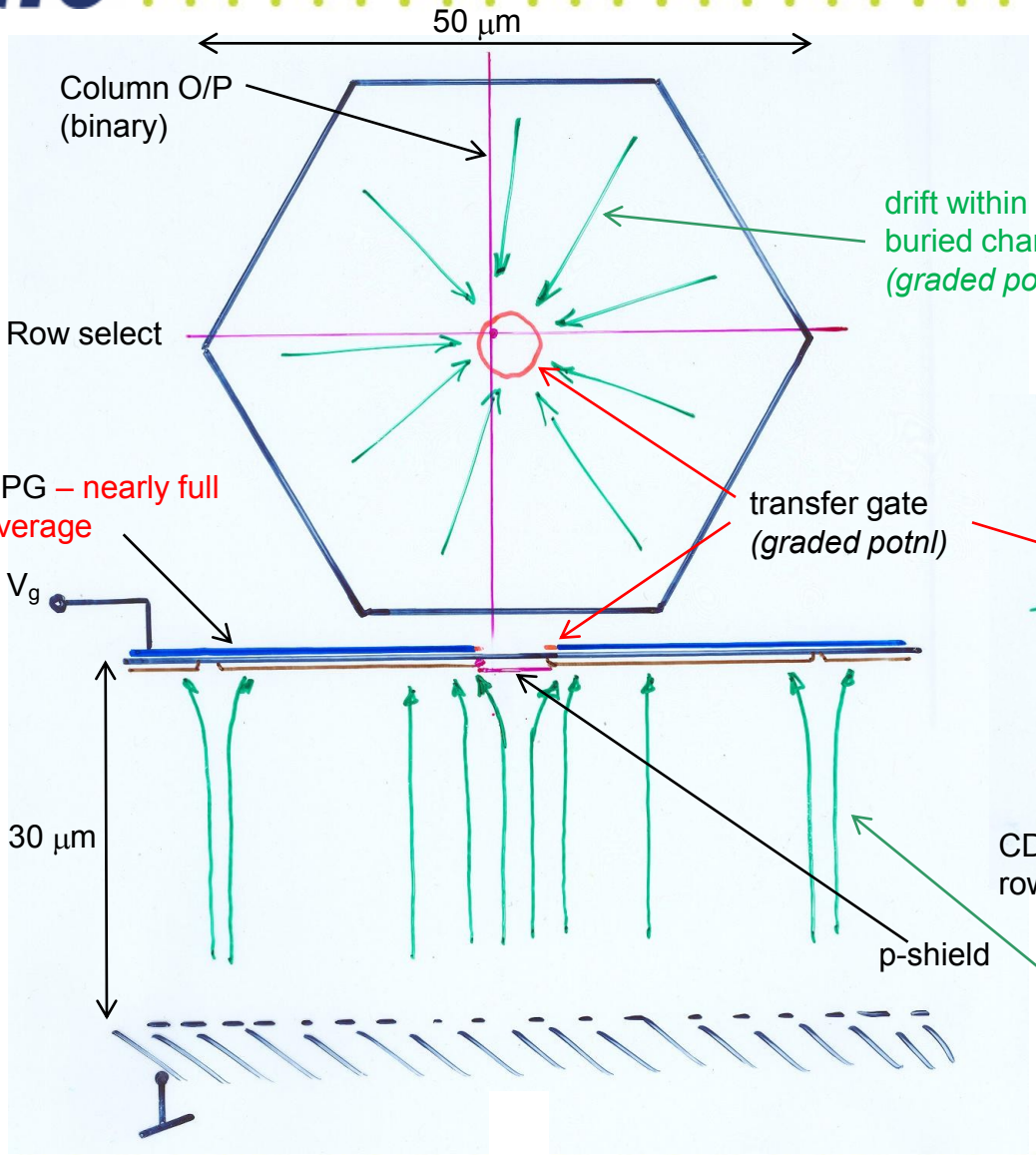
Steve Watson - *RAL*

System scale

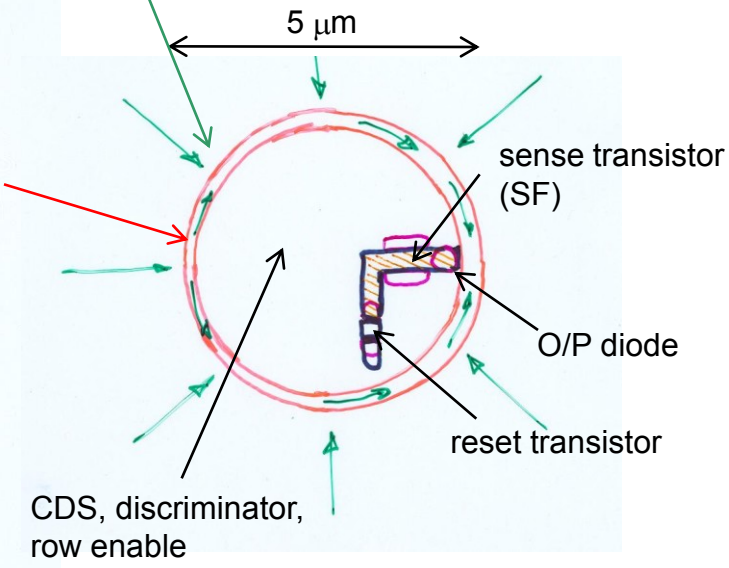


LSST R&D going well – final stages of prototyping. 40 Gpixels will be 'on the line' by 2020. Note also VXD3!

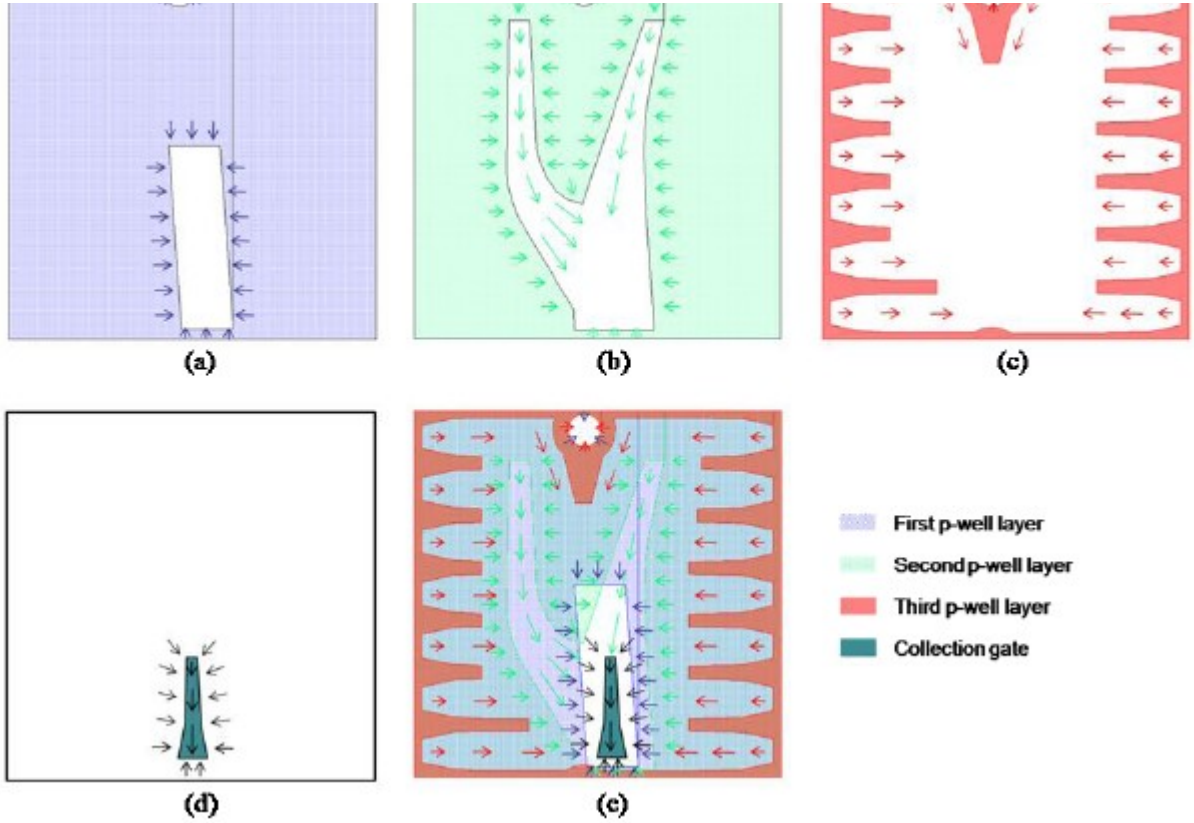
Tracking pixel – unit cell



Requires a *dual gate process,* eg
24 nm (10 V) over the PG, with
4 nm (1.8 V) inside the TG ring



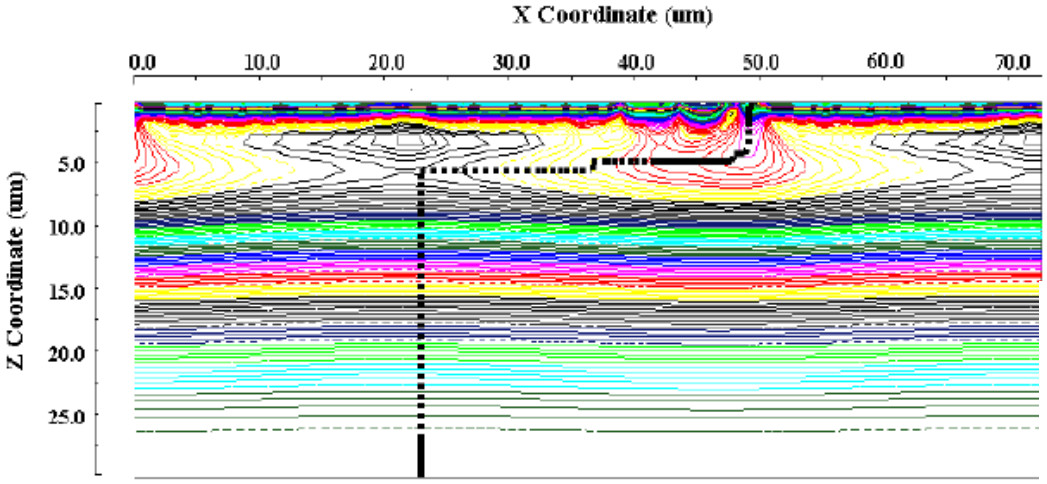
Patterned implants for fast charge collection



Relatively simple process – all implants can be made at the same energy

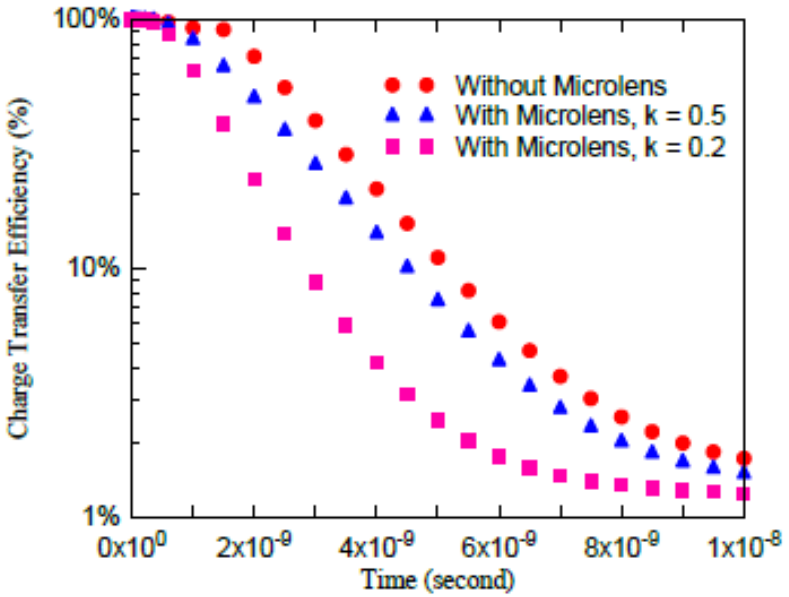
Goji Etoh, 2009.

Similar technology available from e2V for CMOS pixels with dual gate thickness



90% charge collection within ~5 ns from uniform illumination of back surface (simulation)

Goji Etoh, 2009



Timing layers

Regions where 'full' time stamping is needed – 300ns or 10 ns

Various technology options, since material budget is less critical (eg hybrid pixels). However, at a quick look, the separated function monolithic pixels might also be attractive:

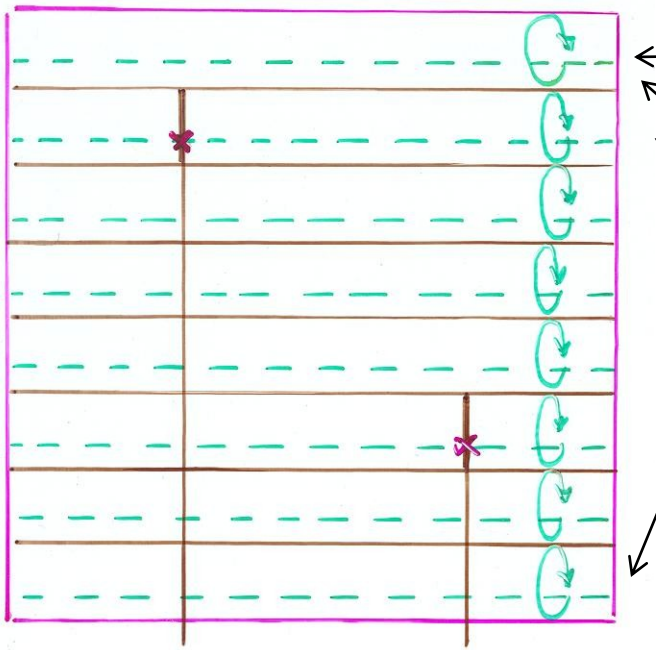
~150 μm diameter should suffice (not needed for precision momentum measurement)

- Fast charge collection from larger pixels needs device simulation
- Front-end comprises in-pixel sense transistor, CDS and discriminator, as for tracking layers
- But now, CDS spans bunch train (1 ms or 180 ns): Sample-1 before start of train, then open TG. Sample-2 senses the true time of charge collection in pixel
- Add time stamp – send fast column signal to periphery, pick up bunch crossing number and store in edge memory
- Also send to periphery (more leisurely column signal) row address and store that
- Between bunch trains, read addresses and time information of hit pixels
- Higher power dissipation of continuously active front-end increases power dissipation (from ~300 W to ~1.5 kW)

Possible SPT for LHC

- Same motivation – greatly reduced material budget. Discovery potential will remain speculative unless such a tracker is built
- Remarkably, expected hit rates at luminosity of HL-LHC (from ATLAS colleagues) still allow us to consider the architecture with time-integrating tracking layers, where integration time is determined by a low power rolling shutter
- Is radiation hardness of these charge-coupled CMOS pixels adequate? Looks OK on a quick check. It helps that they are already low-resistivity structures (typically below 300 Ω.cm), and we aren't suggesting to go below ~40 cm radius into the 'inferno' of LHC vertex detectors
- Timing layers with 25 ns resolution and 100% duty factor will need liquid or evaporative cooling, but that's OK close to the ECAL
- Track trigger if required could be based on mini-vectors from timing layers, possibly linked to vertex detector tracks
- Let's consider the architecture of the crucial tracking layers, which needs to be more adventurous than for the LC, in a little detail …

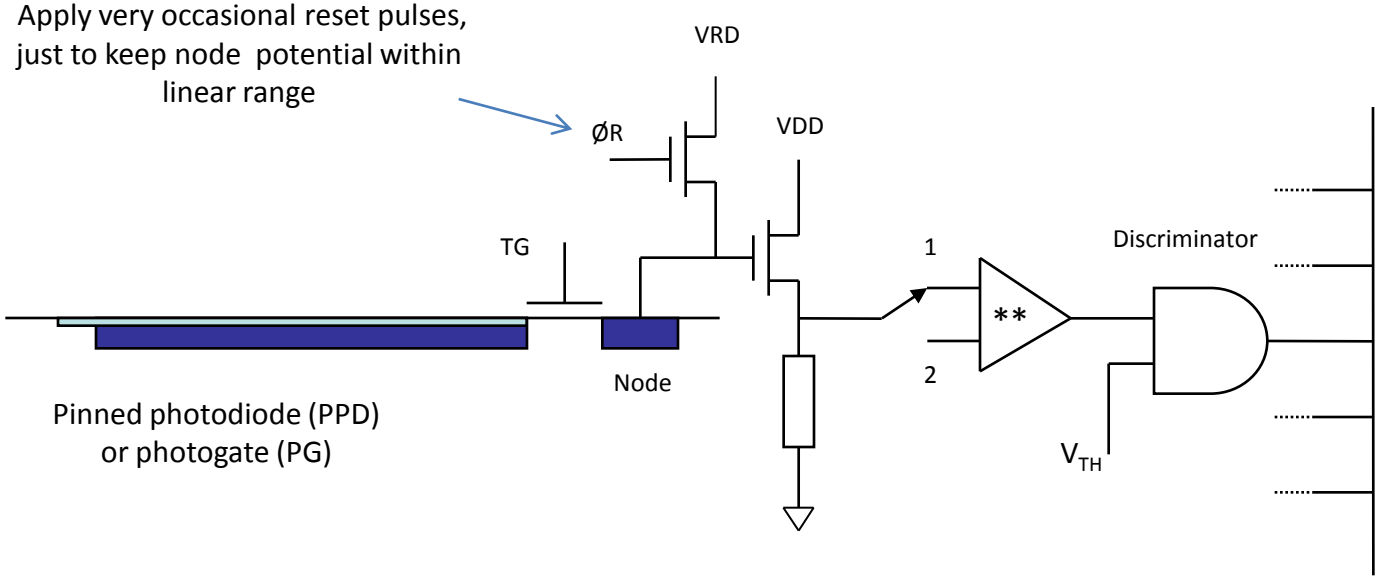
Segmented *rolling shutter* readout ‘comfortable’ example



1 μW per pixel (guesstimate)
1600x8 active pixels
12.8 mW per device, 0.20 mW/cm^2
Maybe double this, 0.40 mW/cm^2 due to edge logic etc
Overall power ~250 W, very comfortable for gas cooling

Suggested Pixel logic

Apply very occasional reset pulses, just to keep node potential within linear range



Pinned photodiode (PPD) or photogate (PG)

200 digital connections for segment M and row N

**

[V(1) - V(2) (held)] alternating with
[V(2) - V(1(held)]
provides CDS signal with time difference equal to rolling shutter period – certainly adequate noise protection

Thanks to David Burt for help with this

Row-enable switches on VDD, then allows adequate settling time to measure the next voltage sample. Tune S/H timing accurately wrt bunch crossing [Signal charge collection needs to be sufficiently prompt to avoid time-split signals between successive samples]

Backgrounds in SPT at LHC

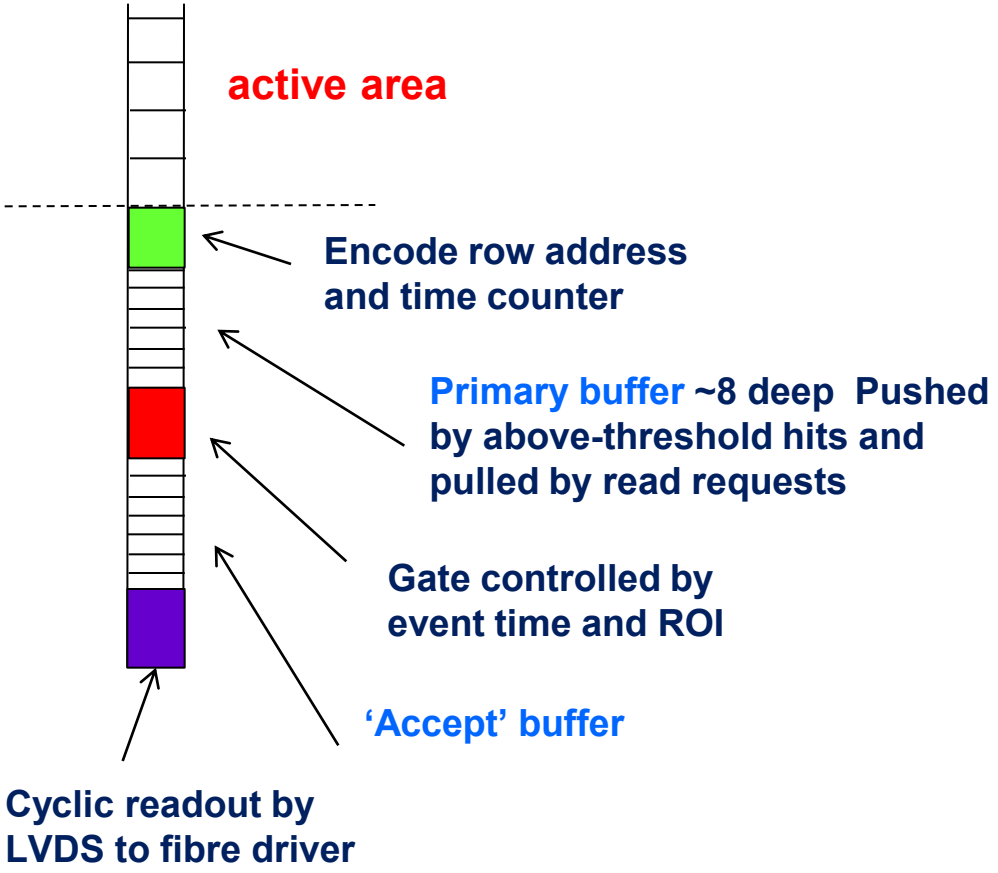
- Thanks to ATLAS colleagues (Nikos Konstantanidis, Gordon Crone, …) for estimated hit densities on tracker layers in HL-LHC, 14 TeV, 25 ns bunch interval, luminosity $5x10^{34}$ cm^{-2} s^{-1}, upgrade layout SLHC_19-13
- To establish feasibility of track-finding, evaluate the search area needed when interpolating between neighbouring layers. Here we benefit from the low mass of these layers, so broadening due to multiple scattering is minimal
- Criterion for a usable hit is freedom from any accidental hit in a 3σ search area. If an accidental hit is present, simply drop that layer from the track fit
- Consider minimum momentum of 10 GeV/c. For lower momenta, increased loss of inner-layer hits is probably acceptable, in terms of momentum precision
- Search region for 90 degrees polar angle is typically 3x3 = 9 pixels

- Case of uniform 10 μs rolling shutter applied to all modules:

Radius (mm)	Hit density clusters per BX/cm^2	Hit density per 10 μs/mm^2	Layer efficiency* %	Data size (Mb)**
380	0.241	0.964	97.8	16.6
501	0.146	0.584	98.7	13.2
622	0.096	0.384	99.1	10.8
743	0.063	0.252	99.4	8.5
1000	0.028	0.112	99.7	5.1

- * Note that background causes loss of *bona fide* hits, but no bias to the track fitting
- ** 54.2 Mb total. This should nearly all be dumped in the sensors. In event building, we would only read data that are in the appropriate time slice and in areas selected by ROIs defined by calorimetry and timing layer vectors. Sipping the appropriate data from the 'LHC firehose' with a 'drinking straw' will be a challenge. *Showstopper or not?*
- With these layer efficiencies, 99.9% of tracks with momentum > 10 GeV/c have 4 or 5 good hits on tracking layers

Consider readout of one column. For hottest region, expect ~4 hits per time slice:



- Assume one or two optical fibres per barrel, ~3 Gbit/s capacity
- Assume L1 trigger rate of 100 kHz
- With 3 bytes per hit, this permits readout of 2500 hits/layer/event
- On inner layer, this allows ~25 cm^2 per event
- Needs study of what is required for realistic ROI definition
- One could of course transfer more data. The fibre drivers would be located close to the ECAL, beyond the critical tracking volume. Also, where will this technology be in 2020?

Will the power requirements for the electronics push us beyond the limits for gas cooling (which may be ~1 kW)? This is probably the most serious threat to this concept at LHC

Synergies and next steps

- Charge-coupled CMOS pixels, developed years ago for high performance cameras, are coming onto the market for scientific imaging as 'scientific CMOS pixels'. Fairchild/Andor/PCO and Hamamatsu are both active
- Jim Janesick's pioneering work with Jazz Semiconductors, and his 'Sandbox' for multi-project wafers, could be very useful for our community
- Jazz were recently awarded a substantial US Government grant to develop advanced imaging devices based on these principles
- e2V are developing very similar devices (segmented rolling shutter) for adaptive optics (EELT in Chile) and for weather satellites (observation of lightning). Features are somewhat complementary to our needs: limited to 1 kfps but they need ~1 e- noise performance
- Next steps for SPT at LHC, if there is interest:
  - Undertake physics simulations and device design, to explore possible showstoppers
  - Power estimation and minimisation for tracker layers. Subthreshold operation of selected transistors. How does power scale with feature size? For 2020 timescale, we could consider moving well below 0.18 μm, and high gate currents might not cause problems
  - If simulations look favourable, consider evaluating existing devices from e2V or Janesick in a test beam, investigating min-I response, radiation hardness, etc
  - Even if these ideas are shot down by this expert audience, maybe others will improve on them. Wonderful as the present tracking systems are, we should not be satisfied with them (my opinion)

Conclusions

- The SPT offers the possibility of high performance tracking over the full polar angle range, with a major reduction in material in all directions, particularly the forward region
- For multi-jet physics (where there's nearly always some activity in the forward region) this looks particularly appealing
- In general, having nearly all the photons convert in the ECAL (or just before it, in timing layers), and good quality tracking of electrons, is desirable
- The needed pixel technology may be available, but there are numerous issues to be studied to establish its applicability to tracking systems
- We can profit from the major developments under way for other scientific applications, as well as night vision devices. Goji Etoh, Jim Janesick and others are keen to collaborate, and Jazz is supported by a recent US Government grant. An inter-disciplinary approach to this R&D looks promising
- By 2020, 40 Gpixel systems for science will exist. Attitudes in our community are more positive than when we started 30 years ago, with pixel-based vertex detectors …

SOME EXPERT OPINIONS IN 1980

"Put such a delicate detector in a beam and you will ruin it".

"Will work if you collect holes, not electrons".

"Far too slow to be useful in an experiment".

"It's already been tried; didn't work".

"It will work but only with ≤ 50% efficiency".

"To succeed, you will have to learn to custom-build your own CCDs: investment millions".

"At room temp it would be easy, but given the need to run cold, the cryogenic problems will be insurmountable".

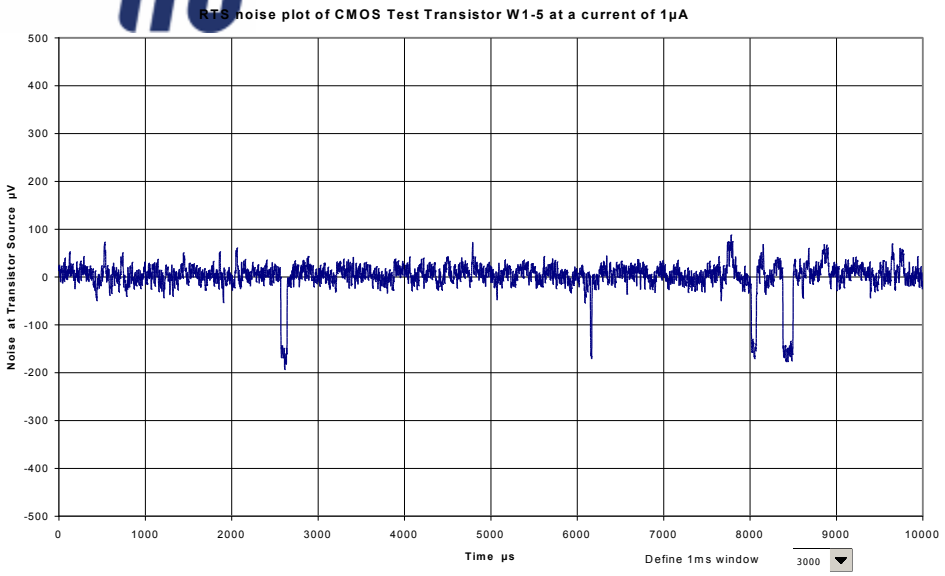
"May work in a lab, but the tiny signals will be lost in the noise (RF pickup etc) in an accelerator environment".

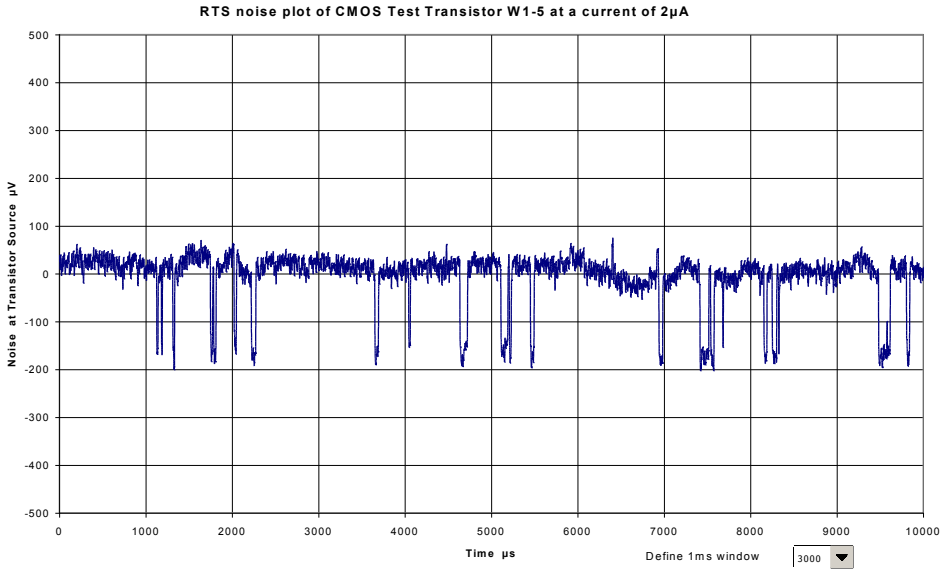
However, Wrangy Kandiah from AERE, Emilio Gatti and Franco Manfredi from Milano, Veljko Radeka from BNL, Joe Killiany from NRL, Herb Gursky from Harvard Smithsonian were supportive

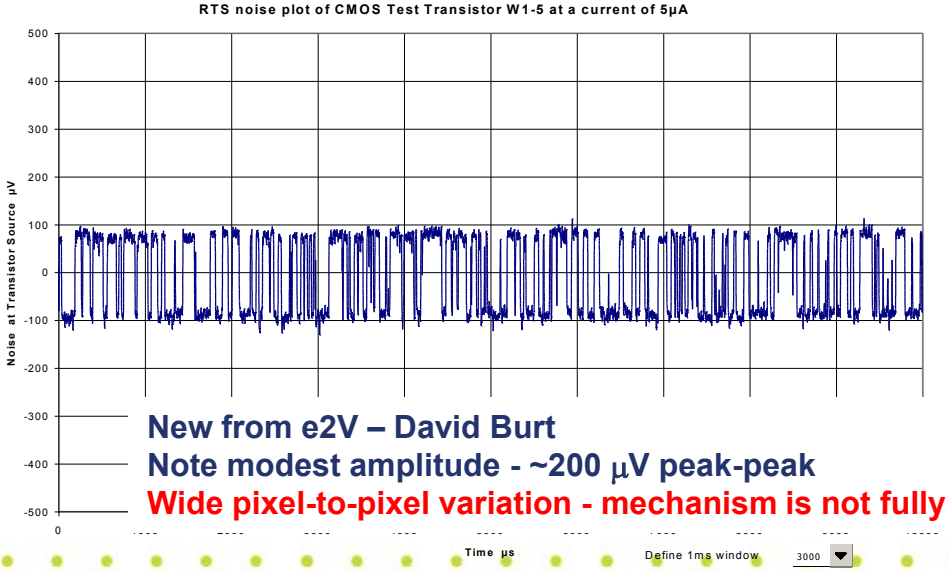
Particle physics funding committee in UK found it 'too speculative'; but Erwin Gabathuler, then director of EP Div in CERN, kindly came to our rescue

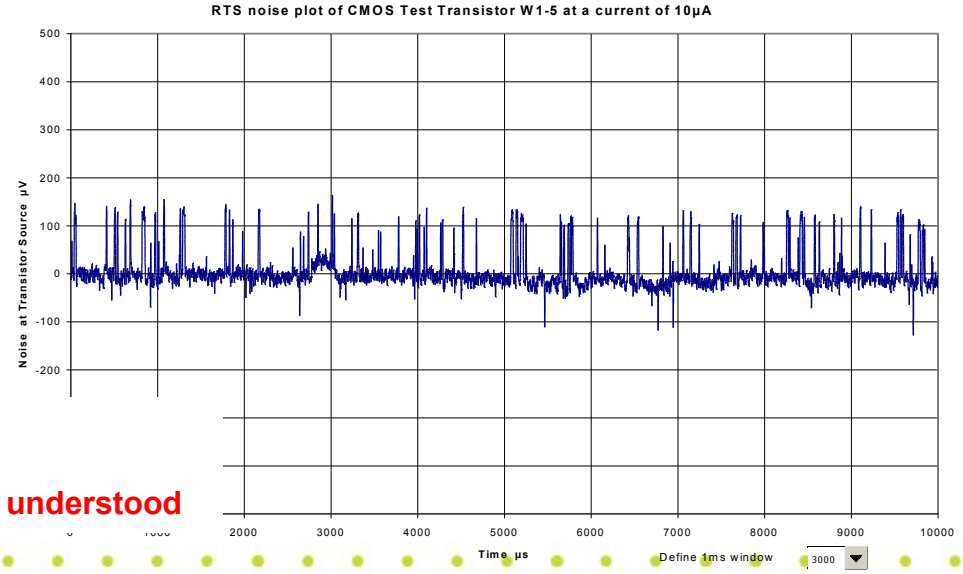
Backup

RT Noise









New from e2V – David Burt

Note modest amplitude - ~200 µV peak-peak

Wide pixel-to-pixel variation - mechanism is not fully understood

- **RT noise is the dominant residual noise source in charge-coupled CMOS pixels. May be triggered by the same mechanism as 1/f noise (tunnelling of charge carriers to *bulk traps* in the oxide) but there's more to it. Maybe the filled trap is critically located near an imperfect source or drain contact, or it may trigger a flow of dark current from a region adjacent to the conducting channel. Some suggestive evidence from studies of RT noise in memory devices (D Burt)**

- **1/f noise (and possibly RT noise) can in principle be reduced by using a buried-channel MOSFET for the source follower. However, producing such devices in the DSM process is a matter of ongoing R&D (e2V and Tower working together). We have seen similar problems with BC transistors from Jazz, but Janesick has been successful, so it isn't fundamental.**

- **RT noise can be effectively suppressed by the in-pixel CDS logic already envisaged to eliminate reset noise**

Cost estimate

- For a tracking system starting construction ~2020, estimates are pretty speculative
- Assume the 'SLD Vertex' approach, as opposed to the typical astronomy approach of fully tested Grade A devices
- This means a simple DC-pass acceptance test by vendor, with full testing by customer (yield was >95% for 8.0x1.6 cm^2 SLD devices)
- Based on *current* Jazz processing costs, we estimate ~$1k per 8x8 cm^2 thinned device
- 12,700 devices (tracking) plus 17,900 devices (timing) → $30M total, but device costs will fall with expanding markets
- Add ~10% for mechanics and off-device electronics
- Somewhat more expensive than SiD tracker, but it remains a small fraction of the overall detector cost, and after taking into account the LC running costs, it could be a clear winner

Recent results from Jim Janesick, reported at workshop on imaging systems for astronomy, San Diego, June 2010. Figure from Janesick SPIE 7742-11 (2010)

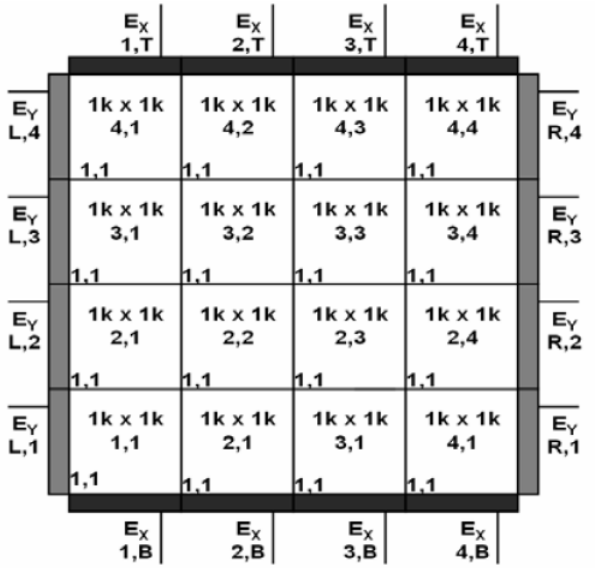


Figure 15. Block diagram of a stitched 4k x 4k imager.

4 x 4 cm^2 devices in Sandbox 6 (SB 6). Yields are 'high'.

10 x 10 cm^2 devices being processed this year in SB 7

World's largest CMOS imaging sensor, by Canon Inc, 20.2x20.5 cm^2 (thanks to Norm Graf for the link)