FE-I4 pixel readout chip and IBL module

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On behalf of ATLAS FE-I4 / IBL collaboration

Vertex 2011 Workshop, Rust - Austria, June 19th - 24th 2011

SI LAB
Silizium Labor Bonn

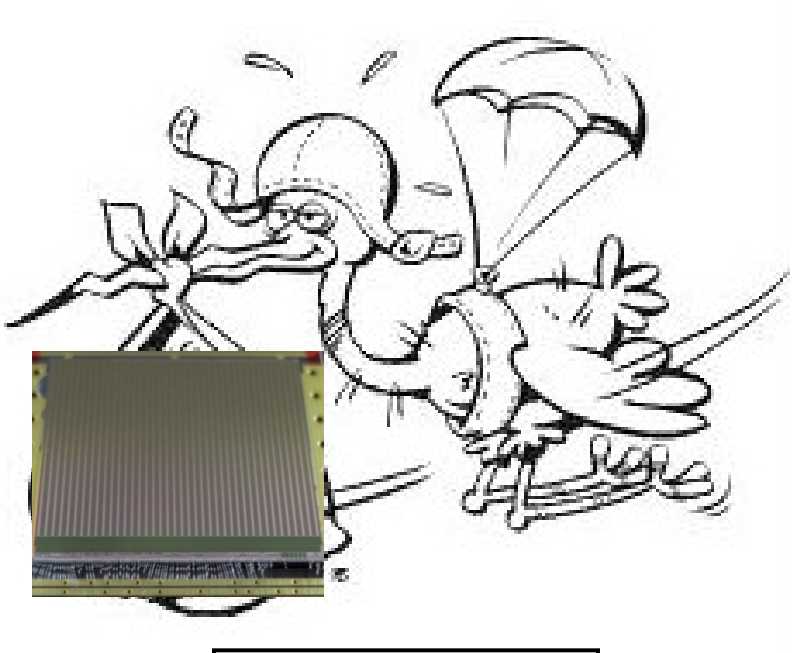
ATLAS Pixel Detector Collaboration

Plan

- FE-I4: A new Front-End generation for the upgraded ATLAS pixel detector.

- IBL module concept.
  - Sensor technologies for IBL.
  - Flex.
  - Thin FE.

- Conclusion.

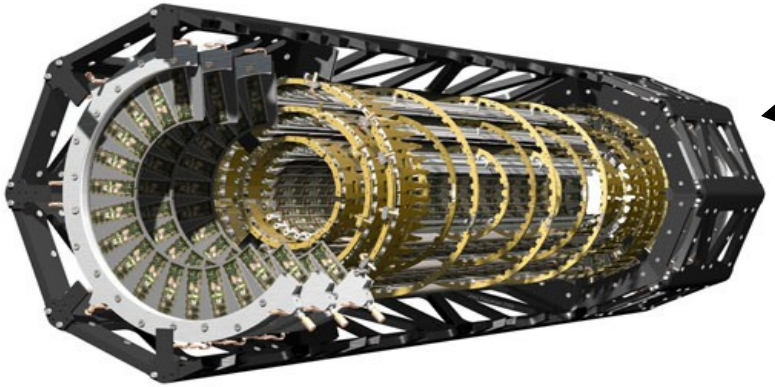


Birth of FE-I4A

FE-I4 what for?

Di Girolamo, Monday

Present beam pipe & B-Layer



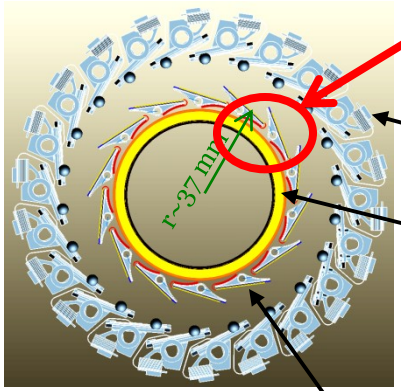
ATLAS Pixel Detector

FE-I3

3 barrel layers / 3 end-caps
end-cap: z± 49.5 / 58 / 65 cm
barrel: r~ 5.0 / 8.8 / 12.2 cm

- Fast IBL ('13): inserted layer in current detector.

FE-I4



Existing B-layer

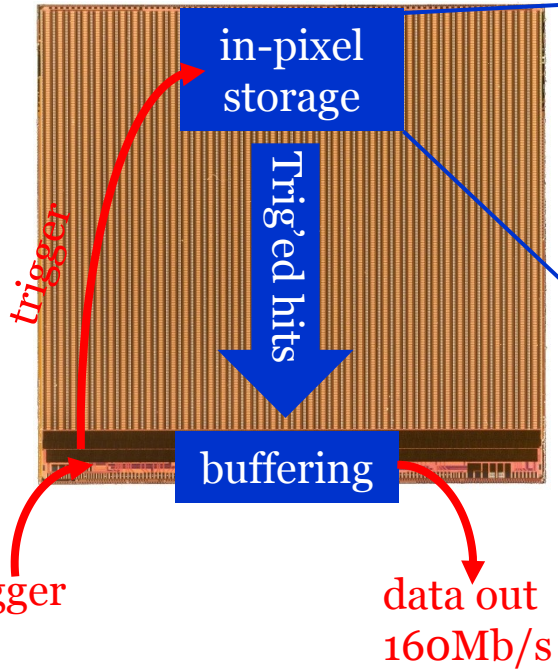
New beam pipe

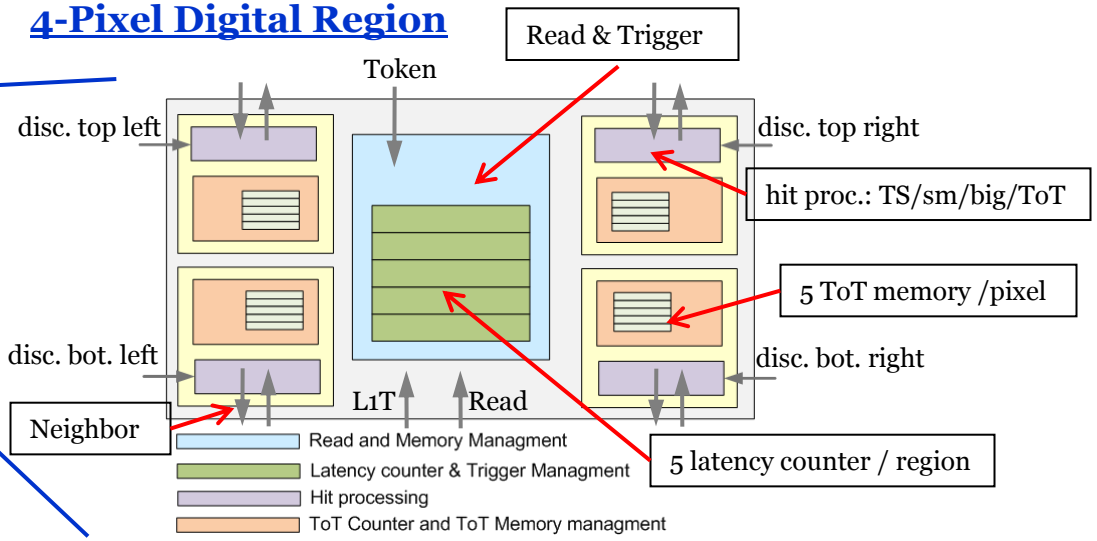
IBL mounted on beam pipe

- Phase1 tentative layout (>'17): 4-5 pixel layers, small radii / large(r) radii (note: Discussion on boundary pixel / short strips, ...).
  - All Silicon.
  - Long Strips/ Short Strips / Pixels.
  - Pixels:
    - 2 or 3 fixed layers at 'large' radii (large area at 16 / 20 / 25 cms?)
    - 2 removable layers at 'small' radii

High hit rate

- FE-I3: All hits go to periphery (column drain architecture).
- FE-I4: local "in-pixel" storage + trigger propagated up the array.



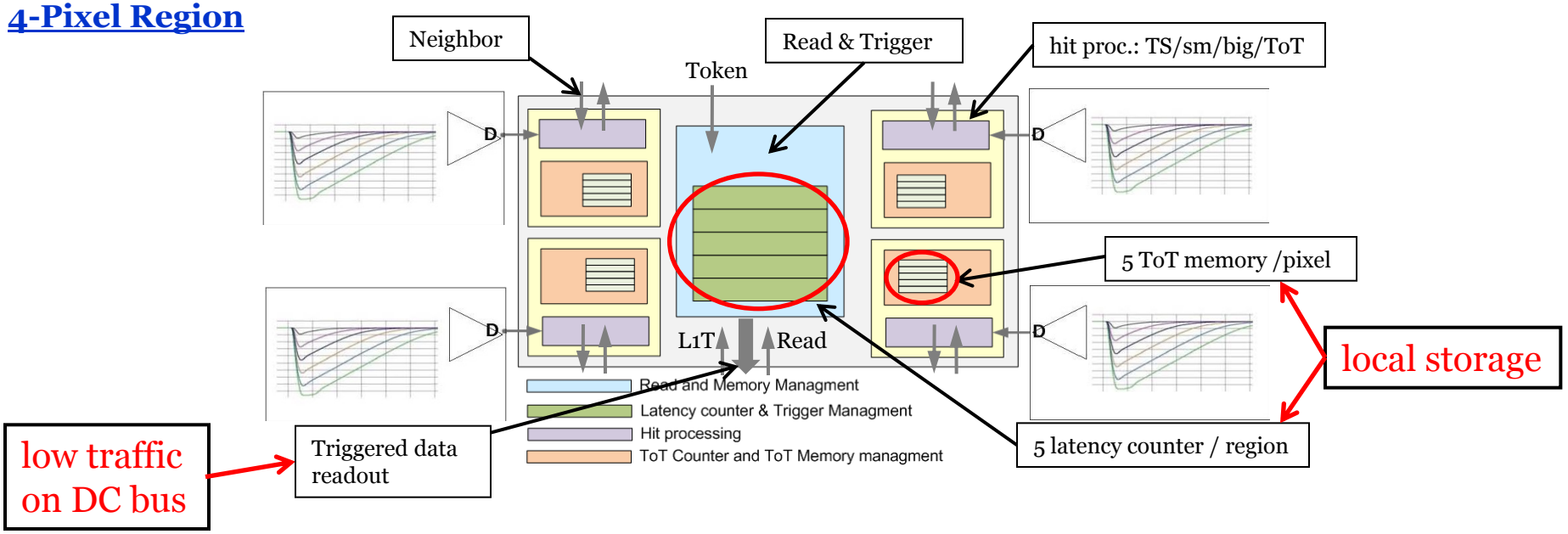


At 3×LHC full lumi, ineff: ~0.6%

4-PDR other advantages: better active fraction (memory in array), low power (un-triggered hits do not move), spatial association.

Digital Pixel: Regional Architecture

4-Pixel Region



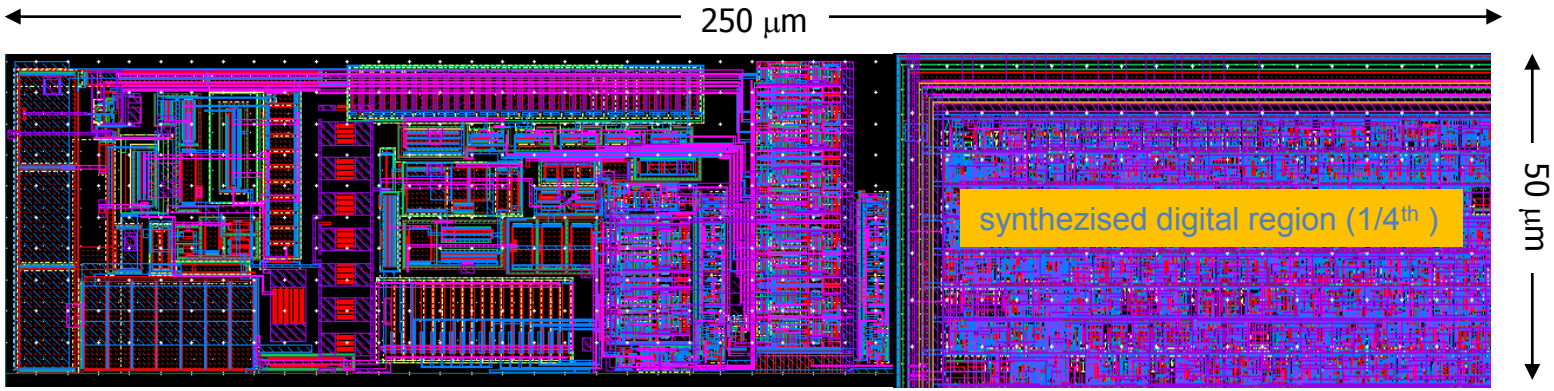
- Store hits locally in region until L1T.
- Only 0.25% of pixel hits are shipped to EoC → DC bus traffic "low".
- Each pixel is tied to its neighbors -time info- (clustered nature of real hits). Small hits are close to large hits! To record small hits, use position instead of time. Handle on TW.

Consequences:

- Spatial association of digital hit to recover lower analog performance.
- Lowers digital power consumption (below 10 µW / pixel at IBL occupancy).
- Physics simulation → Efficient architecture.

Process & granularity

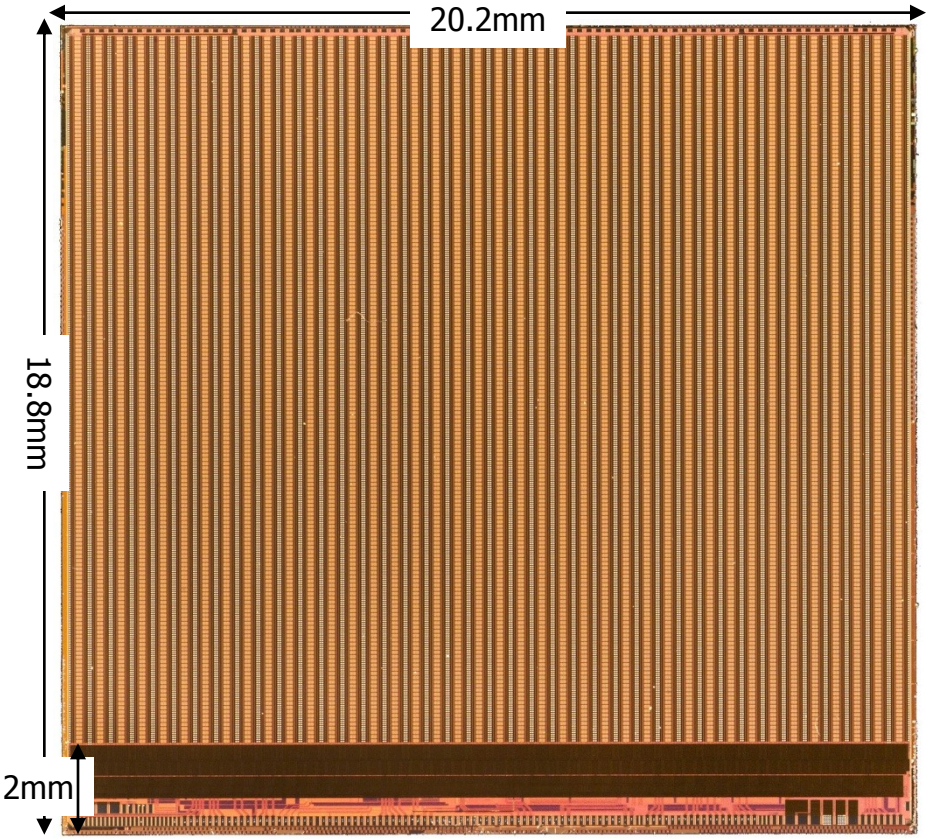
- FE-I3: 0.25µm process, 50×400µm².
- FE-I4: 130nm process, 50×250µm².



- Radiation hardness with minimal effort & substrate isolation (T3 well) → Can use standard synthesized cells!
- Tolerant to 250MRad.
- 8-metal layers, good power distribution → Can make big IC.

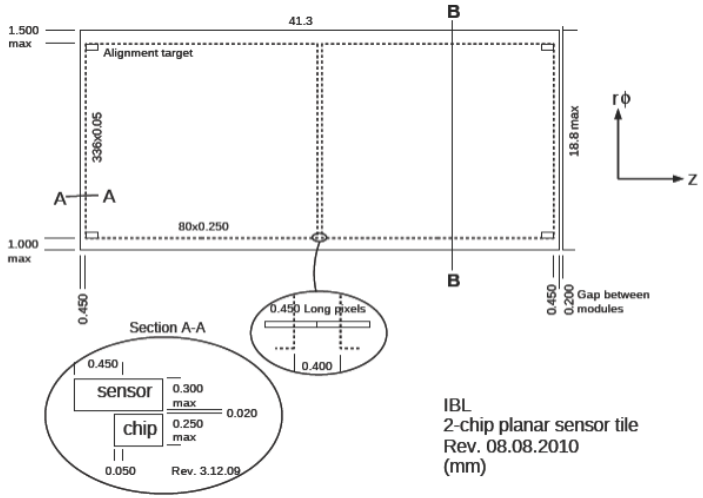
Size of the IC & module concept

- FE-I3: 0.76×1.08cm².
- FE-I4: 2.02×1.88cm².



Active area: ~90%

26,880 pixels (80×336)

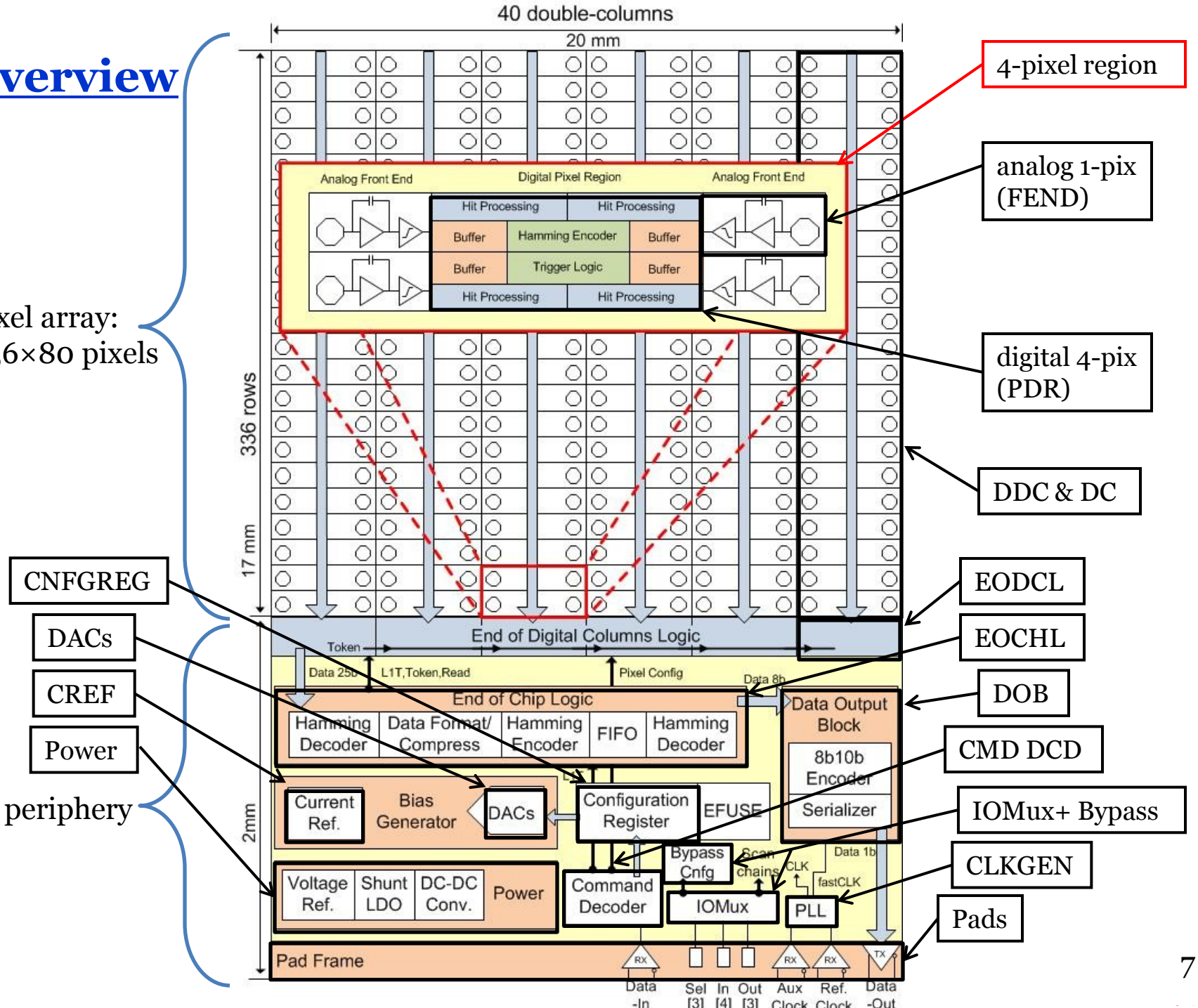


2 ICs: Shared clk and cmd inputs.

But each IC has dedicated output.

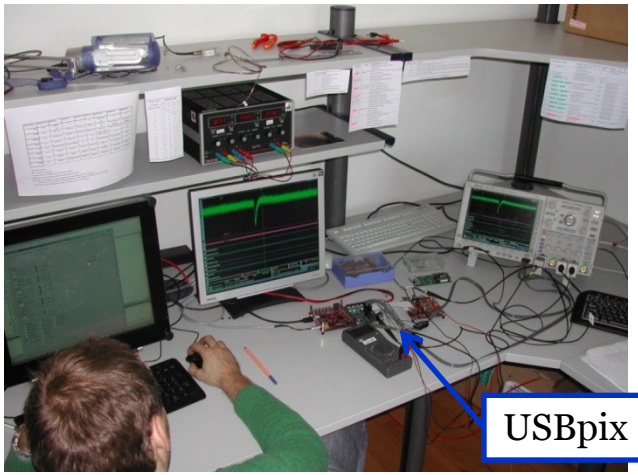
→ Simpler module concept!

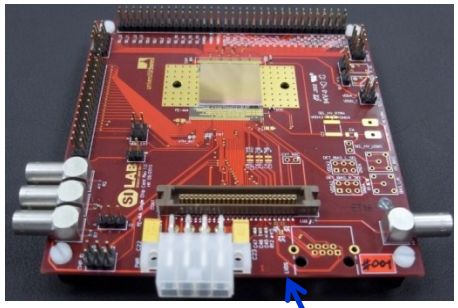
- **Overview**

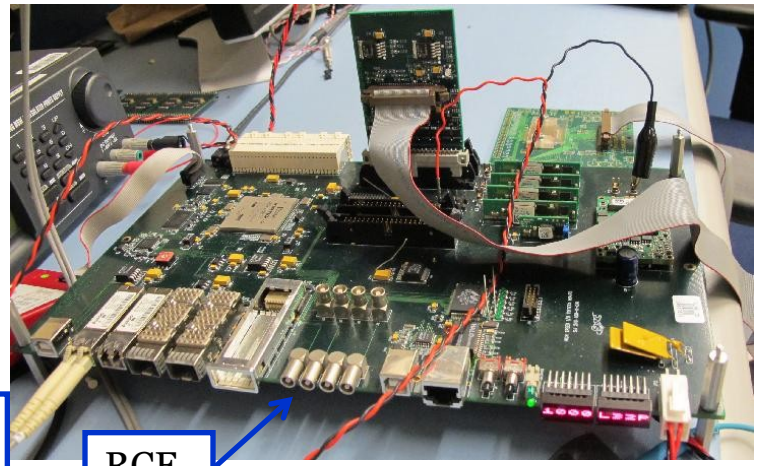

40 double-columns
20 mm
4-pixel region
analog 1-pix (FEND)
digital 4-pix (PDR)
DDC & DC
pixel array: 336×80 pixels
336 rows
17 mm
Analog Front End
Digital Pixel Region
Analog Front End
Hit Processing
Hit Processing
Buffer
Hamming Encoder
Buffer
Buffer
Trigger Logic
Buffer
Hit Processing
Hit Processing
CNFGREG
DACs
CREF
Power
periphery
EODCL
EOCHL
DOB
CMD DCD
IOMux+ Bypass
CLKGEN
Pads
End of Digital Columns Logic
Token
Data 25b
L1T,Token,Read
Pixel Config
Data 8b
End of Chip Logic
Hamming Decoder
Data Format/ Compress
Hamming Encoder
FIFO
Hamming Decoder
Data Output Block
8b10b Encoder
Serializer
2mm
Current Ref.
Bias Generator
DACs
Configuration Register
EFUSE
Bypass Cnfg
Scan chains
CLK
Data 1b
fastCLK
Voltage Ref.
Shunt LDO
DC-DC Conv.
Power
Command Decoder
IOMux
PLL
Pad Frame
RX
RX
RX
TX
Data -In
Sel [3]
In [4]
Out [3]
Aux Clock
Ref. Clock
Data -Out

FE-I4A testing

- Upstream efficient test setup development (FE-I4 emulators) led to test main features of this complex chip in few months.





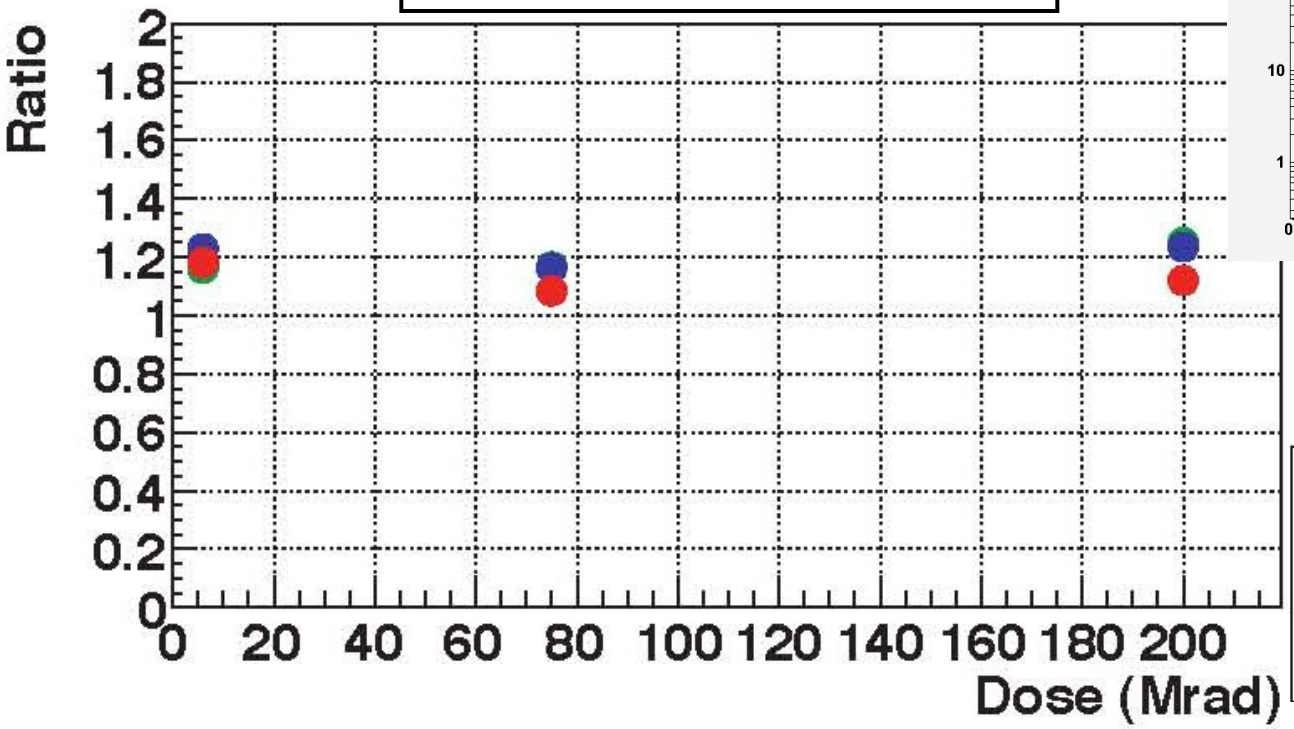


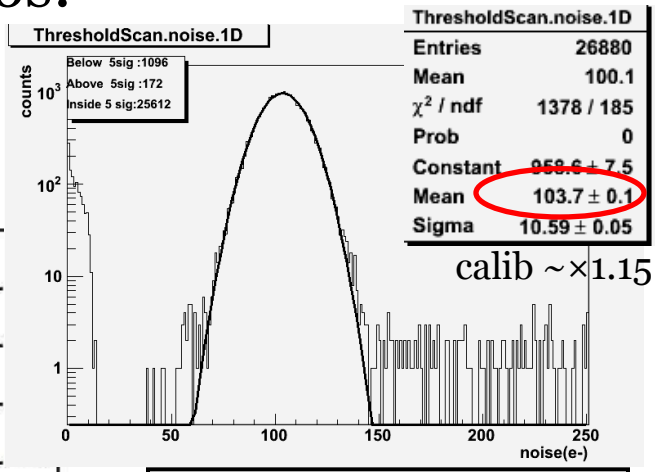
- All digital functionalities OK.
  - 4-pixel digital region.
  - Formatting + Data Transfer (EOCHL + DOB).
  - Communication + memories.
- PLL for 160Mb/s data transfer. Yield ~65-70%
- Powering (Shunt-LDO) working ~specs. (Tuning for IBL on-going)

Dose and noise

- Typical noise bare IC after calibration ~ 110e$^-$.
- 800MeV proton irradiation at Los Alamos:
  - 6 / 75 / 200 MRad.

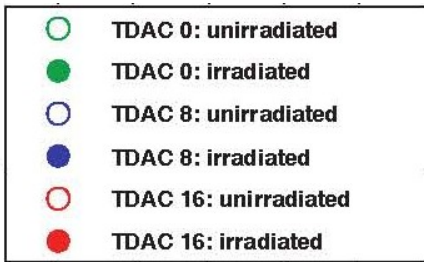
Ratio noise after / before dose





calib ~×1.15

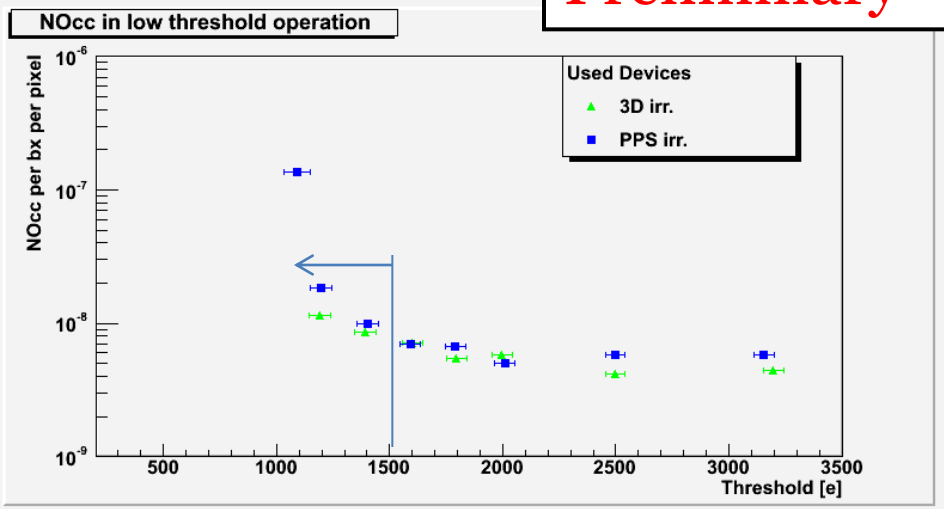
e.g. noise histogram



Low threshold behavior

Preliminary

- Studies on PPS and 3D assemblies irradiated with protons to **5.10^{15} n_{eq}/cm^2**.
- Noise occupancy increase when below ~1500e^-.
- At 1100 e^-, NOcc~10^{-7}. Threshold down to 1100 electrons possible!
- Low threshold operation w. irradiated sensors demonstrated!
- Note: Masked pixel floor = digitally un-responsive pixels.



Malte Backhaus

IBL Sensor Specifications

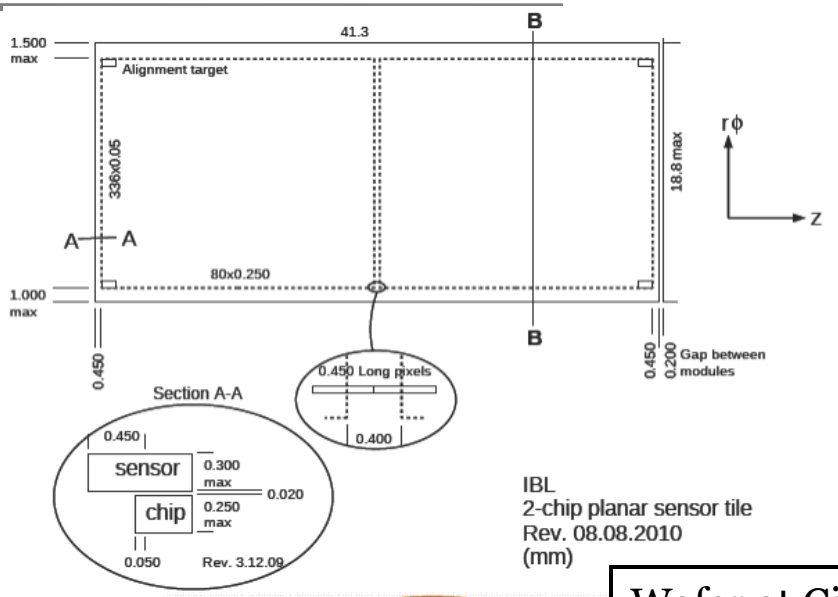
- IBL environment: Radiation hard FE and sensor.
- For now, two different pixel sensor technology candidates: n-in-n planar / partial-3D silicon.
- Specifications:
  - HV: max 1000V.
  - Thickness: 225±25µm.
  - Max. power dissipation: 200mW/cm² at -15°C.
  - No shingling in z → Edge width: below 450µm.
  - Tracking efficiency: above 98%.

- Choice for technology: Install Summer 2013 → Sensor Prod. completed Summer 2012 → Sensor choice in July 2011.

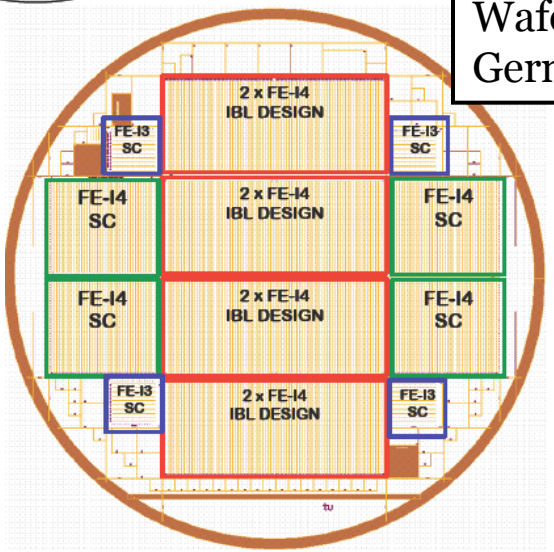
Detailed schedule / Procurement: Pernegger Tuesday

2-Chip Planar Sensor Tile

- Some R&D areas:
  - Slim edge sensors.
  - Radiation damage.
  - Low threshold FE-operation.
  - Low cost, large scale prod.
- Main advantage:
  - All benefits of a mature technology (yield, cost, experience).
- Main challenges:
  - Low Q collection after irrad, HV needed.
  - Inactive area at sensor edge.



Wafer at CiS, Germany

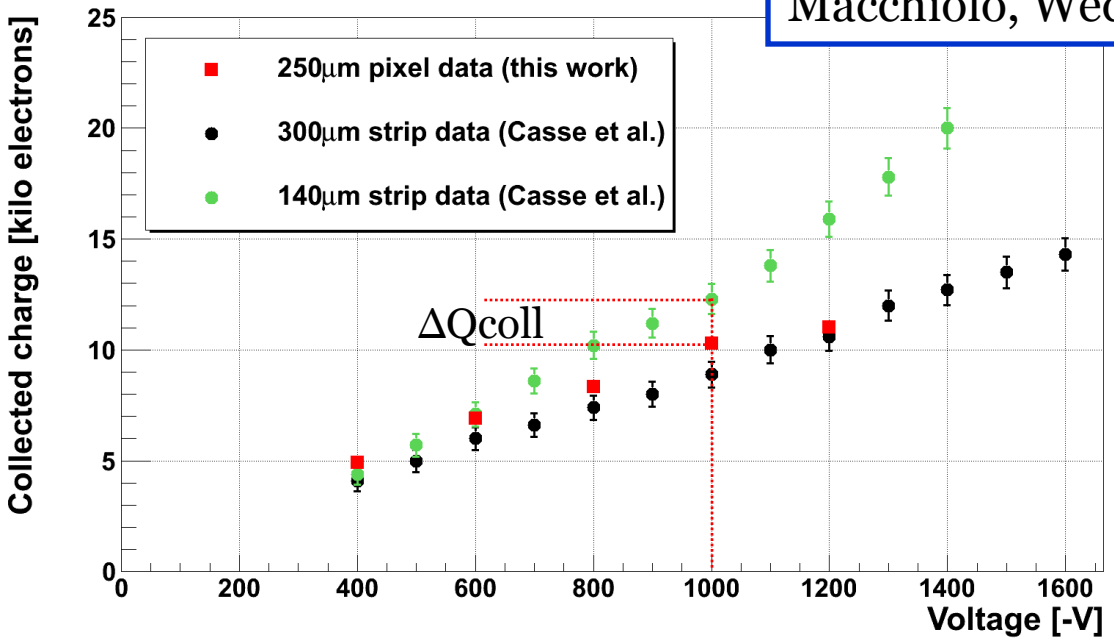


IBL design choice for planar

- n-in-n 200 µm thick slim edge with ~200µm inactive edge.
- Thinner sensors generate more charge after 5.10^{15} n_{eq}/cm^2 than thicker ones at same HV (higher field).
- Low material

good for tracking

Macchiolo, Wednesday

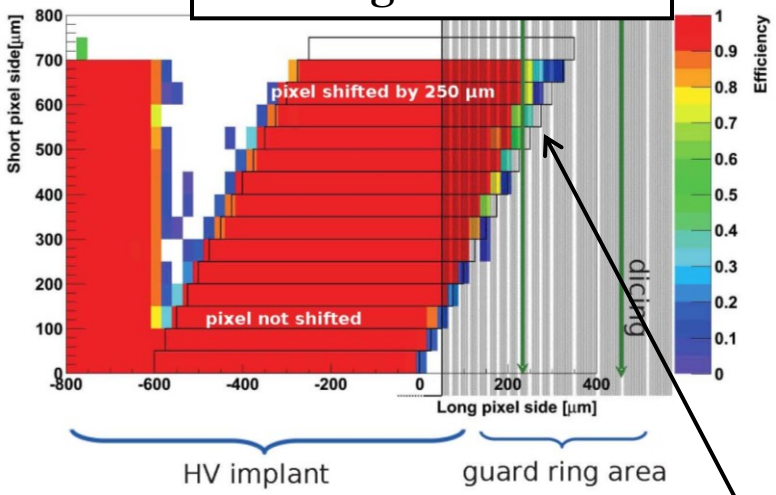


- + Constraints from safe processing at sensor provider + handling by flip-chipping provider → 200µm thick sensor.

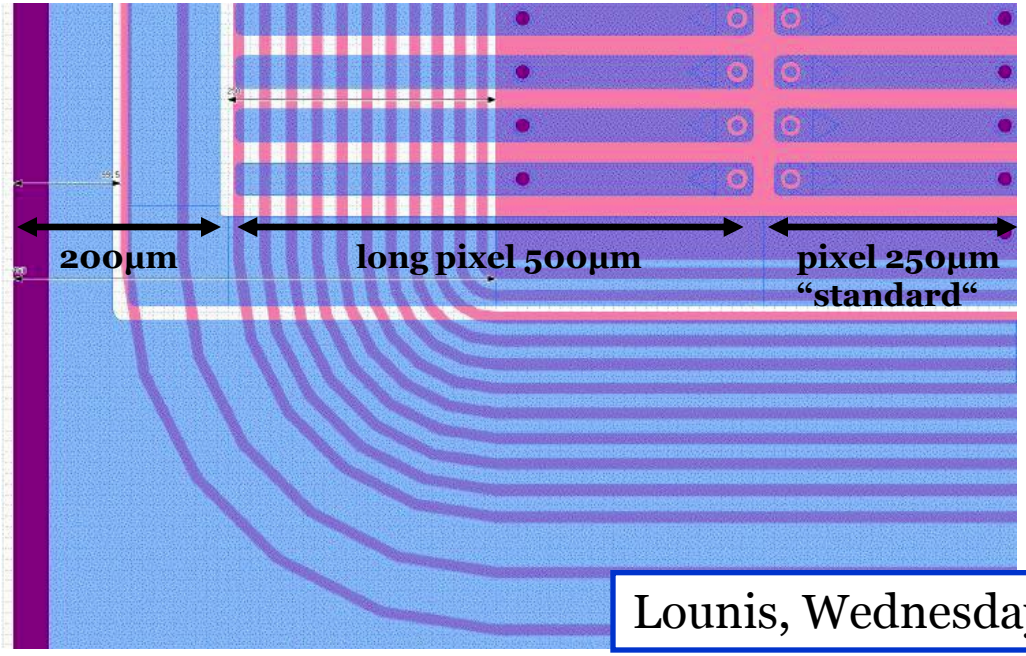
IBL design choice for planar

- n-in-n 200 µm thick slim edge with ~200µm inactive edge.
- As guard ring opposite side from pixel implant, shift guard rings under active pixel region. Lose homogeneity at edge, but after irradiation Qcollection mainly from under pixel implant.

Slim edge studies



from dedicated test structure

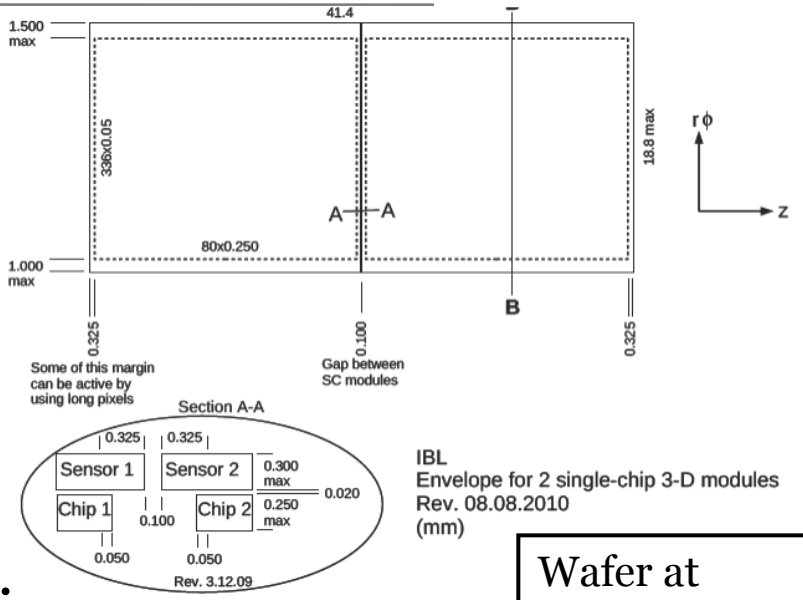


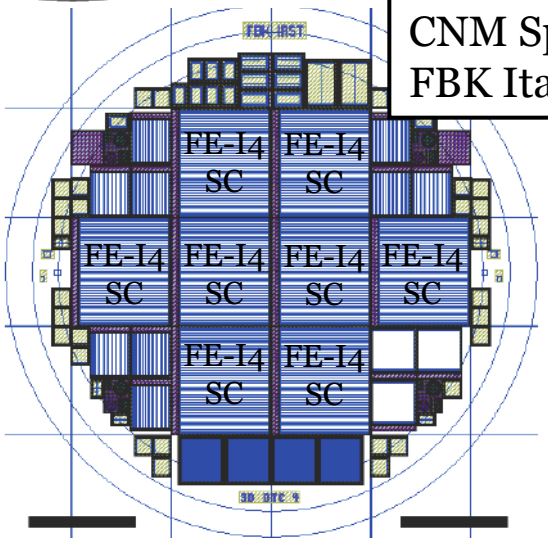
Lounis, Wednesday

Test beam: >99% efficiency (pre-irrad) for 250µm inefficient edge

1-Chip 3D Sensor Tile

- Some R&D areas:
  - Processing of TSV.
  - Yield.
  - Signal vs # electrodes / cell.
- Main advantage:
  - Radiation hardness.
  - Low depletion voltage (max 180V).
  - Active edge.
- Main challenges:
  - Production yield.
  - In-column inefficiency at normal incidence.

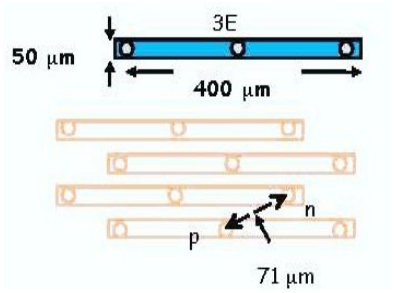


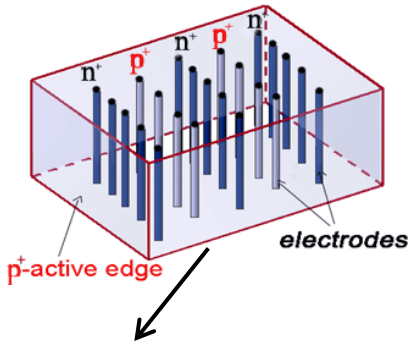


Wafer at CNM Spain / FBK Italy

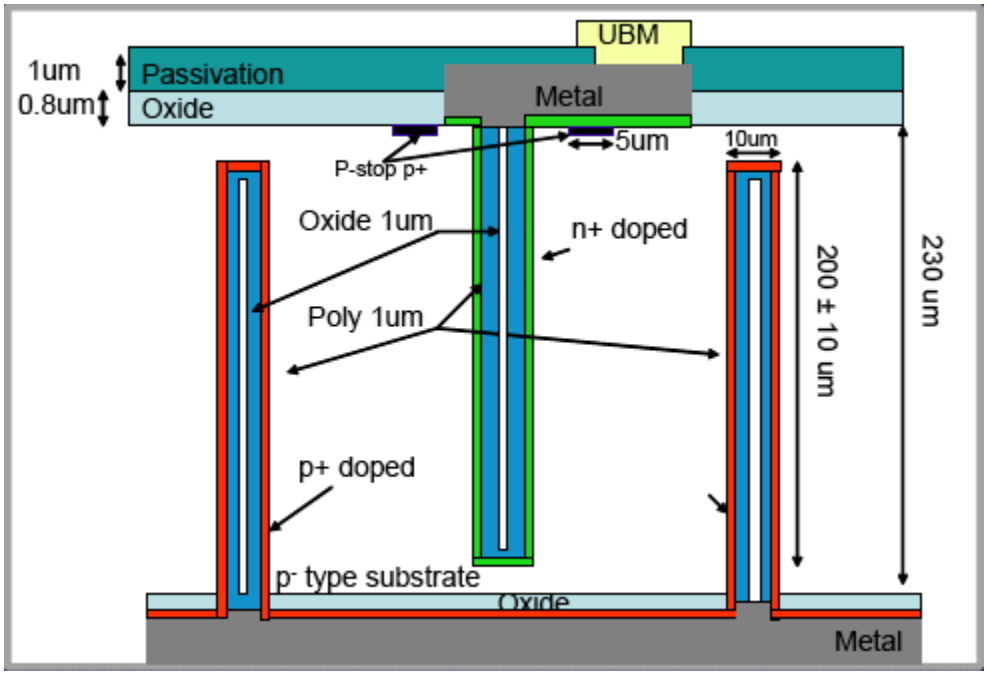
IBL design choice for 3D

- Double-Sided full passing 3D, 2E250 electrode configuration, slim edges:





- 2E250: Inter-electrode pitch ~70μm. Compromise between CCE and capacitive noise.
- Active edges & full 3D processing not established enough on project time scale.

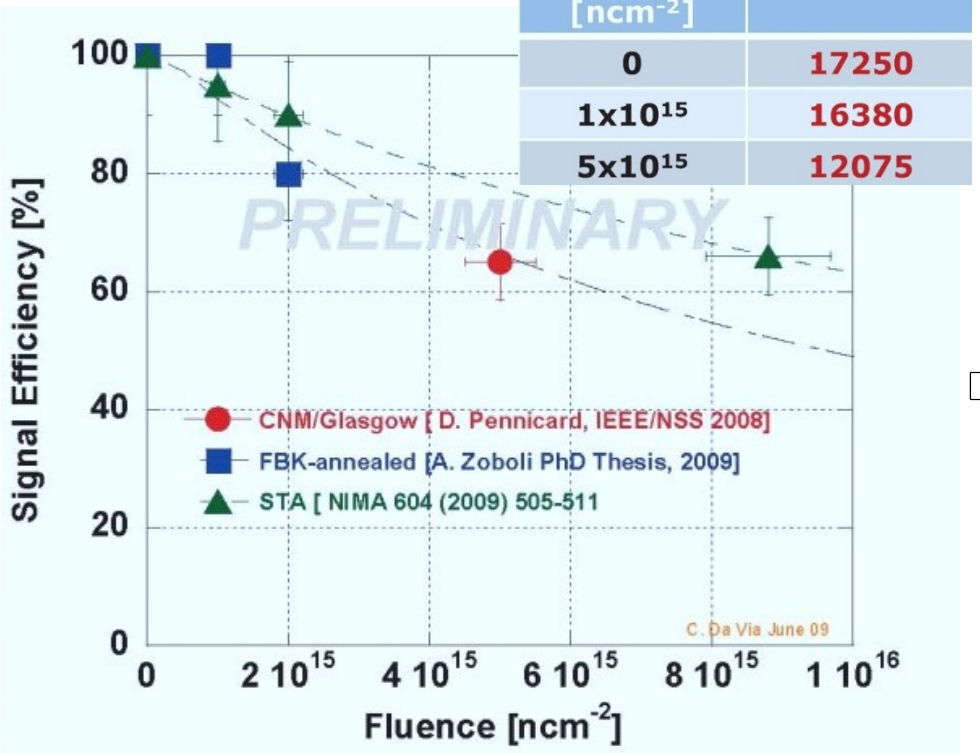


Giacomini, Wednesday

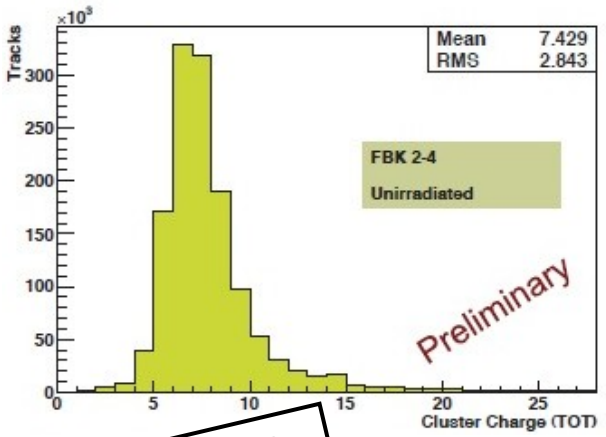
3D charge collection

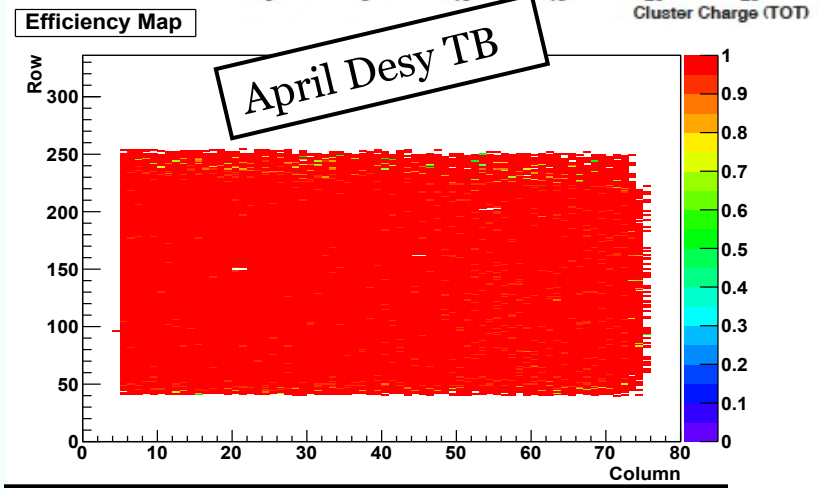
- High charge collection even at 5.10^{15} n_{eq}/cm^2.

Fluence [ncm^{-2}]	MPS [e$^-$]
0	17250
1x10^{15}	16380
5x10^{15}	12075



MPS=230μm x 75e$^-$ = 17 250



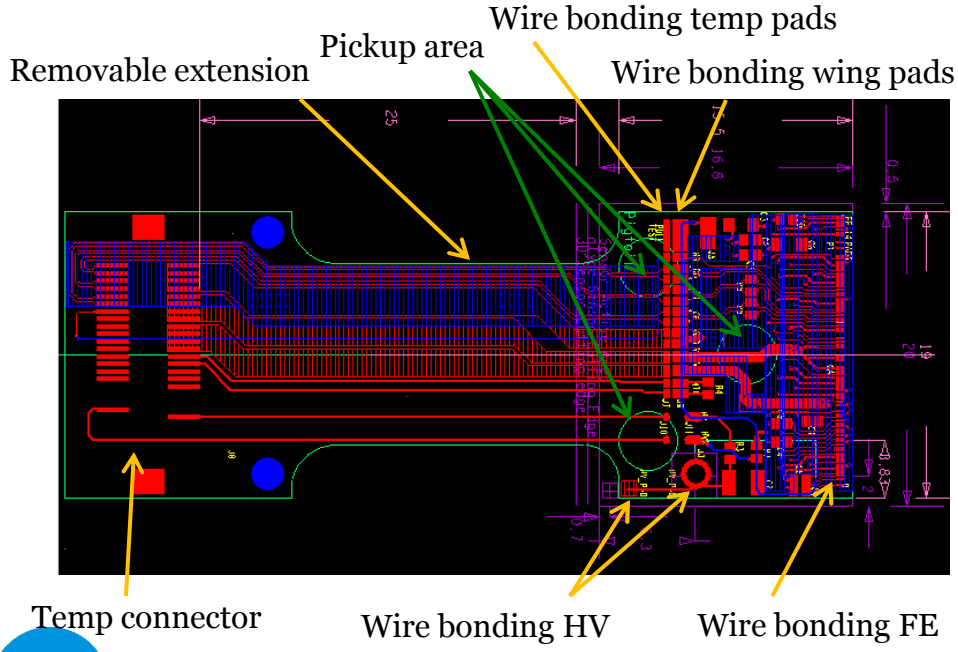


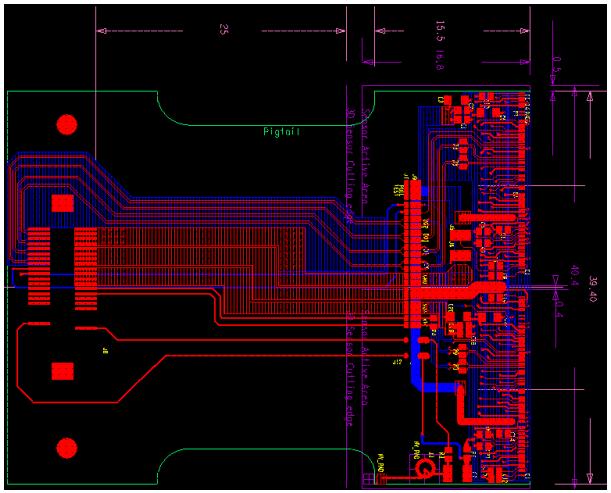
Bates, Thursday

FBK un-irrad. 98% eff for normal incidence → ~100% for tilted tracks

Flex development

- Flex routes signals and supplies from FE/sensor to internal services(sensor: HV ; IC: LV, DCI, CLK, Dout, HitOr).
- Make loading on stave easy (alignment marks, area for pick-up), and testing of module too.
- 2 versions currently developed: Single-Chip or Double-Chip.

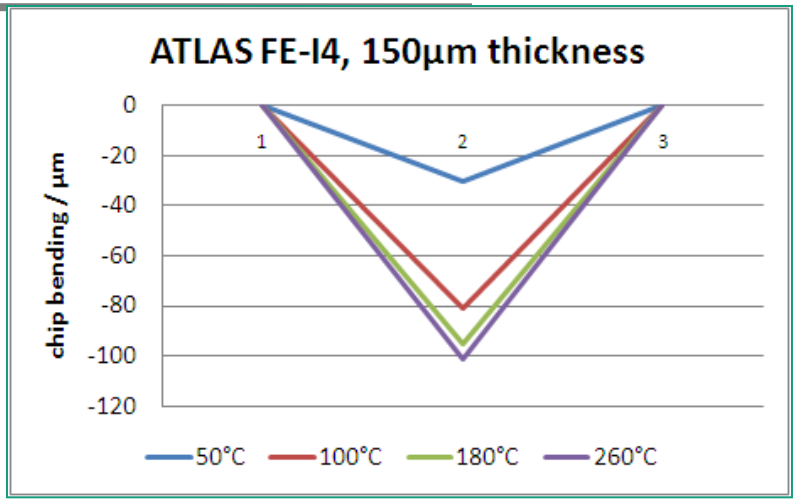


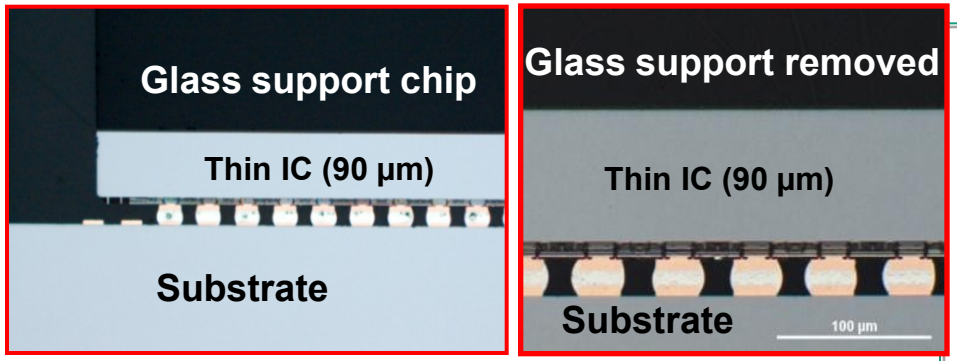


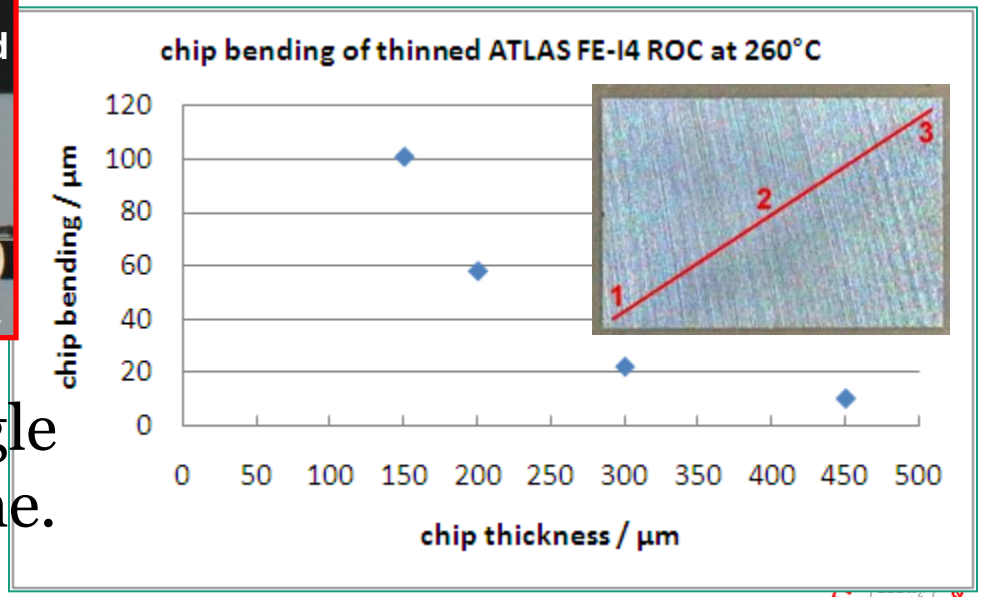
Ordered at Phoenix (Ivrea, Italy), back end June

Thin Chip Bump-Bonding

- Safe bump-bonding requires max bend ~15µm.
- Minimal thickness of 450µm.
- Use temporary glass handling wafer + laser de-bonding.



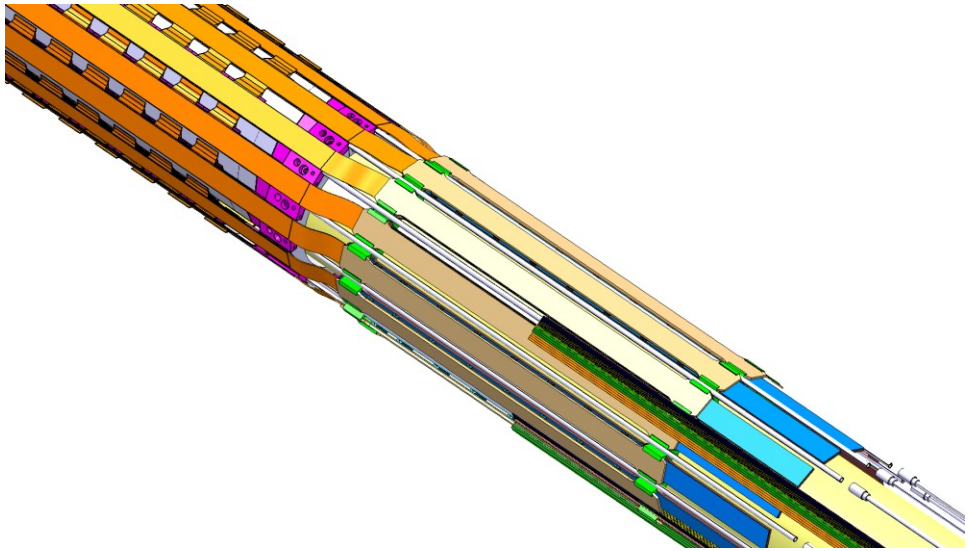




- Prelim test: promising! 8 single chip 150µ assemblies end June.

Conclusion

- Based on success of FE-I4A development, and characterization work of sensor communities.
- "Not much contingency" in schedule means success oriented developments.



- FE-I4B design: July 2011.
- Sensor choice: July 2011.
- IBL module R&D on-going:
  - Flex design.
  - Thin chip bump-bonding

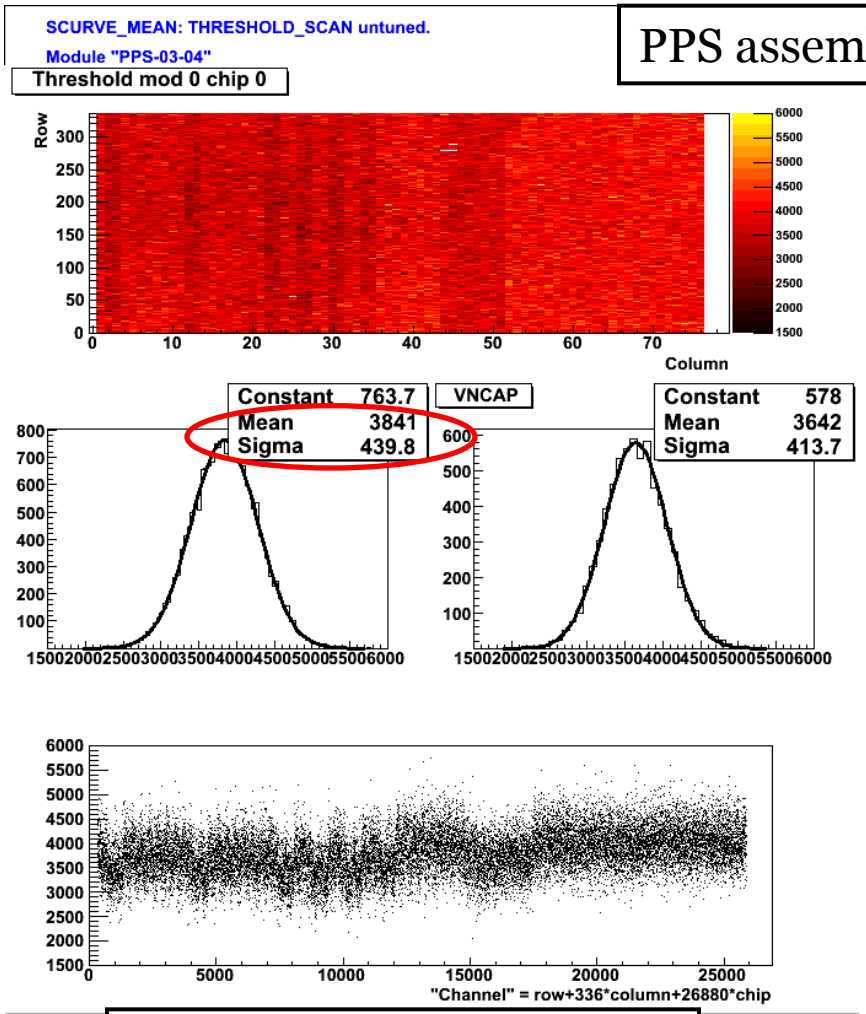
→ fast track IBL with installation in 2013.

Backup

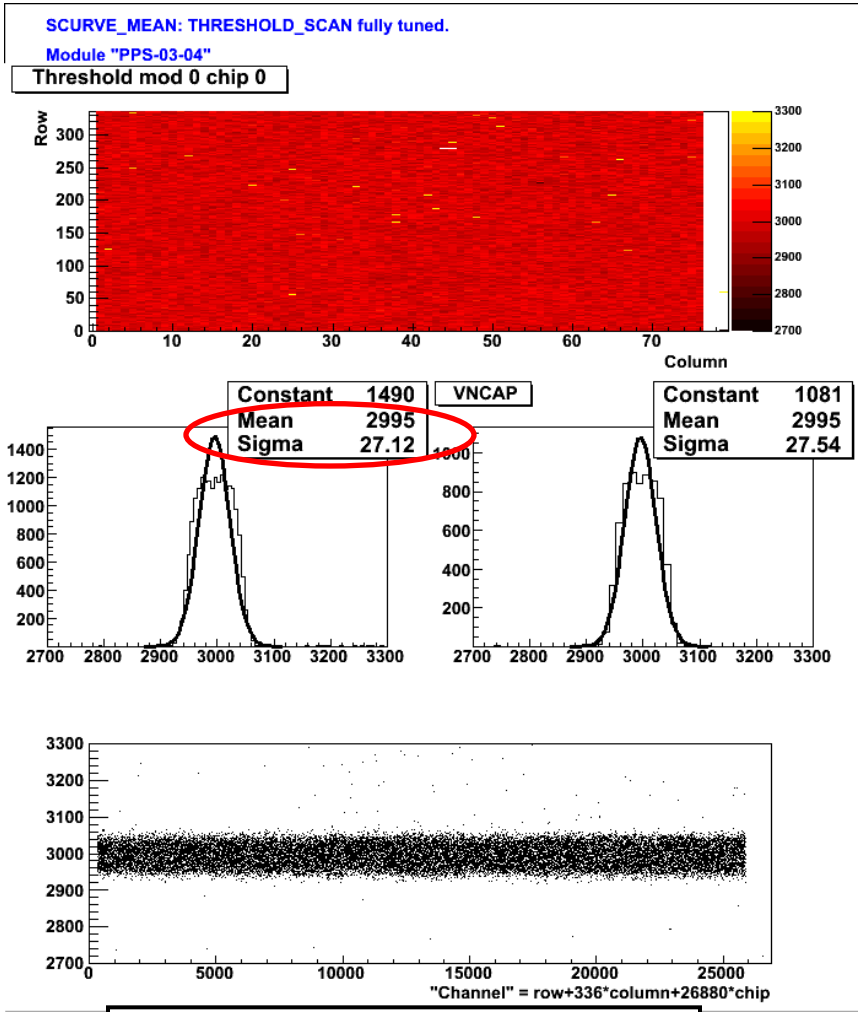
BACKUP

Threshold tuning

PPS assembly



Threshold before tuning

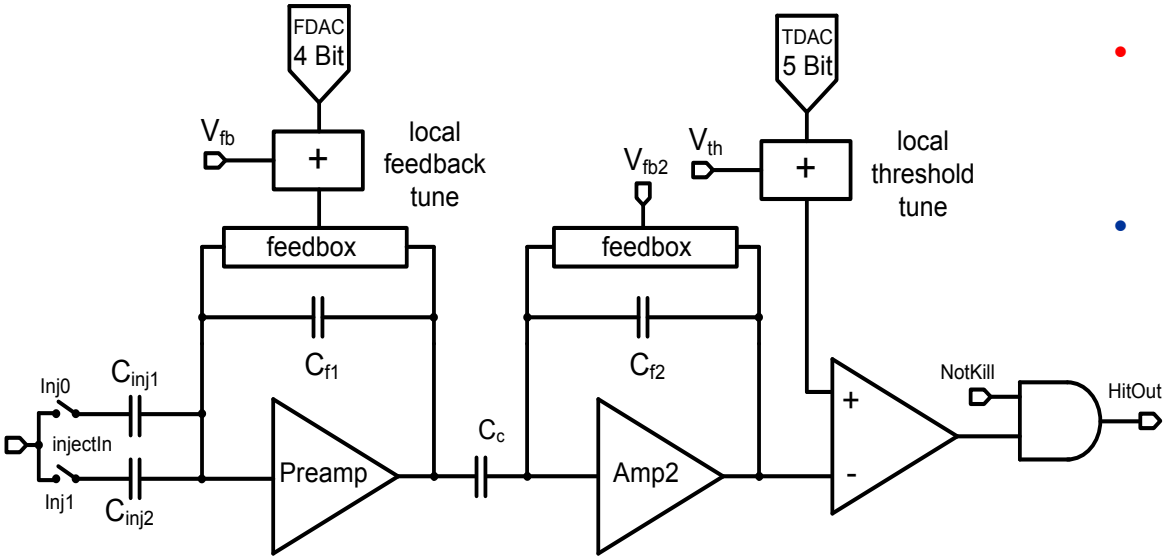


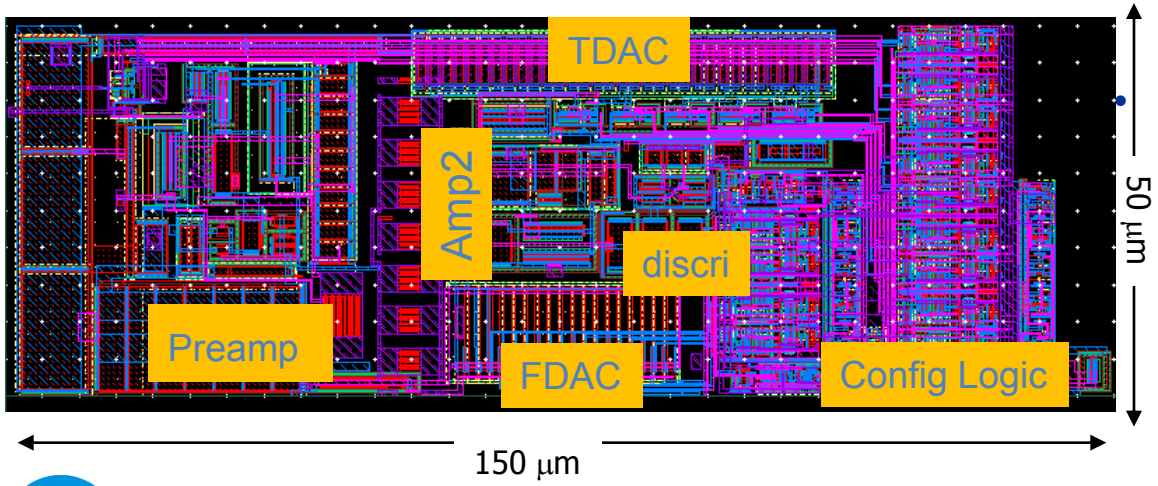
Threshold after tuning

Changes for FE-I4B

- FE-I4A issues to be fixed:
  - Calibration pulser output resistance.
  - SR readback.
  - Range of DACS.
  - Top row power.
  - Skipped trigger counter
  - Reset of EFUSE.
  - Array needs to be uniform: feedback cap, discri, SEU latch.
- New functions:
  - Add global ADC + temp sensing.
  - Change placement & ctrl of analog MUX.
  - 13-b BCID + BCR counter.
  - Event truncation. + fix powering!

Analog Pixel





- In FE-I4_proto1 (FE-I4 prototype submitted in 2008):

- 2-stage architecture optimized for low power, low noise, fast rise time.

→ regul. casc. preamp. nmos input.

→ folded casc. 2nd stage pmos input.

→ Additional gain, Cc/Cf2~6.

→ 2nd stage decoupled from leakage related DC potential shift.

→ Cf1~17fF (~4 MIPs dyn. range).

- 13b configuration:

→ 4 FDAC: tuning feedback current.

→ 5 TDAC: tuning of discriminator threshold.

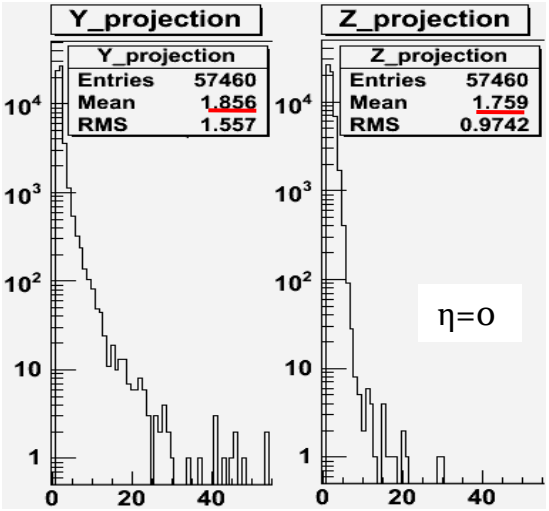
→ 2 Local charge injection circuitry.

→ 1 HitEnable.

→ 1 HitOr.

Performance / Efficiency

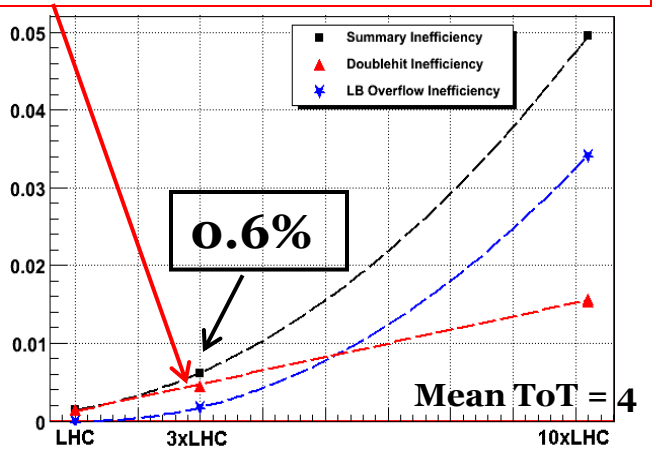
IBL: charge sharing in Z comparable to phi



Regional Buffer Overflow

Memories	Simulation		Analytical	
	IBL	10xLHC	IBL	10xLHC
5	0.047%	2.19%	0.029%	2.25%
6	0.011%	0.65%	0.003%	0.57%
7	<0.01%	0.16%	<0.01%	0.13%

@ IBL rate, pile-up inefficiency is the dominant source of inefficiency



Inefficiency:

- Pile-up inefficiency (related to pixel x-section and return to baseline behavior of analog pixel) → ~ 0.5%.
- Regional buffer overflow → ~0.05%.
- Inefficiency under control for IBL occupancy.

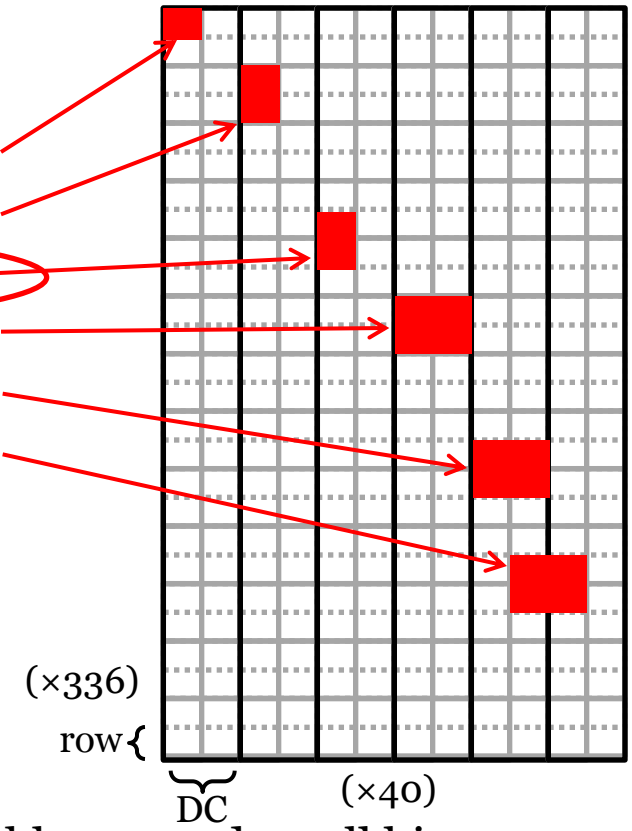
Fixed format clustered data

- compression factor (all at 3×LHC)

  3.7cm (vs. 21cm), η=0

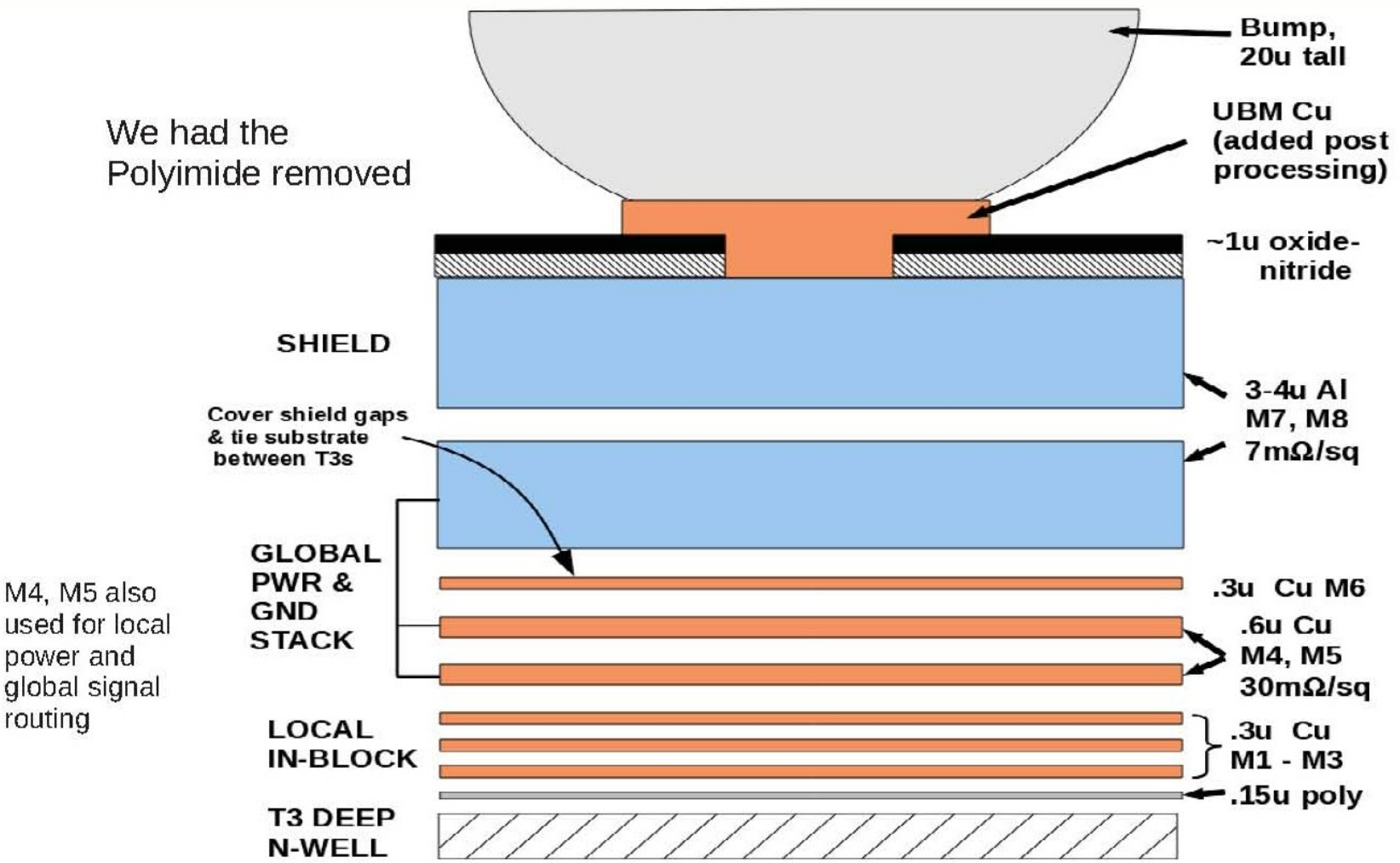
- indiv pixels: 4.09 (0.25)×(7+9+4+2)= 1.00 (1.00) A.U.
- static 1×2: 3.45 (0.18)×(7+8+2×4+2)=0.96 (0.83) A.U.
- dynamic 1×2: 3.02 (0.15)×(7+9+2×4+2)= 0.87 (0.74) A.U.
- static 1×4: 2.86 (0.17)×(6+8+4×4+4)=1.08 (1.08) A.U.
- dyn. in-DC 1×4: 2.43 (0.15)×(6+9+4×4+4)= 0.95 (0.95) A.U.
- dynamic 1×4: 2.13 (0.14)×(7+9+4×4+4)= 0.85 (0.94) A.U.

10^6.count.FE^{-1}.s^{-1} | column | row | ToT | NL



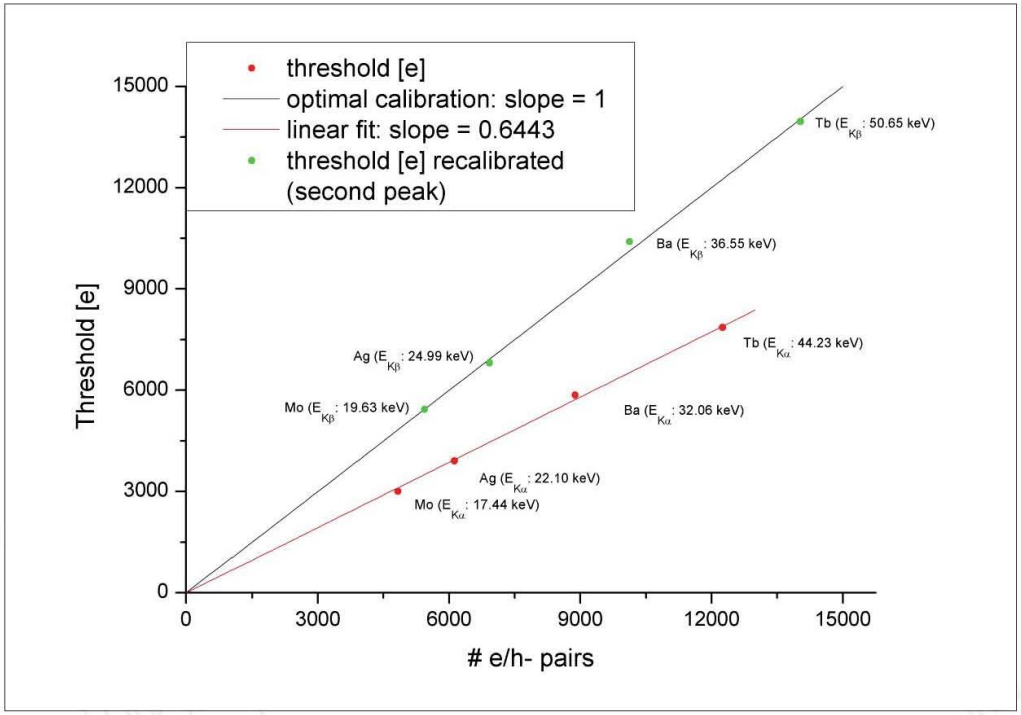
Choice: **Dynamic phi-pairing** (dynamic 1×2) merge neighbours and small hits in process. Compression ok, simple to do and good format, 24 bits (nice for FIFO and 8b10b). Note that hamming decoding needed before formatter.

Metal stack and usage



Chip calibration measurement

- **#e/h-pairs** from Eγ **vs.** measured **threshold** using **calibration from simulation**.



Large uncertainties expected:
~ 10% - 20%

Crosscheck with second method still to come.

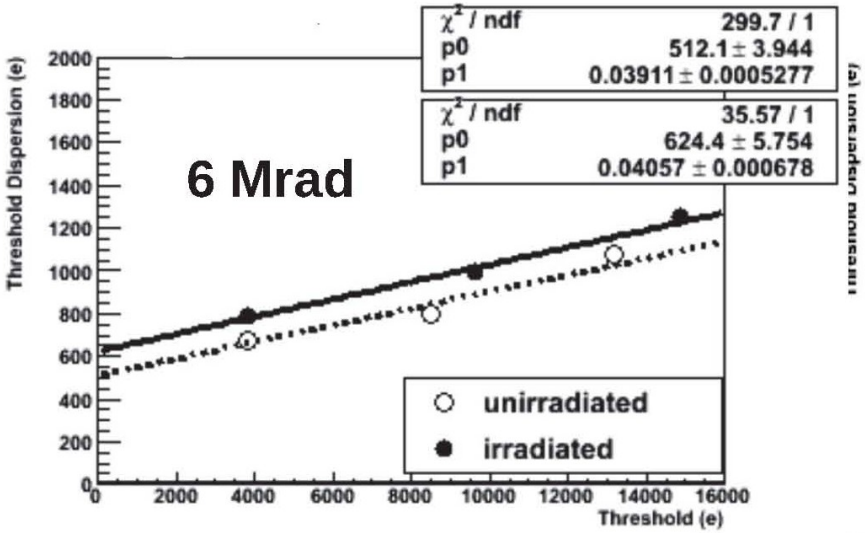
→ Calibration constant in this chip has been underestimated

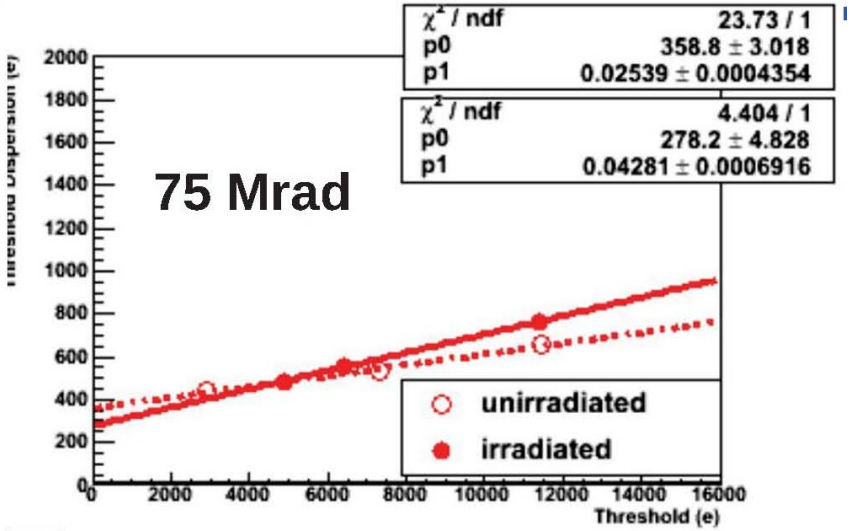
.

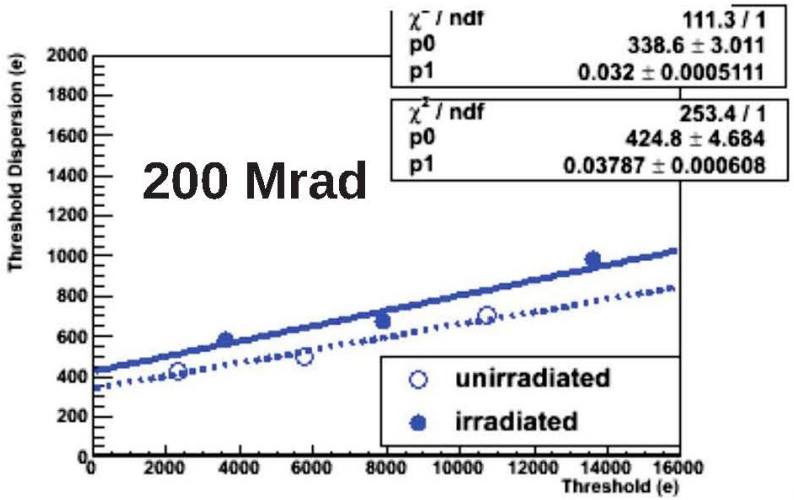
- **#e/h-pairs** from Eγ **vs.** measured **threshold** using **absolute calibration.**

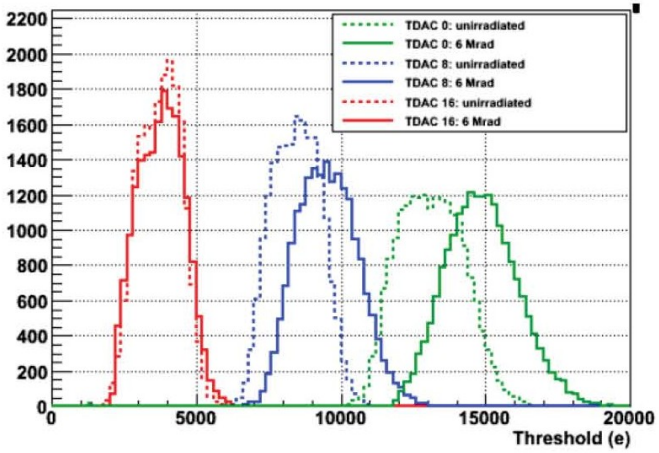
→ **New calibration fits nicely to expected slope of 1.**

Threshold dispersion wrt dose









Digital Region Power

Simulation @1.2V

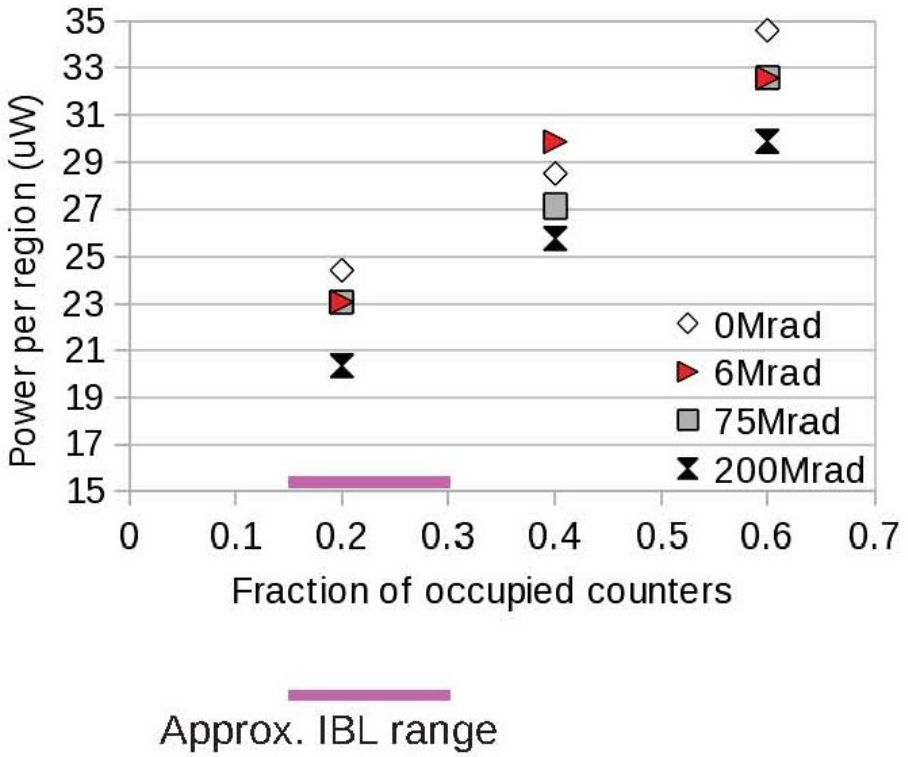
Average power for 4-pixel region at IBL occupancy (MC hits)

Simulation type	Power (avg) [uW]
ETS[1]	42.28
Spectre[2]	25.19
Ultarasim(s)[2]	24.69
Ultarasim(a)[2]	24.73
Ultarasim(ms)[2]	35.12
HSIM[1]	27.64
HSIM[2]	30.98

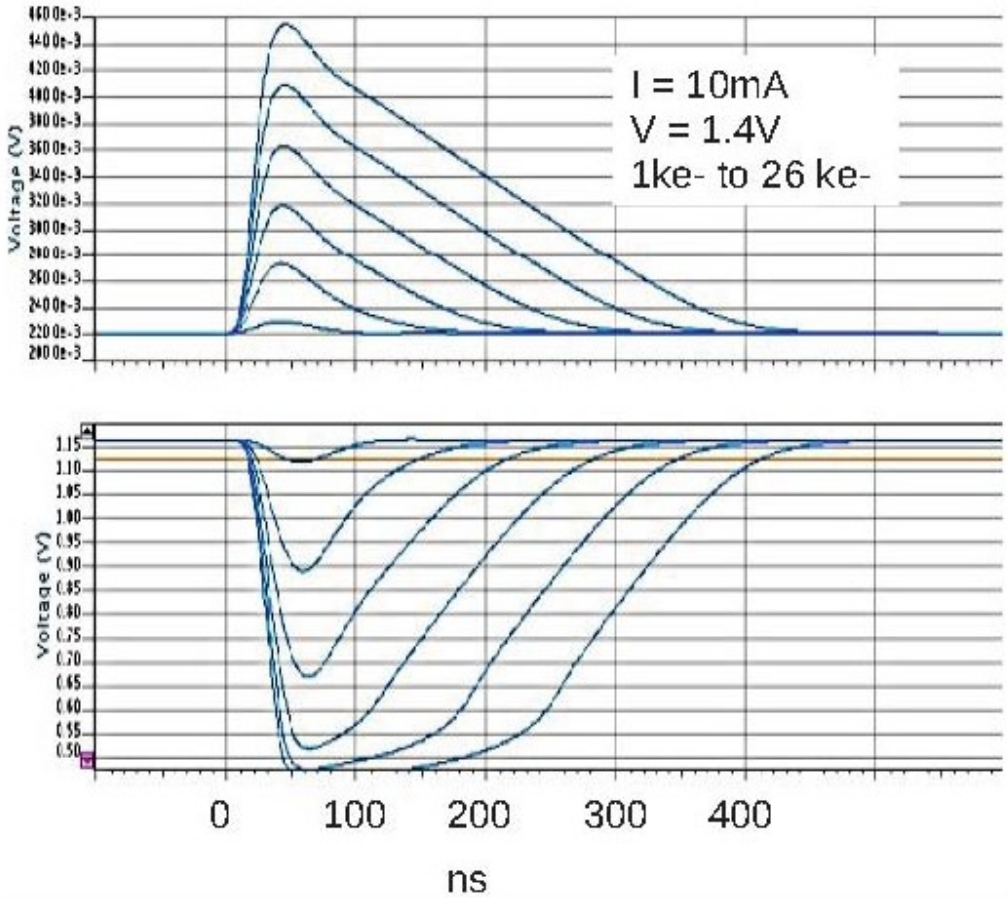
Parasitic extraction done width [1]PEX

Measurement @1.2V

Occupancy faked with periodic charge injection



ToT coding



"True" ToT (clocks)	HitDiscCnfg 00	01	10	11
Below tresh	F	F	F	x
1	0	E	E	x
2	1	0	E	x
3	2	1	0	x
4	3	2	1	x
5	4	3	2	x
6	5	4	3	x
7	6	5	4	x
8	7	6	5	x
9	8	7	6	x
10	9	8	7	x
11	A	9	8	x
12	B	A	9	x
13	C	B	A	x
14	D	C	B	x
15	D	D	C	x
≥16	D	D	D	x

Corrected for timewalk

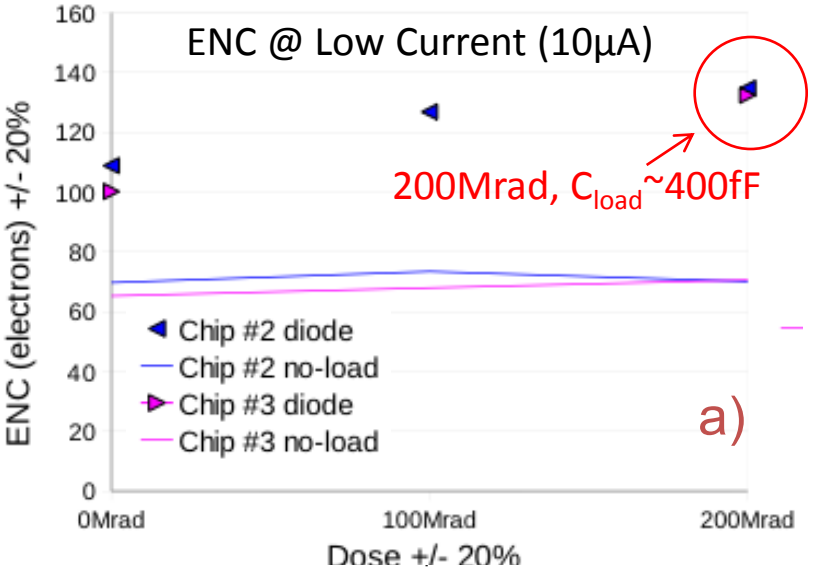
Not corrected for t-wlk

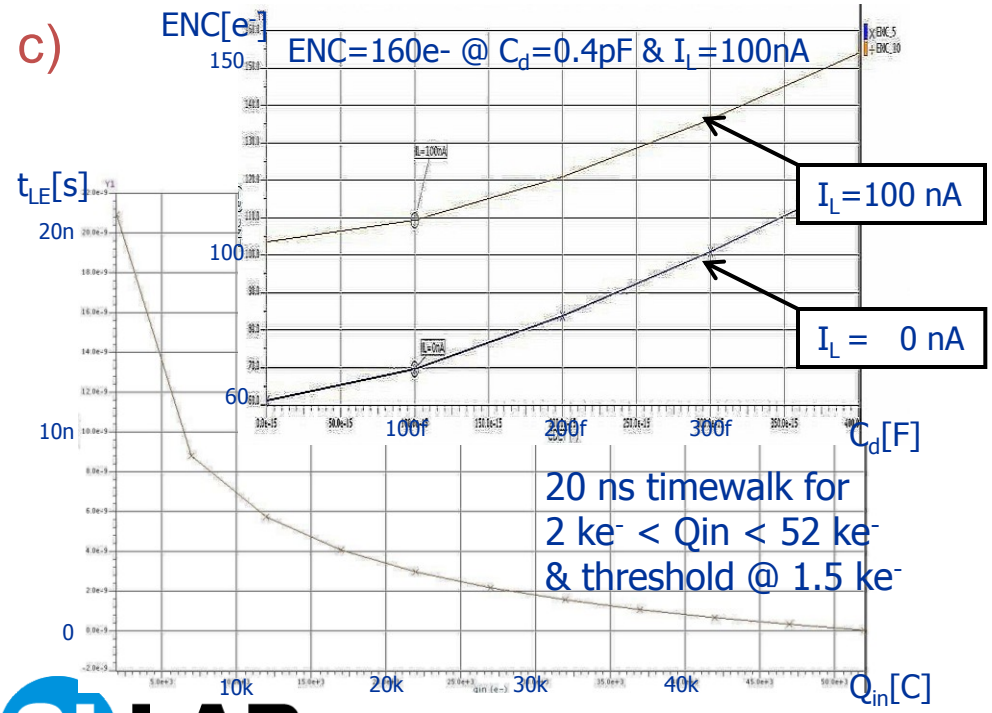
Noise and Radiation Results

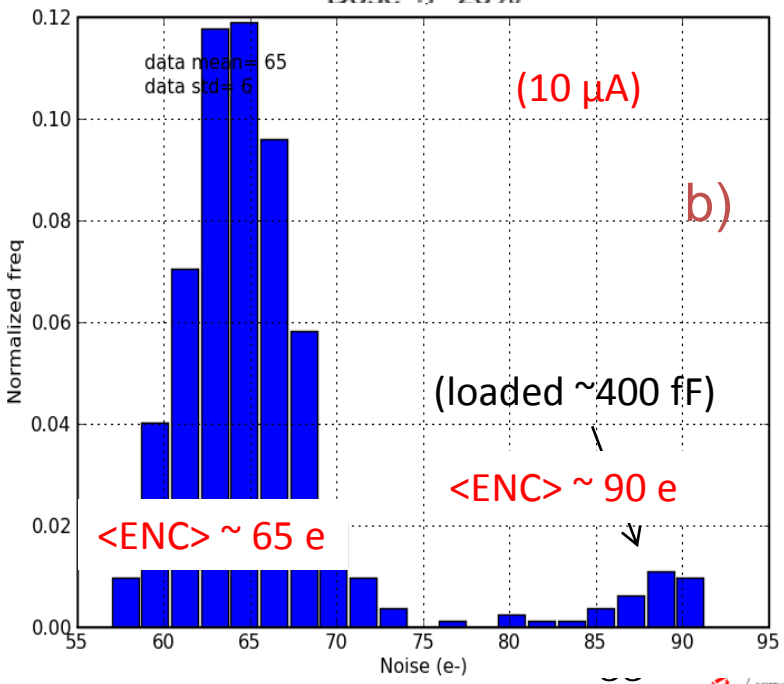
a) ENC on "Collaboration Proto 1" before and after irradiation (200 Mrad)

b) Measured ENC for pixels with and without C_{load}

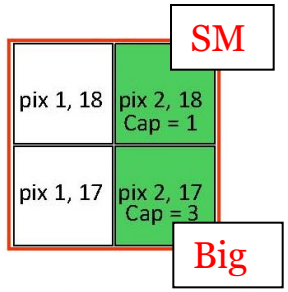
c) Simulated ENC and time-walk @ 10 µA/pixel (preamp-amp2-comparator)



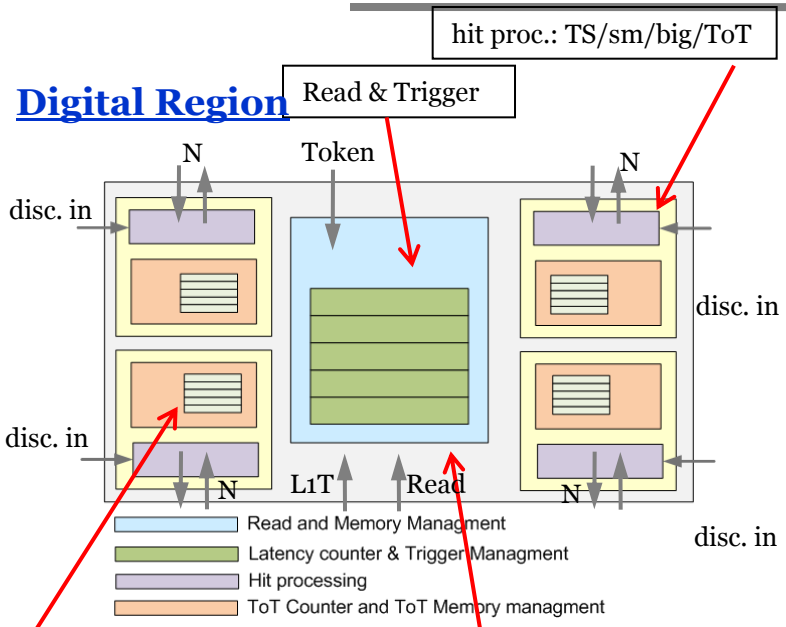




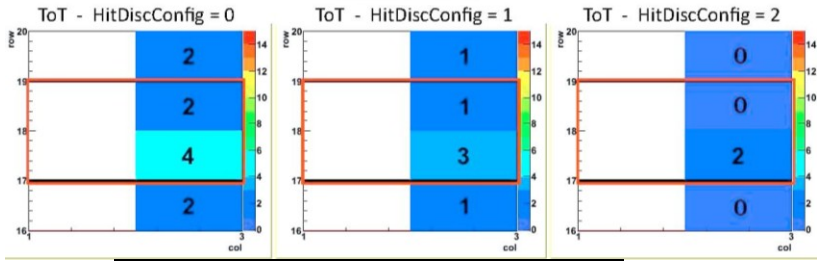
Pixel Digital Region



Digital Region



PlsrDAC = 200

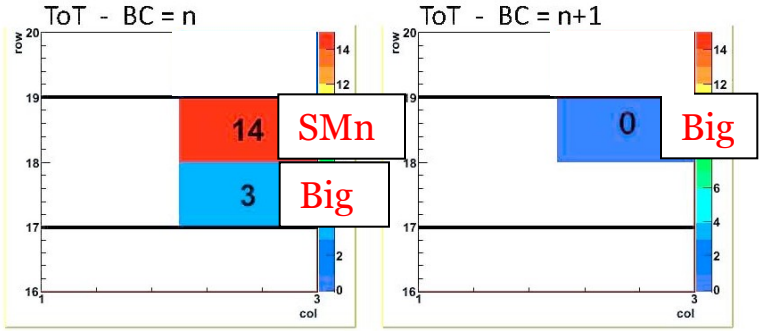


Hit discrimination works

Time Walk (seen for smaller injected charge)

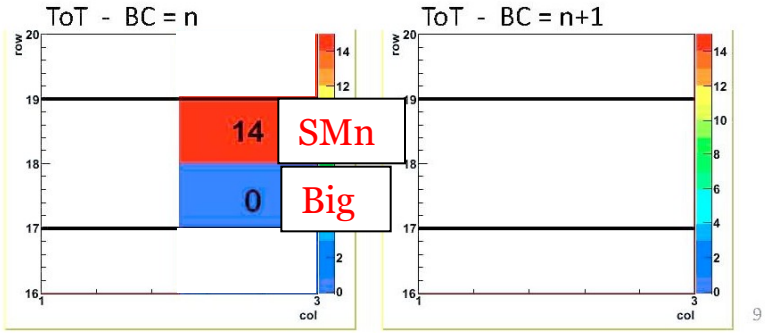
HitDisc=0: small hit is seen in later BC (double counting is known feature)

PlsrDAC = 150



HitDisc=2: small hit is associated to big hit in correct BC

PlsrDAC = 150

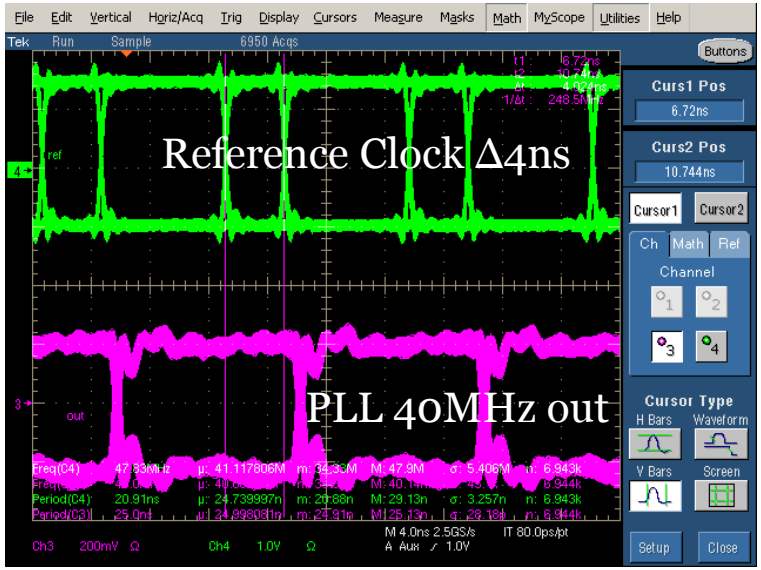


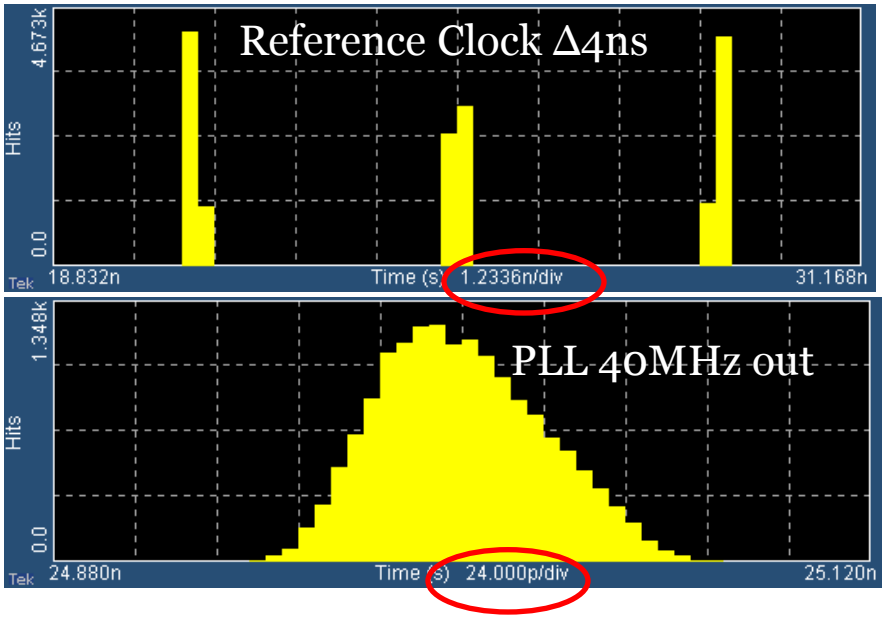
Time walk compensation works

- Power (3.7cm 3xLHC full): ~3-4µW / digital pixel (preliminary)

CLKGEN PLL

- Use as reference clock a clock where every second edge is delayed by 4ns.





Histograms of measured clock periods

Measurement	Sources	Population	Mean	StdDev
Clock Period1	Ch3	10863	6.2502ns	40.938ps
Clock Frequency1	Ch3	10863	160.00MHz	1.0506MHz
Clock Period2	Ch4	2703	25.000ns	4.0761ns
Clock Frequency2	Ch4	2703	41.107MHz	6.8393MHz

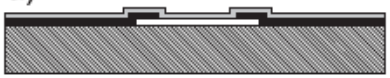
160MHz CLKGEN output

160MHz clock cleaned up!!!

Reference Clock Δ5ns

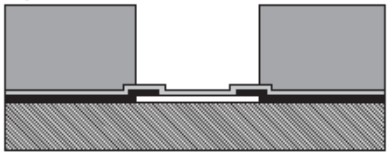
Solder bumping process @ IZM

a)



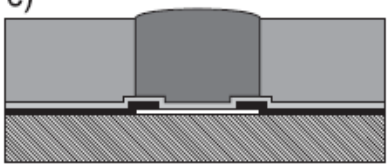
Sputter etching and sputtering of the plating base / UBM

b)



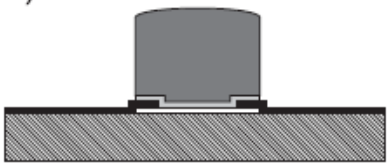
Spin coating and printing of Photoresist

c)



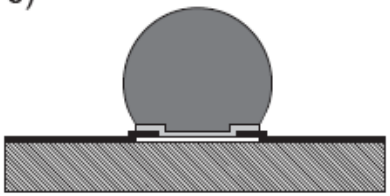
Electroplating of Cu and PbSn

d)

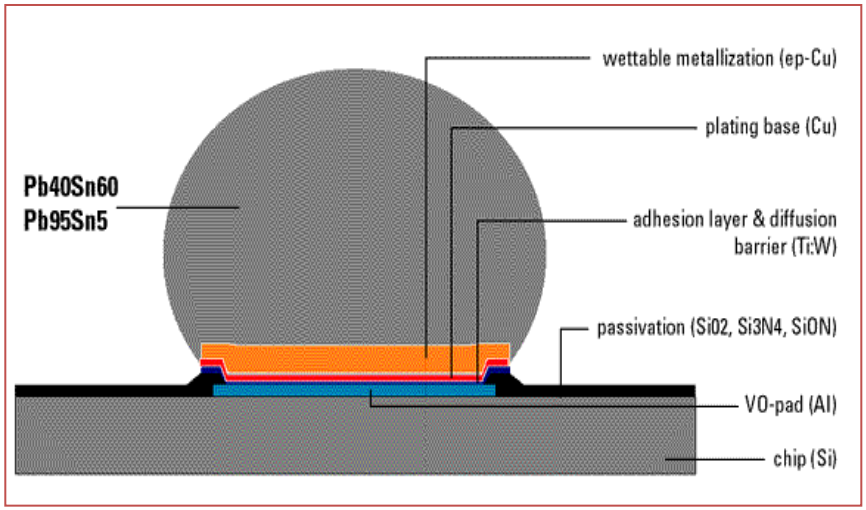


Resist stripping and wet etching of the plating base

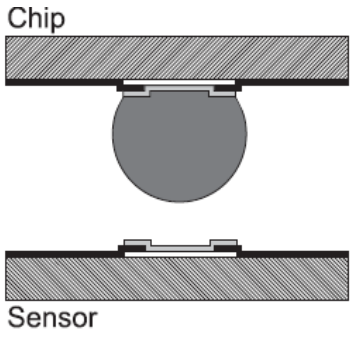
e)

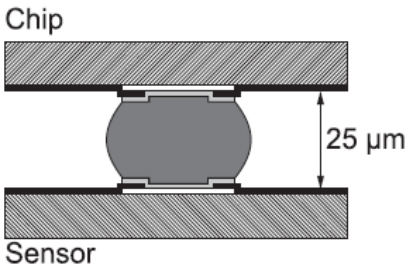


Reflow



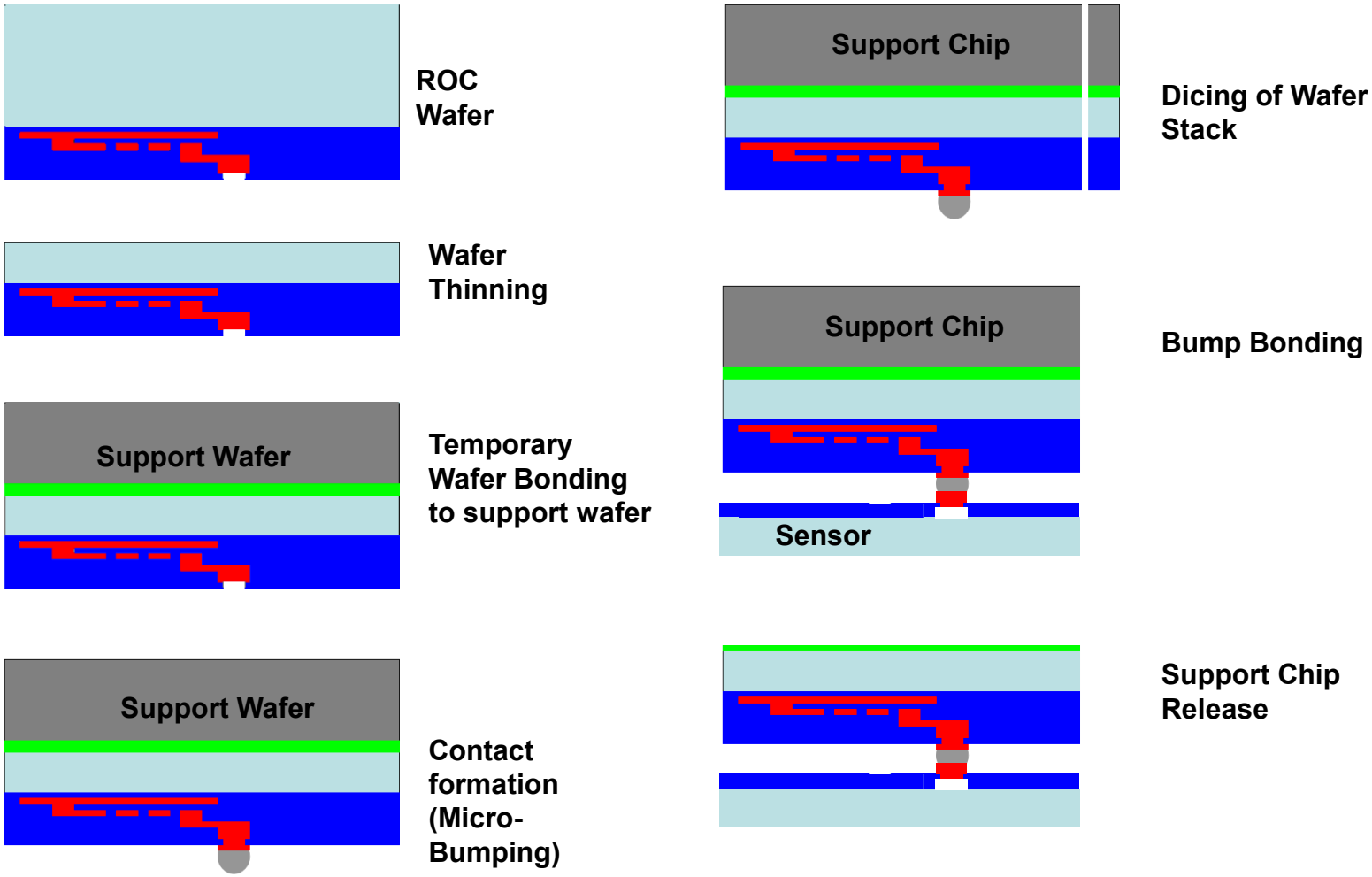
Flip-Chip



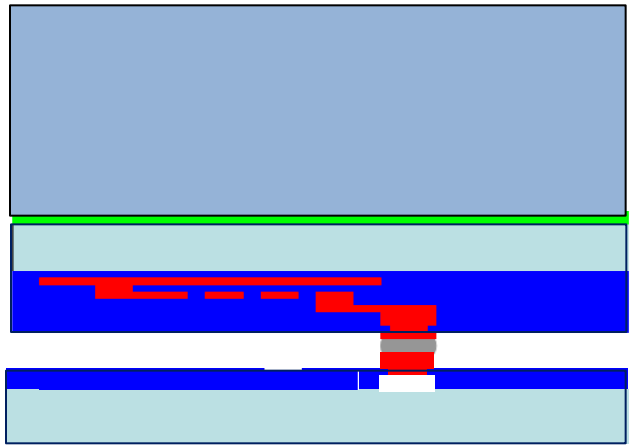


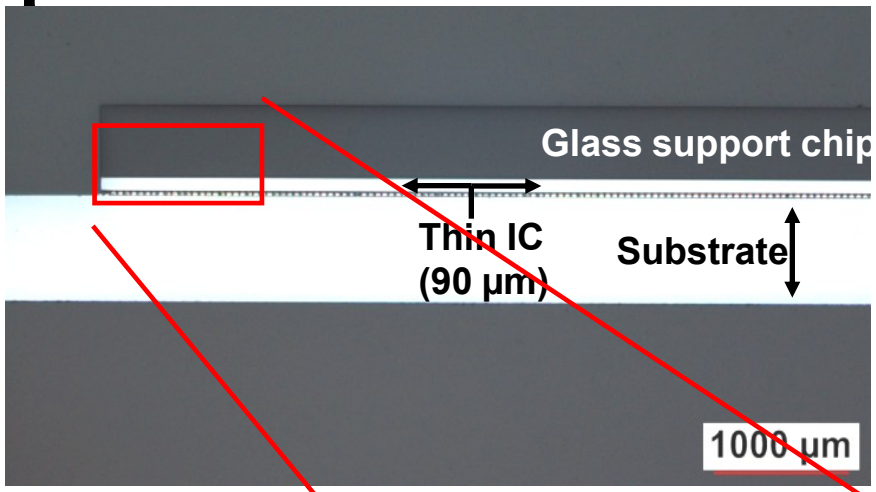
SI LAB
Silizium Labor Bonn

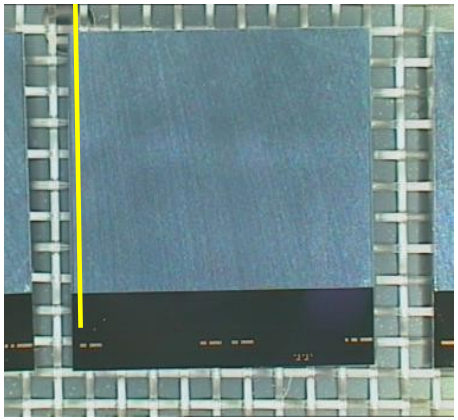
Thin chip modules – Process flow

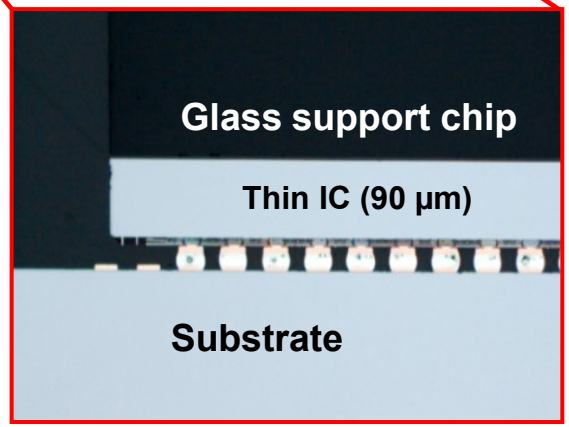


Flip Chip Assembly of Chip + Support



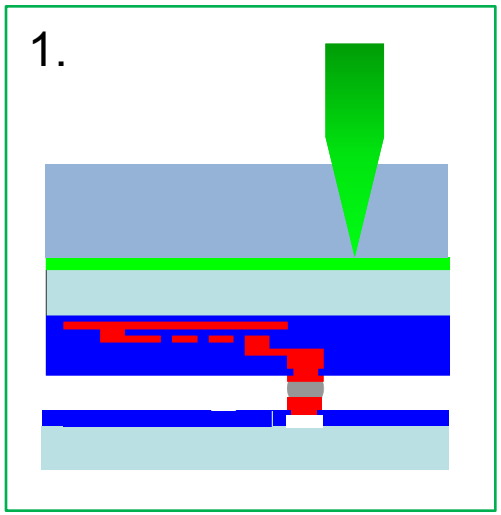


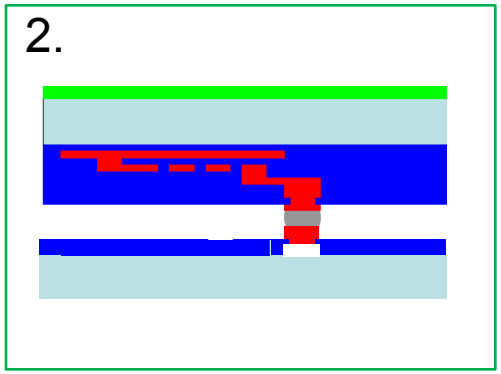


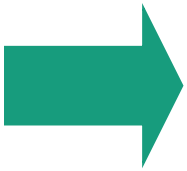


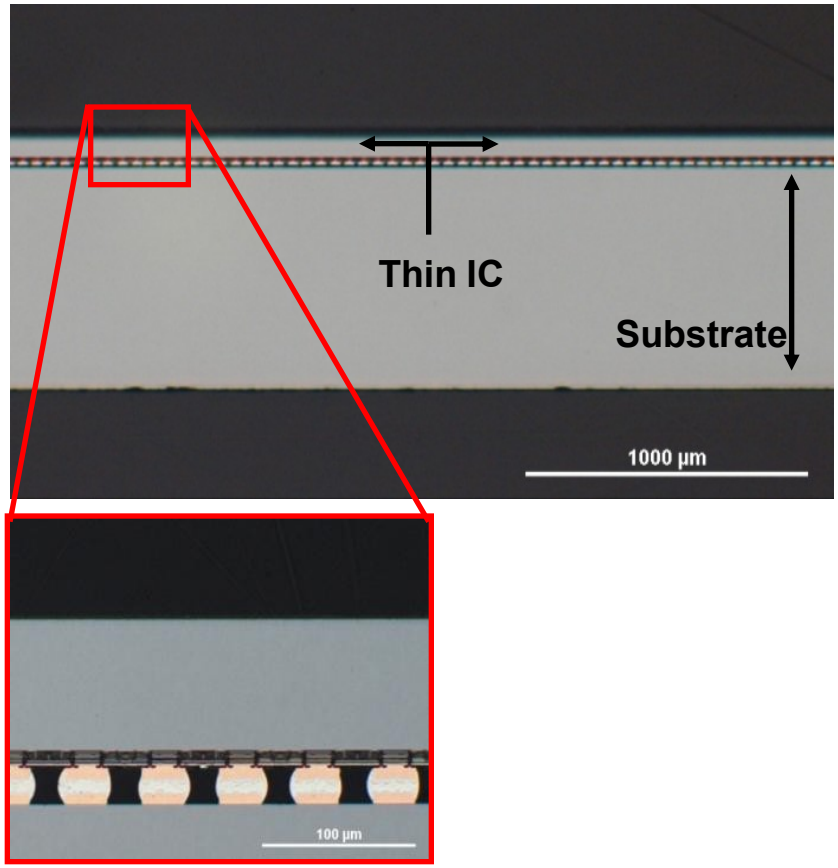
- FE-chip after bump bonding
  size 14x11 mm² (2x1 FE-I3)
- Cross section of the first bump row (yellow line)

Support Chip Release via Laser Debonding









Status thin FE-I4 modules at IZM

- 1 FE-I4 (AUN6NGH) wafer have thinned to 470 µm and has been used for 36 assemblies without any bump defects in the corners.

  → Demonstrate the minimum chip thickness of 450 µm.

- 1st wafer (AWN6TUH) has been thinned to 150 µm, bumped and is currently being used for flip chip assemblies:
  - Already 5 assemblies (3D FBK from ATLAS 09) in our hands.
  - No support chip removal for these assemblies.
  - 16 more single chip assemblies have been flipped:
    - 8 bad chips for adjusting laser parameters
    - 8 good chips
  - 8 are currently at the laser debonding step in US, 8 more will go to another vendor (in Germany) in the next days.

    → Expected delivery in the next 2 weeks.
  - Up to 8 2-chip modules (depending on the number of available FE-I4 chips) will go to flip chip after the finishing of the 1st devices
- 6 more FE-I4 wafers are currently in bump process:
  - 4 wafers with thickness of 150 µm
  - 2 wafers with thickness of 100 µm
  - UBM and bump deposition finished by mid June.