TCAD Simulations of Silicon Strip and Pixel Sensor Optimization

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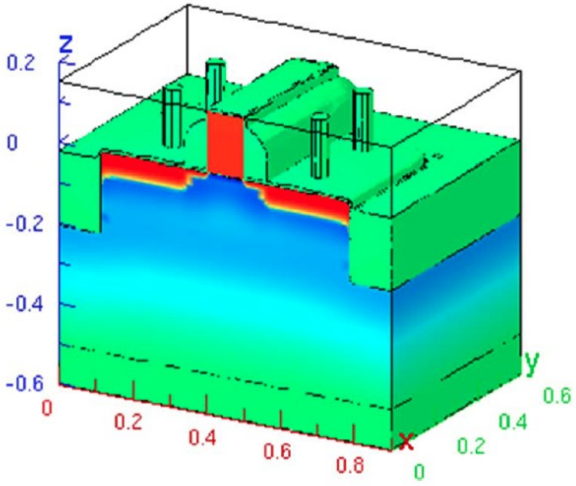
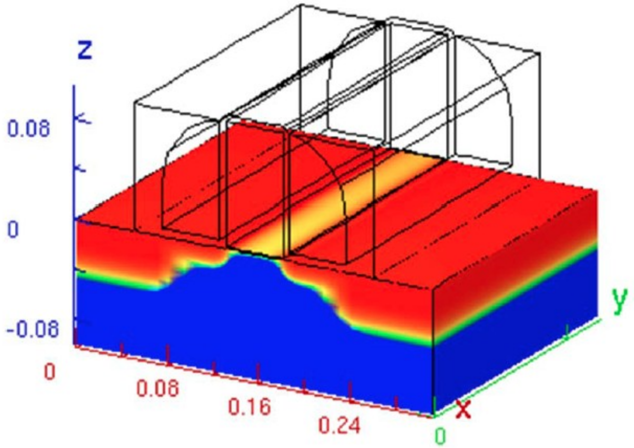
Technology CAD (TCAD)

- TCAD started
  - to build the links between the
  - semiconductor physics and
  - electrical behavior
  - to support circuit design
- Modern TCAD consists of
  - Process simulation, and
  - Device simulation
- Originated from the work of
  - Prof. Robert W. Dutton and his group at Stanford Univ.
- Widely used in semiconductor industry
  - to reduce the development cost and time
  - to understand the physics behind
    - that is even impossible to measure
- TCAD: Computer Aided Design for Semiconductor Technology

MOS transistor



Process simulation



Device simulation

Brief History

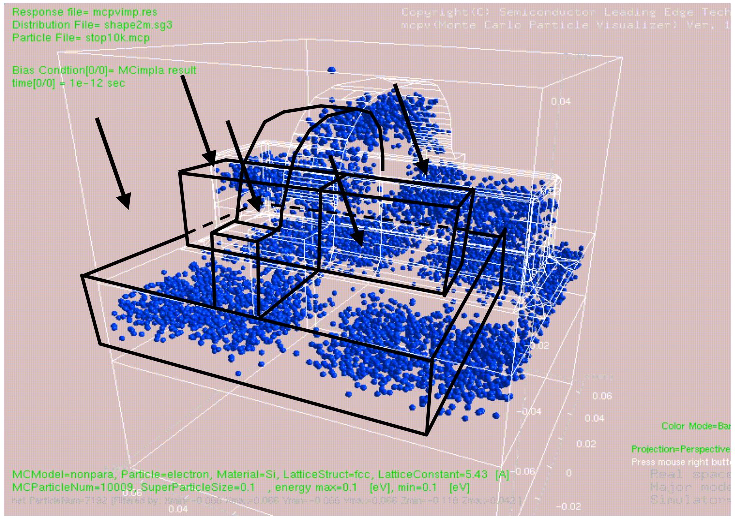
1977: Prof. Dutton, Stanford
  Process/Device sim
  SUPREM-I (1D)/PISCES
1979: Technology Modeling Associates (TMA/Synopsys)
  TSUPREM4 (2D)/MEDICI
1989: Silvaco International
  ATHENA (2D)/ATLAS
1989: Integrated Systems Engineering AG (ISE)/Synopsys
  DIOS (2D)/DESSIS
1992: TMA
  TAURUS (3D TSUPREM4/DEDICI)
1993: Prof. Law, Florida
  Process sim: FLOOPS (3D)
2002: ISE
  FLOOPS (3D)
2005: Synopsys
  Sentaurus (3D TAURUS)

TMA⇒AVANT!/1998⇒Synopsys/2001
ISE⇒Synopsys/2004

Prof. Robert W. Dutton
(from Stanford TCAD Home page)

In Japan,
1996: 3D HyENEXSS (Selete/TCAD Int.)
  Selete: Consortium of 10 semiconductor co.
2011: 3D HyENEXSS (Selete)
  Project ends

Process Simulator Device Simulator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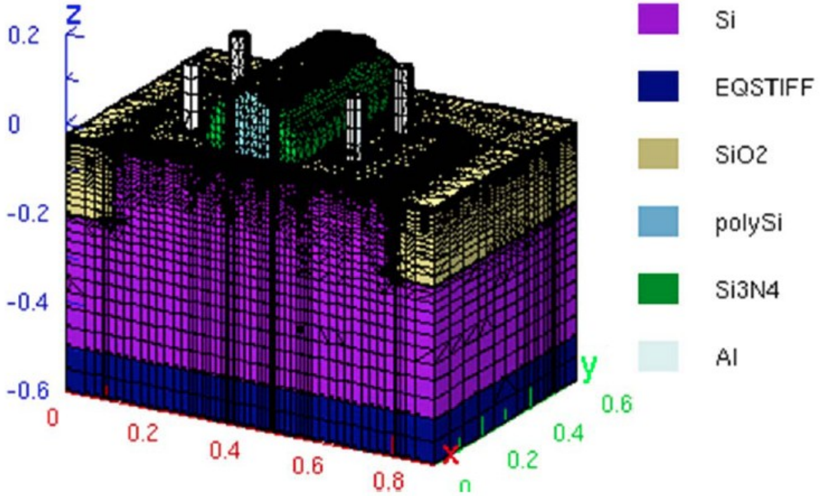
ion-implantation process (M.C.-model)



- Process steps
  - Oxidation
  - Deposition
  - Etching
  - Ion implantation
  - Annealing
- Mostly for process experts
  - Unless you know the process parameters, you have no way to simulate.

- Solving equations
  - Poisson eq. (ψ, n, p)
  - Current continuity eq. *Jn*, *Jp* (ψ, n, p)
  - Heat conduction eq. (“Drift Diffusion model) (TL)
  - …
- Four equations and four variables
  - potential ψ, electron-density n, hole-density p, and lattice-temperature TL

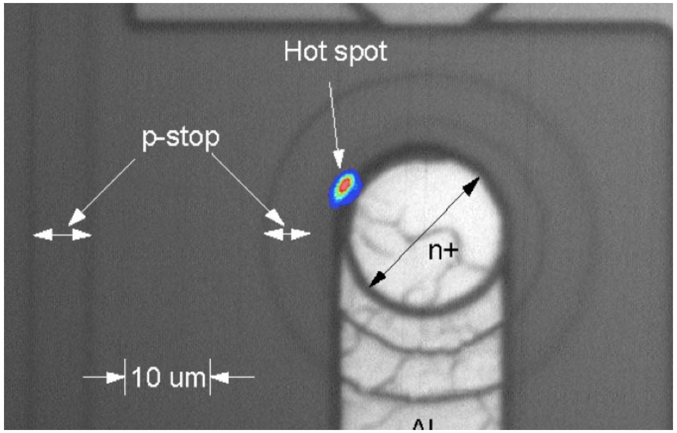
Caveat

- Which physics models and their parameters to use. Device simulator e.g.,
  - Transport models
  - Mobility models
  - Generation-recombination models (SRH, Auger, II, trap, surface…)
    - SRH: Shockley-Read-Hall model
    - II: Impact Ionization model
- Finite Element method
  - A core of the calculation
  - 3D vs. 2D
    - 3D: Usually “very” time consuming
    - 2D: Most of the cases, good enough
  - Meshing: resolution vs. time
  - Convergence of calculations
    - Try and error for finding best procedures (method, physics model)
- The real caveat would be
  - “You get only what you put.”
  - Although semiconductor industry is trying to simulate perfectly, we may still miss models, e.g., for dicing edge, radiation damaged surface...

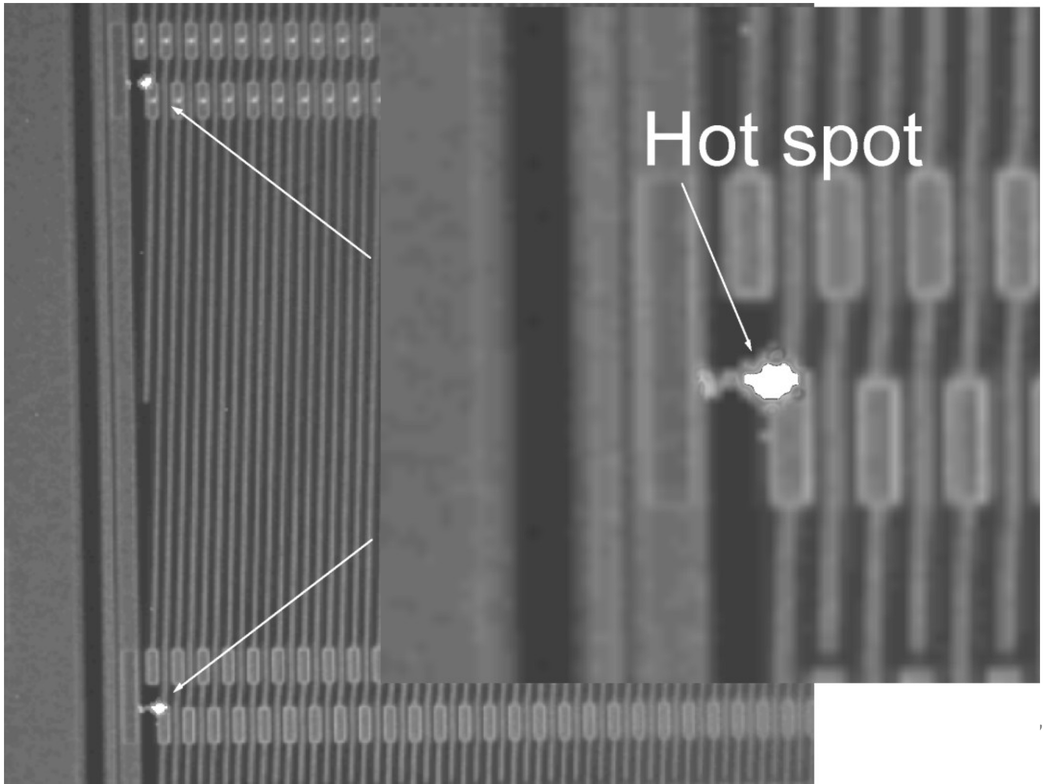
Application for Strip and Pixel Sensor Optimization

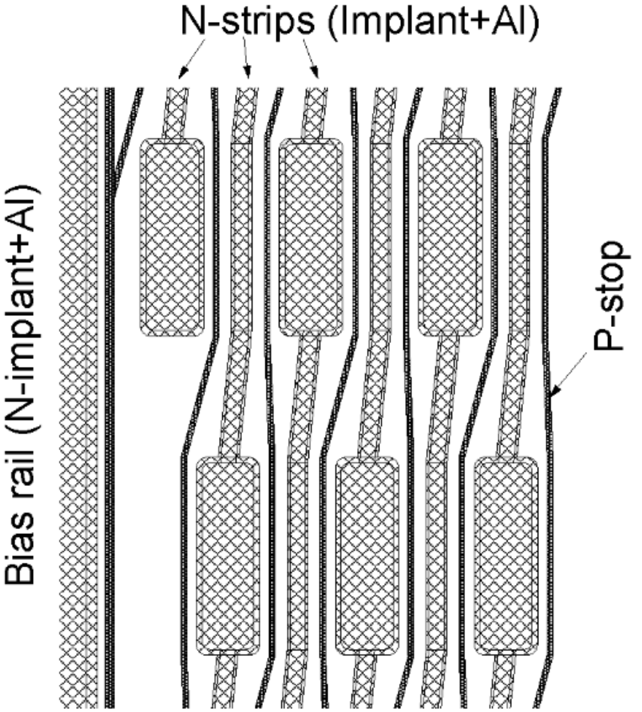
- Number of presentations in this conference
  - Looking forward to what will be presented
- I will report our results of comparison of TCAD simulations and measurements
  - Main goal
    - To develop highly radiation-tolerant silicon “planar” sensors, i.e., to cope with very high voltage operation
      1) P-stops between n-implants
      2) Punch-Thru Protection (PTP) structure
      3) Edge structure
  - Simulator
    - HyDeLEOS (Device simulator) in HyENEXSS
    - 2D simulations

P-stops between N-implants



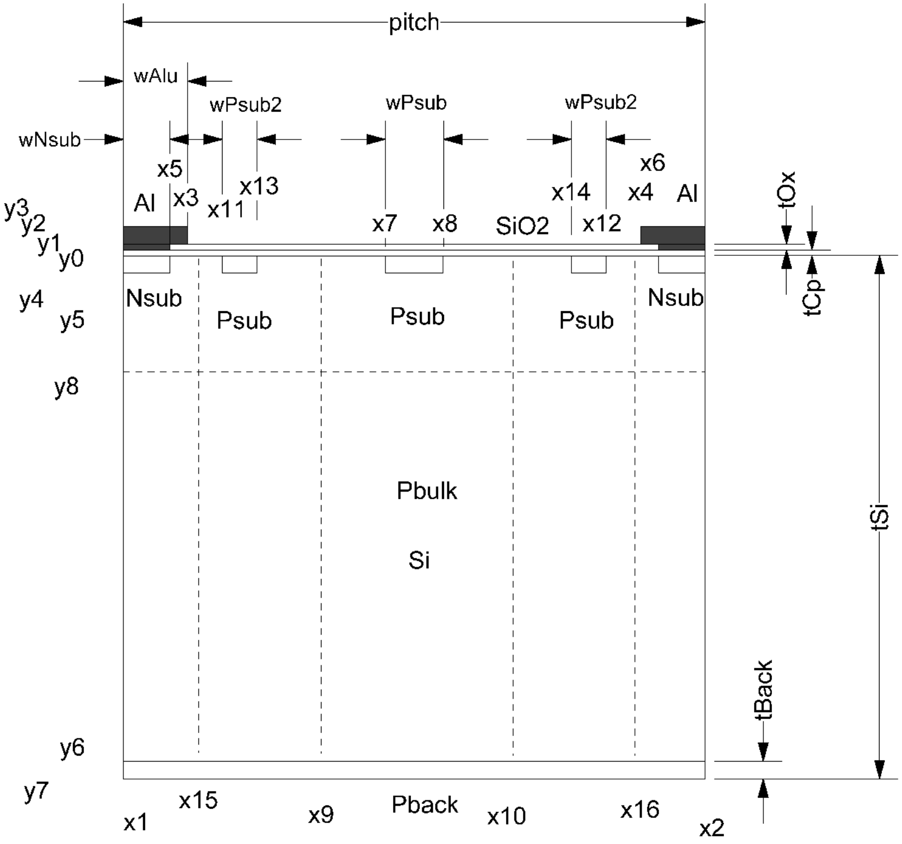
- Problems - Hot spots
  - IR image overlaid on visual image
  - Microdischarge = Onset of leakage current
- What to do the structures to reduce the electric fields?





P-stop Structures Optimization

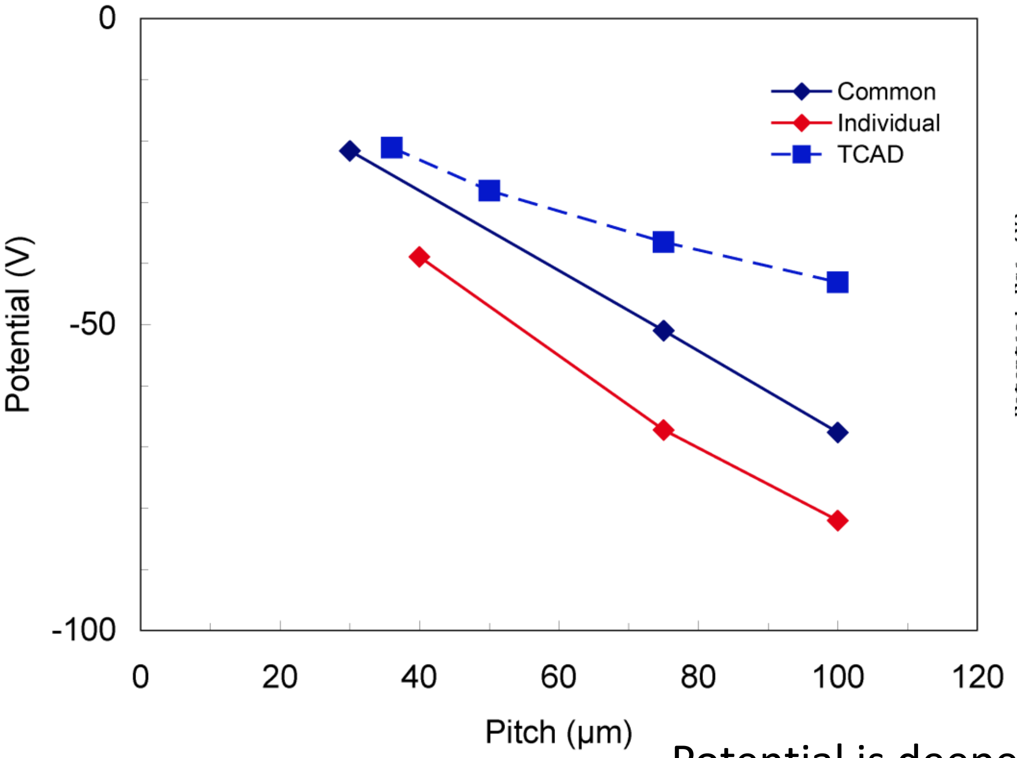
- Multiple lines of p-stops between n-implants
  - 1, 2, 3 p-stops
  - Location of p-stops
  - Distance, gap, …
- Device simulations for electric fields

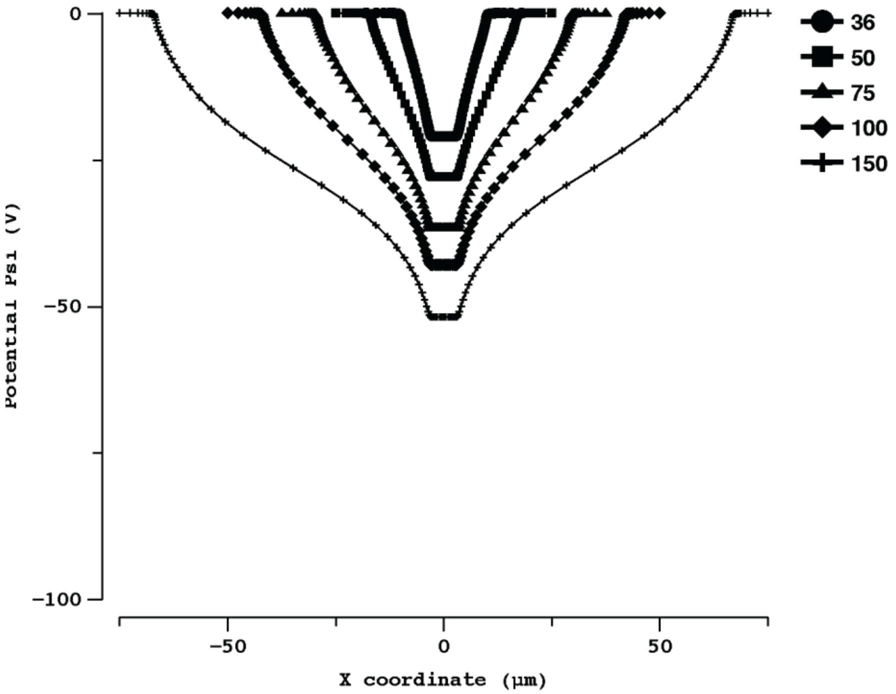


Presented at 7th "Hiroshima" symposium and published in
Y. Unno et al., Nucl. Instr. Meth. A636 (2011) S118–S124

Pitch Dependence

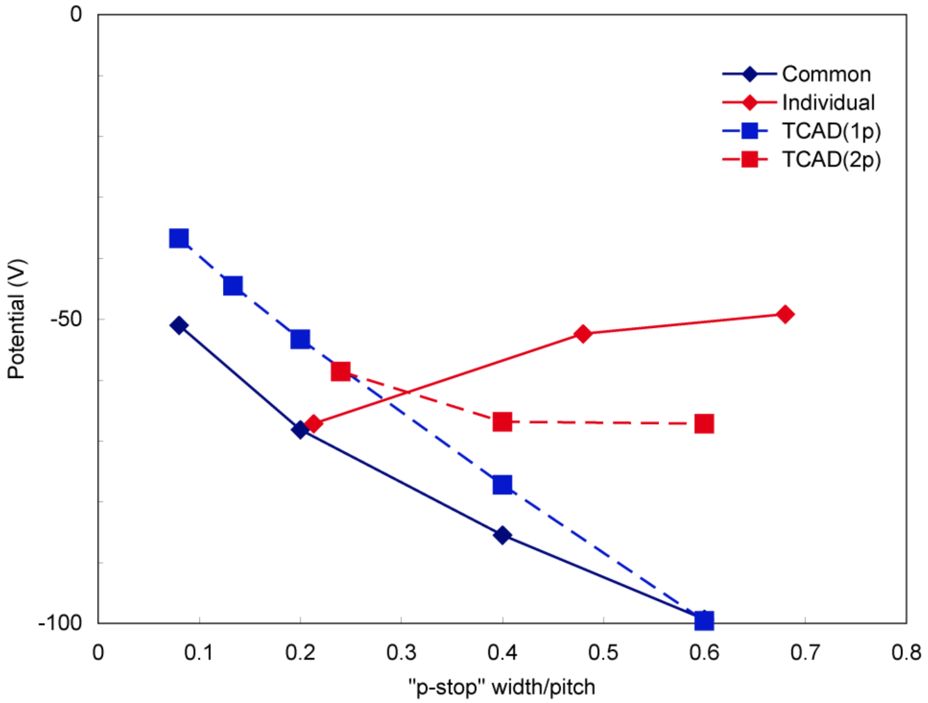
- We have processed test structures and compared with the simulations. New results to this conference.
- Test structures:
  - Common = Common p-stop structure == 1 p-stop line in TCAD
  - Individual = Individual p-stop structure == 2 p-stop lines in TCAD

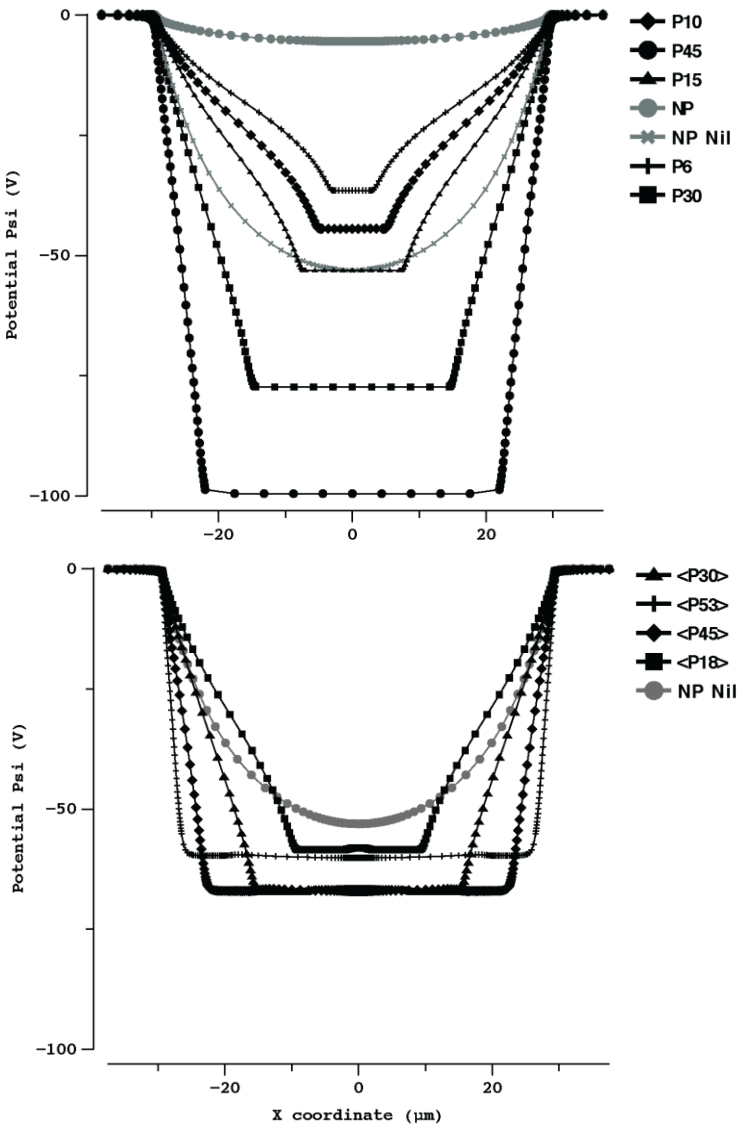




Potential is deeper than TCAD simulations

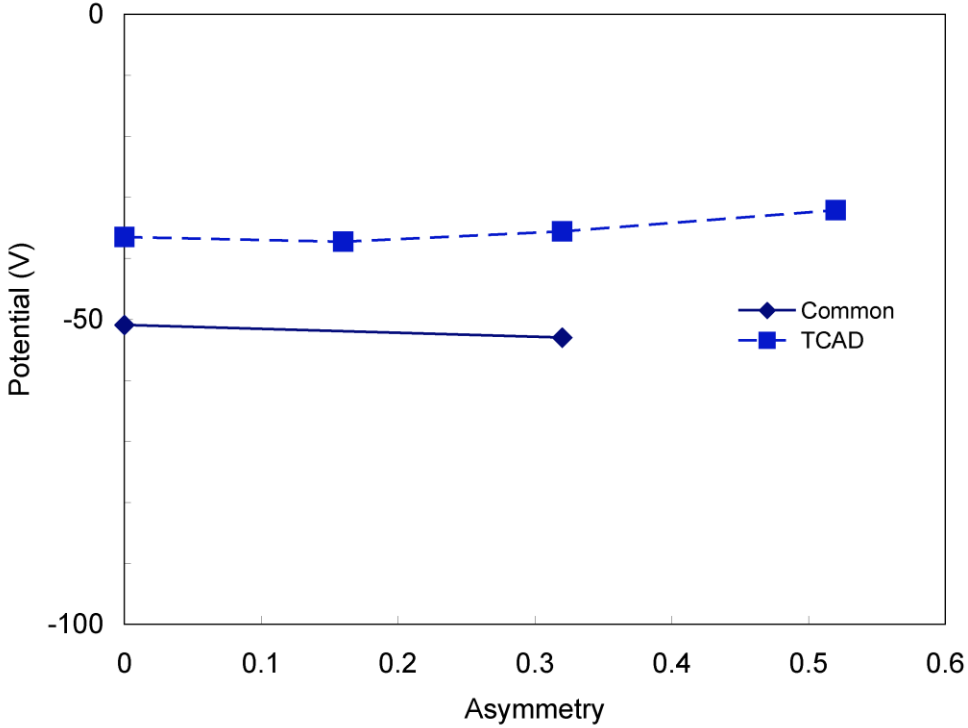
“P stop” Width Dependence

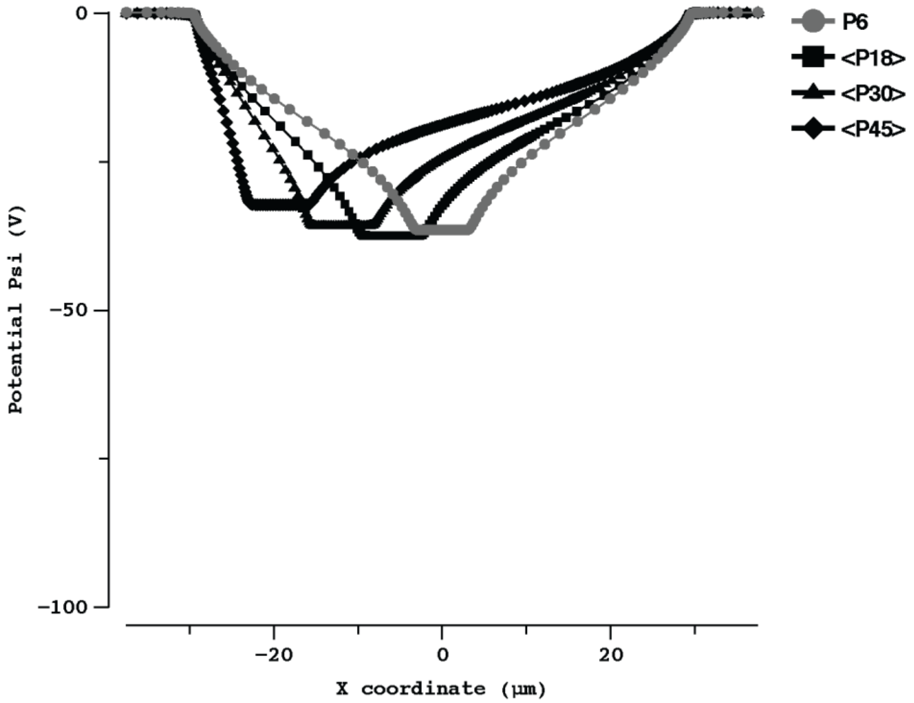




- Common vs. TCAD
  - Consistent trend
- Individual vs. TCAD
  - Potential is shallower in wider separation of p-stops
  - Dependence on Edge-to-Edge width is opposite

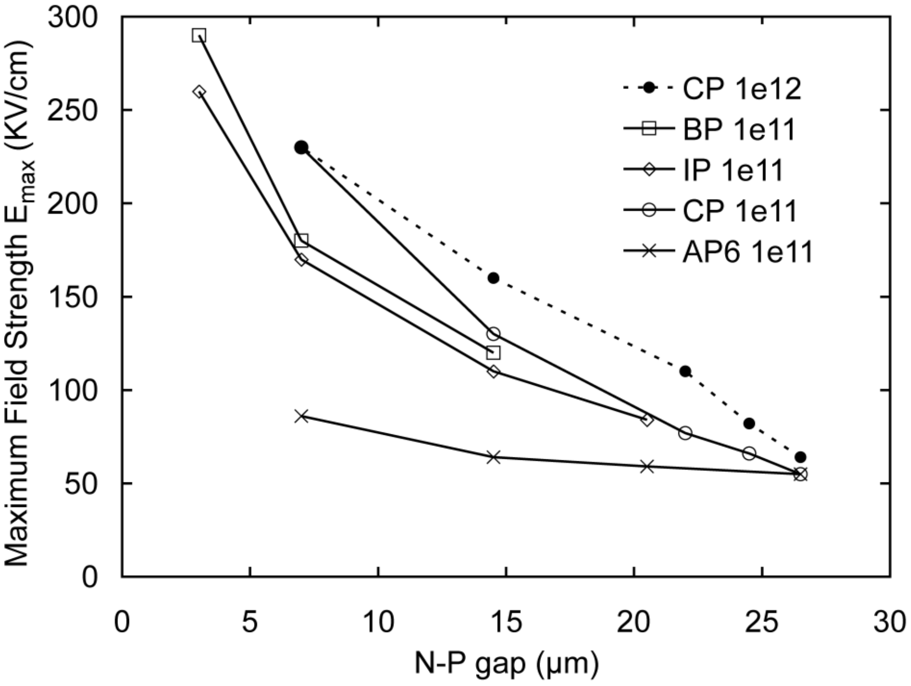
P-stop Position Asymmetry

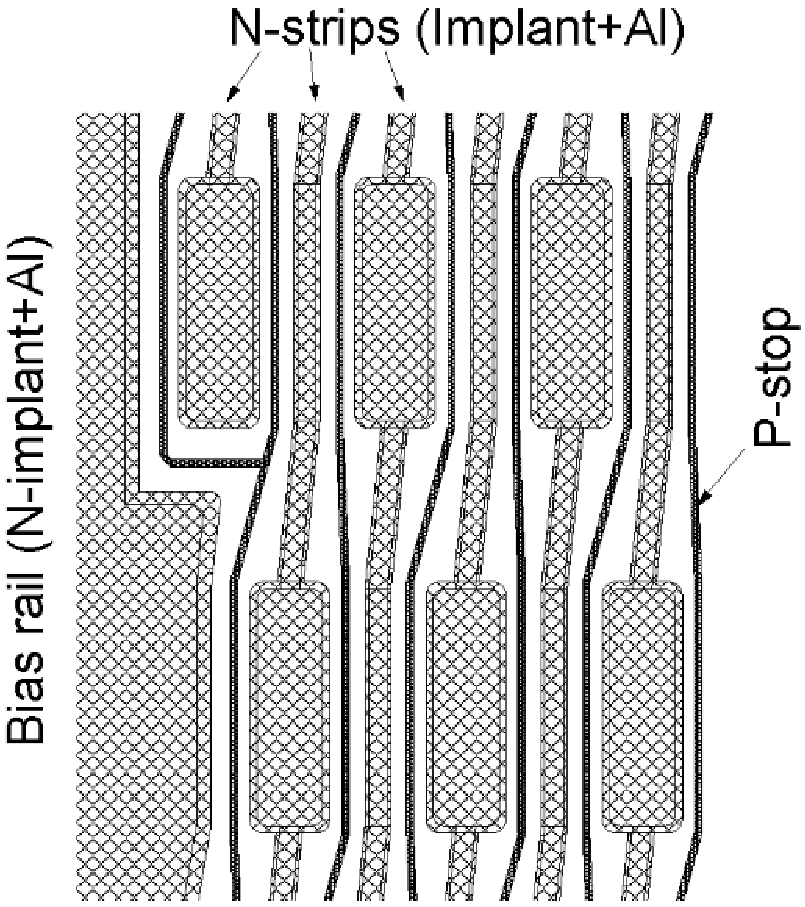




- Potential is rather insensitive to the location of the p-stop
- In optimizing the structures,
  - potential is one story
  - the critical one is the electric field
    - that is virtually impossible to measure,
  - thus TCAD helps…

Optimization of the p-stops

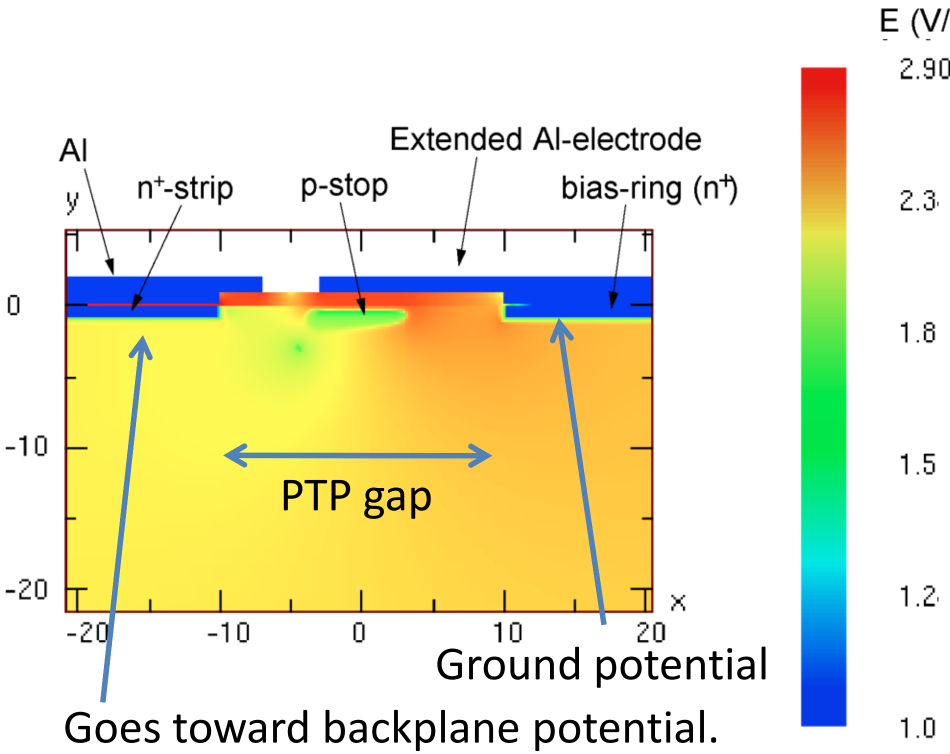




Stereo strip section

- Placement of p-stops
  - Away from the n-implant
  - Symmetrically
- N-implants
  - Narrower pitch but not too narrow
- All these are "Columbus's egg"

New PTP Structure

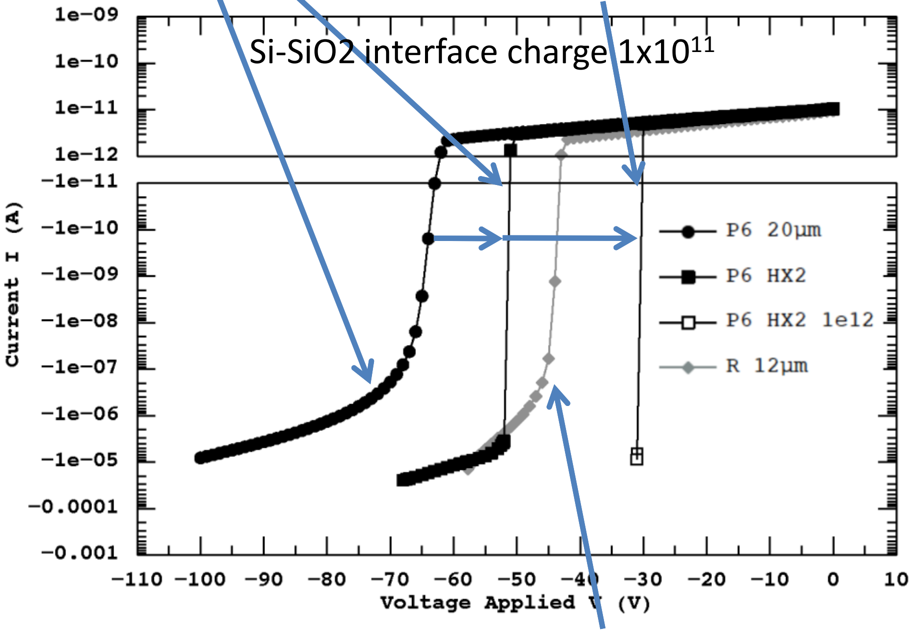


PTP gap

Ground potential

Goes toward backplane potential.

A case of -50 V, with Backplane -200 V



Without extention (gap 20 µm)

With

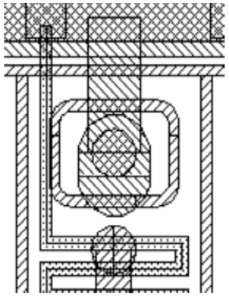
Surface charge-up 1x10^{12}

Si-SiO2 interface charge 1x10^{11}

p-spray (gap 10 µm)

- Punch-Thru-Protection (PTP)
  - keep the potential of the n-strip implant against deposition of large amount of charge to the strip
  - to protect the AC coupling insulator to break (dV < ~150 V)
- P-stop requires more space than p-spray
  - **What to do to keep the onset voltage (and saturated resistance) low?**
- A solution proposed (Y. Unno et al., Nucl. Instr. Meth. A636 (2011) S118–S124)
  - “Gated” PTP structure: the gate is an simple extension of metal (or polysilicon) over the p-stop and beyond

New PTP Test Structures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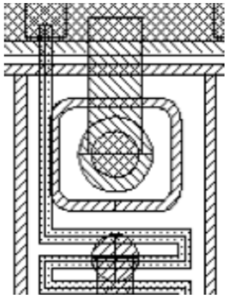
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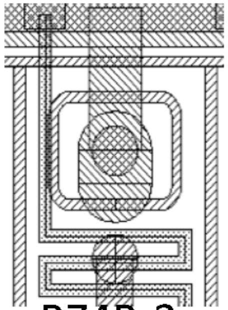
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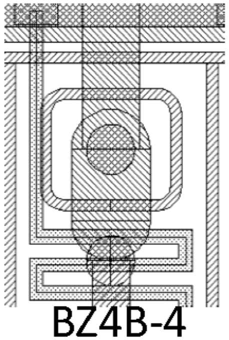
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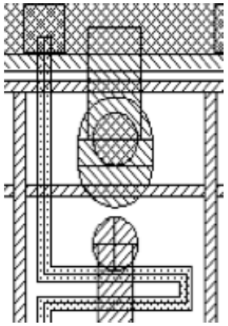
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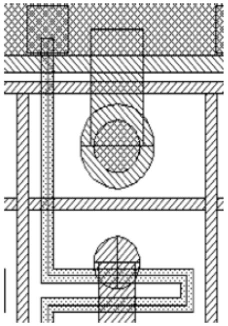
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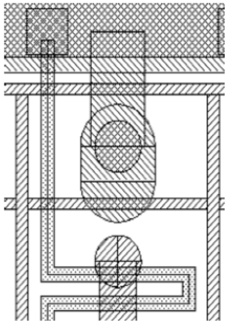
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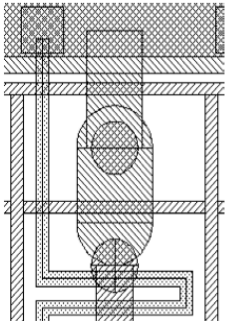
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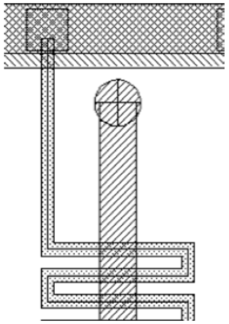
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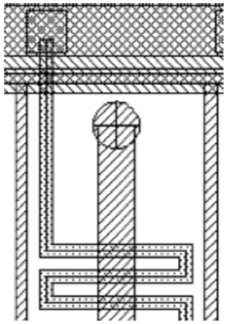
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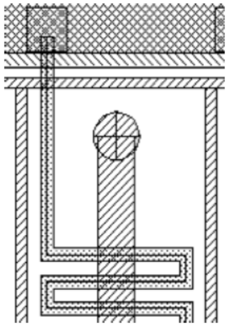
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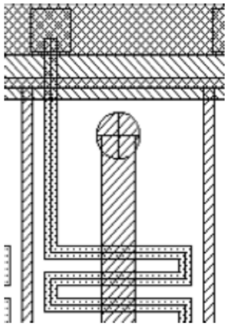
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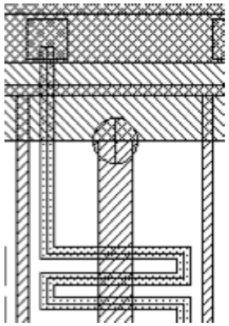
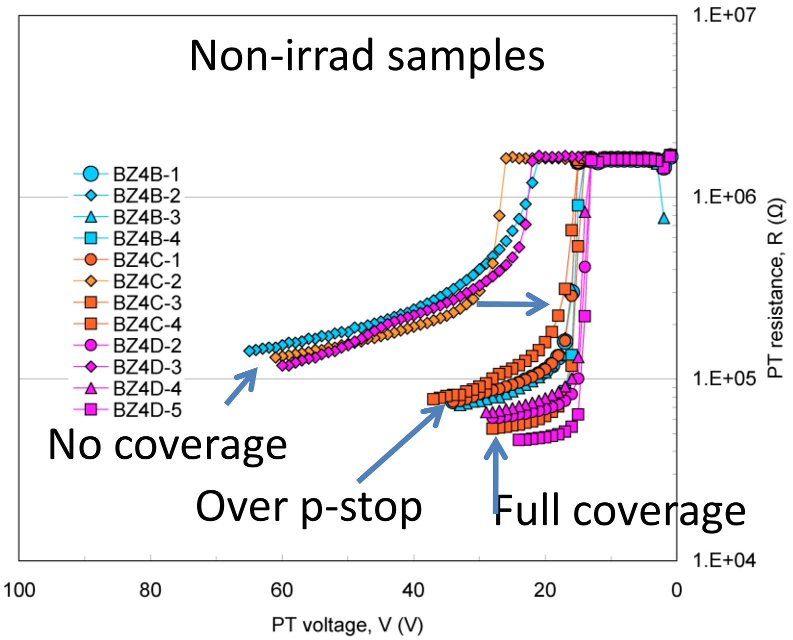
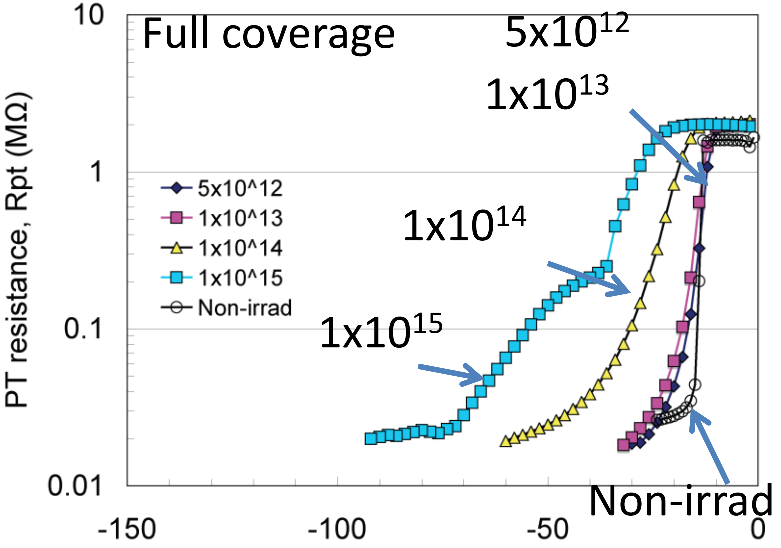

BZ4D-5

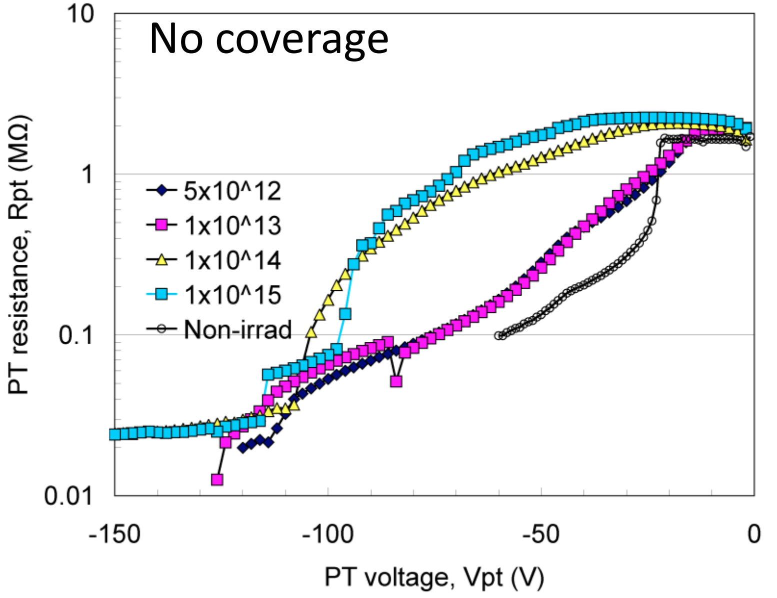
- P-stop
  - B: Atoll type
  - C: Compartment type
  - D: Simplest type
- Gate extension(*)
  - 1: Over p-stop
  - 2: No coverage
  - 3: Over p-stop-2
  - 4: Full coverage
  - (*) D type
    - 1: no p-stop
    - 2-5: = 1-4 of others

New PTP TS Irradiated



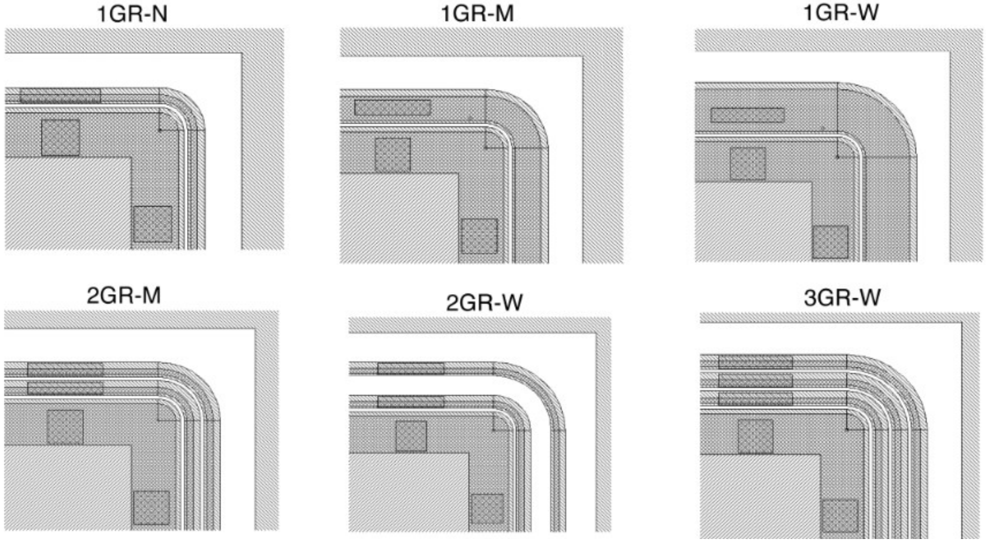
70 MeV protons at CYRIC, Japan

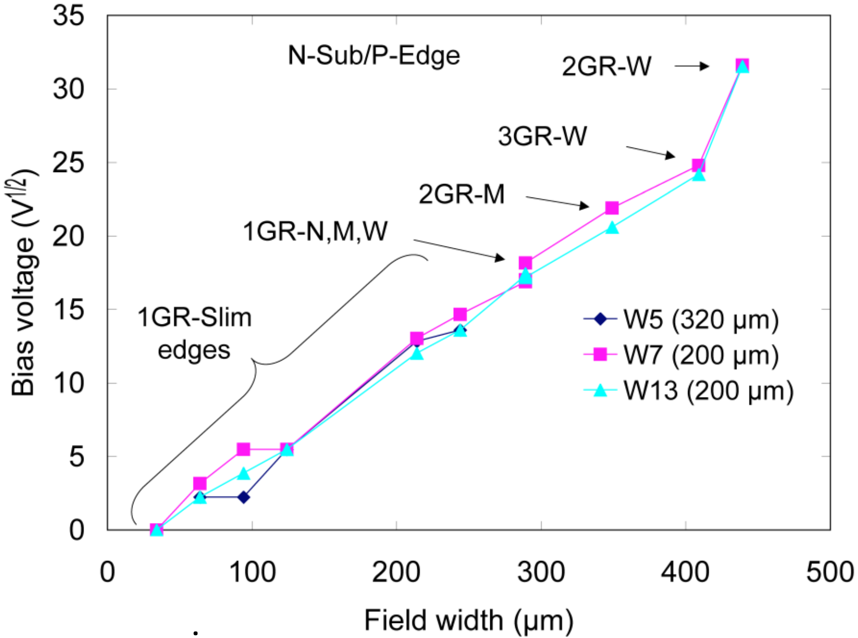


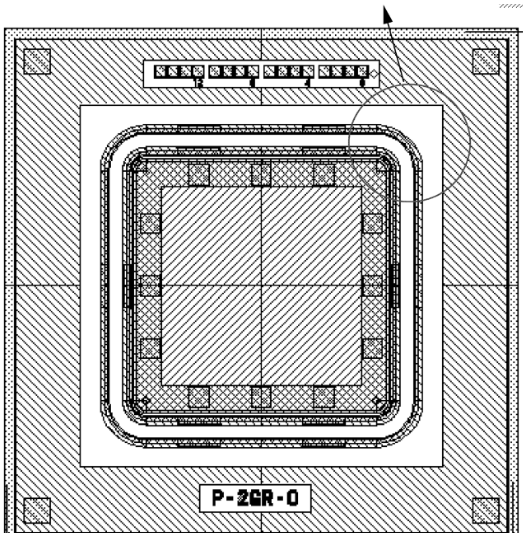


- Non-irradiated samples
  - Onset voltages ~1/2 Simulations
  - Gate effect is consistent
- Irradiated samples
  - "Full coverage" behaves well
  - Simulation with "surface charge" effect does not explain the onset and saturation behavior after irradiation
  - Electric field at the p-stop edge seems lower after irradiation, contrary to an expectation

Edge Structure for High Voltage Operation

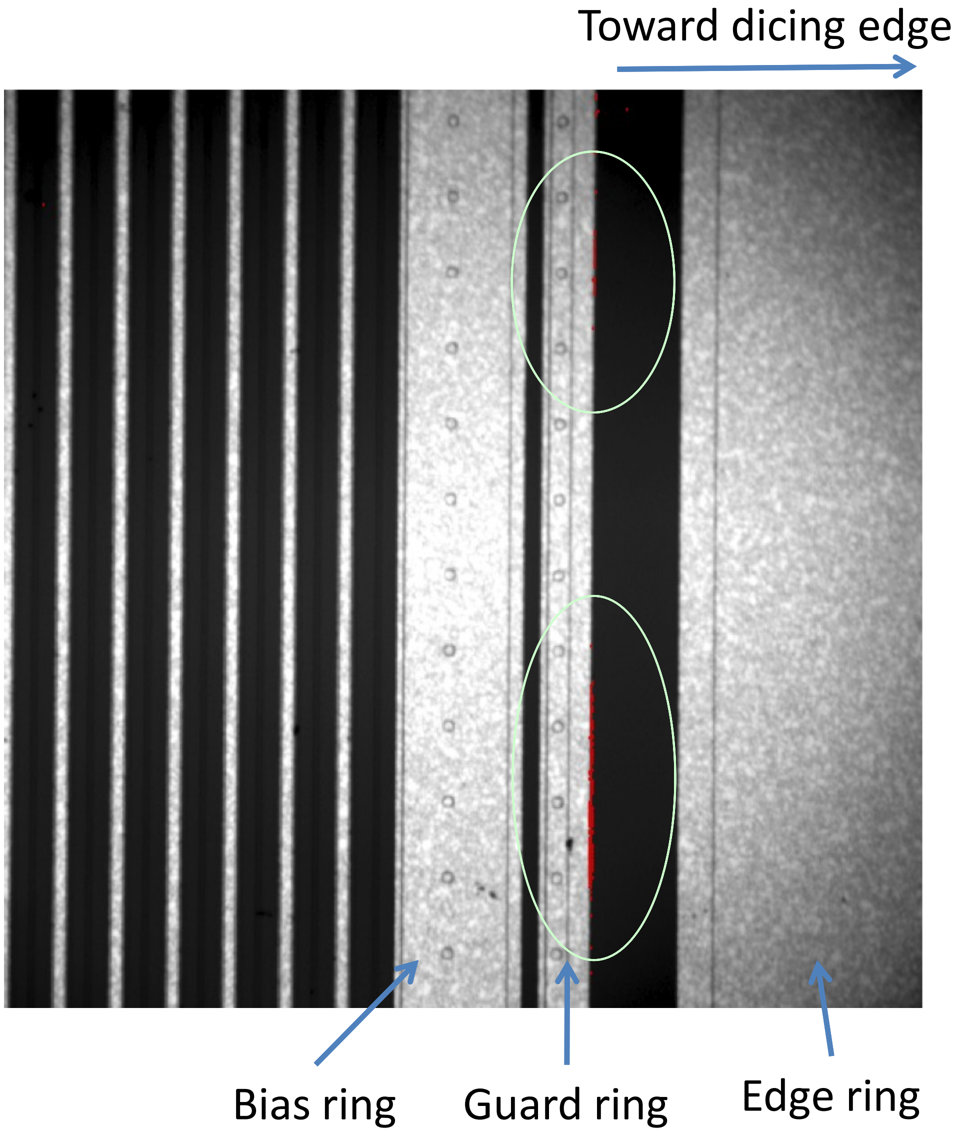






- Planar pixel and strip sensors require
  - very high voltage operation, e.g., 1000 V
  - less dead area in the edge region, e.g., ~450 µm (ATLAS IBL spec.)
- We have shown
  - onset voltage of breakdown is ~linear to $(\text{Voltage})^{1/2}$, i.e., (lateral) depletion
  - implying that the breakdown is at the dicing edge
  - for 1000 V, “field width” of ~400 µm
  - irrelevant to the number of guard rings
  - Y. Unno et al. Nucl. Instr. Meth. A(2011),doi:10.1016/j.nima.2010.12.191
- Can we simulate the breakdown? (Q1)

Another Hot Spot in the Edge

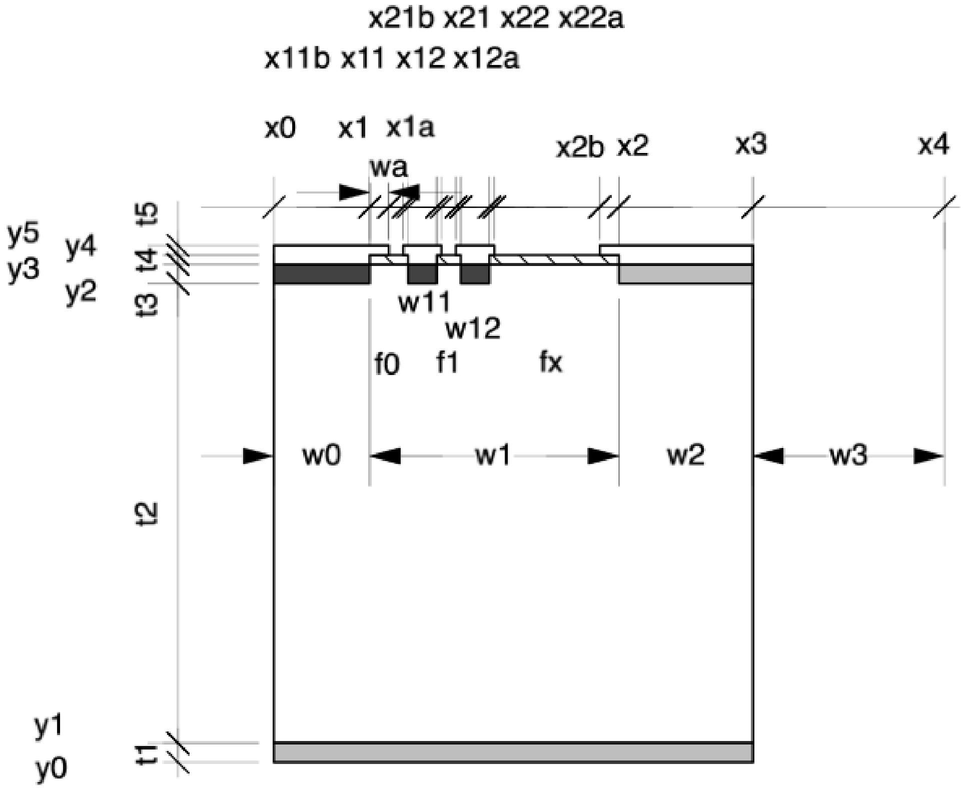


- Microdischarges
  - We have seen occasionally onset of leakage current, after handling the sensors
  - IR imaging reveals hot spots along the edge of the "Guard" ring
- Why?
  - The sensors hold up to 1000 V when delivered
  - Note the host spots are in the "guard" and not "Bias ring"
  - Post-process damage?
  - How to reinforce the edge structures against post-process damage? (Q2)

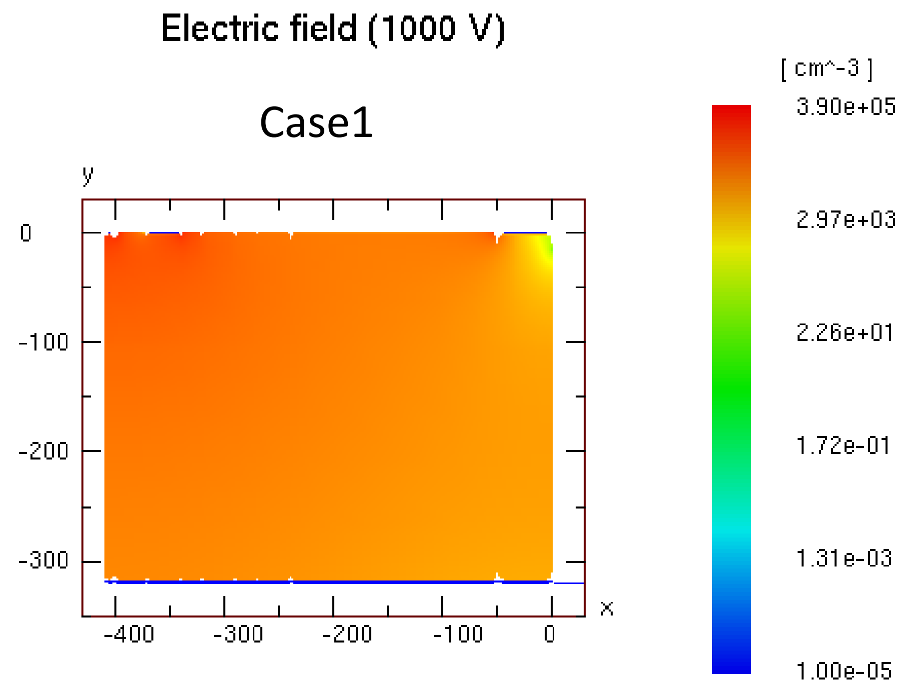
Edge Structures Simulations

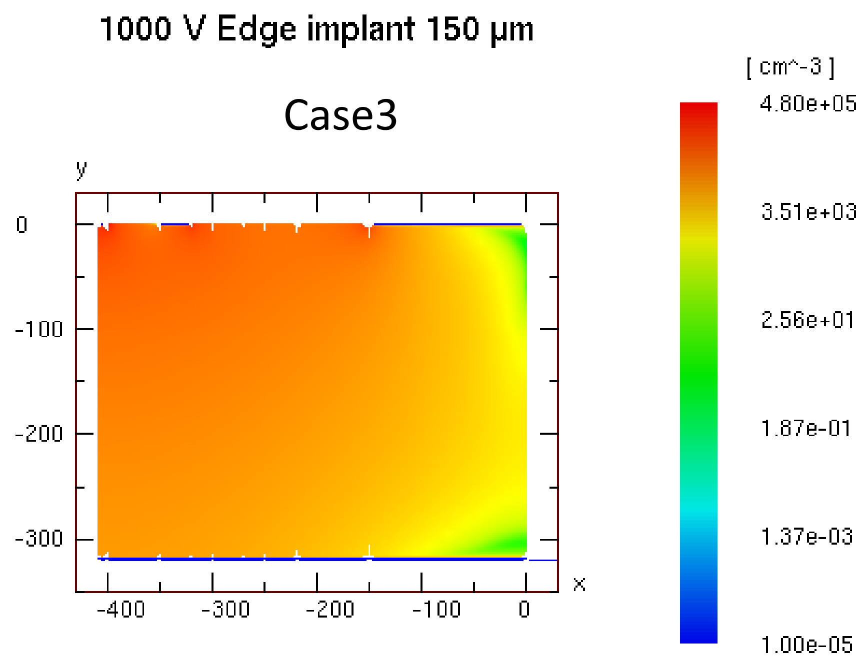
- Geometry
  - 2 guards case is shown
- Material
  - p-bulk(FDV~200 V)
  - Top-Left: bias ring (n+)
  - Top-right: edge implant (p+)
  - f0, f1, f2, …: gap between the implants

Case	w1	w2	f0	f1	f2
1	350	50	50	0	0
2	350	50	30	0	0
3	250	150	50	0	0
4	350	50	50	60	0
5	350	50	50	20	20



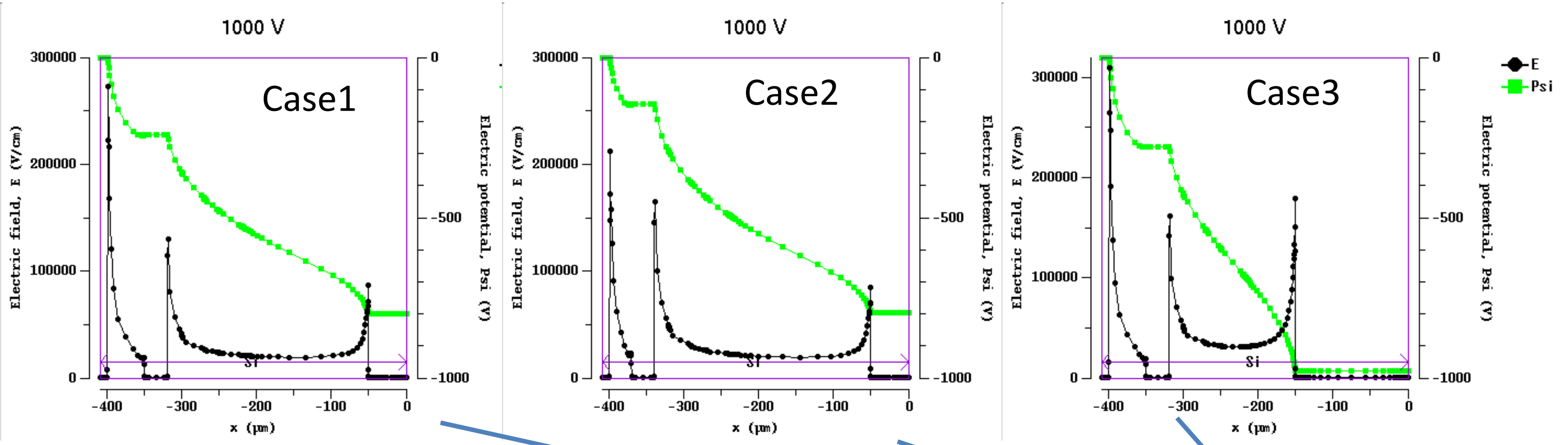
1 guard cases



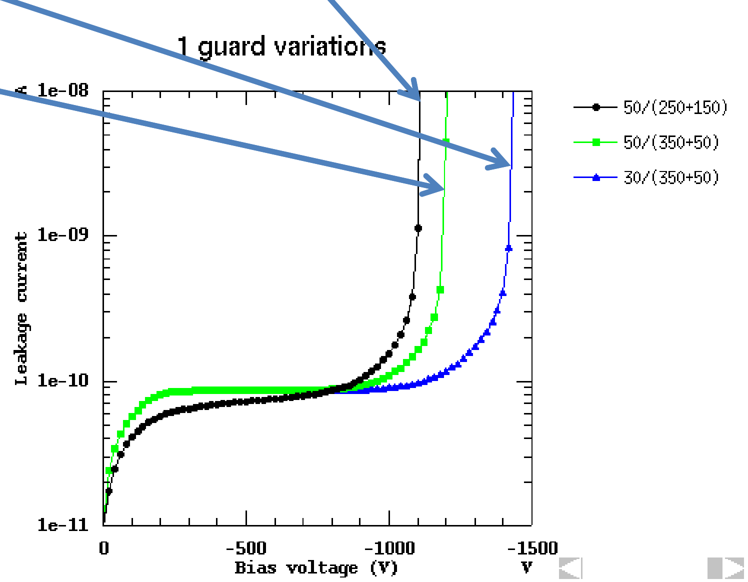


- Electric field distribution
  - at the bias voltage of 1000 V
- Case3 shows
  - low electric field along the dicing edge
    - due to the wide implantation at the edge

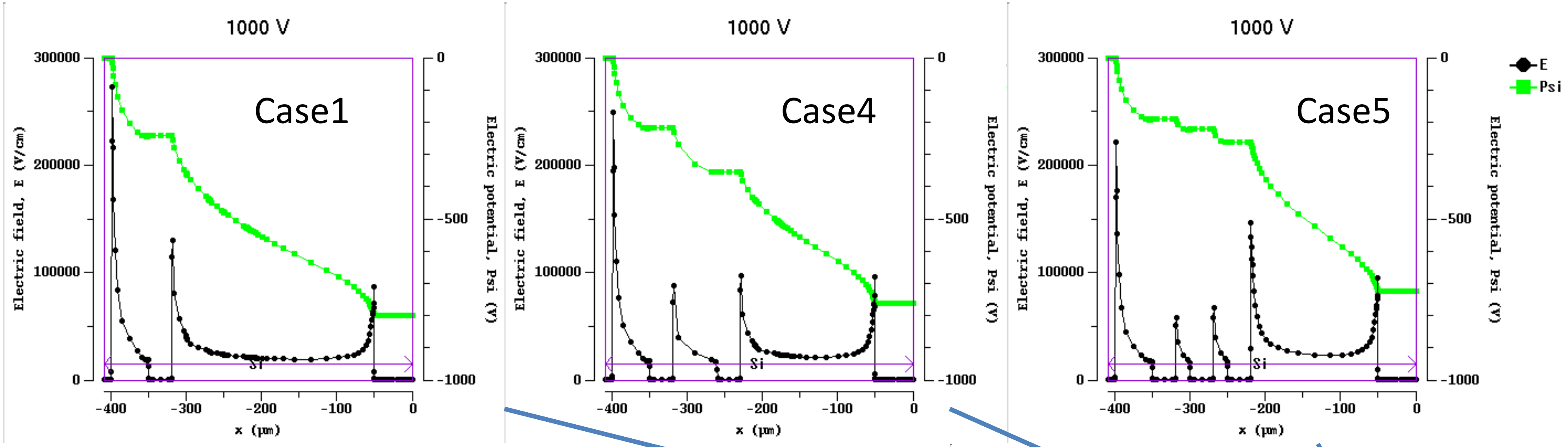
1 guard cases



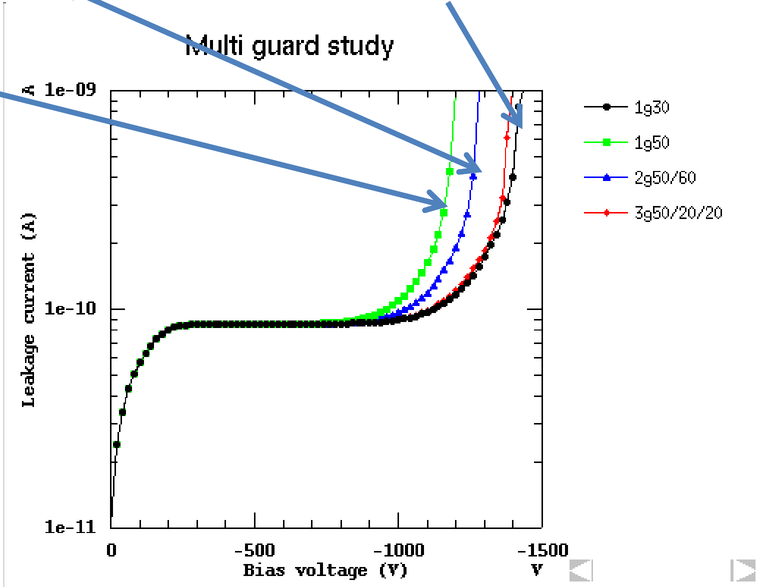
- Close guard has lower peak at the edge of bias ring
  - Accordingly, the breakdown is higher
  - However, the peak of the guard gets higher
- Narrower the edge gap the higher the peaks
- Potential of the edge implant
  - Narrow width: lifted off from the potential of the backside
  - **Wide width: Potential of the edge implant is of the backside**
- Caveat
  - **No dicing edge breakdown is simulated!!**



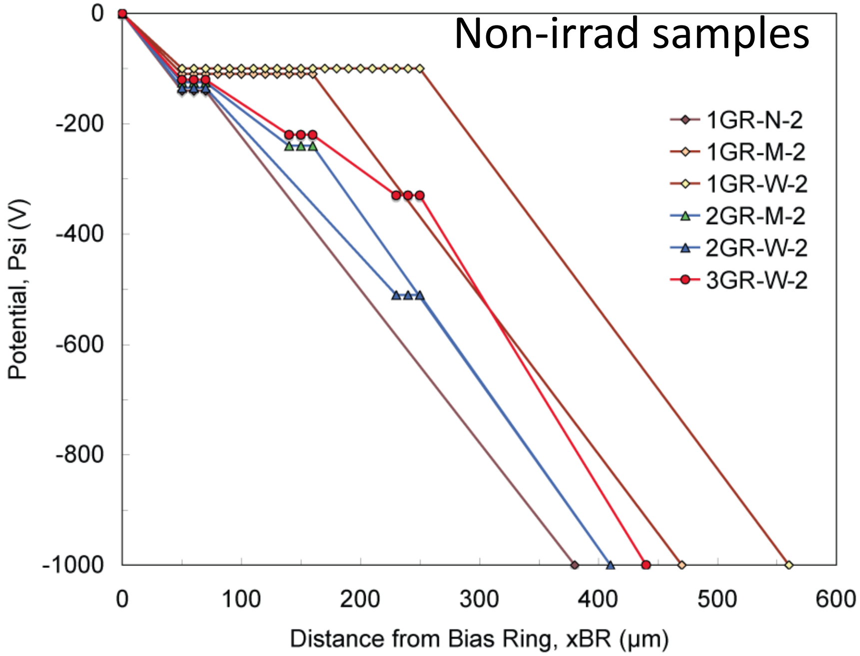
Multi-guard

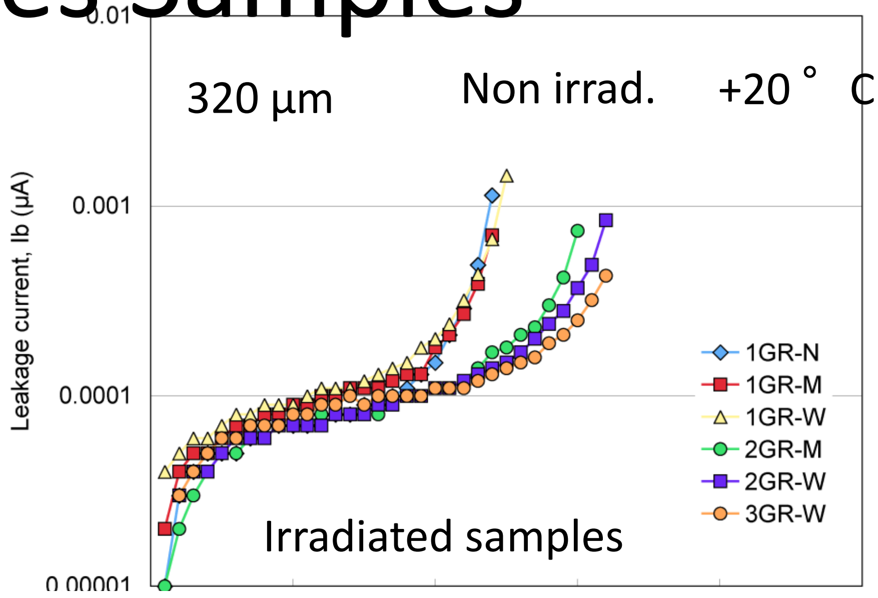


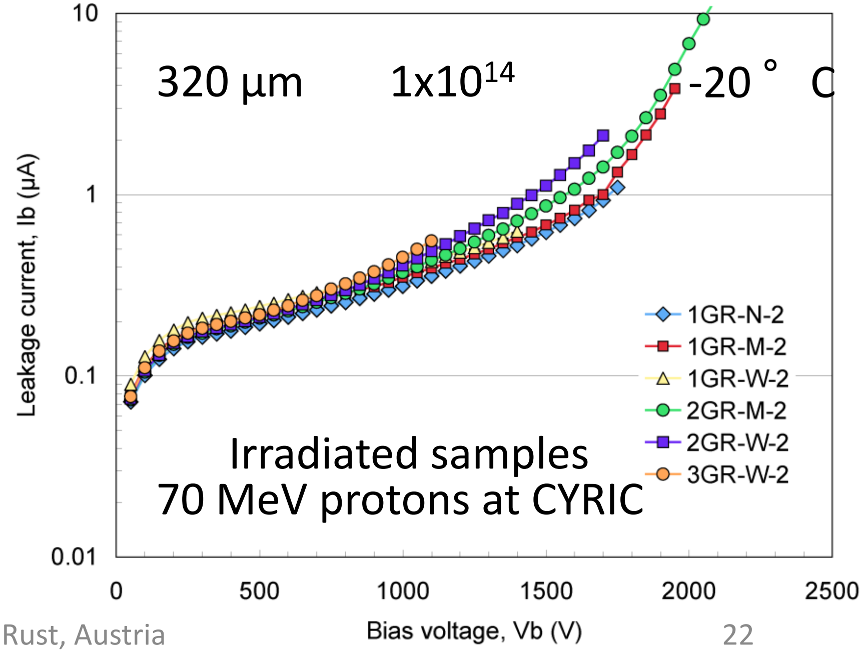
- Multiple guards
  - reduce the peak field at the edge of the bias ring
  - Accordingly the breakdown in the leakage current is getting higher
  - **Potential of the edge implant is lifted off more as the number of guards increases**
- **Q1: Can we simulate the breakdown at the dicing edge?**
  - **No, no dicing edge breakdown is simulated, at least to my knowledge**



Edge Structures Samples







- Same "Field width (350 μm)" for all samples
- Potential of guard rings
  - Consistent with simulations although some discrepancies
    - e.g. potential of 1st guard is shallower than simulation
- Breakdown voltages
  - Non-irrad: 1GR < 2GR ≤ 3GR
  - Irrad (e.g. 1014): 3GR ≤ 2GR ≤ 1GR
  - Trend of Non-irrad. and Irrad. is opposite…

Optimized Edge Structure?

- Q2: How to reinforce the edge structures against post-process damage?
- Answer?
  - Firstly, wider "field width", then secondly,
  - 2-guards seems to be a solution, especially for non-irradiated
    - Details of the 2nd guard have to be decided
  - Once irradiated (to high fluences), little difference in number of guards
- Why not more than 2?
  - We have preferred less guards as long as it is enough because
    - primarily, less edge area
    - others, e.g. no difference after irradiation
    - …

Summary

- TCAD is a great tool
  - For non-process user, Device simulation is the one to use.
  - Finite element method + Semiconductor Physics
  - Simple to use, but
  - Off the paved road (i.e., default values), it is “woods”.
    - Many parameters for many semiconductor physics
    - Computational issues
      - Meshing, convergence, …
  - Limited to the known processes
    - No dicing edge effect (?)
    - No irradiated surface effect (?)
    - “You get what you put” situation
- We have used TCAD for guiding the optimization of the issues associated for very high voltage operation,
  - Comparing with test structure measurements as much as possible.

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