Development and Applications of the Timepix3 chip

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Vertex2011, Rust, Austria.

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Outline

- Medipix / Timepix family of pixel detectors
- Timepix3 : functionality and features
- Design and performance of some basic circuits
- Summary

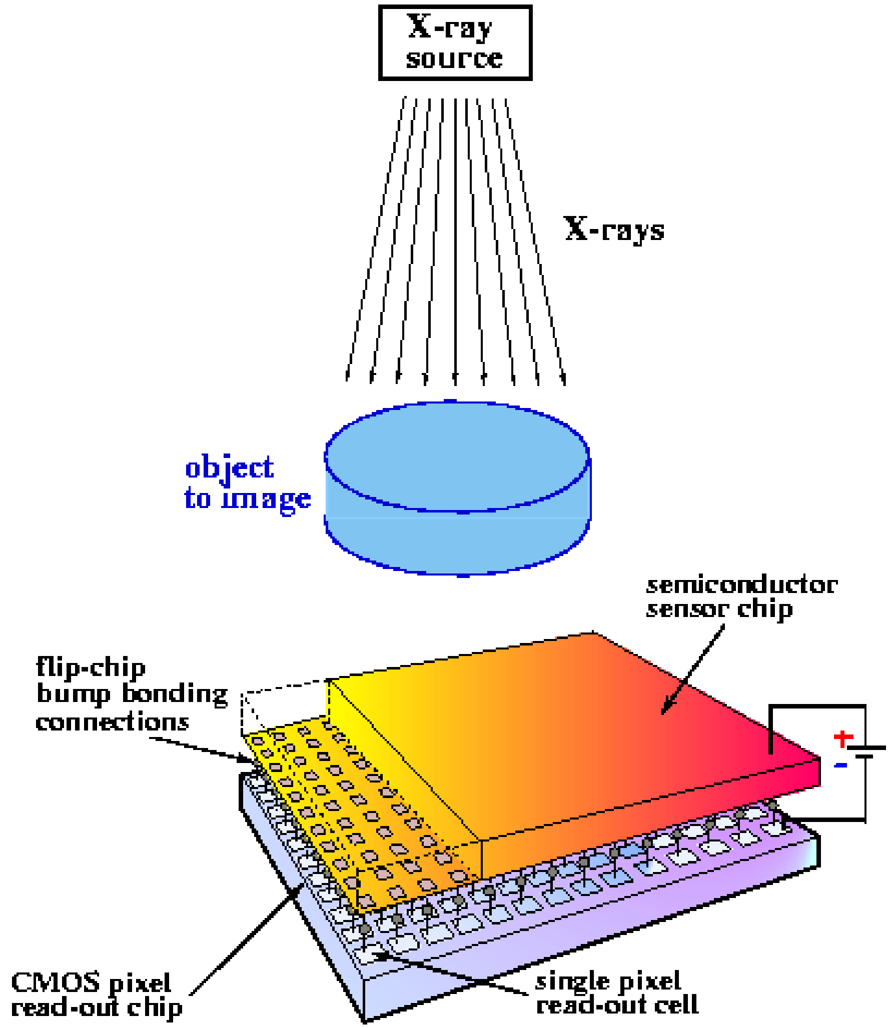
Medipix detectors

- ❑ **Photon (X-ray) counting hybrid pixel detector**
- ❑ **Imaging / medical applications**

1997: Medipix1 (CERN)
- technology: 1µm CMOS
- array: 64 x 64
- pixel: 170 um x 170 um

2001-2005: Medipix2 (CERN)
- technology: 0.25µm CMOS, 6-metal
- array: 256 x 256
- pixel: 55 um x 55 um
- energy resolved photon counting

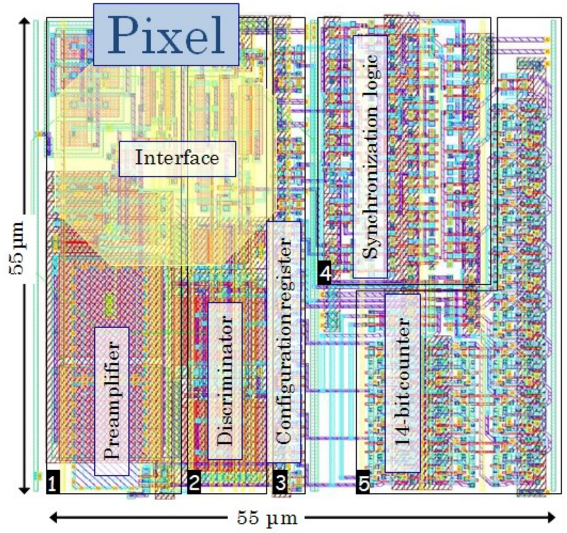
2009: Medipix3 (CERN)
- technology: 0.13µm CMOS, 8-metal
- array: 256 x 256
- pixel: 55 um x 55 um
- charge summing mode
- improved energy resolution



Timepix pixel readout chip

- ❑ **TPC / micro-pattern gas detectors applications**
- ❑ **measures hit arrival time *OR* energy deposit on each pixel**

2007: Timepix (CERN)
- external clock : 100 MHz
- full frame readout : serial port (10ms/frame)



Limitations
- any event readout requires full frame
- no zero suppression
- dead time (no continuous readout)
- time resolution is only 10ns (bin size)
- slow front-end (time-walk ~120ns)

Timepix3 project: design goals and current status

Timepix3 is an approved project of the Medipix3 collaboration with an assigned budget (2-engineering runs in 2012, 130nm CMOS)

- **wide range of non-HEP applications:**
  - **X-ray imaging**
  - **Dosimetry**
  - **Compton camera, gamma polarization camera, fast neutron camera, nuclear fission, astrophysics …**

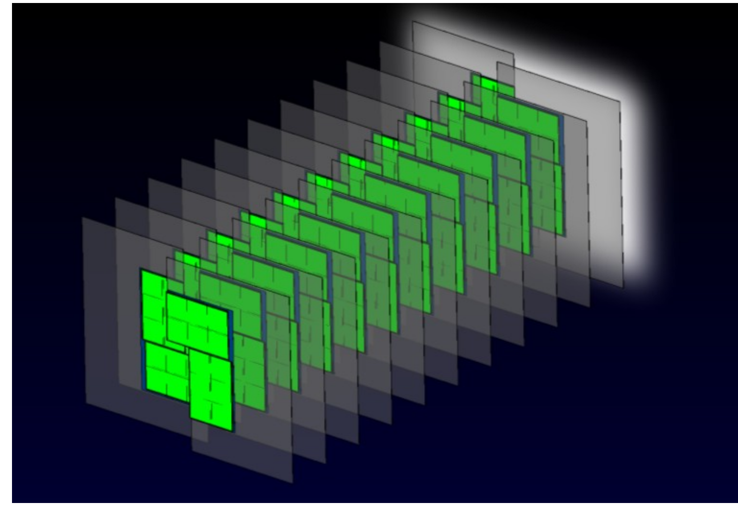
- **time-resolved imaging**
- **hit (photon) → ToA & ToT**
- **continuous & sparse readout**
- **minimum dead time**

- **suitable for HEP applications**

Required readout chips for the HEP applications

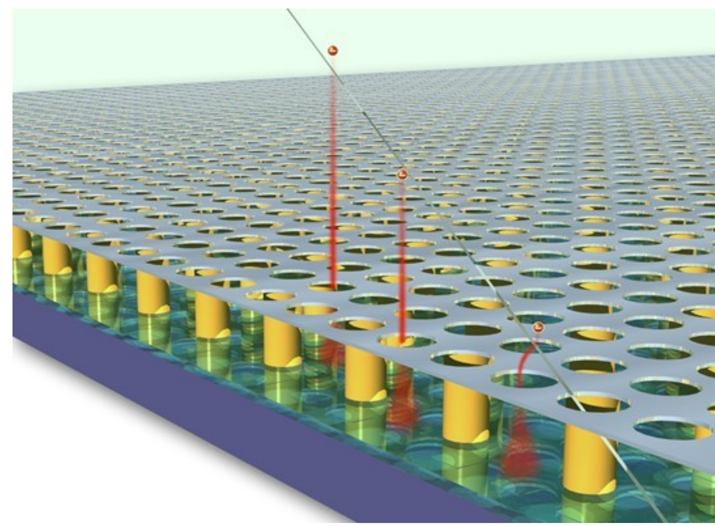
❑ Upgrade of the LHCb VELO detector: VELOPIX

- minimum pixel size
- extremely high illumination:
  up to 290 Mhits/cm^2/s
- continuous data readout
- sparse data (zero suppression)
- charge measurement



❑ Micro-pattern gas avalanche detectors: GOSSIP, TPC etc.

- minimum pixel size
- high time resolution: ~ 1ns
- wide dynamic range : ~ 100µs
- charge measurement
- high sensitivity : threshold ≈ 350e$^-$



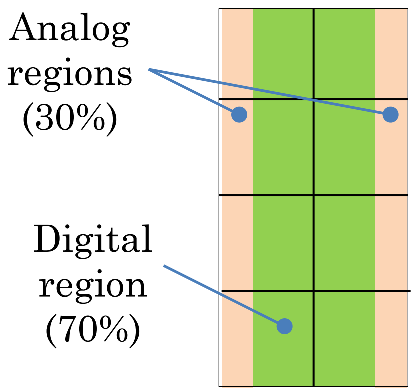
Timepix3: main features

Feature	Value
technology	130nm CMOS
pixel array	256 x 256
pixel size	55µm x 55µm
input charge	both : h^+ and e^-
sensor leakage current compensation	Yes
data acquisition	ToA &ToT / only ToA / Event count & Integral ToT
minimum threshold	> 500 e^- (1.8keV)
peaking time	~ 15ns
time walk (charge collection time)	< 25ns
Time resolution / range	1.6nsec / 410µsec
ToT accuracy / range	25ns / 25.6 µsec (~150 Ke^-)
readout	Continuous sparse / Non-continuous sparse
output bandwidth	2.56Gbps
count rate	up to $20 \bullet 10^6$ cm^{-2} sec^{-1}
data transmission	Conventional (separate Clock) / Clock&Data Encoded8b/10b
Power consumption	~ 20µW/pixel (1.3W/chip)

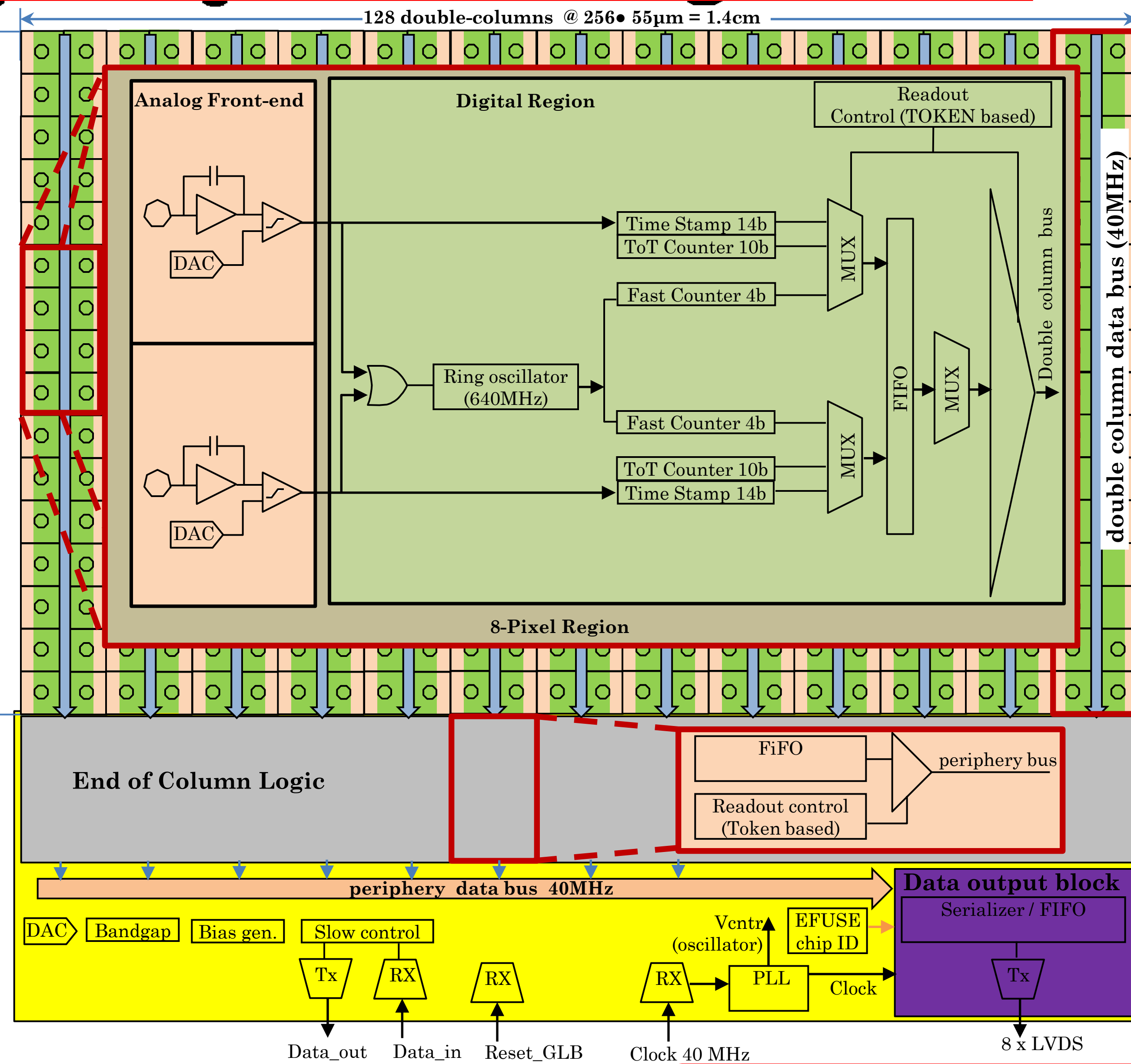
Timepix3: top level block diagram

pixel: 55μm x 55μm

- Super Pixel: 8pixels @ 4 x 2



- 64 Super Pixels in a DC
- 128 Double Columns (DC)
- Super Pixel FIFO : 2-events
- DC bus: 40MHz
- End-of-DC FIFO: 4-events
- Periphery bus: 40MHz @ 44b
- Output Serializer / FIFO

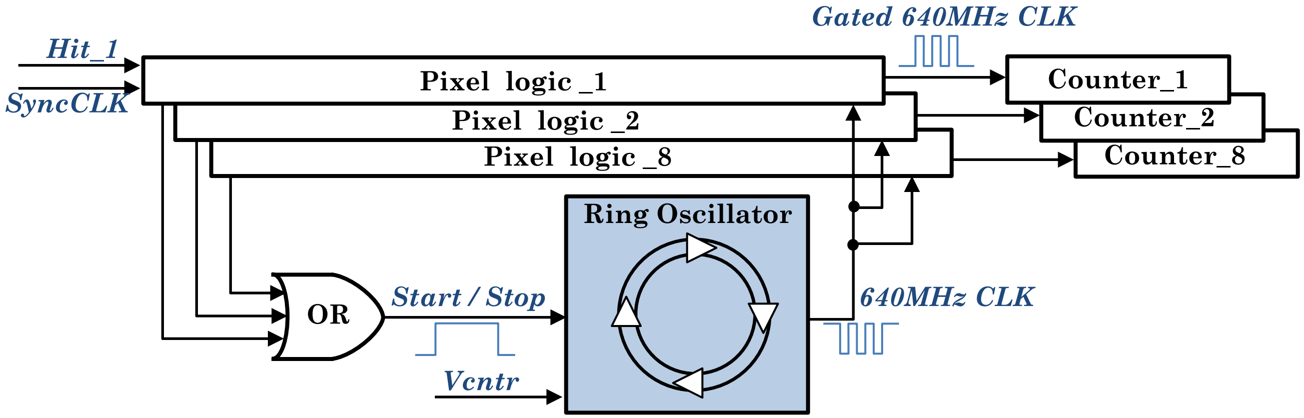


Timepix3: modes of operation

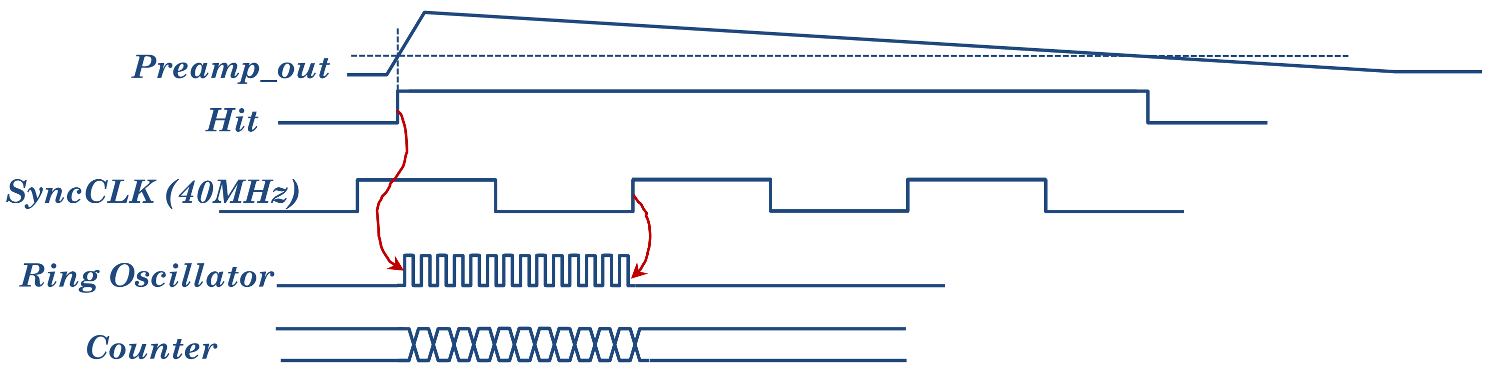
	Data acquisition mode		
	ToA & ToT	Only ToA	Event Count & Integral ToT
Data format	Fast Time (640MHz @ 4b) & Slow Time Stamp (40MHz @ 14b) & ToT (40MHz @10b) & Pixel coordinate (16b)	Fast Time (640MHz @ 4b) & Slow Time Stamp (40MHz @ 14b) & Pixel coordinate (16b)	Event Count(10b) & Integral ToT (14b) & Pixel coordinate (16b)
Double hit resolution (per pixel)	ToT + 700ns	> 450ns	-
Readout	**continuous** sparse data readout with zero-suppression		**non-continuous** sparse data readout with zero-suppression
	Max counting rate < 1kHz/pixel		Max counting rate < 100kHz/pixel
Full chip readout time	-		1.6msec

High resolution TDC

Shared Ring Oscillator architecture (per Super Pixel)

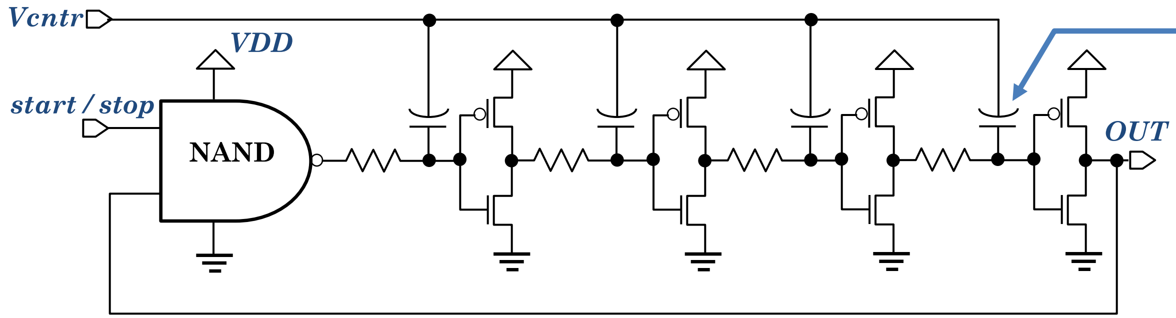


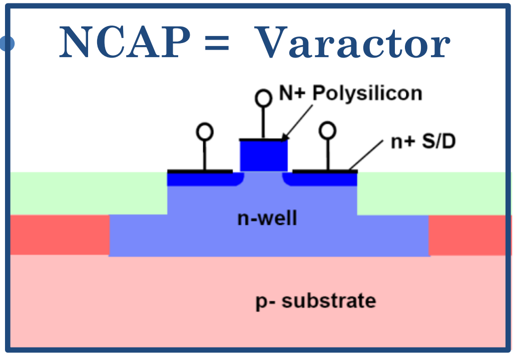
Time diagrams



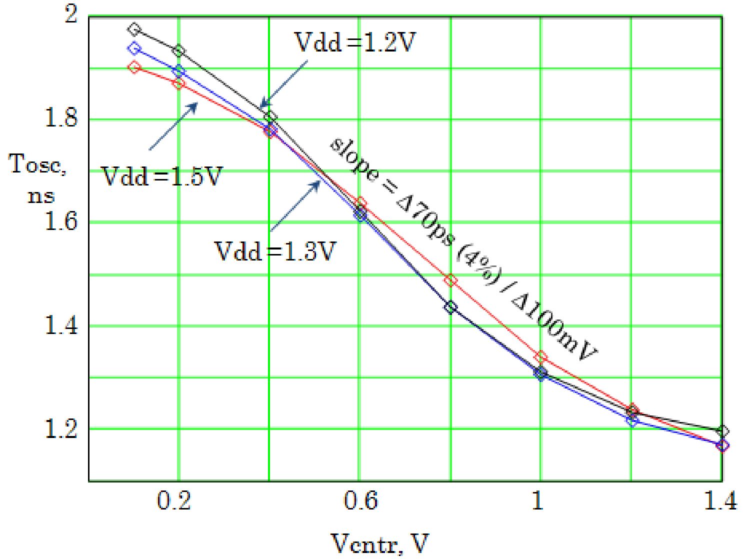
- low switching activity ~10^{-5}
- negligible power consumption
- compact design (~10% of the pixel area)

RC Ring Oscillator

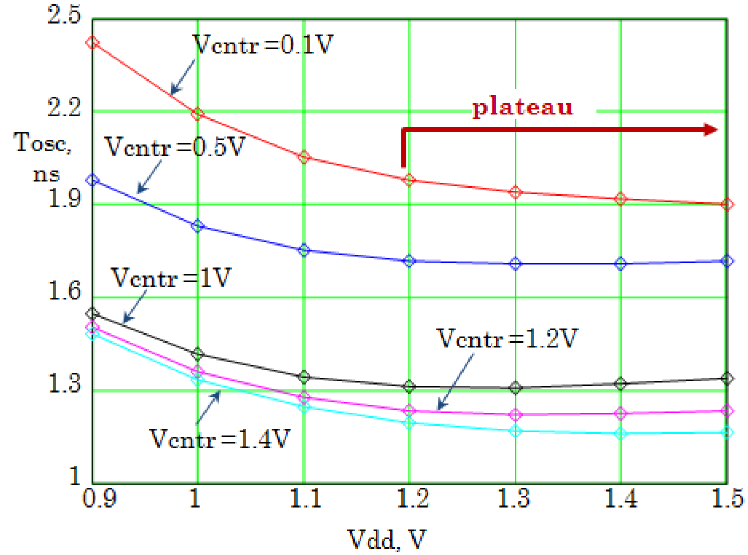




Control characteristic



Effect of the power supply voltage

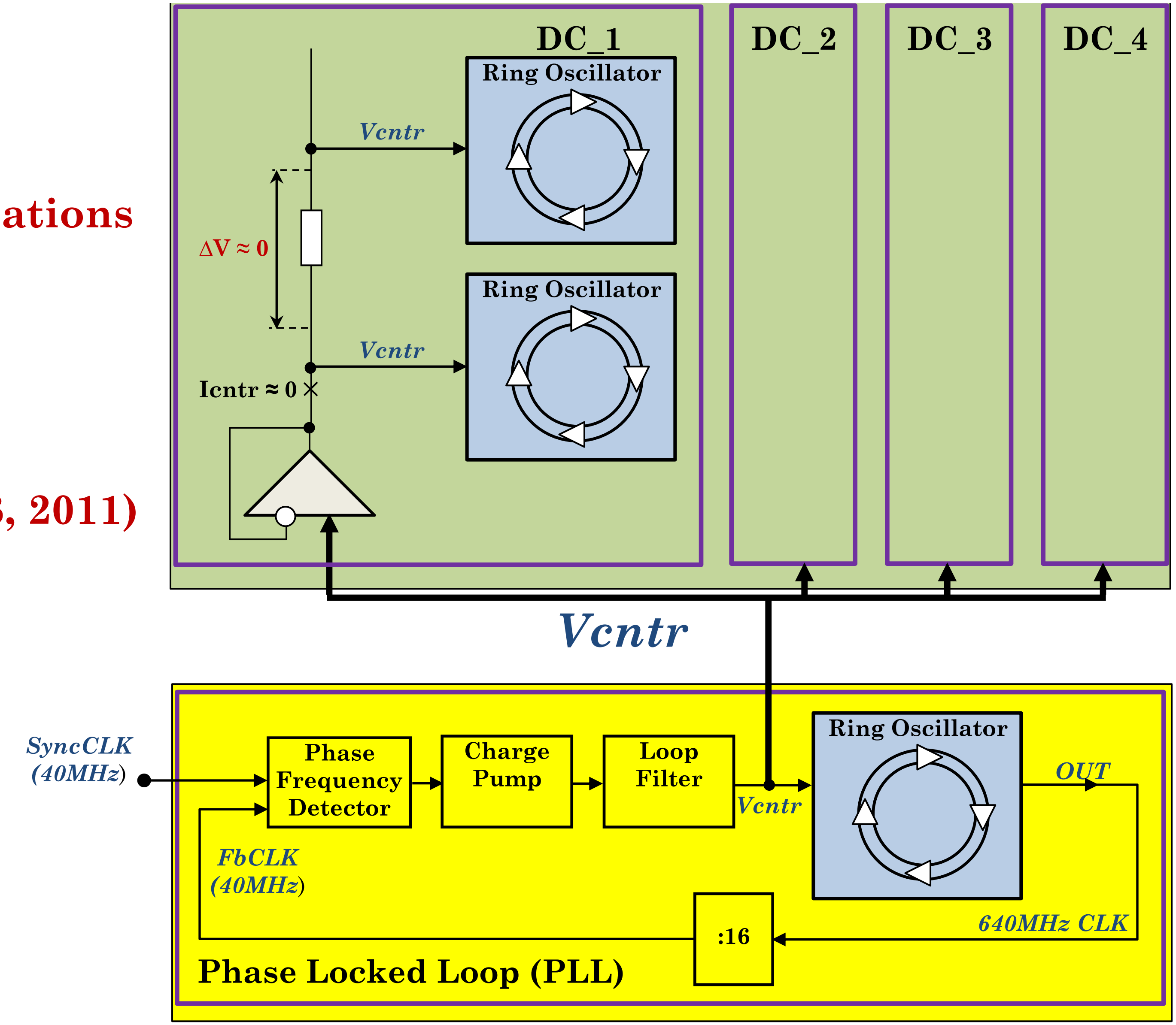


- voltage-controlled
- low sensitivity to the power supply
- channel-to-channel mismatch ~1%

TDC's array with a PLL control

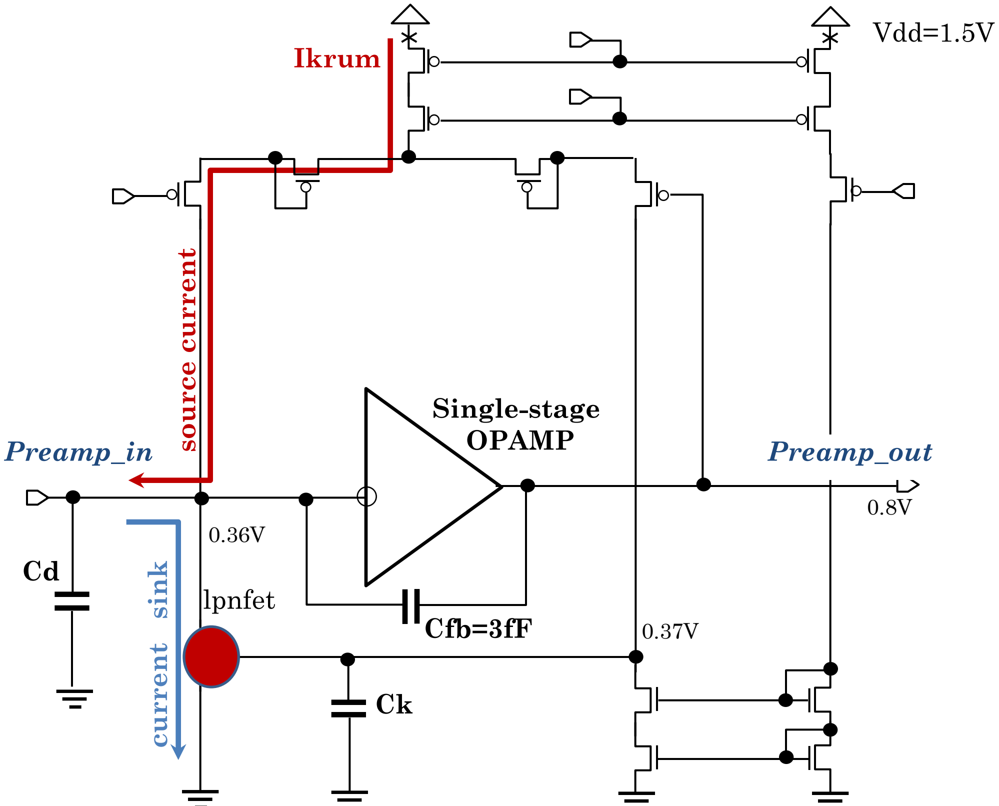
Features

- immunity to variations
- good uniformity
- Gossipo-4 (Aug 8, 2011)

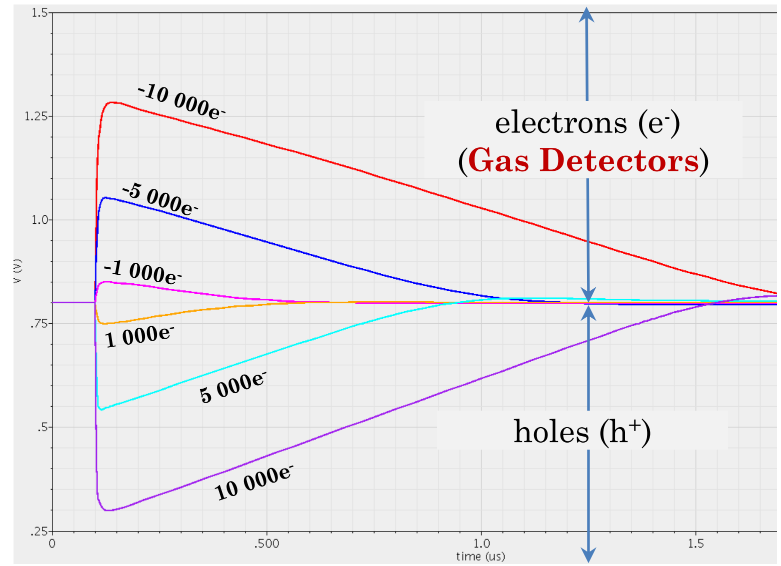


Charge sensitive preamplifier

- ❑ based on Krummenacher scheme
- ❑ both input signal polarities (h^+ and e^-)



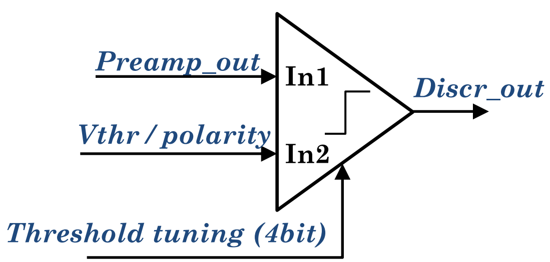
Preamp_out signals



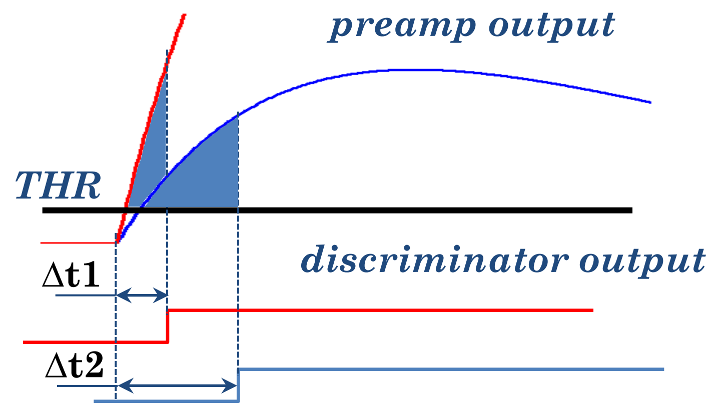
- ➢ high gain (50mV / 1ke$^-$)
- ➢ minimum time-walk (peaking time ~ 10ns)
- ➢ low noise ($\sigma \approx 75e^-$ @ Cd=25fF)
- ➢ power 4.5µW (3µA @ 1.5V)

Pulse height discriminator

- ❑ threshold tuning per pixel (4bit)
- ❑ fast response

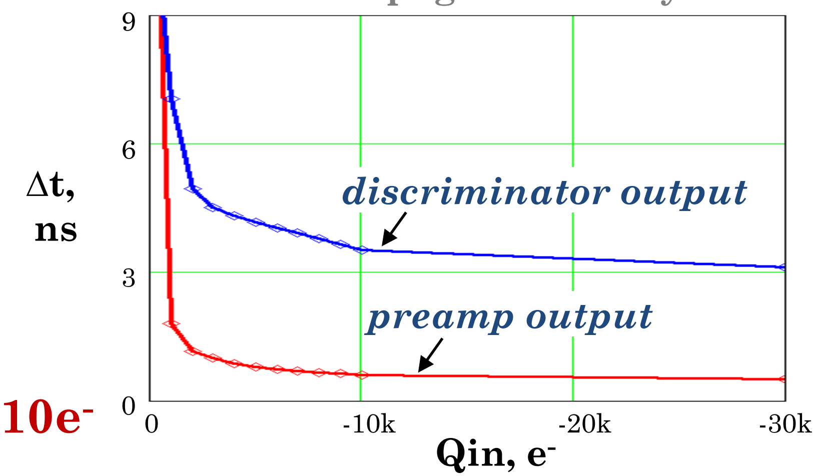


Time diagrams



- ➢ power ≈ 6μW (4μA @ 1.5V)
- ➢ internal delay ≈ 3ns
- ➢ threshold mismatch ≈ 150e$^-$
- ➢ threshold mismatch (with tuning) ≈ 10e$^-$

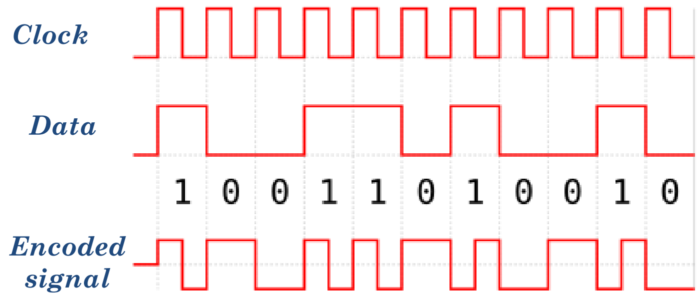
Propagation delay



Readout of the chip

Conventional readout link

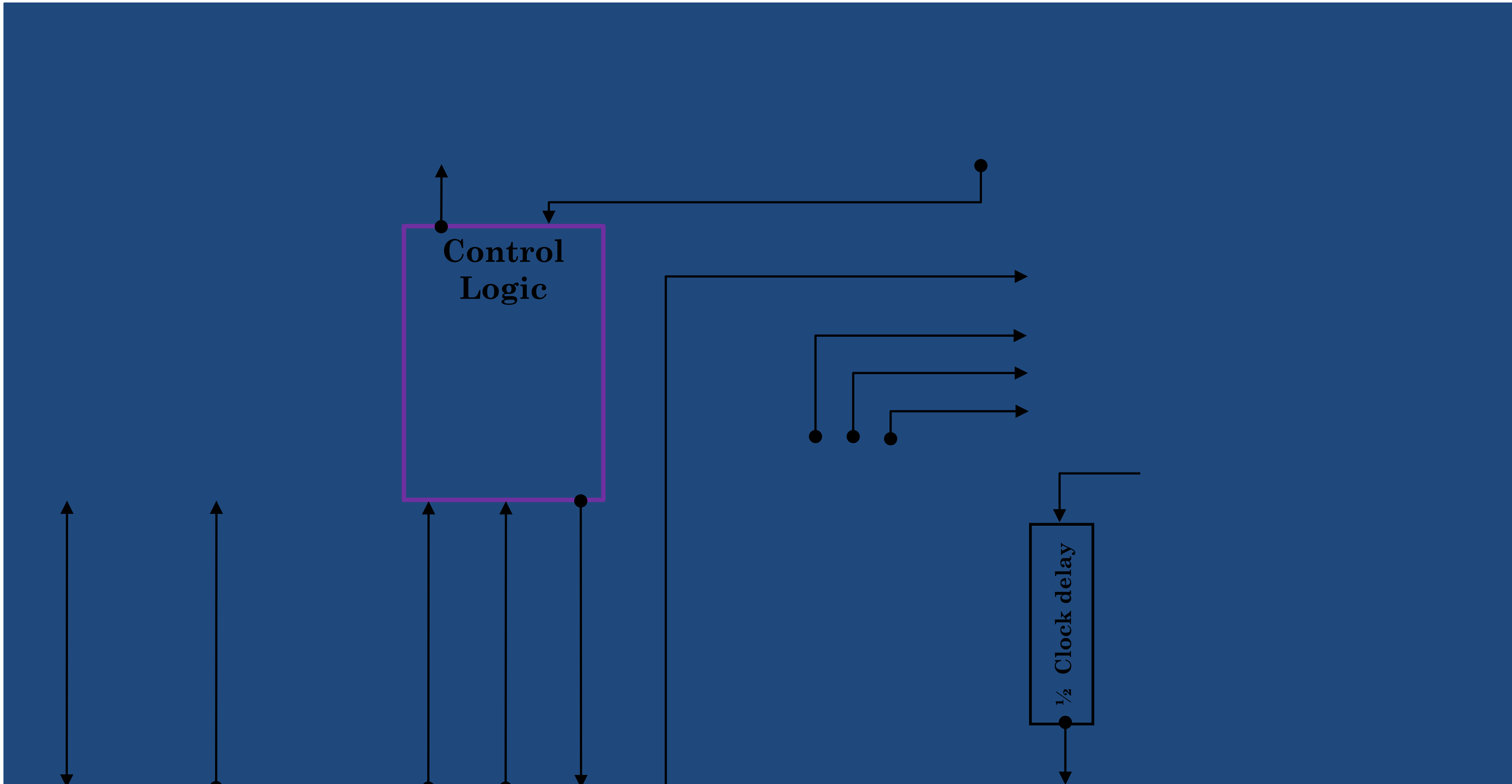
Embedded clock readout link



- data bus and clock bus are separate
- synchronization loss at high rate

- 8b/10b encoding: 8b-word by 10b symbol
- continuous activity for clock recovery
- NO clock/data skew and synchronization issues
- disparity correction (between 1's and 0's)
- DC balance control
- data alignment

Timepix3: interface part



- Two modes of operation :
  - encoded Clock – Data output (at 640 MHz)
  - separate Clock and Data outputs (at 320MHz, 160MHz ….)
- selectable readout speed

Summary

- **Timepix3 pixel readout chip is being developed in the frame of the Medipix3 collaboration for a wide range of applications**

- **the chip is defined as a 256 by 256 pixel array (~2cm^2) where each pixel measures 55µm by 55µm**

- **for each hit both time-of-arrival will be measured with 1.6ns accuracy as well as charge deposit (time-over-threshold method)**

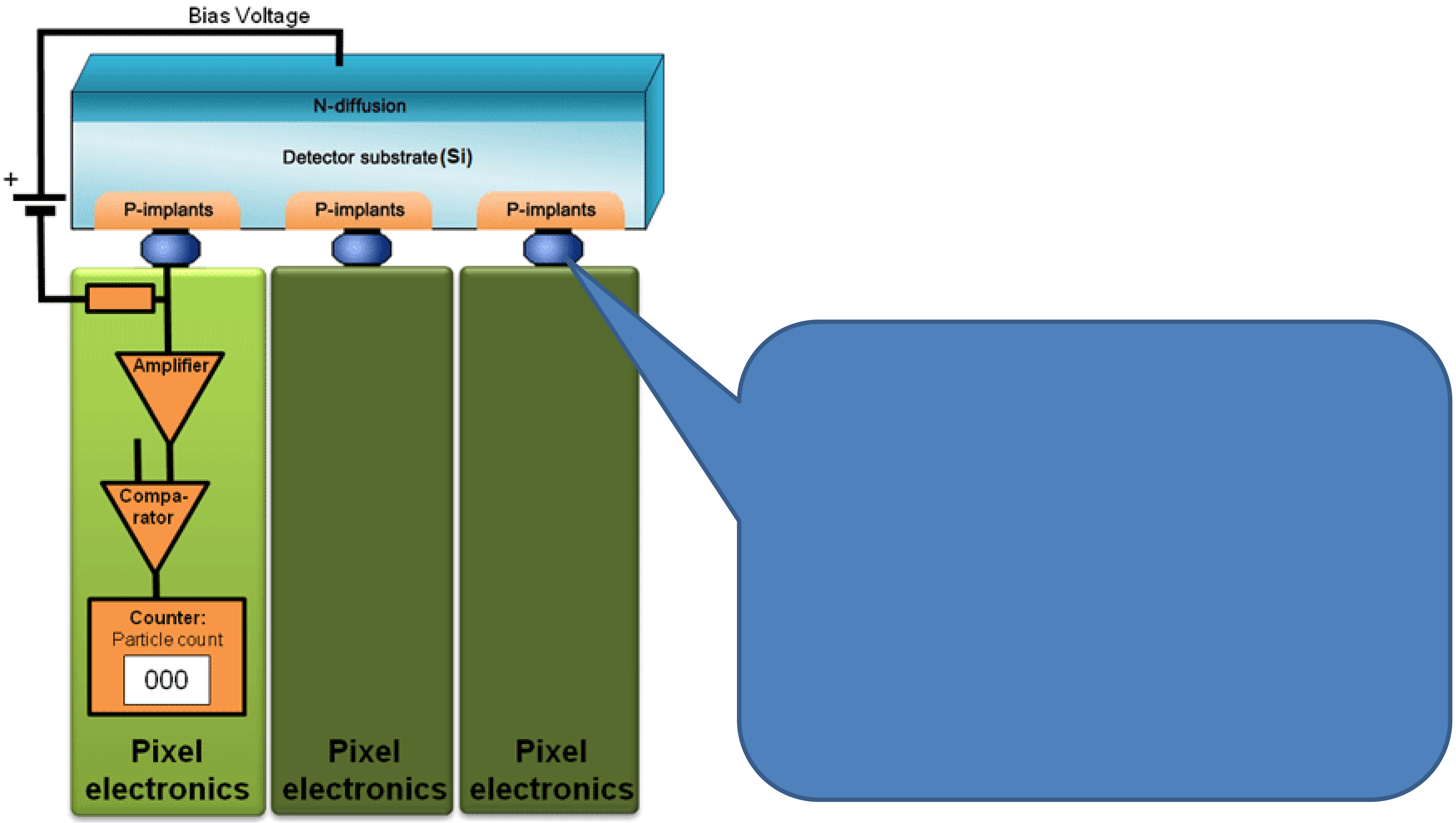
- **the chosen architecture allows for continuous readout of the sparsely distributed data with the hit rate up to 20 $\bullet 10^6$ cm^{-2} sec^{-1}**

- **event count mode will also be available for imaging applications and for calibration**

- **the chip is planned for submission in the beginning of 2012**

Spare slides

Medipix-based detectors: the sensor



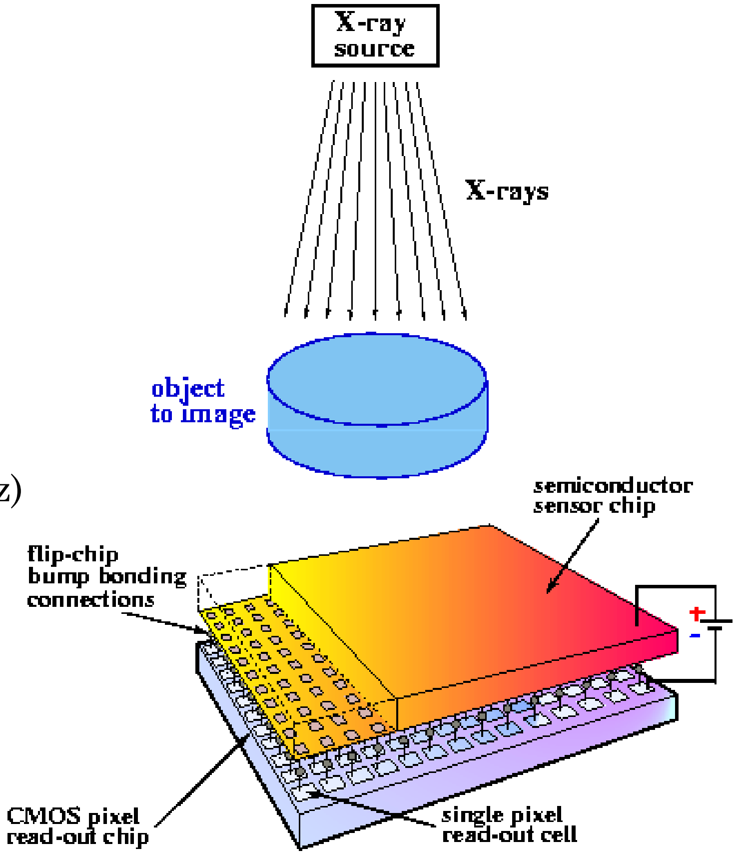
Medipix family detectors

- Photon (X-ray) counting hybrid pixel detector
- Imaging / medical applications

1997: Medipix1 (CERN)
- emerged from LHC1/Omega3 (technology: 1µm CMOS)
- array: 64 x 64 / pixel: 170 um x 170 um / active area: 1.2cm^2
- min detectable signal : 1 400 e$^-$ (5.1 keV in Si)
- counter-per-pixel: 15-bit
- shift register-based readout: 16b output bus @ 10 MHz (384µs)

2001-2005: Medipix2 (CERN)
- technology: 0.25µm CMOS, 6-metal
- array: 256 x 256 / pixel: 55 um x 55 um / active area: 2cm^2
- energy window resolved photon counting: 2 discriminators
- counter-per-pixel: 13-bit (14-bit) (max counting rate : 100kHz)
- frame-based readout via: an LVDS TX: 1b @160MHz (< 9.2ms)
  32-bit parallel port (< 300us@100MHz)
- 3-side buttable: chip interface at one side only

2009: Medipix3 (CERN)
- technology: 0.13µm CMOS, 8-metal
- array: 256 x 256 / pixel: 55 um x 55 um / active area: 2cm^2
- highly configurable
- improved energy resolution: charge summing mode
- per pixel: 2 discriminators and 2 counters
- continuous count-read mode : second counter is a storage buffer
- designed for TSV (through-silicon via)

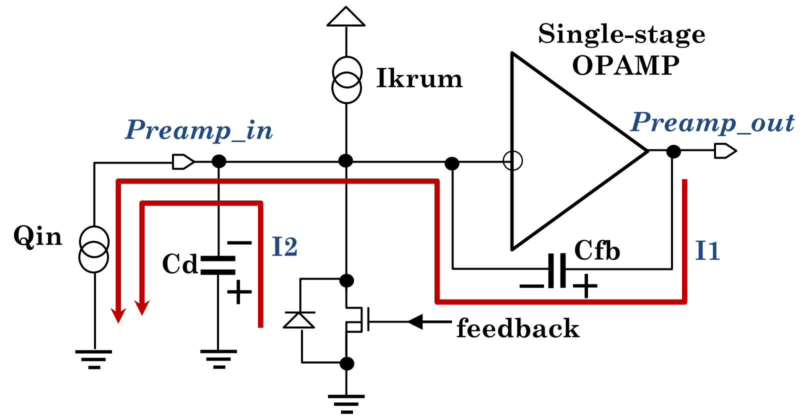


Preamp: main specifications

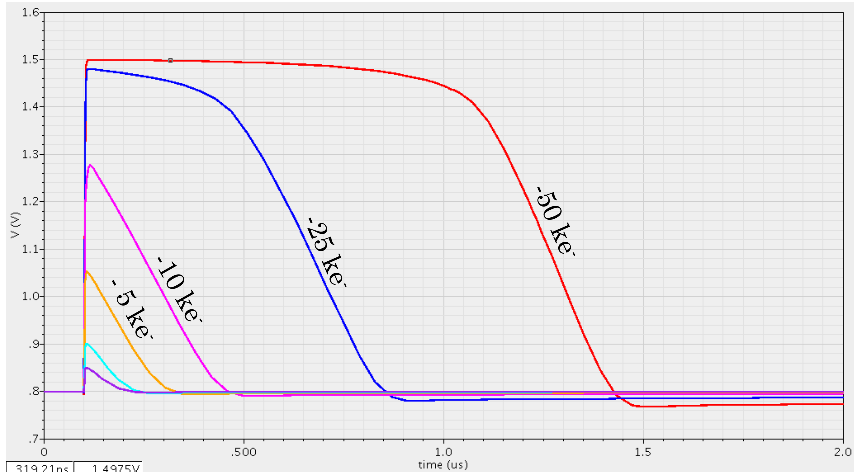
	Simulation Results (Xavi)	Simulation Results (Vladimir Gromov)
Pixel size	55 µm x 55 µm	ok
Analog pixel area	55 µm x [10…20] µm	ok
Pixel matrix	256 x 256	ok
Input charge	Bipolar (h^+ and e^-)	ok
Leakage current compensation	YES	**limited by the value of the Ikrum for electron signals**
Detector capacitance (Planar detector)	< 50 fF	**10fF (Gas Detectors)**
Peaking time	<25ns if Cd<70fF	**8ns (Cd=10fF), 11ns (Cd=25fF), 17ns (Cd=50fF)**
Preamp output linear dynamic range (Cf=3fF)	< 15 Ke^-	**Gain=48mV/1Ke^- → Output range = 1Ke^-•800mV/48mV ≈ 12 Ke^-**
Timewalk	<25ns [@ Qin>Threshold]	**< peaking time**
Return to zero (Tunable)	YES (ΔIkrum)	**hole signals: not monotonous**
TOT linearity and range	Monotonic up to ~150 Ke^- @Ikrum 10nA	**limited linearity in the range: ± 800mV • (Cd+Cf) ≈ ± 150 Ke^- if Cd=25fF, Cf=3fF** **INL=15%;**
Return to zero full chip spread (TOT spread)	< 5%	**Qin=30ke^- @ holes= ± 20% (σ= 5%); electrons= ± 12% (σ= 3%)**
ENC (σ_{ENC})	0.57*Cd[fF]+61 [e-] → ~75 e^- @ Cd=25fF	**σ = 64 e^- (Cd=0fF), σ = 68 e^- (Cd=10fF), σ = 76 e^- (Cd=25fF)**
# Thresholds	1	ok
Discriminator response time	<5ns [if Qin>Threshold + 5 Ke^-]	ok
MC simulated Threshold spread	~200 e^-	**Preamp out: 30mV (p-p) → 625 e^- (p-p) → σ = 100 e^-** **Discriminator input referred : 21mV(p-p) → σ = 73 e^-** **Overall: 37mV (p-p) → σ = 125 e^-**
Threshold spread after tuning (4 bits)	~20 e^-	**8 e^-**
Full chip minimum detectable charge	6*sqrt(ENC²+Threshold_mismatch²) → ~475 e^- @ Cd=25fF	ok
Pixel analog power consumption	8.4 µW static (Preamp 3.6 µW and 4.8 µW Discriminator) 2.4 µW dynamic (only @ HIT)	**Preamp: 3µA • 1.5V = 4.5 µW (static)** **Discriminator: electrons 6µA • 1.5V = 9 µW (static)** **holes: 4µA • 1.5V = 6 µW (static)**
Stability (Phase Margin)	-	**Phase margin = 44°** Worst case: Ikrum =10nA, Cd=25fF, Vdd=1.5V, Ck=3.6pF

Charge deposit measurements: time-over-threshold method

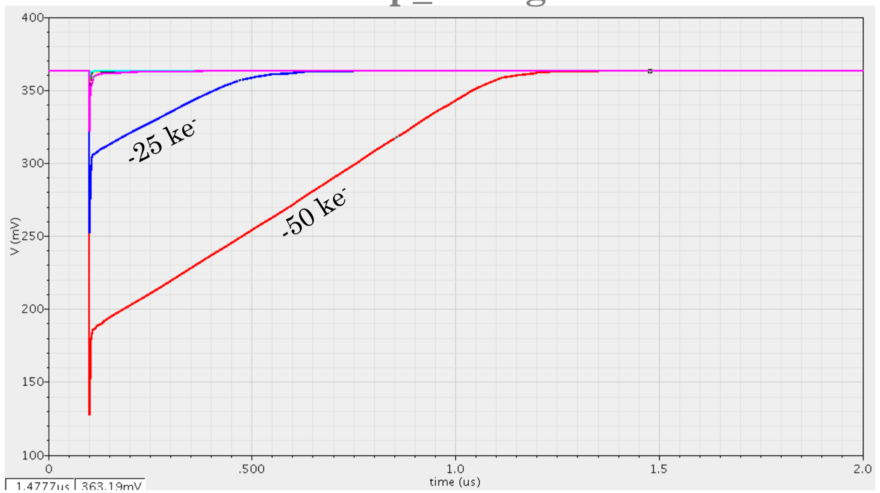
- wide dynamic range : ± 100 ke⁻



Preamp_out signals



Preamp_in signals



- Qin < 15ke⁻ : input charge stored on Cfb
- 15ke⁻ <Qin < 100ke⁻ : input charge stored on Cd
- 100ke⁻ < Qin : input charge is drained be the parasitic diodes
- discharge current is signal-dependent → (INL ≈ 10%)
- channel-to-channel ToT mismatch ≈ 25%

Accuracy of the ToT measurements

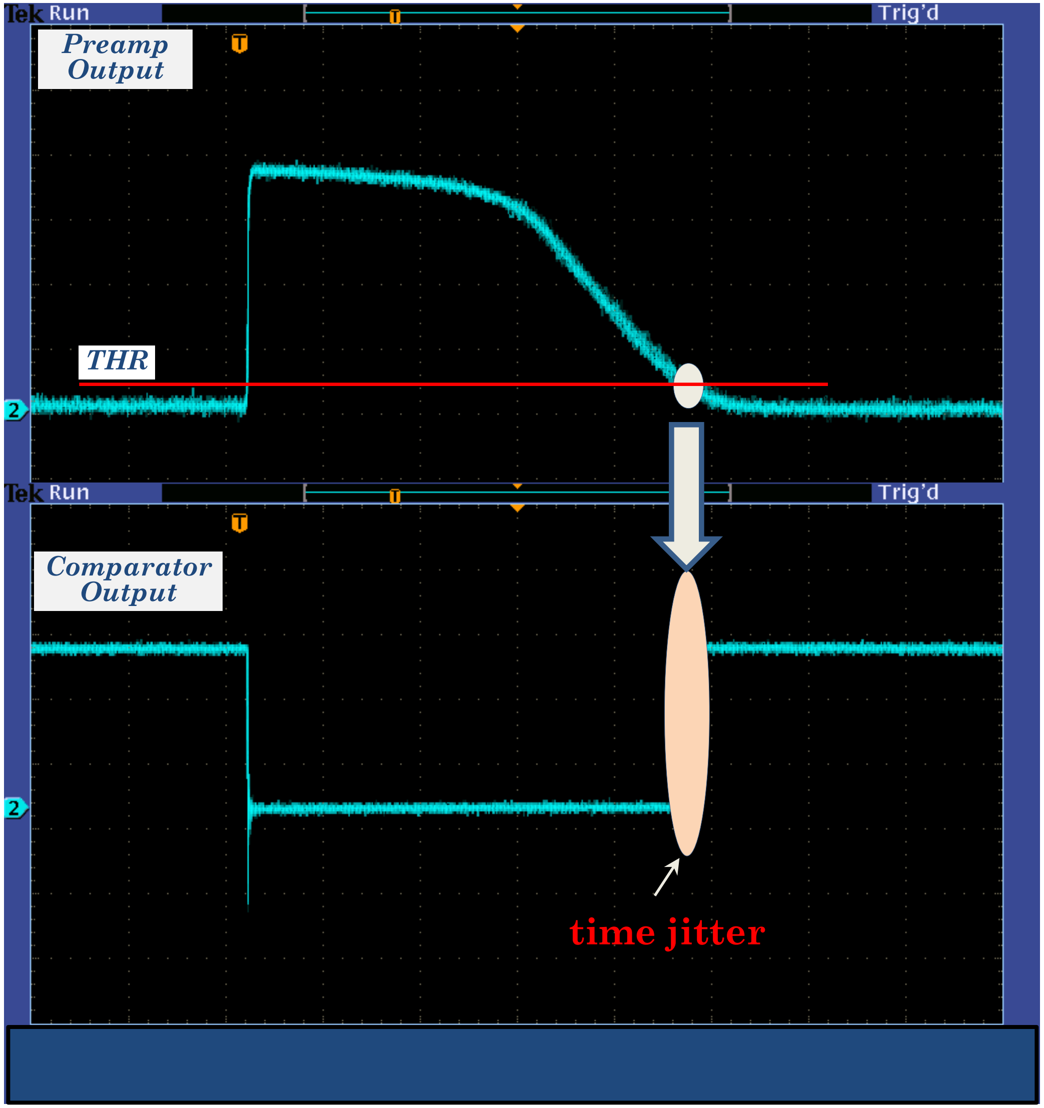
❑ electronic noise causes time jitter: $\sigma^{\text{jitter}} = \sigma(U_{out}^{\text{noise}}) / [dU/dt]$

Qin	ToT	ToT accuracy 6 • σ(jitter) / ToT
-2 ke$^-$	0ns	∞
-4 ke$^-$	86ns	14%
-6 ke$^-$	147ns	8.2%
-8 ke$^-$	207ns	5.8%
-10 ke$^-$	267ns	4.5%
-20 ke$^-$	546ns	2.2%
-30 ke$^-$	801ns	1.5%
-50 ke$^-$	1260ns	0.9%
-100 ke$^-$	2050ns	0.6%

ToT= Qin / Idis

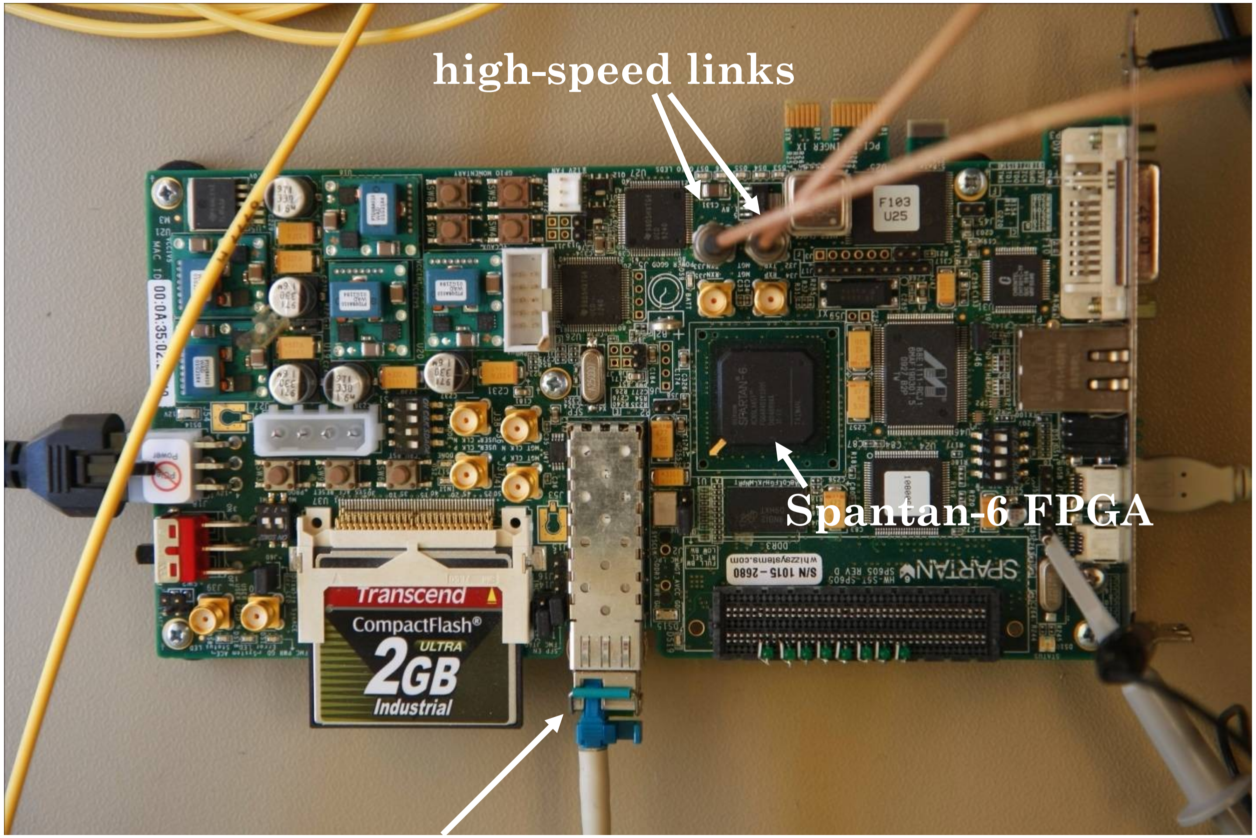
$\sigma(\text{jitter}) = \sigma(U_{out}^{\text{noise}}) / [dU/dt]$ ↓ Idis/Cfb

$$\sigma(\text{jitter}) / ToT = \sigma(U_{out}^{\text{noise}}) \bullet C_{fb} / Q_{in}$$



- **lowering of electronic noise**
- **decreasing of the feedback capacitor**

Spartan-6 evaluation board (Peter Jansweijer)



supports links running at 640MHz

Serial Clock Divider

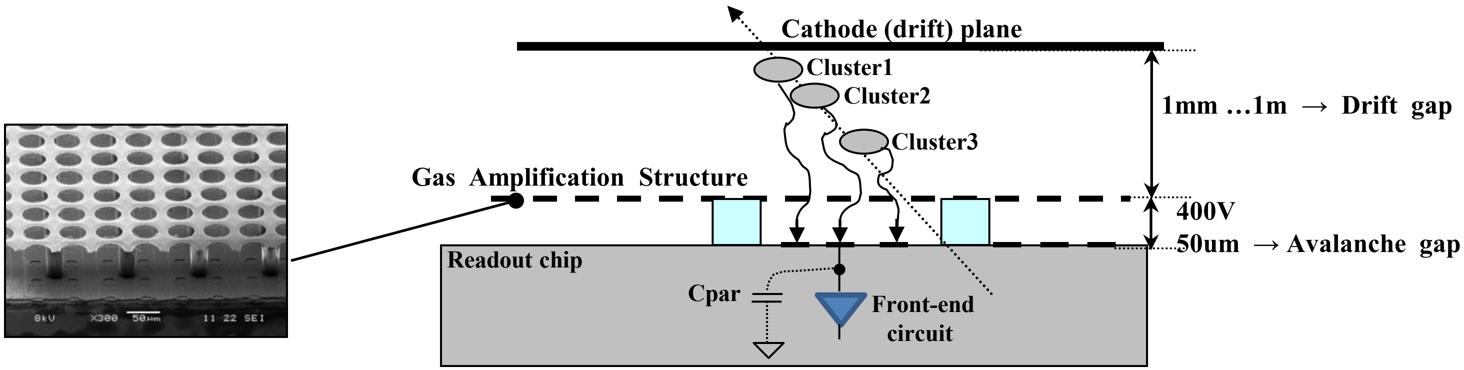
Each receiver PMA module has a D divider that divides down the clock from the PLL for lower line rate support. This divider is set by the PLL_RXDIVSEL_OUT attribute and can be changed dynamically via the DRP port for protocols with multiple line rates. The control for the serial divider is described in Table 4-14.

Table 4-14: **RX PLL Output Divider Setting**

Line Rate Range (GHz)	D Divider Value	Attribute Setting
2.457 to 3.125	1	PLL_RXDIVSEL_OUT = 1
1.2288 to 1.62	2	PLL_RXDIVSEL_OUT = 2
[illegible]	4	PLL_RXDIVSEL_OUT = 4

Micro-pattern gas detectors: layout and features

Gas-avalanche detector combining a gas layer as signal generator with a CMOS readout pixel array



- **particle track image (projection)**
- **3D track reconstruction**
- no sensor leakage current compensation
- low parasitic capacitance (less than 10fF)
- micro-discharges in avalanche gap