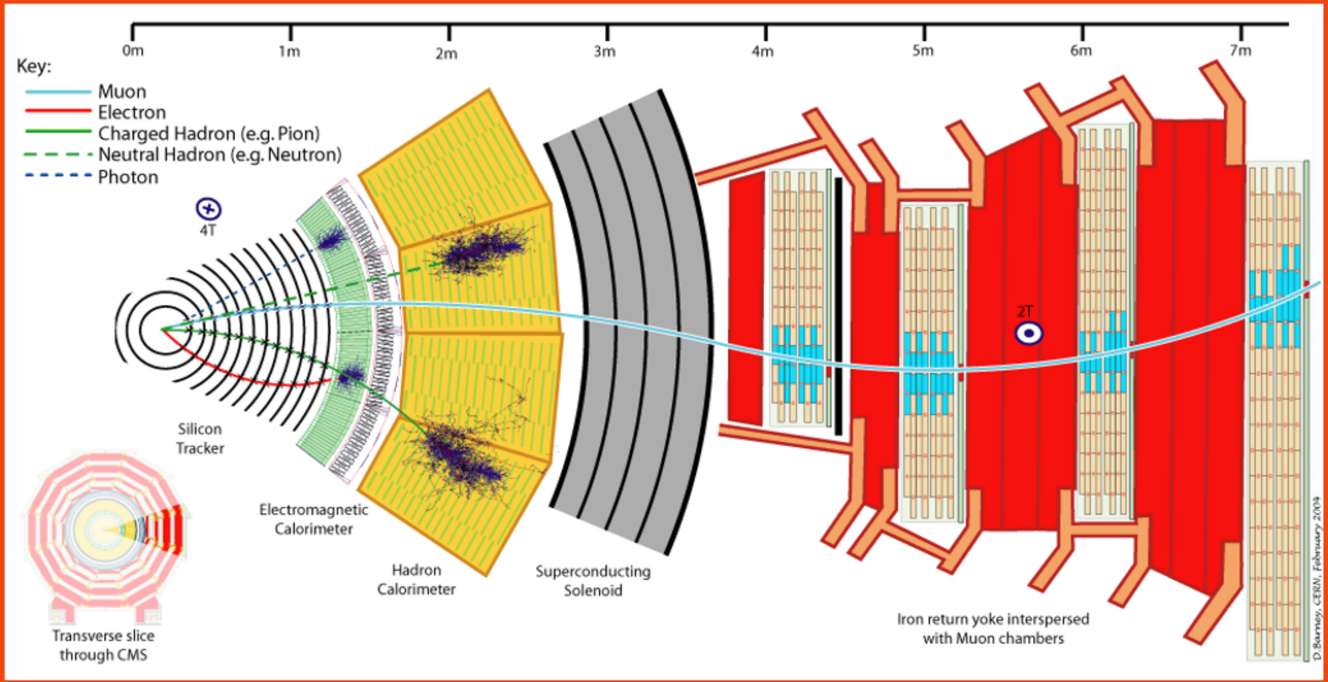


Tracking & Triggering

Devices and Front End to measure and reconstruct the trajectories of charged particles or searching for interesting events (or removing background events)

TRIGGER or TRIGGERLESS ?
The LHCb Muon Detector

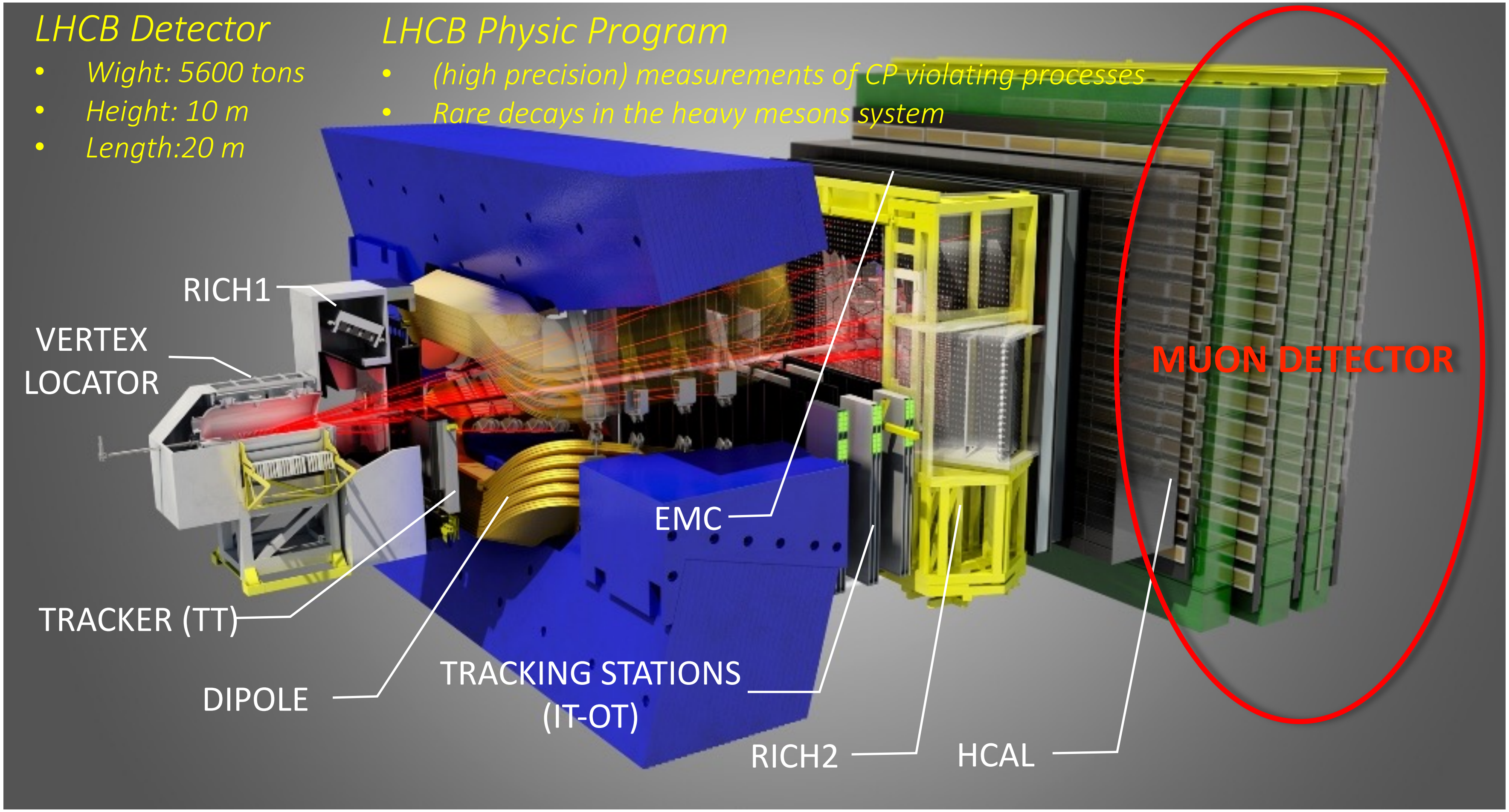
TRACKING: The KLOE-2 C-GEM IT
[A Binary Readout Detector]

TRACKING: The BESIII C-GEM IT
[Improve the Spatial Resolution]

Upgrades

Conclusions

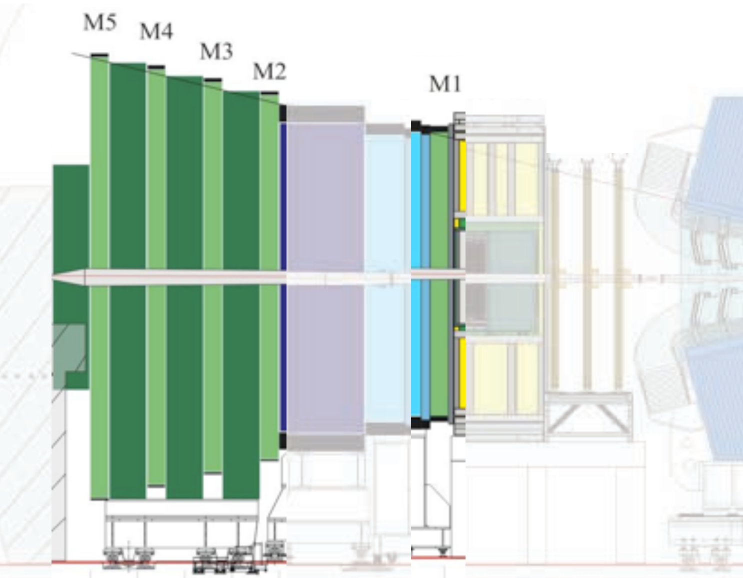
LHCb - 2010: start data taking



MUON SYSTEM: Selection of high P_T muons at trigger level and offline muon identification

The LHCb Muon Detector

Selection of high PT muons at trigger level and offline muon identification



Readout type	**Region**
MWPC	
Wire pads	R4
Mixed wire-cathode pads	R1-R2 in M2-M3
Cathode pads	everywhere else
GEM	
Anode pads	M1R1

- *5 stations M1-M5 each equipped with 276 multi-wire proportional chambers*
- *Inner part of M1 equipped with GEM detectors*

REQUIREMENTS

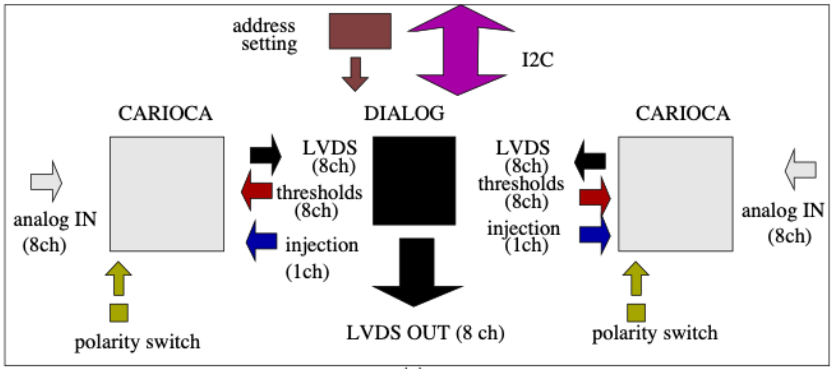
- *A muon trigger in LHCb requires a hit in 5 muon stations within a 25 ns time window*
- *> 99% detection efficiency for each station in a 20 ns time window*
- *< 3.5 ns rms time resolution for each bi-gap*

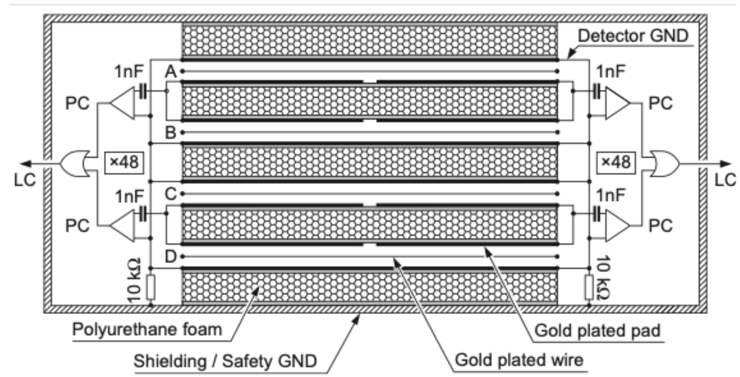
TRIGGER

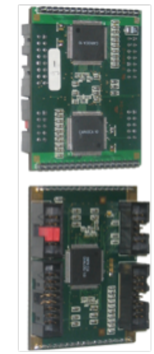
- *L0 (first Level) implemented in hardware with 4 μs latency*

LHCb Muon Detector - On Detector Electronics

FUNCIONS







CARIOCA

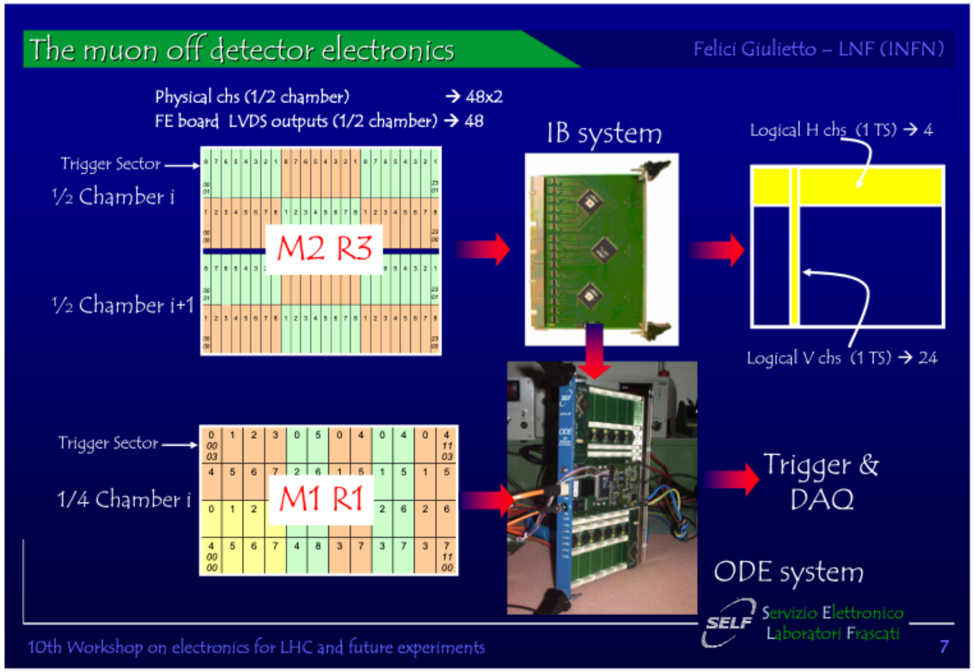
- *8 channels*
- *Pseudo-differential inputs*
- *LVDS output signals*
- *Positive/Negative input signals*
- *14mV/fC @ 0 pF – 7.8mV/fC @220 pF*
- *≈ 2000 pF + 42e/pF (positive/negative slightly different)*
- *200 fC dynamic range*
- *≈ 10 ns peaking time*
- *≈ 50 ns average pulse width*
- *≈ 50 ohm input impedence*
- *≈ 1 μs baseline restorer response time*

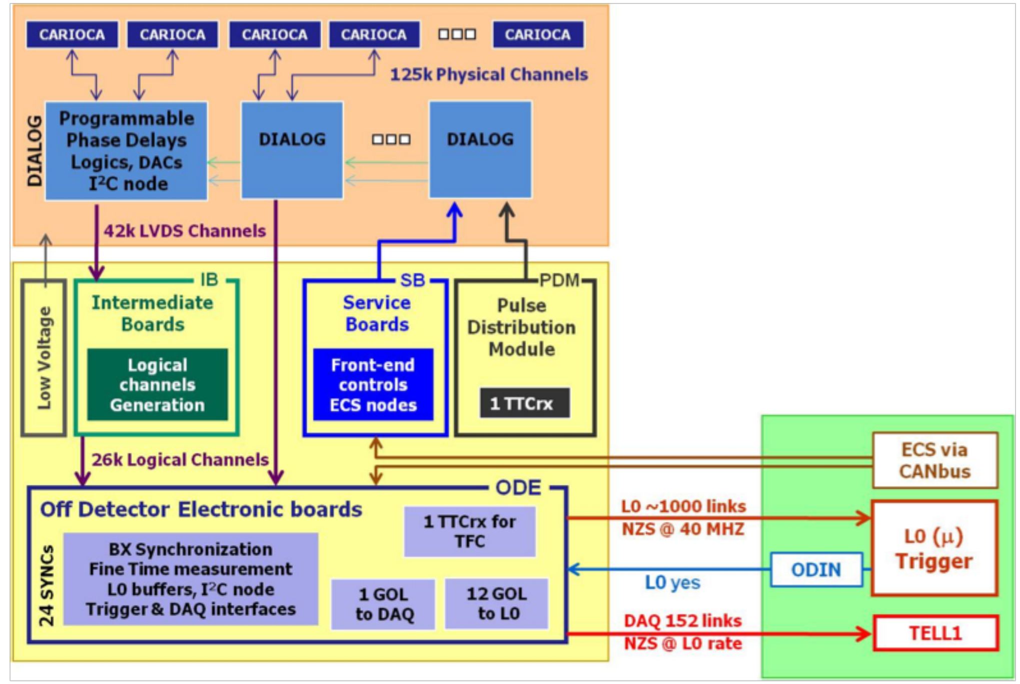
DIALOG

- *16 input channels - 8 output channels*
- *16 programmable delays @ 1 ns step for detectors time alignment*
- *Combine the 16 input to produce trigger information*
- *DAC thresholds*
- *Monitor channels rates*

$C_D \approx 30 \div 230$ pF

LHCb Muon Detector - Off Detector Electronics





ODE SYSTEM

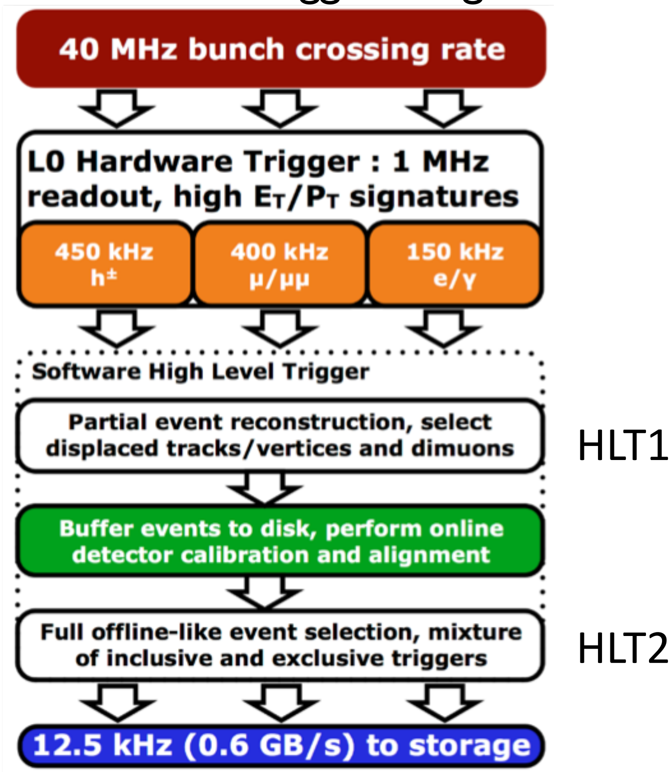
- *Sync data with the master LHCb clock*
- *Group data in Trigger Unit*
- *Serialize and sent data (GOL) to the L0 muon trigger @40 MHz*
- *Measure hit arrival time (with respect ti the BC) @1.5 ns resolution (4 bits TDC)*
- *Sent data to TELL1 in case of trigger (@ 1MHz)*

➡ *TDC information required to synchronize all redout channels (time resolution of the muon system)*

The LHCb Trigger [2010] - Hardware Trigger

2010-2012	2013 2014	2015-2018	2019 2021	2022-2024	2025 2027	2028-2020	2031	2032-2034	2035	2036
RUN 1	LS1	RUN 2	LS2	RUN 3	LS3	RUN 4	LS4	RUN 5	LS5	RUN 6

LHCb 2015 Trigger Diagram



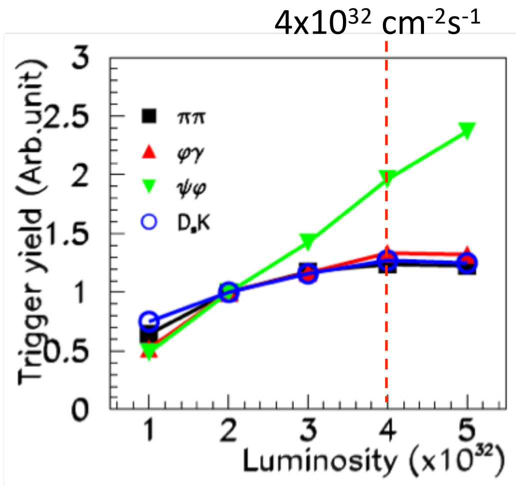
TWO STAGE SYSTEM

- *L0 (level 0 trigger) implemented in hardware*
- *HLT (high level trigger) implemented in software*

L0 TRIGGER

- *Rate reduction from ~ 13 MHz to 1 MHz*
- *4 μs latency*
- *Based on Muon System & Calorimeter information*
- *Select events with both high P_T muons or or large transverse energy deposits in calorimeter*

LHCb Muon Detector – Why the Upgrade ?



Hadronic channel saturation

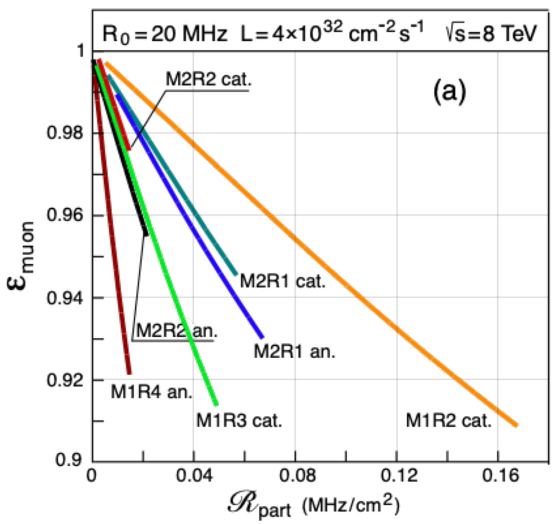
LHCb MAXIMUM ACQUISITION RATE

- *L0 hardware trigger based on E_T and muon P_T*
- *L0 max readout rate ≈ 1.1 MHz*

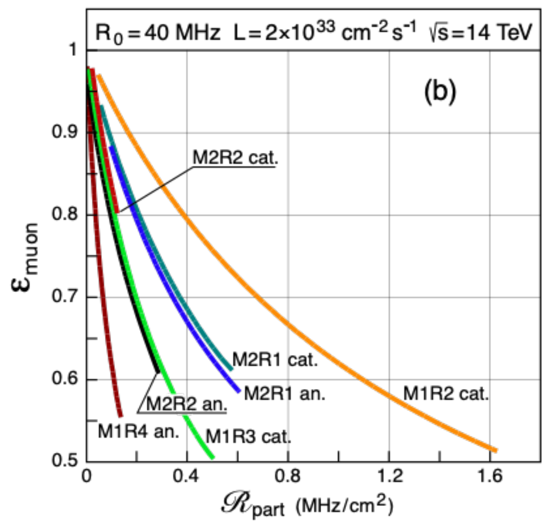
UPGRADE TO A FULL SW TRIGGER
(full event reconstruction)

MUON DETECTION INEFFICIENCY due to DEAD TIME

2009-2013



FUTURE RUNs EXTRAPOLATION



MUON DETECTOR

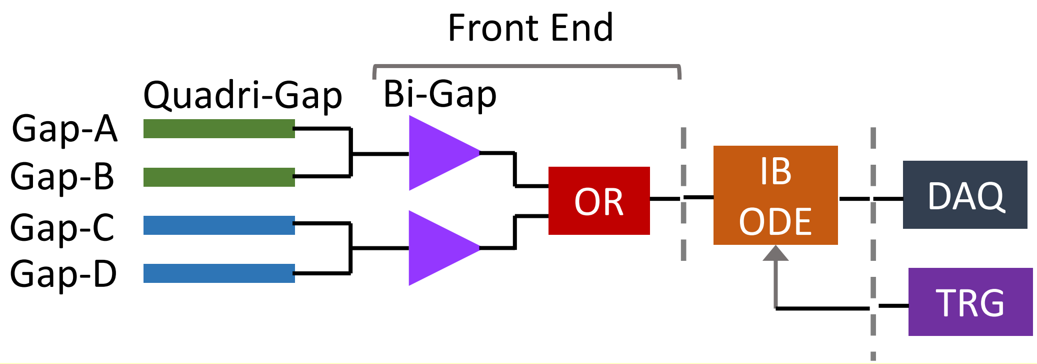
Dead time is a limiting factor for MWPC belonging to M1 and M2 internal regions

- *Remove M1 station*
- *Shielding*
- *Increase the granularity removing the logical channels*

LHCb Muon Detector – RUN 1- RUN4 Readout

FE readout electronics (RUN1-RUN2):

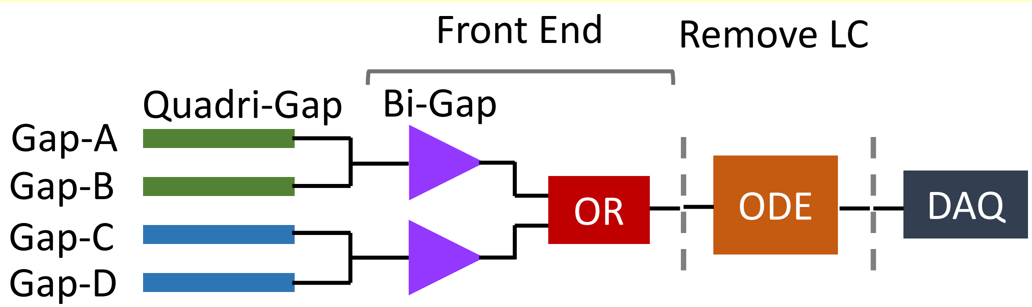
- *phisical OR of 2 gaps*
- *Further Logica OR of the bi-gaps*
- *Luminosity: $1x10^{27} \div 2x10^{31}$*



2010-2018 → $\mathcal{L}_{int}$ = 10 fb^{-1}

FE readout electronics (RUN3 – RUN4):

- *phisical OR of 2 gaps*
- *Further Logica OR of the bi-gaps*
- *Triggerless operation*
- *Luminosity: $2x10^{33}$*



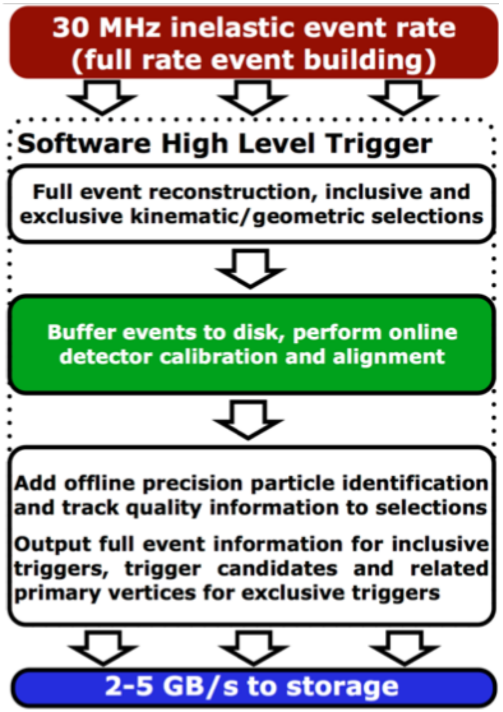
2022-2030 → $\mathcal{L}_{int}$~ 50 fb^{-1}

RUN5 - RUN6

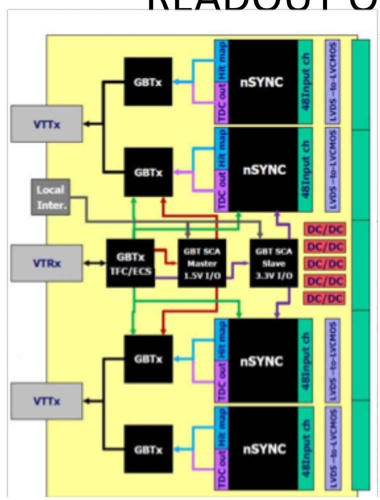
LHCb Muon Detector – The Phase I Upgrade

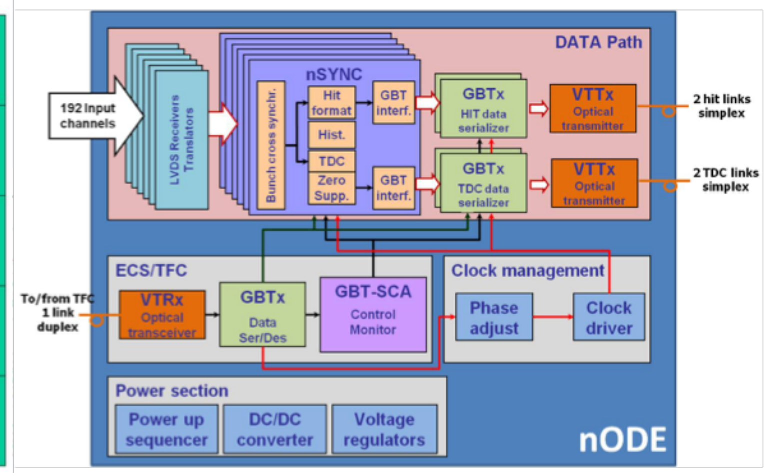
2010-2012	2013 2014	2015-2018	2019 2021	2022-2024	2025 2027	2028-2030	2031	2032-2034	2035	2036
RUN 1	LS1	RUN 2	LS2	RUN 3	LS3	RUN 4	LS4	RUN 5	LS5	RUN 6

$\mathscr{L} \sim 2 \times 10^{33}$ sec^{-1} cm^{-2}

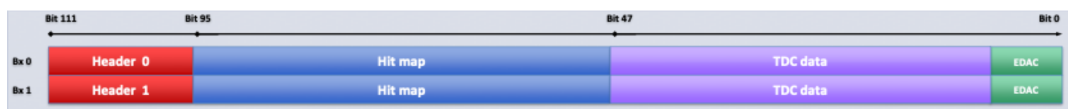


READOUT OF ALL PHYSICAL CHANNELS





TELL40

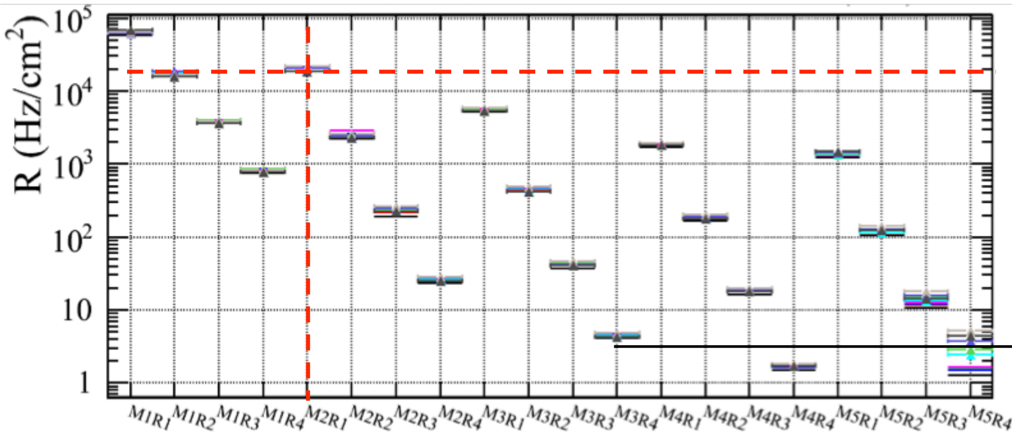


Frame (Header + Hit Map + TDC Data Zero Suppressed) transmitted to the GBT @ 320 Mbits/s

TRIGGERLESS OPERATION

LHCb Muon Detector – The Phase II Upgrade

2010-2012	2013 2014	2015-2018	2019 2021	2022-2024	2025 2027	2028-2030	2031	2032-2034	2035	2036
RUN 1	LS1	RUN 2	LS2	RUN 3	LS3	RUN 4	LS4	RUN 5	LS5	RUN 6



RUN5 FORESEEN RATE: Stations 2&3 Regions 1&2

		pad/gap	C (pF)	Rate 1 gap (kHz/cm2)	Rate/PAD 1 gap (KHz)
M2R1	12	896	29,63	998,3	835,5
M2R2	24	896	59,26	97,5	163,2
M3R1	12	896	34,67	574,8	562,7
M3R2	24	896	69,34	71,5	139,8
M4R1	12	896	40,10	211,3	239,2
M4R2	24	896	80,20	30,2	68,2
M5R1	12	896	45,93	178,8	231,7
M5R2	24	896	91,86	19,9	51,5

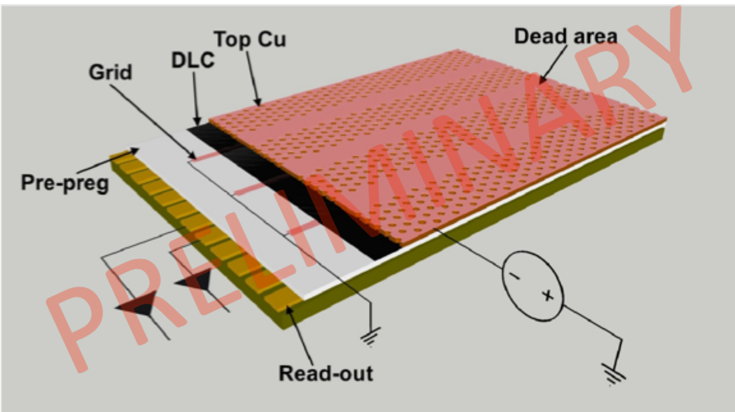
PRELIMINARY

RUN5 → $\mathscr{L} \sim 1.5 \times 10^{34}\ \mathrm{sec}^{-1}\ \mathrm{cm}^{-2}$

- *Use new detector technologies*
- *New Front-End design to manage the higher luminosity*
- *Full software trigger and all detectors readout @ 40 MHz*

LHCb Muon Detector – RUN5: R1 & R2 Detector Upgrade

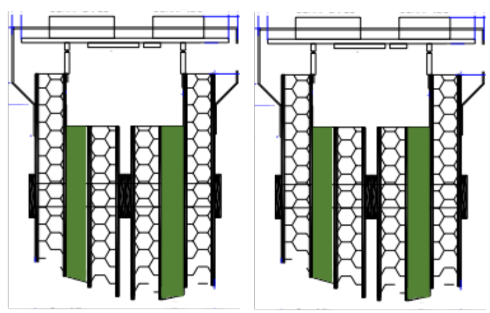
2010-2012	2013 2014	2015-2018	2019 2021	2022-2024	2025 2027	2028-2030	2031	2032-2034	2035	2036
RUN 1	LS1	RUN 2	LS2	RUN 3	LS3	RUN 4	LS4	RUN 5	LS5	RUN 6



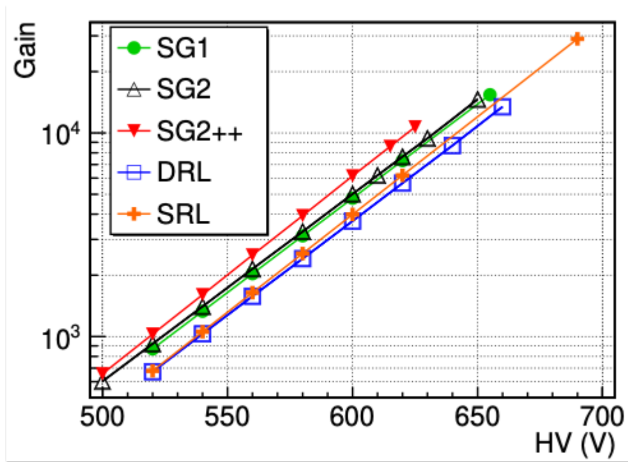
OPTION FOR M2-M5 INTERNAL REGIONS

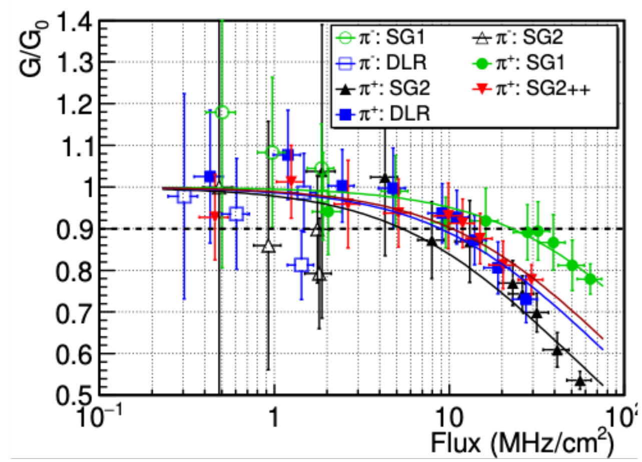
R-WELL SILVER GRID LAYOUT

conductive grid deposited on the DLC layer used to evacuate currents



R-WELL Chambers – 4 gaps





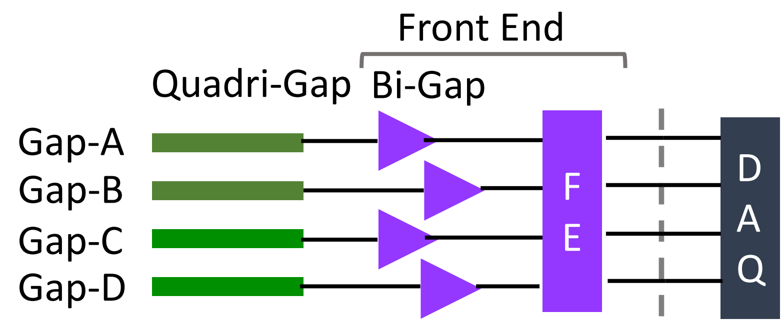
G.Bencivenni et al. - The µ-RWELL for high rate application - International conference on Instrumentation for Colliding Beam Physics - Novosibirsk, Russia

LHCb Muon Detector - RUN 5: Readout Electronics Upgrade

RUN5 - RUN6
2032-2040

$\mathcal{L}$ = 1-2 x 10^{34}

$\mathcal{L}_{int}$~ 300 fb^{-1}



TRIGGERLESS OPERATION THROUGHPUT DOMINATED BY UNCORRELATED HITS

Example

- *frame: 5 bits (timing) + 32 bits (bc counter/chip id/error correction etc)*
- *64 chs asic*
- *ASIC Throughput ≈ 840 kHz pad rate x (5x64 + 32) bits ≈ 300 Mbps*
- *M2R1 chamber requires 56 asic @ 64 chs*
- *R1 is made of 12 chambers*

~ 200 Gbps !!!!

REMOVE BACKGROUND

LHCb Muon Detector - RUN 5: Readout Electronics Upgrade

	Region	#cmb/region	Occupancy	ASIC-64/cmb	Nch/ASIC	hitON 16 tetra-gaps	UL99% 16 tetra-gaps
Inner Region	M2R1	12	0,0048	56	64	0,08	1
	M2R2	24	0,0013	56	64	0,02	1
	M3R1	12	0,0033	56	64	0,05	1
	M3R2	24	0,0011	56	64	0,02	1
	M4R1	12	0,0018	56	64	0,03	1
	M4R2	24	0,0007	56	64	0,01	1
	M5R1	12	0,0018	56	64	0,03	1
	M5R2	24	0,0005	56	64	0,01	1
Outer Region	M2R3	72	0,0181	12	32	0,14	1
	M2R3 new	40	0,0171	24	32	0,14	1
	M2R4	128	0,0170	3	16	0,07	1
	M3R3	48	0,0180	12	32	0,14	1
	M3R4	192	0,0108	3	16	0,04	1
	M4R3	48	0,0127	6	32	0,10	1
	M4R4	192	0,0037	3	16	0,01	1
	M5R3	48	0,0154	6	32	0,12	1
	M5R4	192	0,0075	3	32	0,06	1

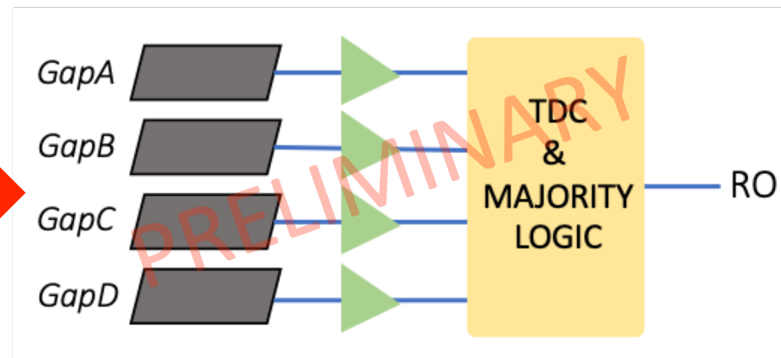
PRELIMINARY

Occupancy estimation

- hitON: prob. majority validate a hit
- UL99%:prob. (Max(NhitON)>UL) < 1%

Max hitON ~ 15%
Max UL99% = 1

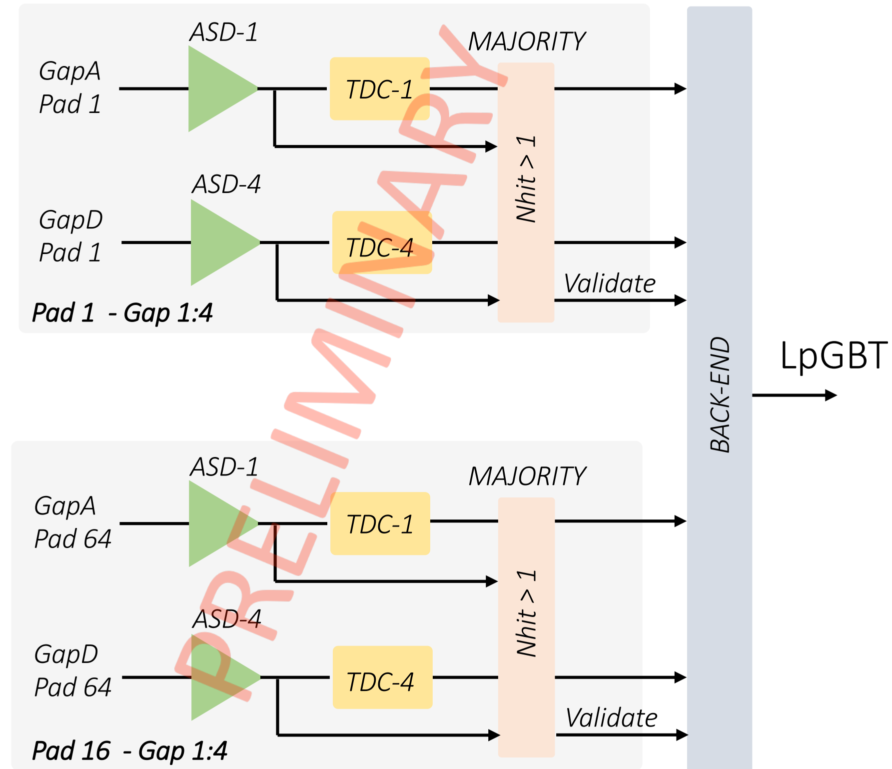
ACQUIRE THE SINGLE GAP AND USE MAJORITY LOGIC



LHCb Muon Detector - CONCLUSIONS

Data Frame (example)

Fixed Header Field 8 bits	BXID count	4 bit
	BXID Wrap Around	1 bit
	No Data	1 bit
	Length	2 bit
Variable Data Field 16 bits	Time	4 bit
	Address	4 bit
	Majority Map	4 bit
	Spares	4 bit



64 chs ASIC

BW_{MIN} = 40 MHz x (8 bit + [hitON x 16]) = 416 Mbps

⬇

Up to 14 FE chip per Data lpGBTx @ 640 Mbps

Although LHCb detector will be operated in triggerless mode a local trigger at FEE level can be considered as a measure to reduce the overall system throughput.

BACKGROUND RATE MUST BE CAREFULLY EVALUATED IN DATA-PUSHING ARCHITECTURE SYSTEM

TRIGGER: WITH or WITHOUT ?
The LHCb Muon Detector Case

TRACKING: The KLOE-2 C-GEM IT
[A Binary Readout Detector]

TRACKING: The BESIII C-GEM IT
[Improve the Spatial Resolution]

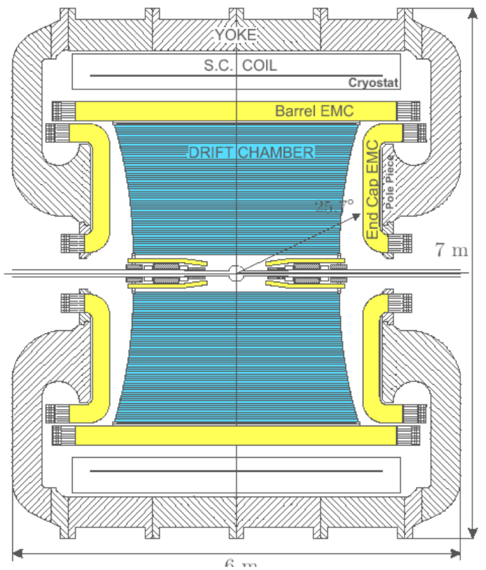
Upgrades

Conclusions

The KLOE 2 IT [2012]: the Detector

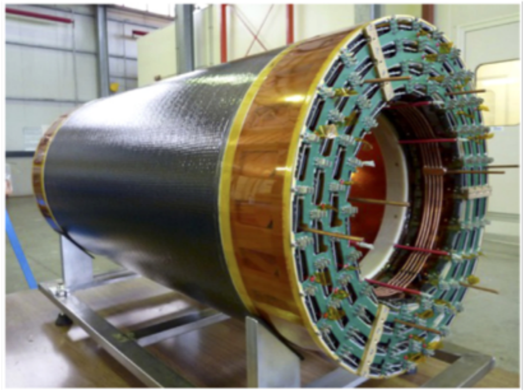
OBJECTIVES

- ***Extend the KLOE program on kaon physics***
- ***Test of fundamental symmetries***
- ***Quantum** interferometry*



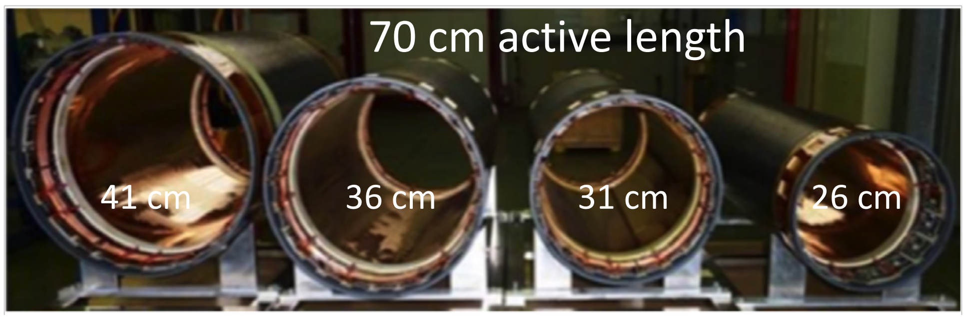
- 3/2/2/2 70 cm active length
- 650 μm XV pitch strip RO
- 25 kchs GASTONE FEE
- 1600 HV chs
- triple GEM layout
- Ar/Iso: 90/10 gas mixture
- 12000 gas gain
- 2% X_0 material budget

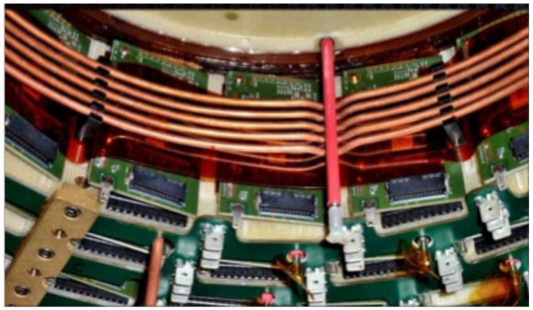
The required vertex detector performances are: 300 μm spatial resolution on the transverse plane and 500 μm along the beam line



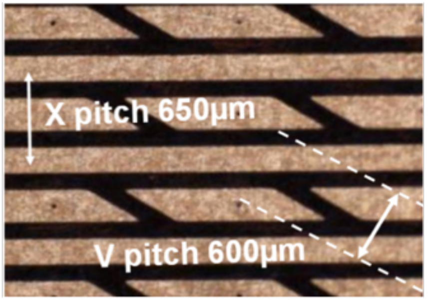
C-GEM working conditions

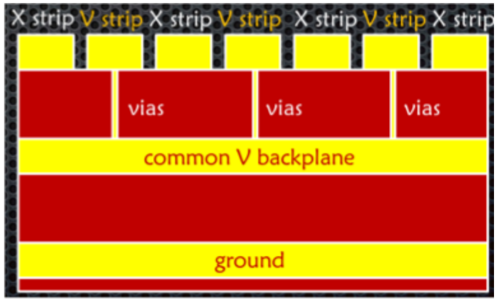
kV/cm				V		
Drift	T1	T2	IND	G1	G2	G3
1.5	3	3	6	280	280	270





The KLOE 2 IT [2012]: the READOUT

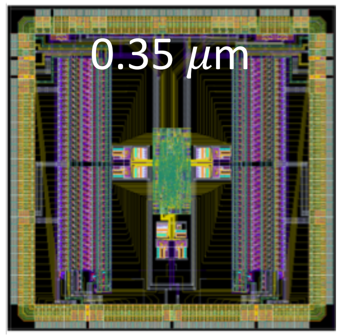


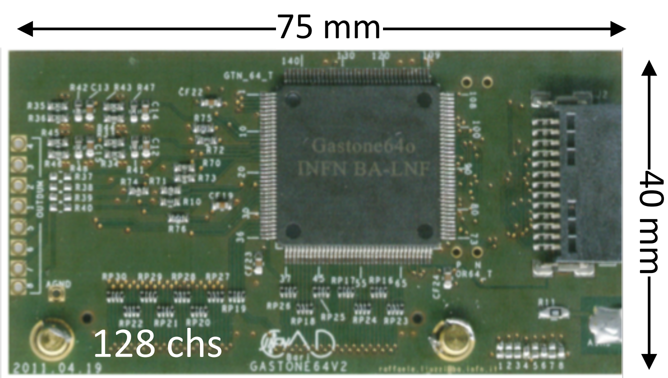


Kapton-Copper multilayer flexible circuit

- *X-wiew: longitudinal strips (250 μm - 100 pF)*
- *V-wiev: connection of pads through conductive vias and a common backplane (1 - 200 pF)*

N channels	64
Chip dimensions	4.5×4.5 mm^2
Input impedance	120 Ω
Charge sensitivity	16 mV/fC ($C_{det}=100$ pF)
Peaking time	90 ns ($C_{det}=100$ pF)
Crosstalk	$<3\%$
ENC	800 e^-+40 e^-/pF
Power consumption	~6 mW/ch
Readout	Serial LVDS (100 Mbps)

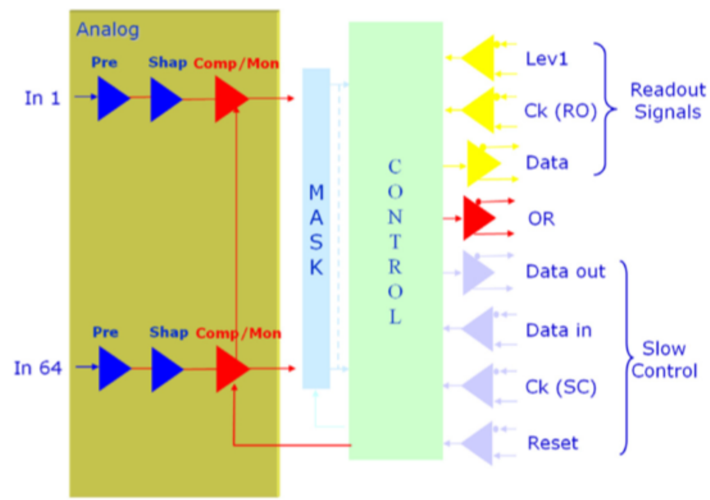




Output Frame

Header	10 bit
Trigger Number	5 bit
Chip ID	9 bit
Data	64 bit
Ending frame	8 bit

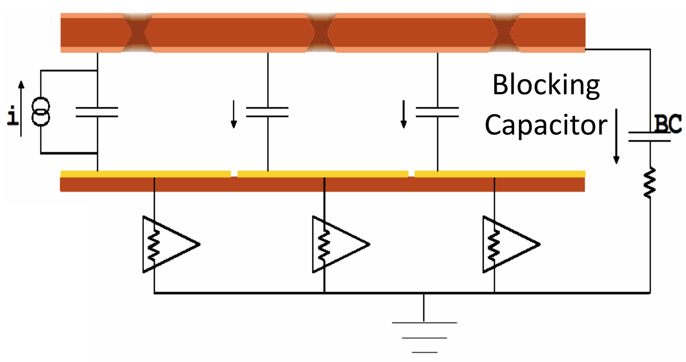
GASTONE
(Gem amplifier Shaper Tracking ON Events)

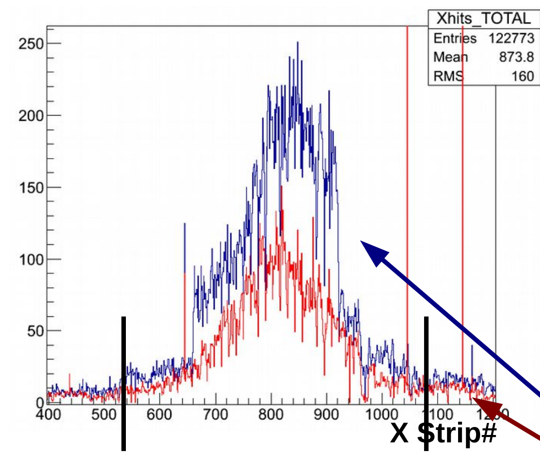


200 ns ÷ 1 μs output monostable to take into account L1 latency

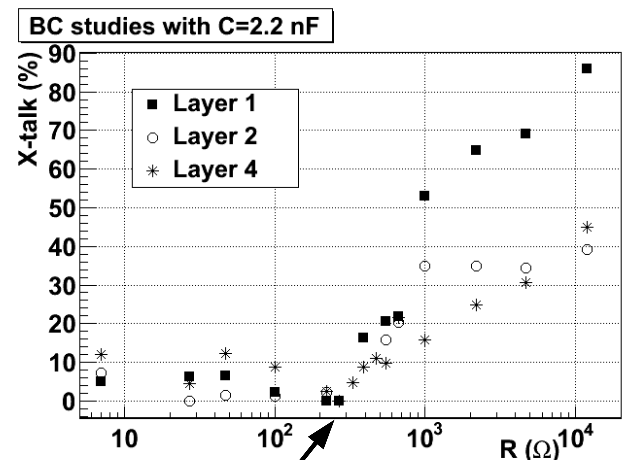
The KLOE 2 IT [2012]: HV FILTER NETWORK ON GEM3

- Correlated Noise observed on the CGEM
- The effect was explained with a capacitive coupling between G3 bottom and the readout plane. A large charge deposit on G3 bottom can induce signals on all the strips/pads facing the HV μsector then generating Large Hits Multiplicity Events.
- The effect can be strongly reduced by means an RC circuit (LHCb experience) between G3 bottom and the readout plane reference ground plane.





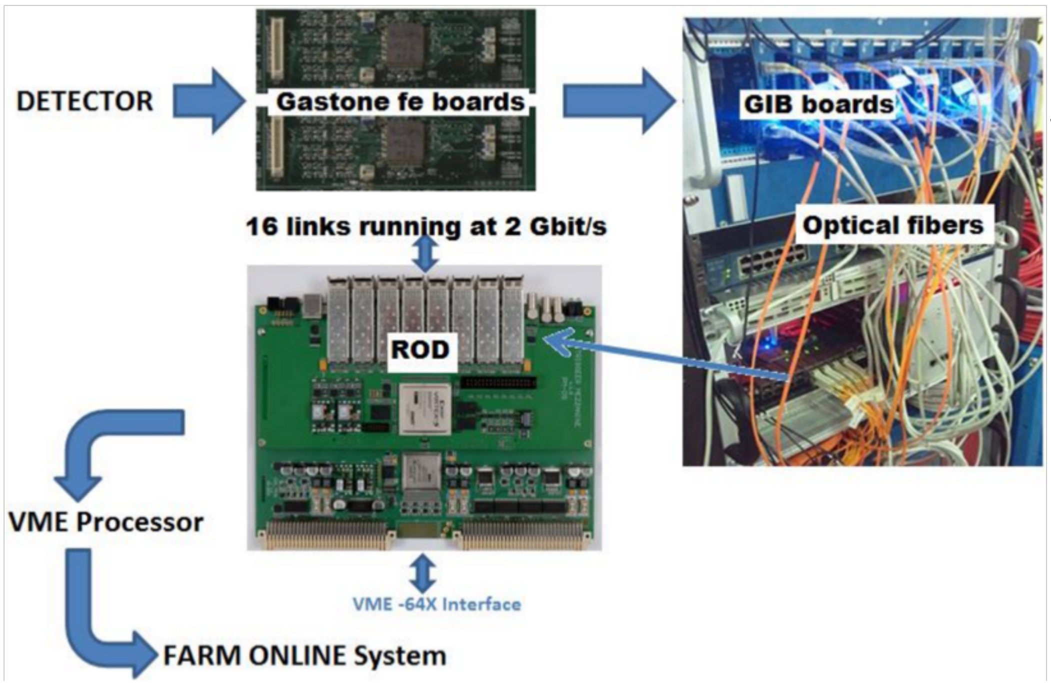
Strips range of integration

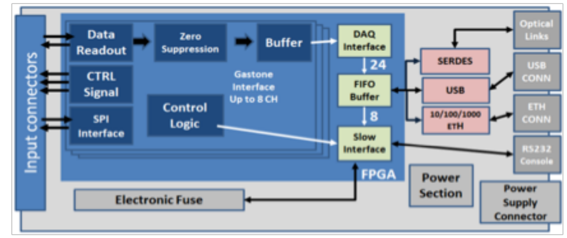


assuming R_{min} the value minimizing the integral of the entries we defined:

$$X-talk(R)=\frac{\int_{Strips\ range} Entries(R) - \int_{Strips\ range} Entries(R_{min})}{\int_{Strips\ range} Entries(R_{min})}$$

The KLOE 2 IT [2012] : the READOT





GIB (General Interface Boards): based on Xilinx virtex 4FX FPGA with embedded IBM Power PC (PPC405 @ 300MHz)

- *2 Gbps Optical port* } DAQ
- *Gigabit Ethernet* } DAQ
- *USB2* } DEBUG
- *RS232* } DEBUG

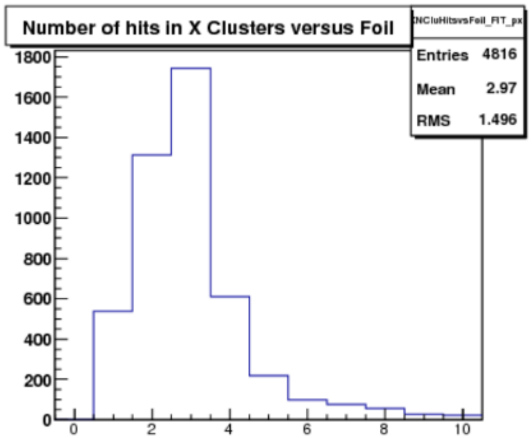
ROD (Read Out Driver): VME board; receives data delivered by GIBs

- *16 optical links @ 2Gbps*
- *First level event building*
- *VME bus is used to communicate with the original KLOE DAQ system (BW limited @ 2.6 Gbps)*

- Luminosity ≈ 5x 10^{32} cm^{-2} s^{-1}
- Trigger rate ≈ 20 kHz
- Channels ≈ 25k
- Hit position information

} ≈ 500 Mbps

The KLOE 2 IT: Some Results

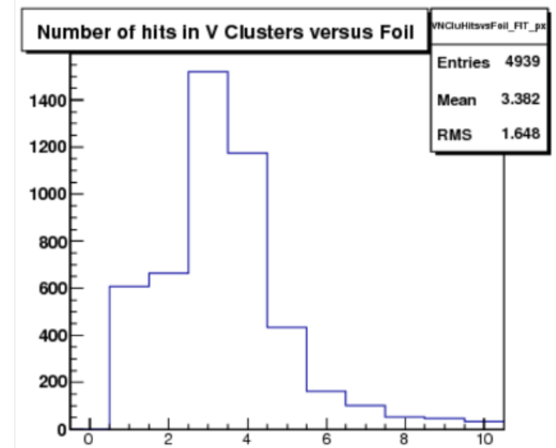


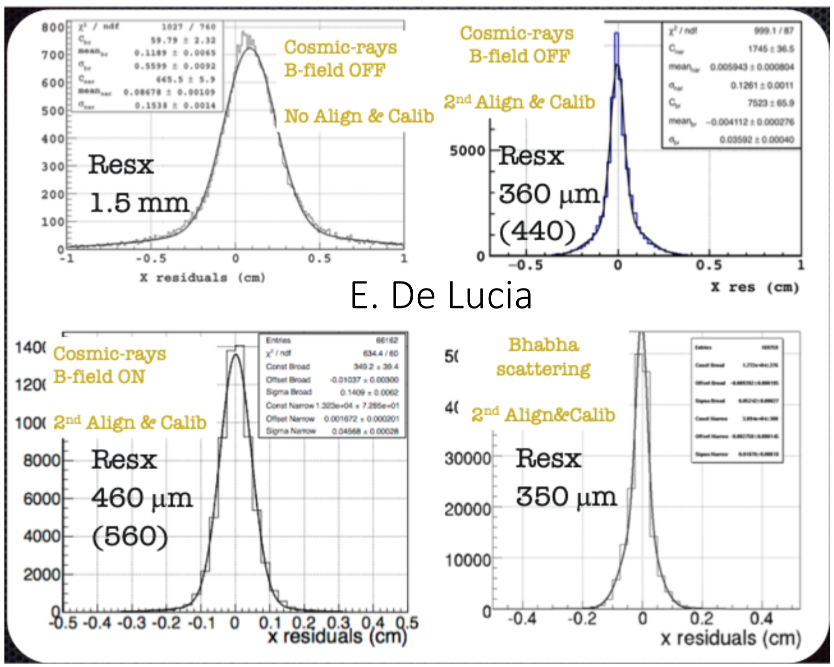
STRIP MULTIPLICITY

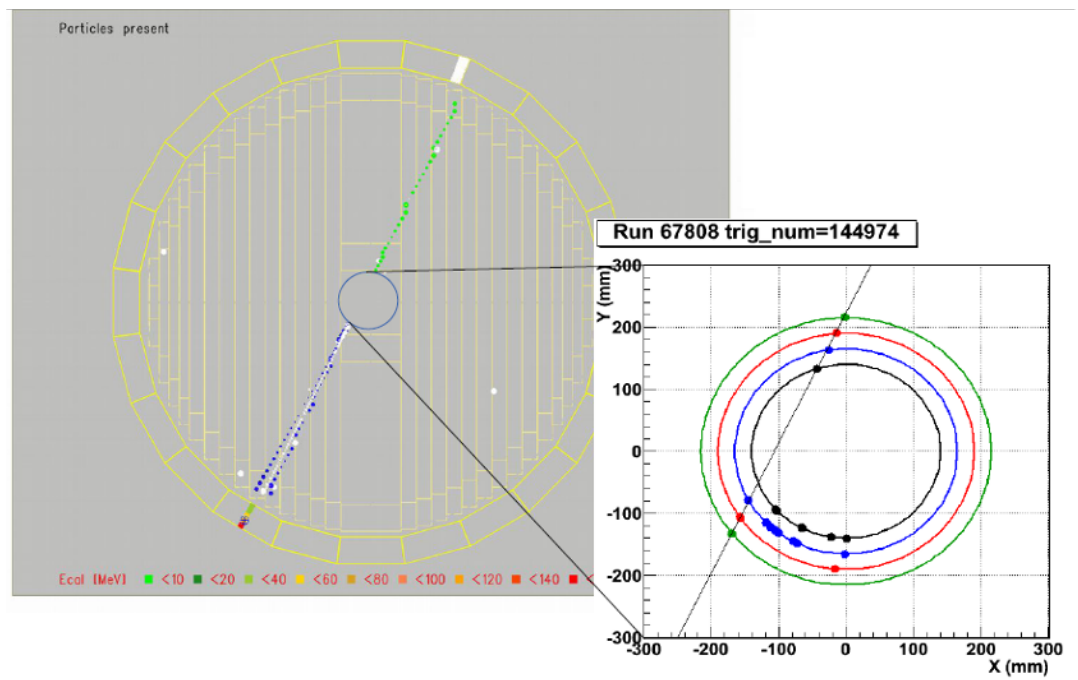
$$\sigma_x = pitch/\sqrt{12}$$

$Q_{TH} \simeq 3.5$ fC

Cluster Multiplicity ≃ 3 for both view







TRIGGER: WITH or WITHOUT ?
The LHCb Muon Detector Case

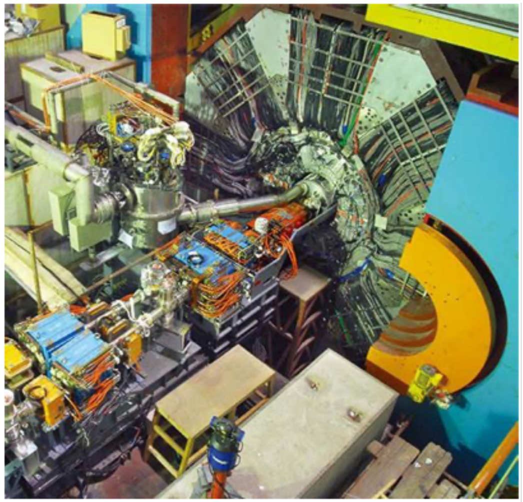
TRACKING: The KLOE-2 C-GEM IT
[A Binary Readout Detector]

TRACKING: The BESIII C-GEM IT
[Improve the Spatial Resolution]

Upgrades

Conclusions

The BESIII IT: The Detector



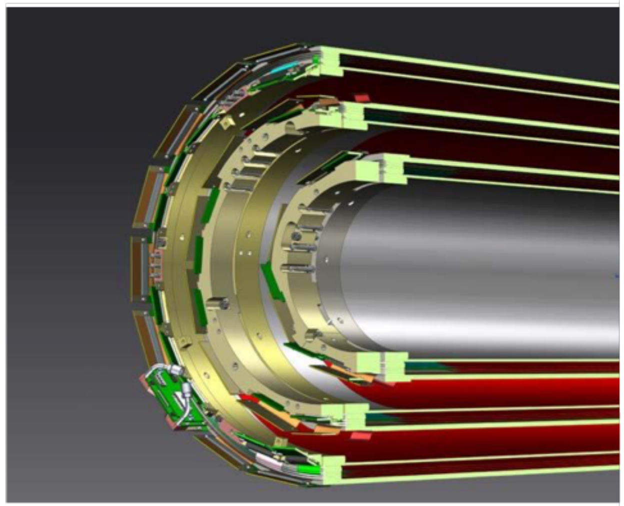
BES SPECTROMETER

BEPCII

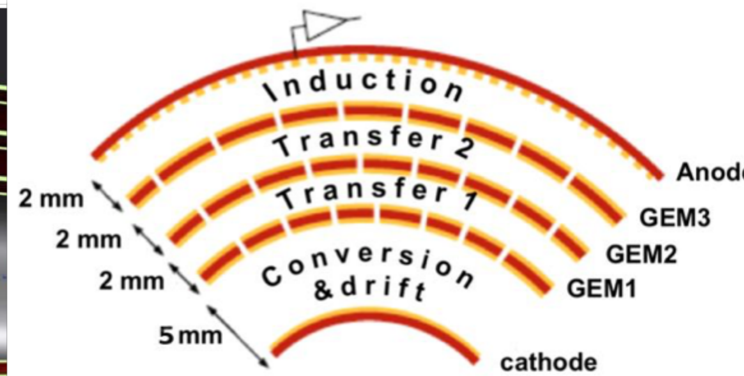
- Energy 2-5 GeV
- Luminosity 10^{33} cm^{-2} s^{-1}

OBJECTIVES

- Charm Physics
- Tau Physics
- Charmonium decays
- Light hadrons spectroscopy
- New Physics



C-GEM TRACKER CAD MODEL



SINGLE LAYER INTERNAL LAYOUT

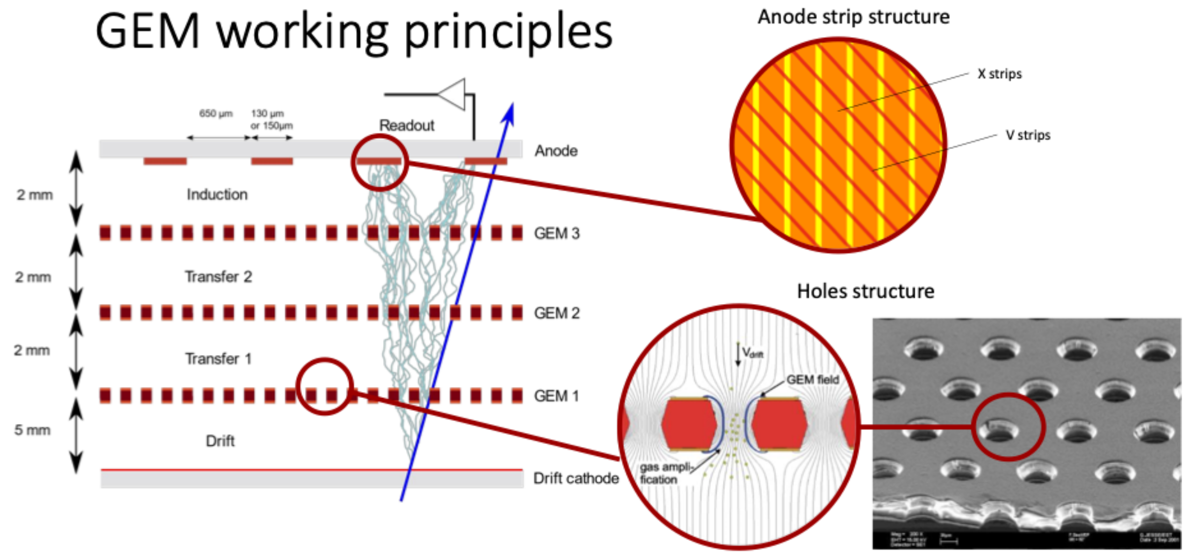
DIMENSIONS

- L1: L=532 mm, ⌀ ≃ 54 mm
- L2: L=690 mm; ⌀ ≃ 243 mm
- L3: L=847 mm; ⌀ ≃ 324 mm

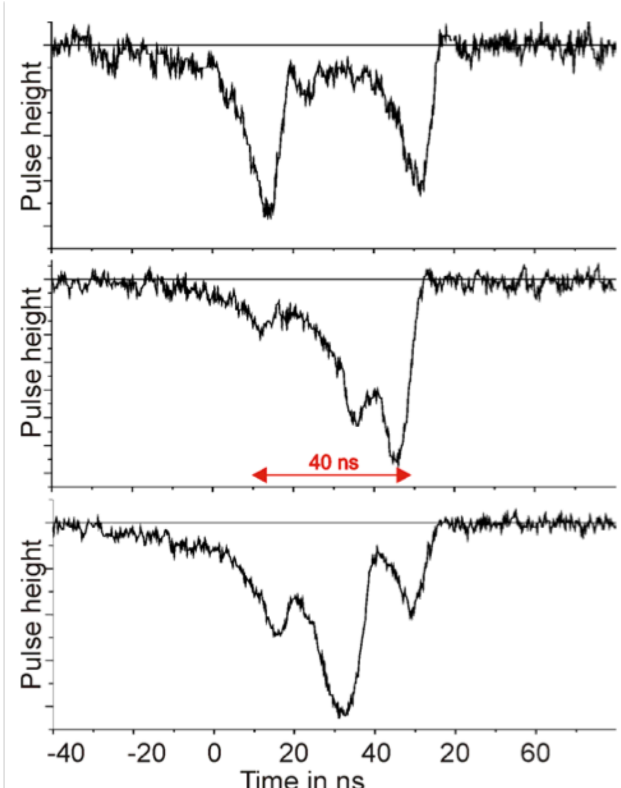
IT REQUIREMENTS

- Radial resolution < 130 µm
- Resolution along the beam direction < 500 µm
- Time resolution about 5 ns
- Momentum resolution σPt/pt ~0.5%
- Material budget X0~ 0.5% for each layer

The BESIII IT: GEM Detectors



Triple GEM signal example
[3 mm Drift Gap]



Signal shape to 350MeV Pions using a fast (2ns peaking time) amplifier.

Gas : ArCO2, 70/30 %
Drift Velocity : ~7.5cm/us @ 5kV/cm
Hence 3mm Drift ~ 40ns

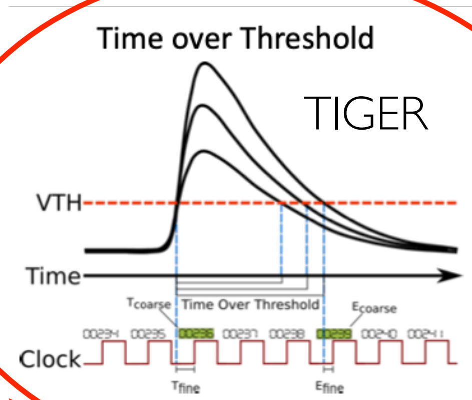
Signal Shape not predictable due to ionization clusters in the drift region

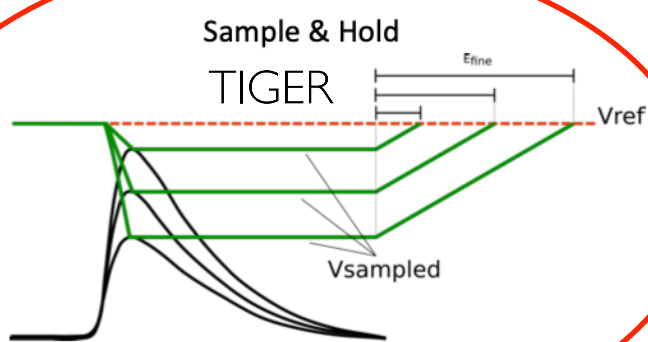
Paul Aspell - VFAT3 for the CMS GEM Muon upgrades
Alberto Bortone - Electronics readout for the CGEM - Inner Tracker: TIGER ASIC and electronics chain

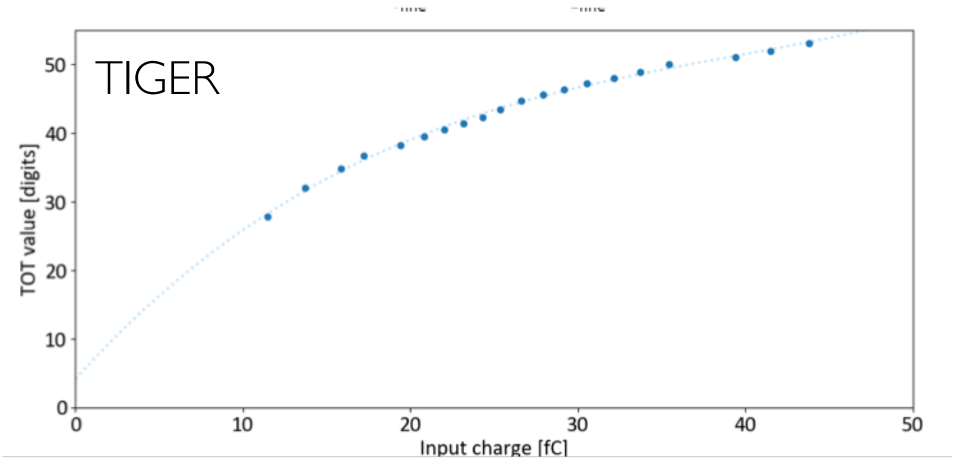
The BESIII IT: Space Resolution - the Charge Centroid Method

Gaussian Distribution

$$x_{CC} = \frac{\sum_i x_i q_i}{\sum_i q_i}$$

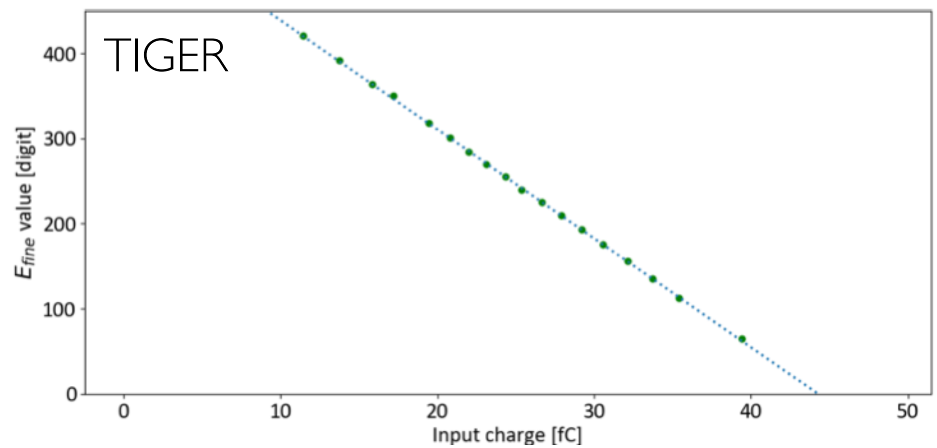






FAST

but sensitive to signal shape



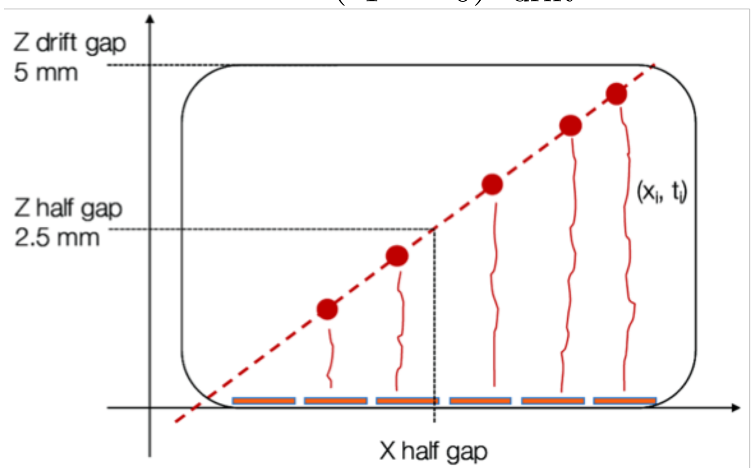
PRECISE

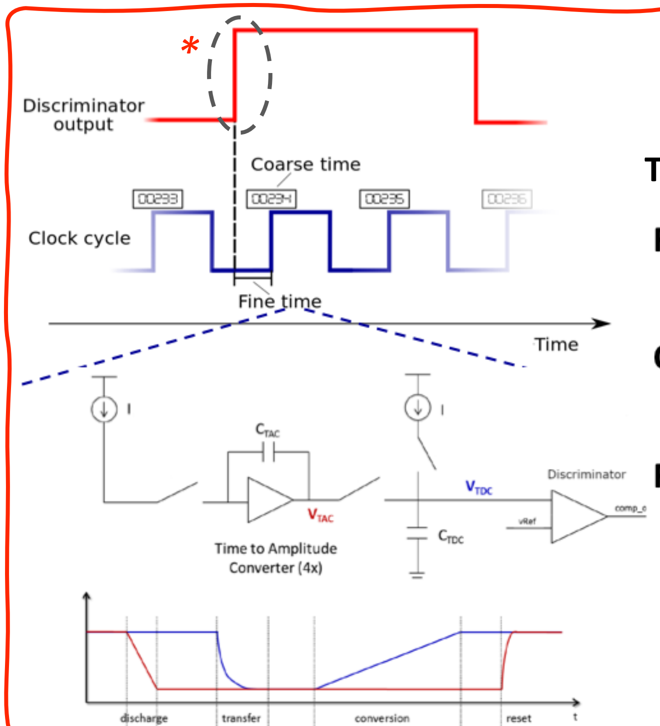
but slower and sensitive to shaping time (amount of collected charge)

The BESIII IT: Space Resolution - the µTPC Method

Improve Space Resolution

$$z = (t_1 - t_0)v_{\mathrm{drift}}$$





TIGER

Three accuracy levels (@ 160 MHz)

Frame-word

Clock counter cycles roll-over

204.8 µs time resolution

Coarse time

Hit clock cycle (16 bit counter)

6.25 ns time resolution

Fine time

Time to the next clock cycle

50 ps binning

T = *Coarse × 6.25 ns – (Fine-min) × binning*

4 TAC per shaper for event de-randomization

1 Wilkinson ADC per branch

Requirements

- *Overall time resolution must be enough good to resolve different arrival times*
- *Readout must be highly segmented*

* *Time measurement could limit the final spatial resolution accuracy*

F. Cossio, A mixed-signal ASIC for time and charge measurements with GEM detectors, Ph.D. thesis, PoliTO, 2019

Alberto Bortone - Electronics readout for the CGEM - Inner Tracker: TIGER ASIC and electronics chain

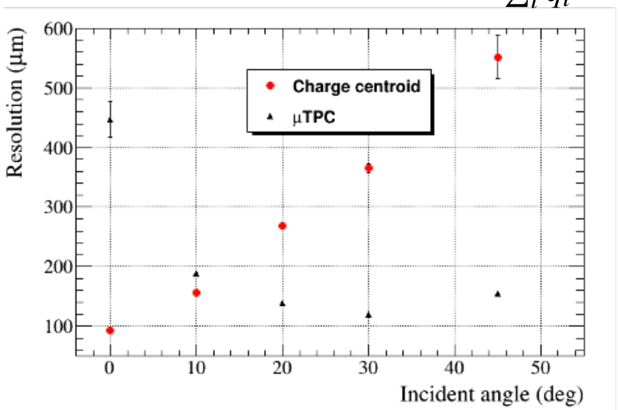
The BESIII IT: The TIGER ASIC

Time accuracy is limited by:

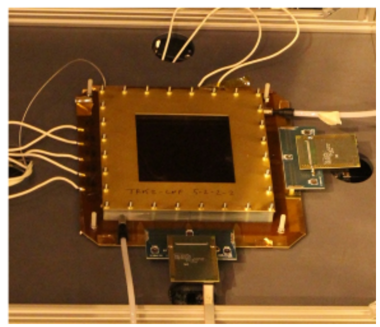
- *Signal jitter (due to noise)*
- *Time walk (due to amplitude variations)*

Charge measurement could be used to reduce the time-walk contribution (not easy because the input signal shape)

angle ≠ 0 and B = 0 $< x >= \frac{\sum_i x_i q_i}{\sum_i q_i}$



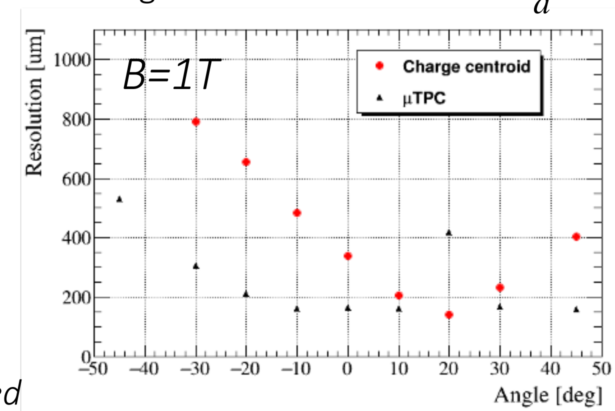
H4 line of SPS (CERN)



Ar/CO_2 – Lorentz Angle = 20 deg.

≈ 130 µm spatial resolution is obtained combining the two methods

angle ≠ 0 and B ≠ 0 $x = \frac{\frac{gap}{2} - b}{a}$



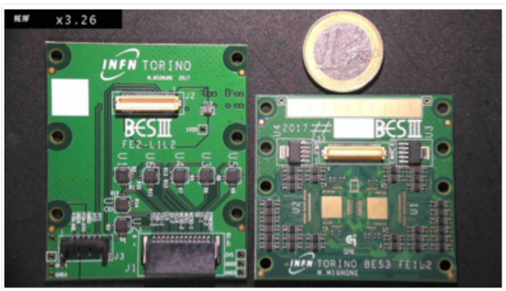
F. Cossio, A mixed-signal ASIC for time and charge measurements with GEM detectors, Ph.D. thesis, PoliTO, 2019

The Cylindrical GEM Inner Tracker of the BESIII experiment: prototype test beam results; Journal of Instrumentation, Volume 12, July 2017

Spieler: Radiation Detectors and Signal Processing – IV. Signal Processing Univ. Heidelberg, Oct. 10-14, 2005

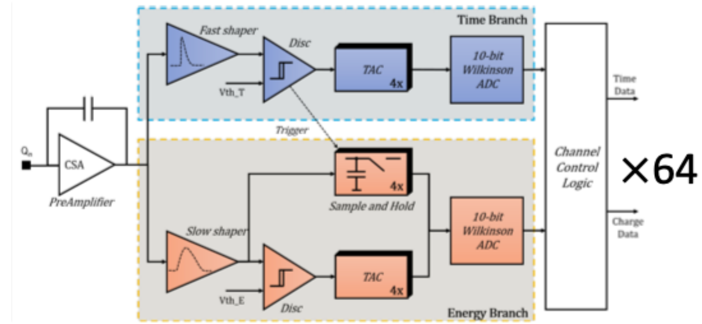
The BESIII IT: On Detector Electronics

THE TIGER ASIC

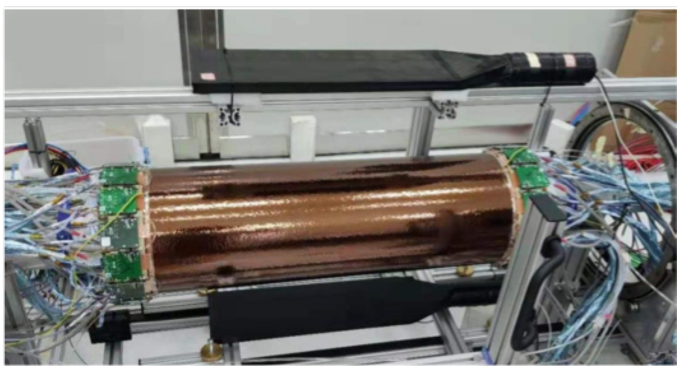


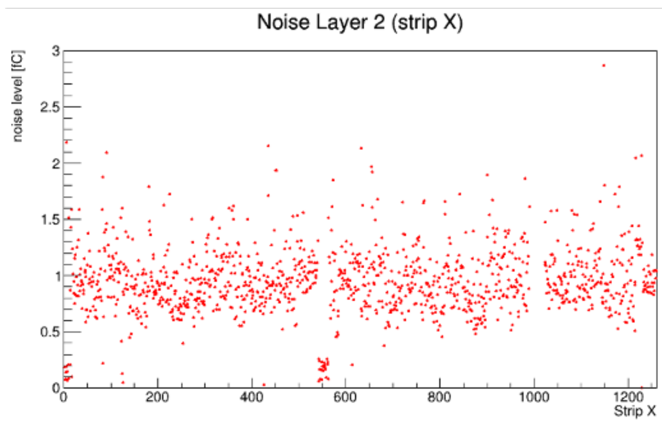
Chip features:

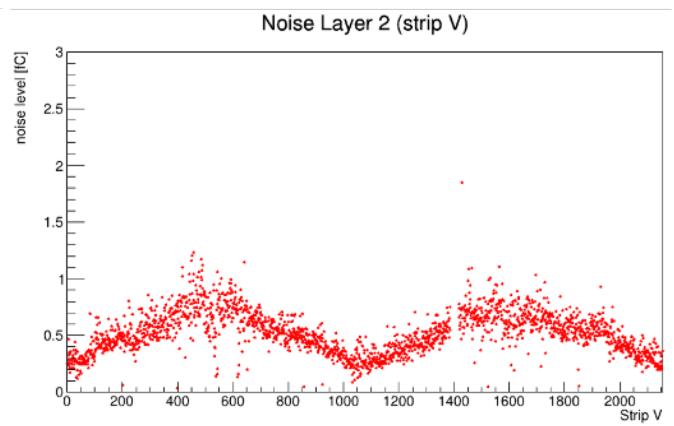
- 64 channels
- Power consumption < 12 mW/channel
- Sustained event rate 100 kHz
- Input dynamic range up to 50 fC
- Time resolution < 5 ns
- ENC < 2000 e$^-$ rms with 100 pF input capacitance
- Analog read out providing charge and time measurement
- Digital logic protected from single event upset (SEU)
- Tunable internal test pulse generator
- 110 nm technology



THE BEIJING SETUP (L1 & L2)

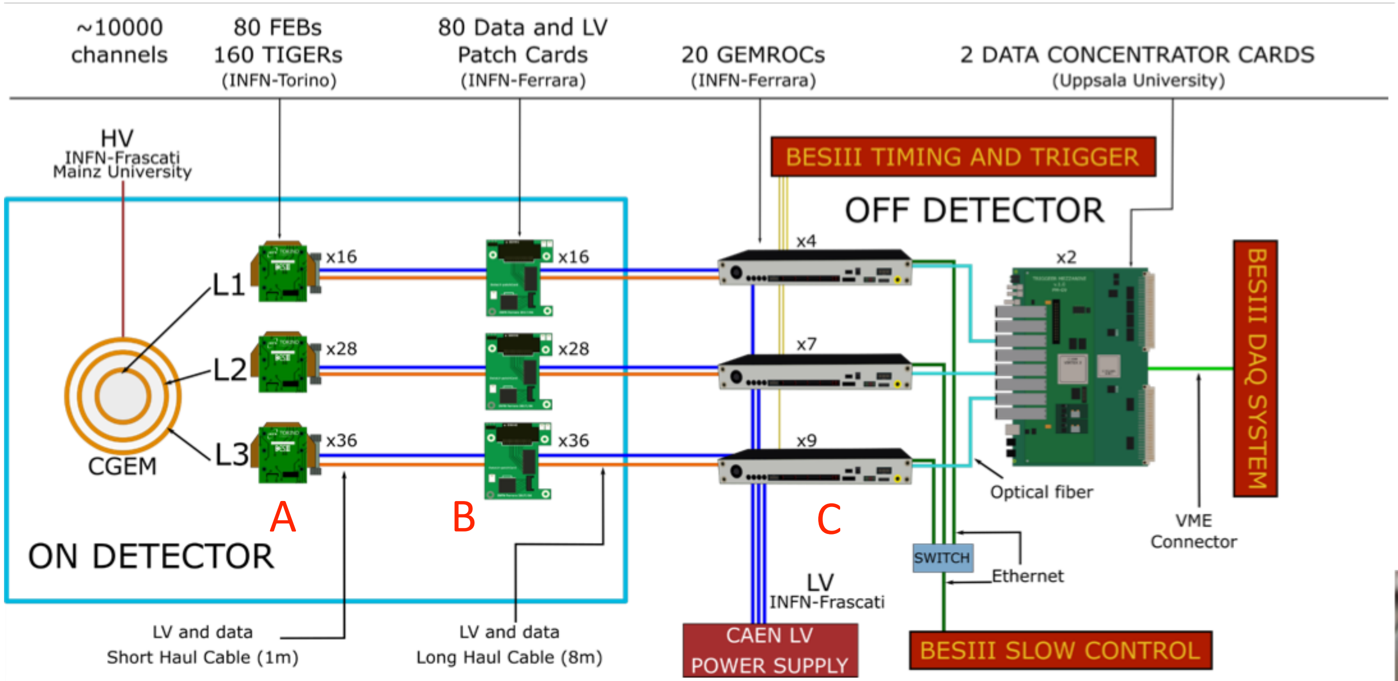


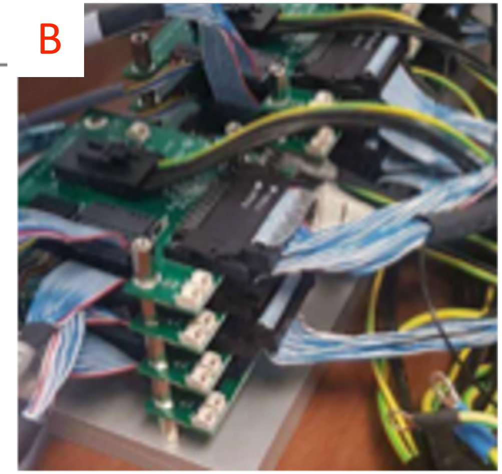


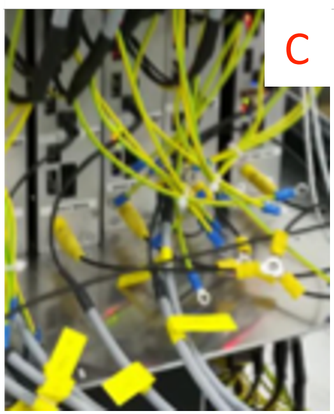


TIGER: A front-end ASIC for timing and energy measurements with radiation detectors in Nuclear Inst. And Methods in Physics Research, A924 (2019), pp 181-186

The BESIII IT: The Full RO Chain







THE IT READOUT CHAIN IS FULLY WORKING AND USED FOR COSMIC RAY DATA TAKING

TRIGGER: WITH or WITHOUT ?
The LHCb Muon Detector Case

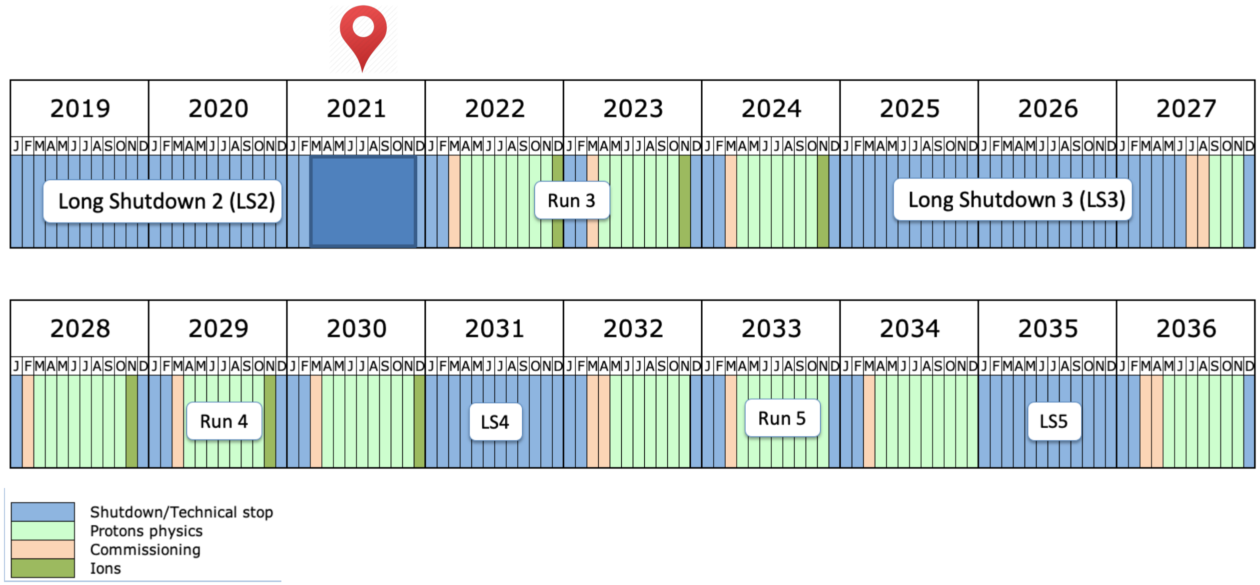
TRACKING: The KLOE-2 C-GEM IT
[A Binary Readout Detector]

TRACKING: The BESIII C-GEM IT
[Improve the Spatial Resolution]

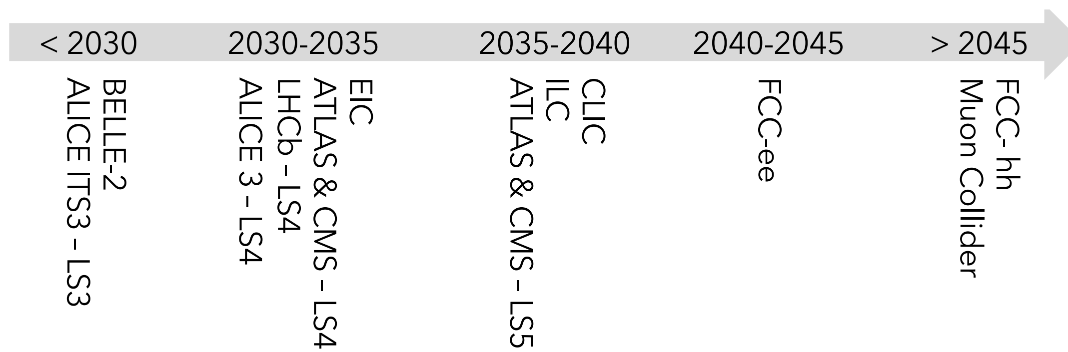
Upgrades

Conclusions

Upgrades



Upgrades and new collider projects timeline



[Requirements, emerging technologies and challenges for detectors and future colliders]

TRIGGER: WITH or WITHOUT ?
The LHCb Muon Detector Case

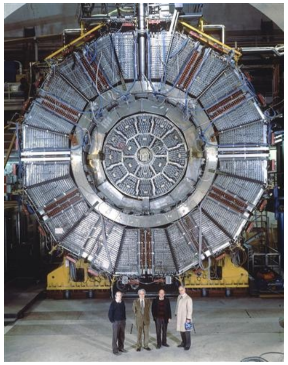
TRACKING: The KLOE-2 C-GEM IT
[A Binary Readout Detector]

TRACKING: The BESIII C-GEM IT
[Improve the Spatial Resolution]

Upgrades

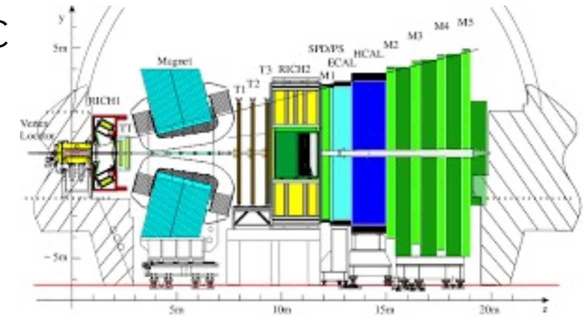
Conclusions

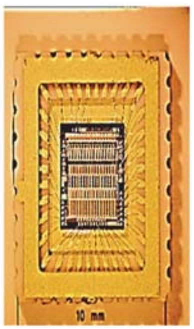
Conclusions: from 1988 to 2021



1988: ALEPH Experiment @ LEP
- ≈ 700 kchs
- ≈ 0.5 MB/s data thrghouput

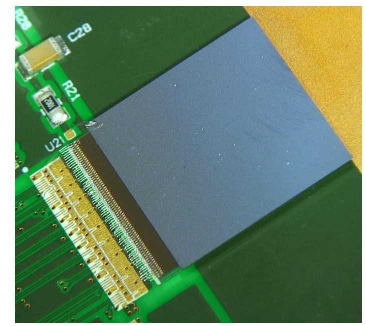
2021: LHCb Experiment @ LHC
- ≈ 1.1Mchs
- ≈ 50 GB/s data thrghouput





1986: UA1 & UA2
- AMPLEX: 16 chs for Silicon Pad detector
- 3 um technology

2021: LHCb
- VeloPix: 256x256 pixels
- 130 nm technology

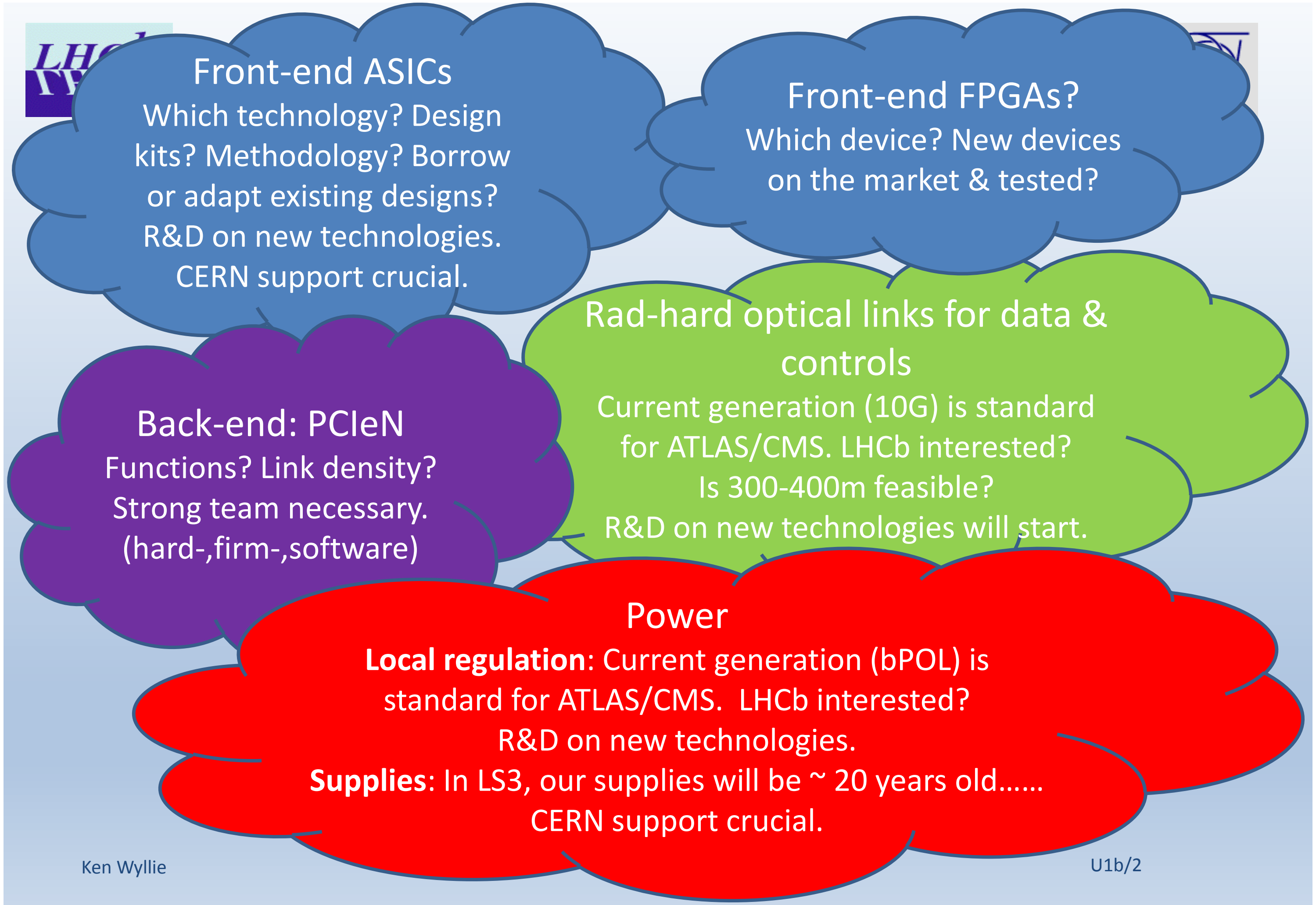


1985: XC2064
- 64 logic blocks
- 2 um technology

2021: VIRTEX UltraSCALE
- millions logic blocks
- 16 nm technology

LHC / HL LHC will extend beyond the 2040; what should we expect ?

Conclusions: many devices are (probably) going to change



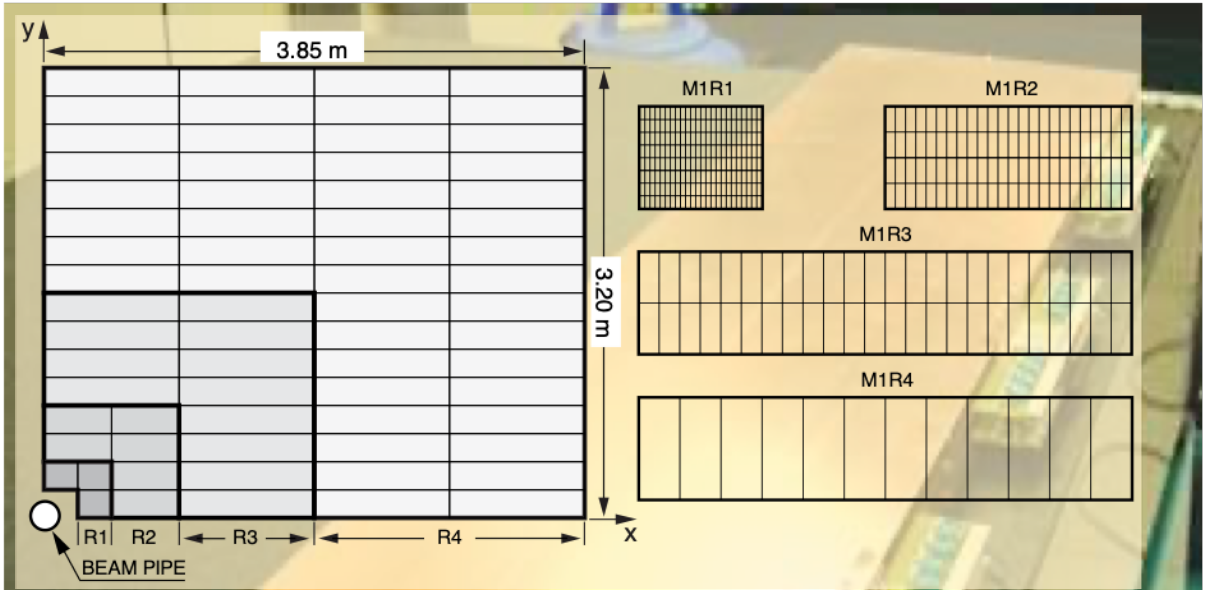
Conclusions: What do not change in Detector Instrumentation

- Know the detector (and readout electrode) features
  - If you have a GEM or R-WELL detector delivering for example 36 fC it does not mean you can use this value for S/N estimation; ex. you could have bidimensional readout and moreover you have to take into account the strip multiplicity and the gas gain fluctuation
- Know the behavior of the FEE devices
  - Input impedance value and stability (low input channel impedance minimize crosstalk and input time constant)
  - Front End performances degradation as a function of parasitic capacitance
  - Recovery time
- Minimize ground loops
  - Very rarely your on-detector asic/board will have the performances you measured in a test-bench when you installed them on the detector (in the worst case you can experience instability); use low-impedance and short connections to the reference plane as much as possible
- Work together the mechanical designer and the ASIC designers
  - Mechanical design are generally focused on the detector side design (tolerances, gas tight, materials etc), while, for example, for stable system working conditions we need low impedance connections to the detector reference electrode
  - Gas discharge: also the quietest gas detector can have gas discharges; ASIC designers must be conscious of the problem both for the input protection and for the recovery time
- High Voltage is not just a cable to connect to the detector
  - HV is connected to the most sensitive section of the detector
  - In most cases HVPS are not so quiet
  - HV long cables can pick-up noise

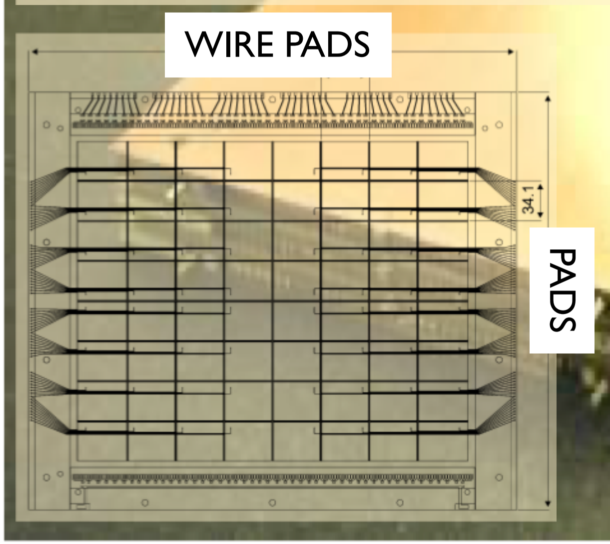
THANK YOU

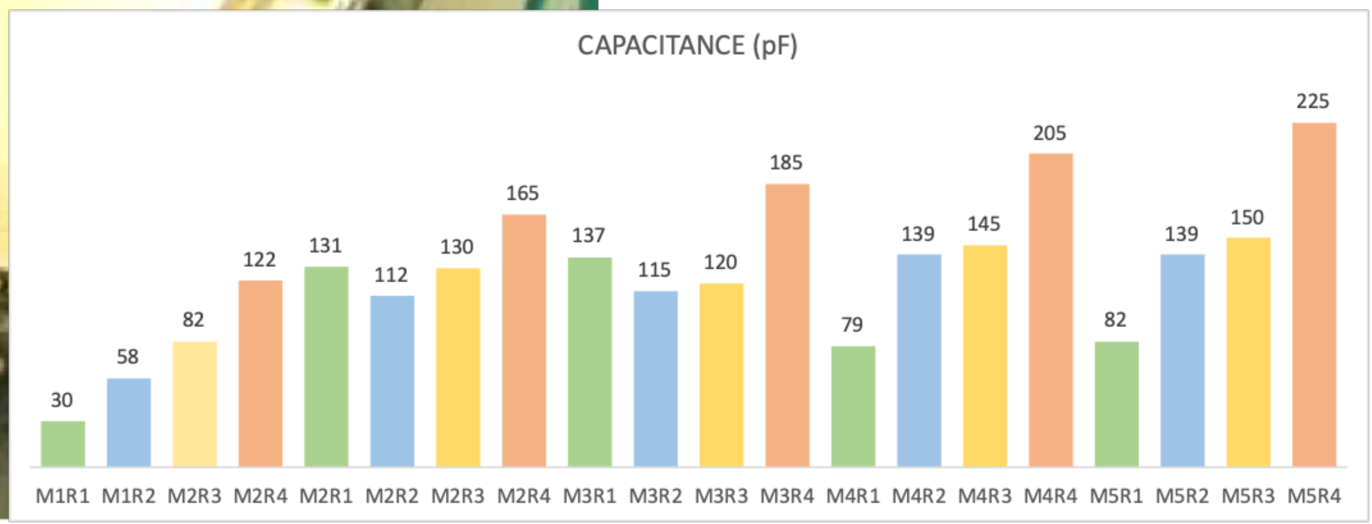
SPARES

LHCb Muon Detector - some details # I



Parameter	Design value
No. of gaps	4 (2 in M1)
Gas gap thickness	5 mm
Anode-cathode spacing	2.5 mm
Wire	Gold-plated Tungsten 30 μm diameter
Wire spacing	2.0 mm
Wire length	250 to 310 mm
Wire mechanical tension	0.7 N
Total no. of wires	$\approx 3 \cdot 10^6$
Operating voltage	2.5–2.8 kV
Gas mixture	Ar / CO_2 / CF_4 (40:55:5)
Primary ionisation	$\simeq 70\,e^-$/cm
Gas Gain	$\simeq 10^5$ @ 2.65 kV
Gain uniformity	±20% typical
Charge/MIP (one gap)	$\simeq$ 0.6 pC @ 2.65 kV





LHCb Muon Detector - CARIOCA

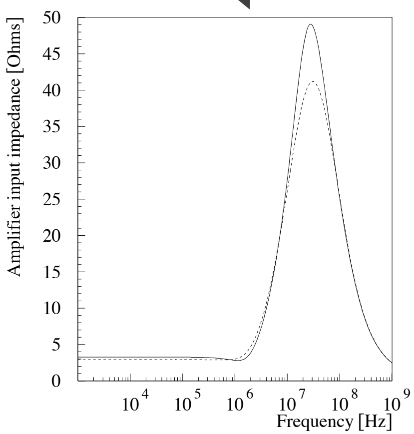
reduce crosstalk due to capacitive coupling between between contiguous channels
$Z_{IN} \simeq 50\ \Omega$

- Wire chamber full drift time ≃ 30 ns
- Charge collected in (the first) 10 ns:
  - 40 fC on the wire pads
  - 20 fC on the cathode pads

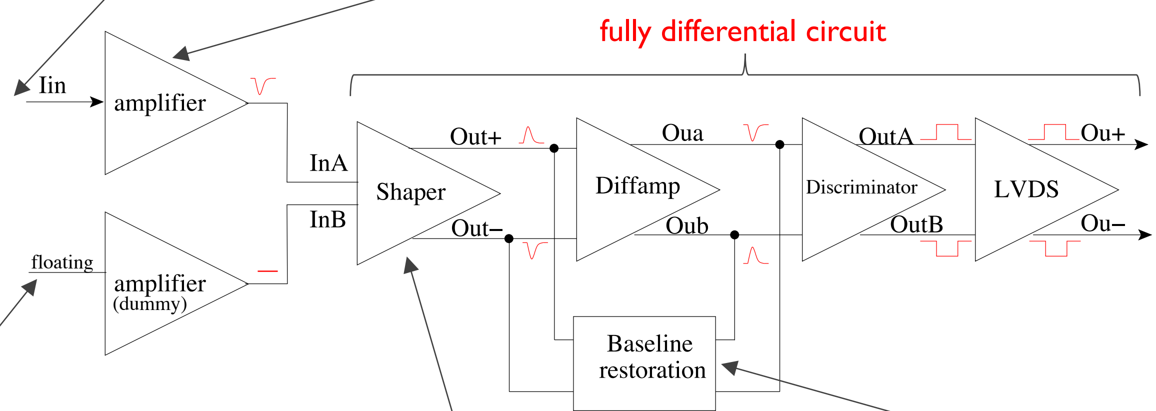
MWPC output

- Precision in muon arrival time measurement (< 3 ns)
- Fast rising edge detector output signal (t_r< 1 ns)

current mode amplifier for fast response



fully differential circuit



capacitive coupling to GND
$C_{COUPLING} \approx$ pad capacitance

amplifier & shaping
Long tail (ion mobility) ≈ 1/(t+1.5 ns)

non-linear baseline restorer
Reduce baseline fluctuations

CARIOCA-GEM: ion-cancellation tail circuit removed; shaping amplifier gain increased by a factor 1.5; 14 ns peaking time
NB: a spark protection circuit has been added to protect the preamplifier input

LHCb Muon Detector - FEE Operating Conditions

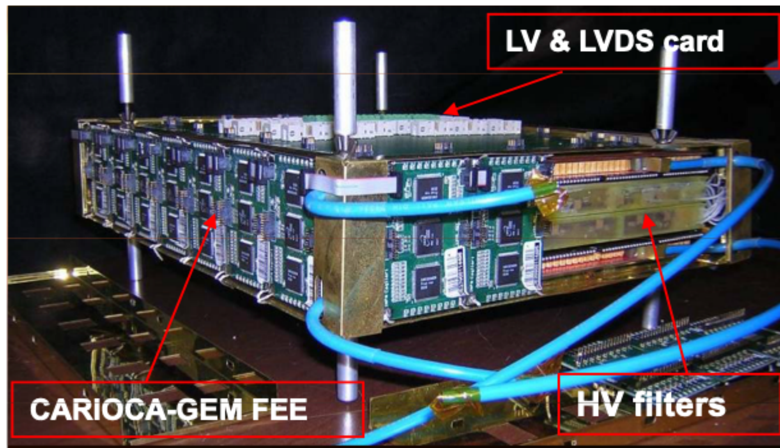
LHCb Muon System

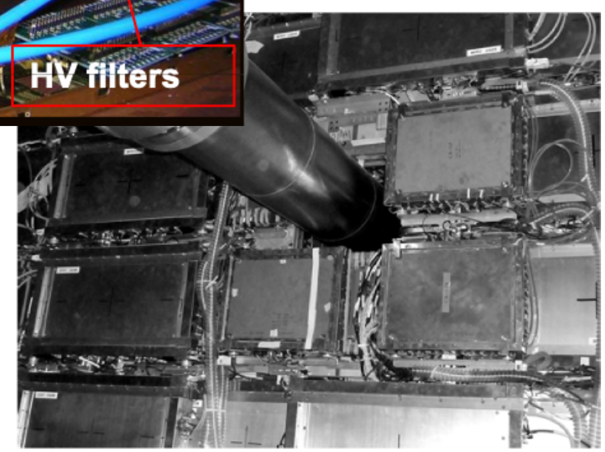
- *1368 MWPC with different size/readout*
- *≈ 120k readout channels*
- *Fine threshold tuning requires single channel setting*
- *Bias in the CARIOCA discriminator stage*

➡ *Single channel noise parameter simulation and measurement*

Threshold Scan

Region	Sensitivity mV/fC	C_{det} pF	*bias* reg.(fC)	ENC fC
M1R2	16	50	-	0.33
M1R3	13.4		-	0.40
M1R4	10.8		11 (2.39)	0.82
M2R1W	15	70	-	0.53
M2R1C	10	120	12 (2.82)	1.09
M2R2W	14	80	-	0.48
M2R2C	11	100	11 (2.35)	0.97
M2R3	11.7	66	11 (2.21)	0.89
M2R4	10		11 (2.58)	1.13
M3R1W	14	80	-	0.47
M3R1C	10	130	11 (2.58)	1.14
M3R2W	14	90	-	0.57
M3R2C	11	110	11 (2.35)	1.02
M3R3	11.5	72	11 (2.25)	0.93
M3R4	10		10 (2.35)	1.15
M4R1	15	70	10 (1.56)	0.60
M4R2	10.2	110	12 (2.76)	1.11
M4R3	10.1	115	13 (3.02)	1.18
M4R4	8.3	192	11 (3.11)	1.47
M5R1	15	70	11 (1.72)	0.62
M5R2	10	121	10 (2.35)	1.17
M5R3	9.6	137	12 (2.94)	1.27
M5R4	7	228	11 (3.69)	1.86



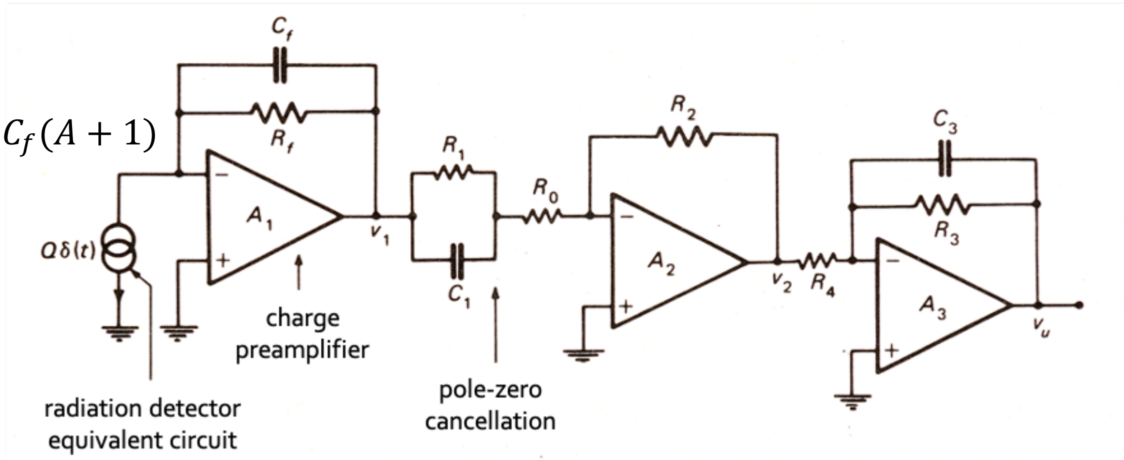


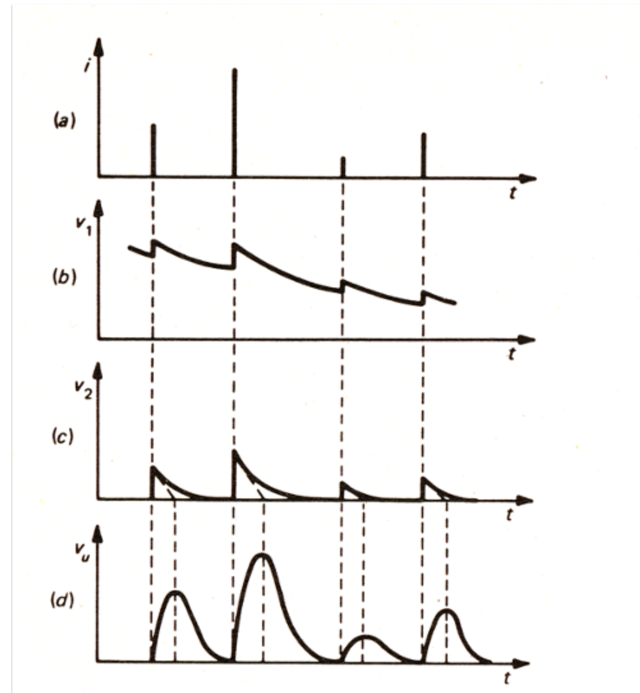
$$Th = \frac{Sens_{chmbtype}}{2.35} \cdot ENC \cdot S$$

S= safety factor (5 or 6)

A SHORT REMIND – SIGNAL PROCESSING ELECTRONICS

$C_i = C_f(A+1)$





ENC → Equivalent Noise Charge = input charge that produces an output amplitude equivalent to the output noise

Simplify the calculation of $\frac{S}{N} = \frac{Q}{ENC}$ $ENC^2 = F_p i_n^2 \tau + F_s C_d v_n^2 \frac{1}{\tau}$

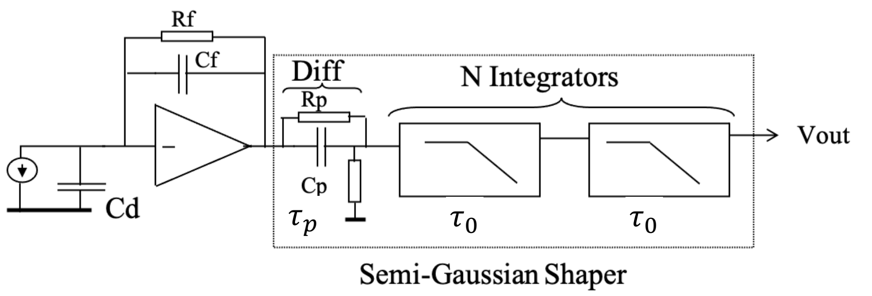
$\tau = shaping\ time;\ F_p\ \&\ F_s = shaper\ form\ factor$ parallel noise series noise

- NOTE: A = A(f)
- Parallel noise
  - detector leakage current
  - bias resistor
  - feedback resistors
- Series noise
  - Transistor gate noise
  - Device series resistance
  - Amplifier load resistor

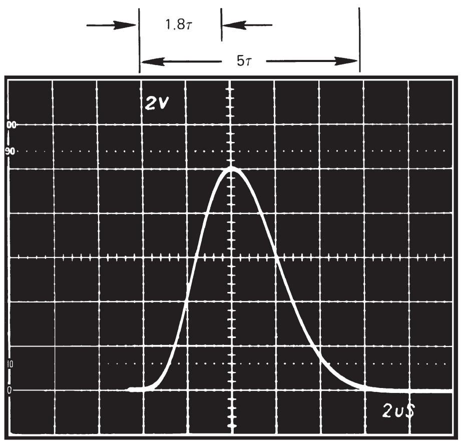
FRACTION OF INPUT CHARGE MEASURED: $\frac{1}{1+\frac{C_{det}}{C_i}}$

Assuming: A=10^3, C_f=1pF → C_i=1nF
- C_{det}=10pF : Q_i/Q_s=0.99
- C_{det}=500pF : Q_i/Q_s=0.67

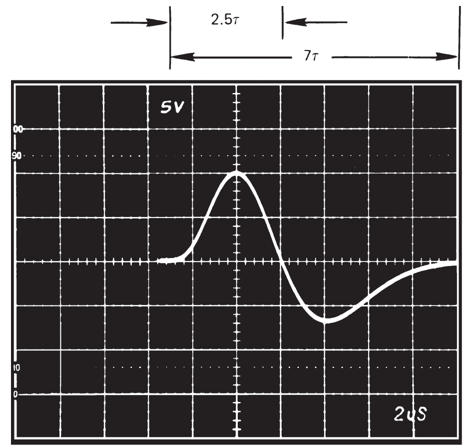
SEMI-GAUSSIAN PULSE SHAPING



$$V_{OUT} = \frac{Q}{C_f} \cdot \frac{1}{(1 + s\tau_f)} \cdot \left[\frac{(1 + s\tau_p)}{(1 + s\tau_0)}\right] \cdot \left[\frac{A}{(1 + s\tau_0)}\right]^n$$



a. Unipolar Output.



b. Bipolar Outputs.

SEMI GAUSSIAN SHAPING

- Improve signal to noise ratio (> 15%)
- Reduce pulse signal width (up to 50% with respect to the CR-RC filter)
- Reduce pulse dead time

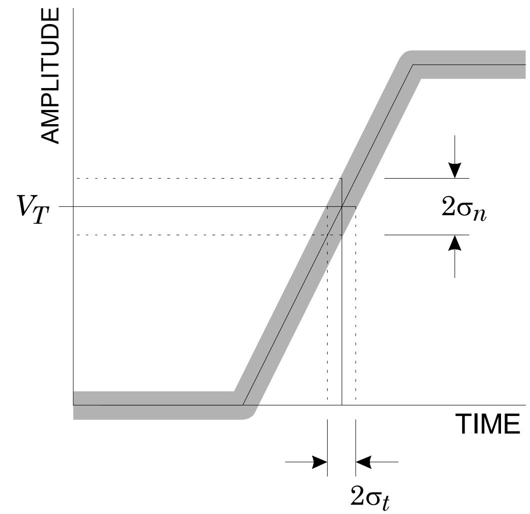
BIPOLAR SHAPING

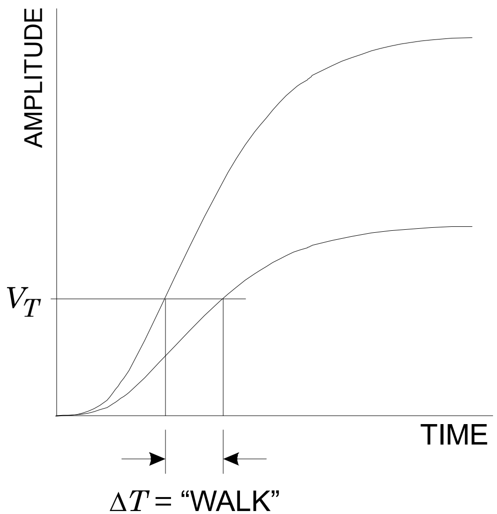
- Minimize baseline shift in AC coupled circuits for variable counting rate
- Timing applications (zero crossing)
- Worst S/N ratio

* From ORTEC

Discriminated Signal Output Jitter

$$\sigma_t = \frac{\sigma_n}{\left.\frac{dV}{dt}\right|_{V_T}} \approx \frac{t_r}{S/N}$$





- Fixed Threshold Trigger → threshold crossing time is a function of the signal amplitude
- For fixed rise time the time-walk can be compensated (in software) by measuring the pulse height
- The compensation method fails if both signal shape (i.e. rise time) and amplitude vary
- Time-walk can be reduced by setting low thresholds or using constant-fraction discriminator technique

Spieler: Radiation Detectors and Signal Processing – IV. Signal Processing Univ. Heidelberg, Oct. 10-14, 2005

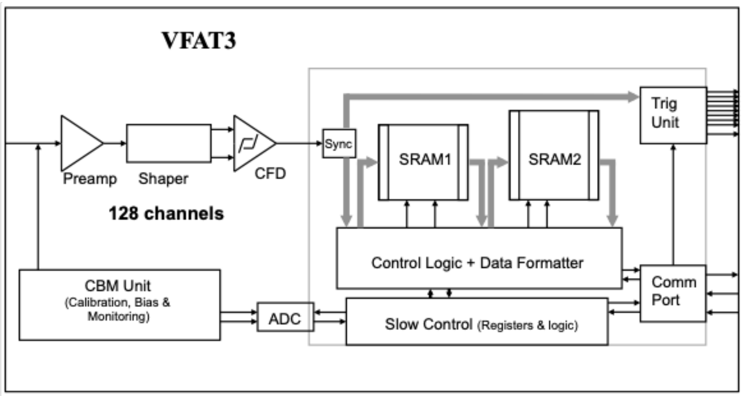
(AVAIBLE) DEVICES for μPattern Detectors

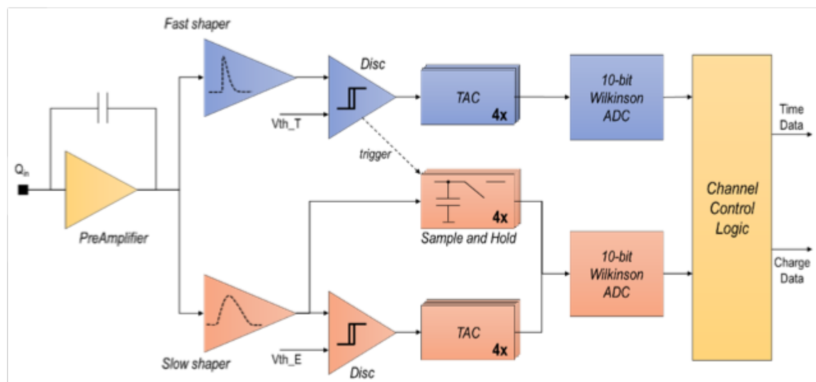
VFAT3 - CMS Upgrades (GEM Readout)

Channels	128
Signal charge polarity	positive/negative
Progammabe gain	1.25 - 50 mV/fC
Peaking time	25,50,75,100 ns
Detector capacitance range	9-88 pF
Dynamic range	20,50,100,200 fC
Linearity	<1% of dinamic range
Power consumption	<2.5 mW/ch
ENC	620-1079 + (about) 30e/pF
Comparator	LE/CFD
Timing Walk (CFD)	< 0.4 ns (3fC-30 fC)
LV1 Latency	0.025-25.6 us
LV1 rate	up to 2 MHz
Trigger	Fixed latency, 8 sLVDS pairs @ 320 Mbps
Trigger	Fast OR 2 channels
Zero suppression	
Compatible with GBTx and LpGBTx	
Radiation tolerant	

TIGER – BES IT

Channels	64
Power consumption	< 12 mW/ch
Sustained event rate	100 kHz
Input dynamic range	50 fC
Peaking time	60/170 ns
Charge and Time measurement	
ENC	2000 erms @100pF
Time resolution	<5 ns
TDC max rate capability	1 MHz (limited by pile-up)
4 LVDS links @ 200 MHz DDR	
Data Pushing back-end architecture	
Digital logic protected from SEU	
110 nm technology	



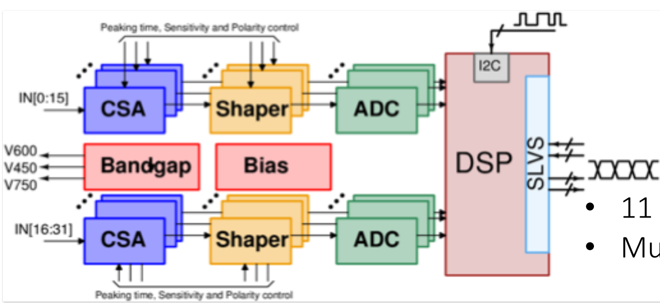


Paul Aspell - VFAT3 for the CMS GEM Muon upgrades
Alberto Bortone - Electronics readout for the CGEM - Inner Tracker: TIGER ASIC and electronics chain

(AVAIBLE) DEVICES for μPattern Detectors

SAMPA – ALICE TPC & MCH

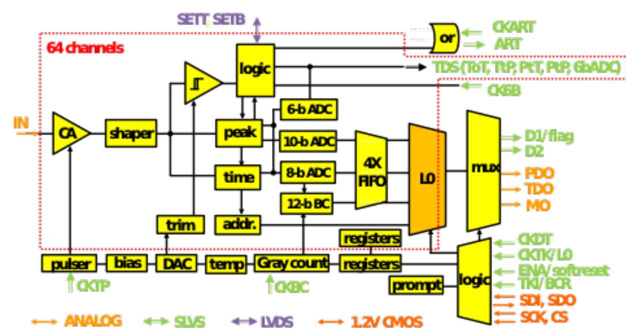
Specification	TPC	MCH
Voltage supply	1.25 V	1.25 V
Polarity	Negative	Positive
Detector capacitance (Cd)	18.5 pF	40 pF–80 pF
Peaking time (ts)	160 ns	300 ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 600 e@ts = 160 ns*	< 950 e@Cd = 40 pF* < 1600 e@Cd = 80 pF*
Linear Range	100 fC or 67 fC	500 fC
Sensitivity	20 mV/fC or 30 mV/fC	4 mV/fC
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts = 160 ns	< 0.2%@ts = 300 ns
ADC effective input range	2 Vpp	2 Vpp
ADC resolution	10-bit	10-bit
Sampling Frequency	10 (20) Msamples/s	10 Msamples/s
INL (ADC)	< 0.65 LSB	< 0.65 LSB
DNL (ADC)	< 0.6 LSB	< 0.6 LSB
ENOB (ADC)**	> 9.2-bit	> 9.2-bit
Power consumption (per channel) CSA + Shaper + ADC	< 15 mW	< 15 mW
Channels per chip	32	32



- 11 – 320 Mbps e-links
- Multiplexed channels

VMM3
(someone call it the "Swiss-Army" asic)

channels	64
Signal charge polarity	positive/negative
Gain	0.5,1,3,4.5,6,9,12,16 mv/fC
Peaking time	25,50,100,200 ns
Full baseline return	less than 600 ns
Detector Capacitance	few pF to 3 nF
Charge and Time measurements	
neighbor logic	
Fast outputs	
Power consumption	
Digitazion time	40/220 ns
TAC slope adj	60,100,350,650 ns
Readout Mode	Two phase mode Continous mode (4 MHz) Level 0 mode
Output Thrghouput	560 Mbps (8b/10 encoding)
Radiation tolerant	



VMM3, an ASIC for Micropattern Detector - 5th International Conference on Micro-Pattern Gas Detectors (MPGD2017)
SAMPA Chip: the New 32 Channels ASIC for the ALICE TPC and MCH Upgrades - Topical Workshop on Electronics for Particle Physics, Karlsruhe Institute of Technology (KIT)