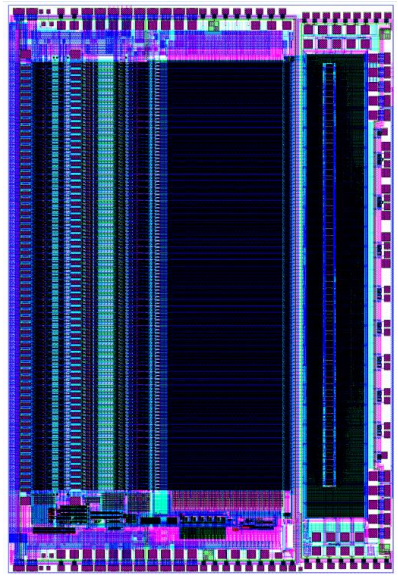
SMX2.2, a 128 Channel, Event-Driven Tracking Chip for Silicon and Gaseous Detectors

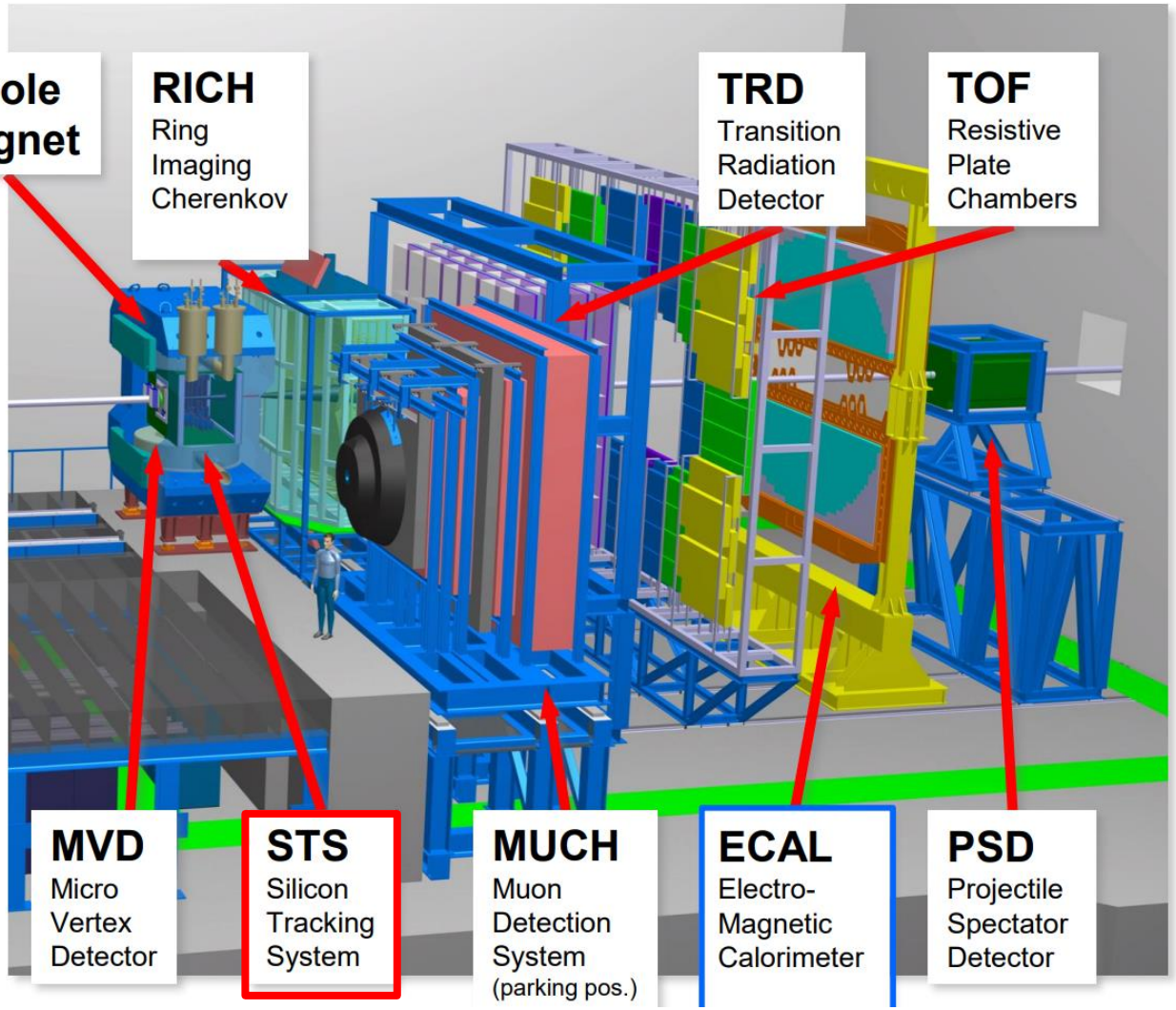


Krzysztof Kasinski, Robert Szczygiel, Weronika Zubrzycka, Rafal Kleczek, Piotr Otfinowski[1]
Ralf Kapell, Piotr Koczon, Joerg Lehnert, Anton Lymanets, Osnan Maragoto-Rodriguez,
Adrian Rodriguez-Rodriguez, Christian J. Schmidt, Carmen Simons[2]

for the CBM Collaboration

[1]AGH University of Science and Technology, Cracow, Poland
[2]GSI Helmholtzzentrum fuer Schwerionenforschung GmbH, Darmstadt, Germany

CBM Detector Structure

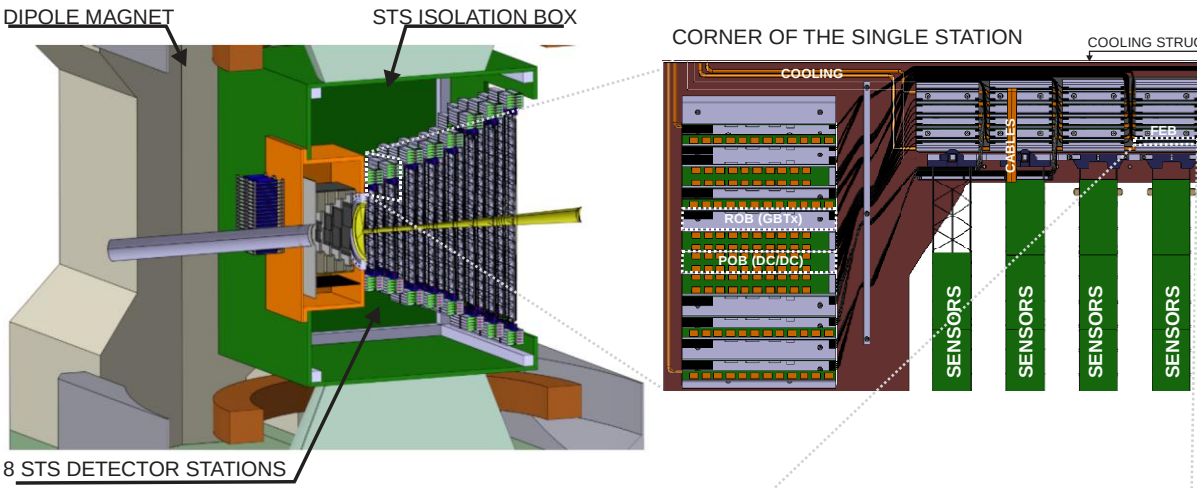


- Tracking acceptance: $2° < \theta_{lab} < 25°$
- Free streaming DAQ
- R_{int} = 10 MHz (Au+Au)

  $R_{int} \approx 0.5$ MHz
  full bandwith:
  Det. – Entry nodes
  reduced bandwidth
  Entry nodes – Comp. farm

  with
  R_{int} (MVD)=0.1 MHz
- Software based event selection

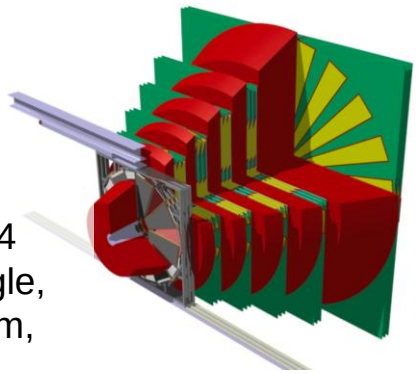
STS



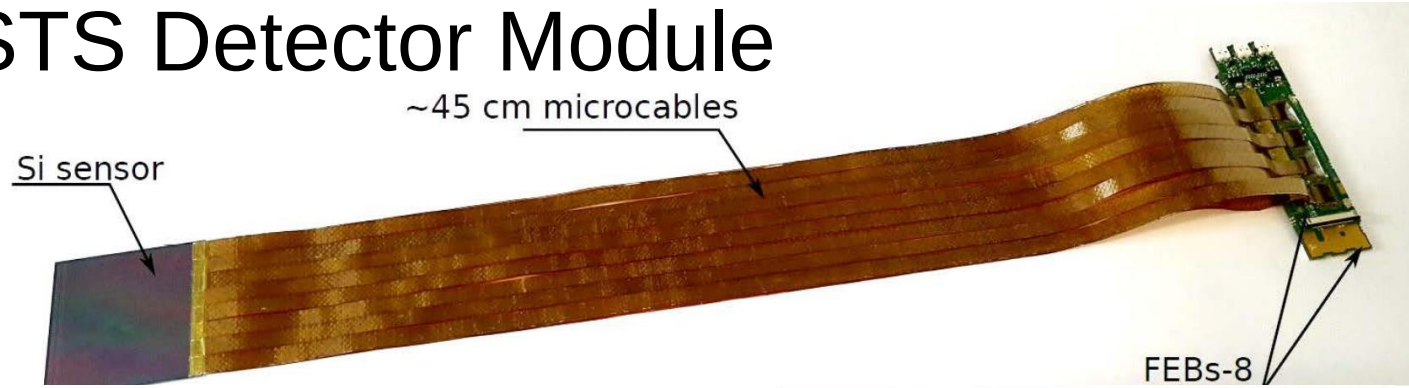
STS metrics:
>1 790 000 channels
>14 000 ASICs
1752 FEBs
600 ROBs, 78 DPB s

double–sided, micro-strip, 1024 channels per side, 7.5°stereo angle, **58 μm pitch**, lengths 20 - 120 mm, 300 μm thickness,

MUCH



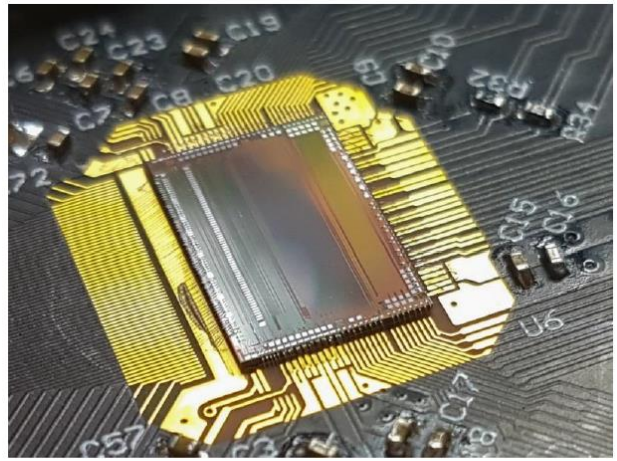
STS Detector Module



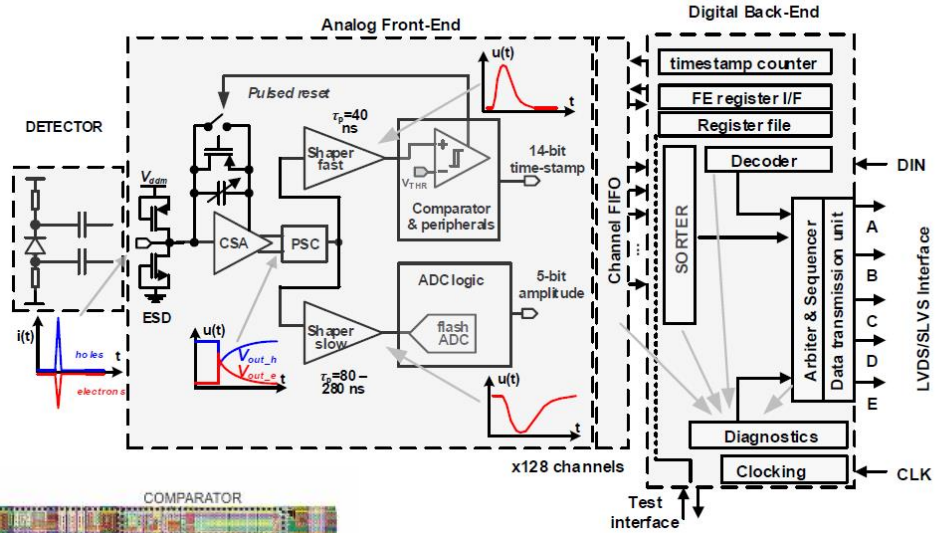
SMX2.2 chip

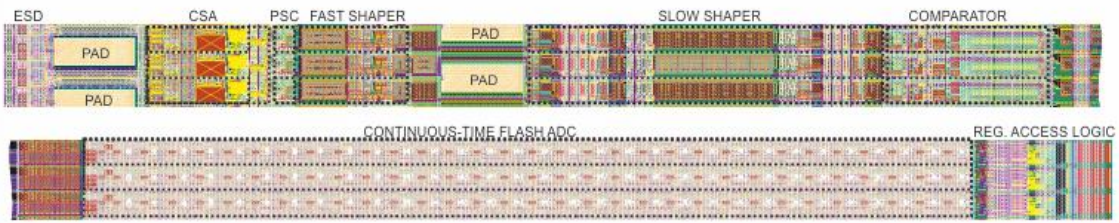
Features:

- Low power, self-triggering ASIC
- 128 channels + 2 test channels
- Time resolution ~ 5 ns
- Provides digitized hits with:
  - 5 bit Energy Resolution.
  - 14 bit Time stamp.
- Linearity range up to 15 fC
- Radiation hard layout



Parameter	Value
Process	180 nm CMOS MM/RF
Chip area	10.0 mm × 6.75 mm
Channel number	128 + 2 test
ADC bits	5
Input charge frequency	max. 500 kHz
Power Consumption: Uninitialized Initialized	0.6 – 1.2 W/chip 1.023 W/chip @ I_d=2 mA 8 mW/channel
Offset spread of fast channel	1.12 mV rms / 0.015 fC rms (after correction)
Offset spread of ADC [fC]	0.09 (before correction) [39] 0.02 (after correction)
Gain Fast shaper (STS) Slow shaper (STS)	 73 mV/fC 32.7 mV/fC
Gain spread: Fast shaper Slow shaper	 0.8 % 0.5 % (after calibration)
Slow shaper peaking time [ns]	90 / 180 / 262 / 332
Yield	>91% (146 ASICs tested on PCBs)





History

STS-XYTER 1.0 First full-size prototype. CBM-net compatible.

STS-XYTER 2.0 **Key changes:** back-end re-design for GBTx, multiple functional improvements. Added VREFT (common ADC threshold). STS/MUCH gain switching. Pogo-prober suport.

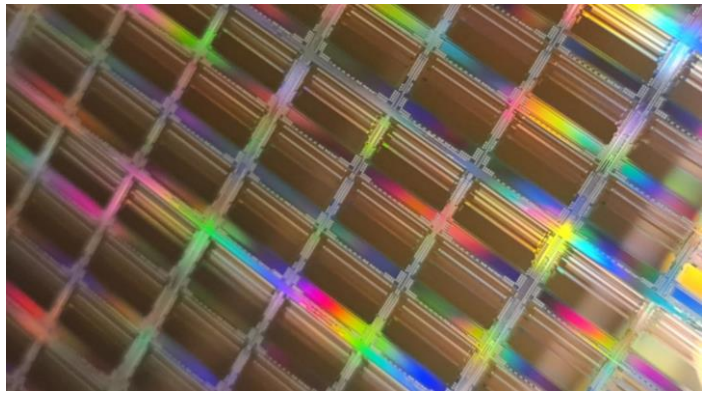
STS-XYTER2.1 was fabricated on 2018 MPW run and thoroughly tested (LAB, mini-STS, irradiation sessions). **Key changes:** Removed MOS-based ESD protection, external ESD-TEST IC to test different protection approaches. Improved layout SEU/TID. VREFT improved resolution. Noise improvements (e.g, reduced series R on-chip). Biasing Improvements (even/odd discrepancies). STS/MUCH calibration support. Added on-chip diagnostic ADC.

- STS-XYTER2.2 Was fabricated and delivered Sept 2020. Full Reticle Engineering run.

Thoroughly tested (system-level, irradiation).

Changes:

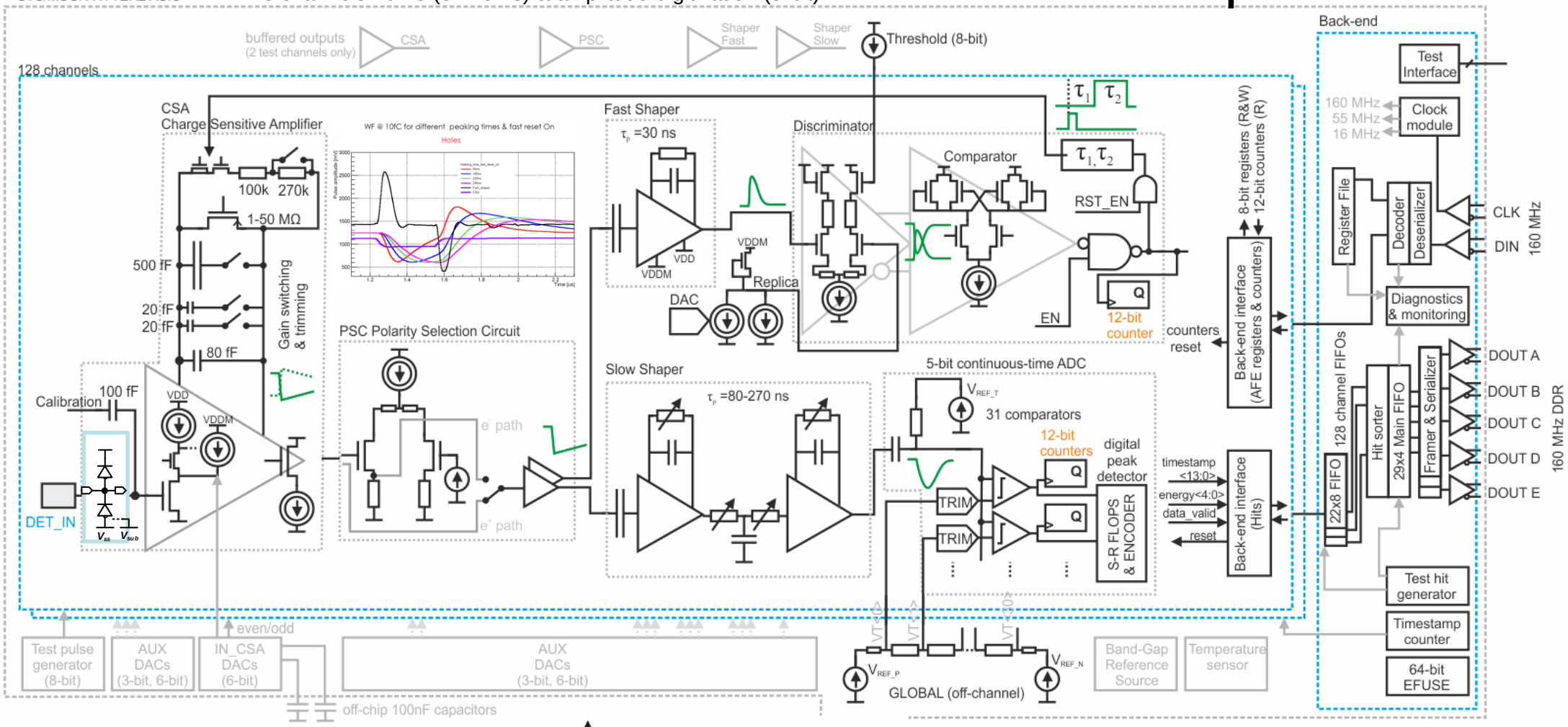
- Diagnostic: more potentials added for on-chip monitoring (all VDDs)
- Layout: reduce risk of short during bonding of digital power
- Analog: implement diode-based ESD protection of the inputs
- Analog: reset timing modification
- Digital: fix read-back of 5 registers



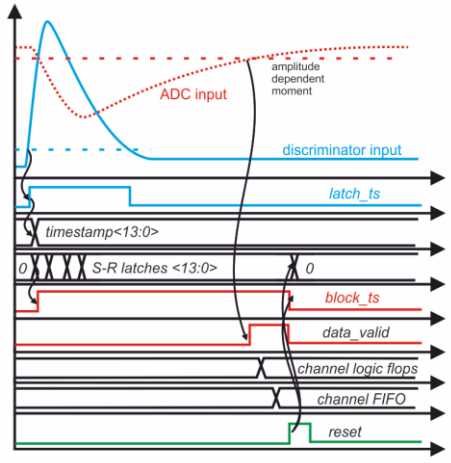
SMX 2.2 Chip architecture

STS/MUCH-XYTER2 ASIC

128 channels - time (3.125 ns) & amplitude digitization (5-bit)



0-12 fC electrons & holes (STS)
gain switching & trimming
250 khit/s rate (pulsed reset)
80-280 ns shaping time (slow path)
time-walk corrected offline
continuous-time ADC + peak det.
P=8.5-10 mW/channel (incl. logic)



SELF-TRIGGERED MODE

Back-end:

- control via synthesized reg & AFE DICE cells
- 9.41 – 47 Mhit/s/ASIC data BW
- dedicated protocol
- throttling, diagnostic features
- link loopback (multi-level)
- 64-bit e-fuse for traceability

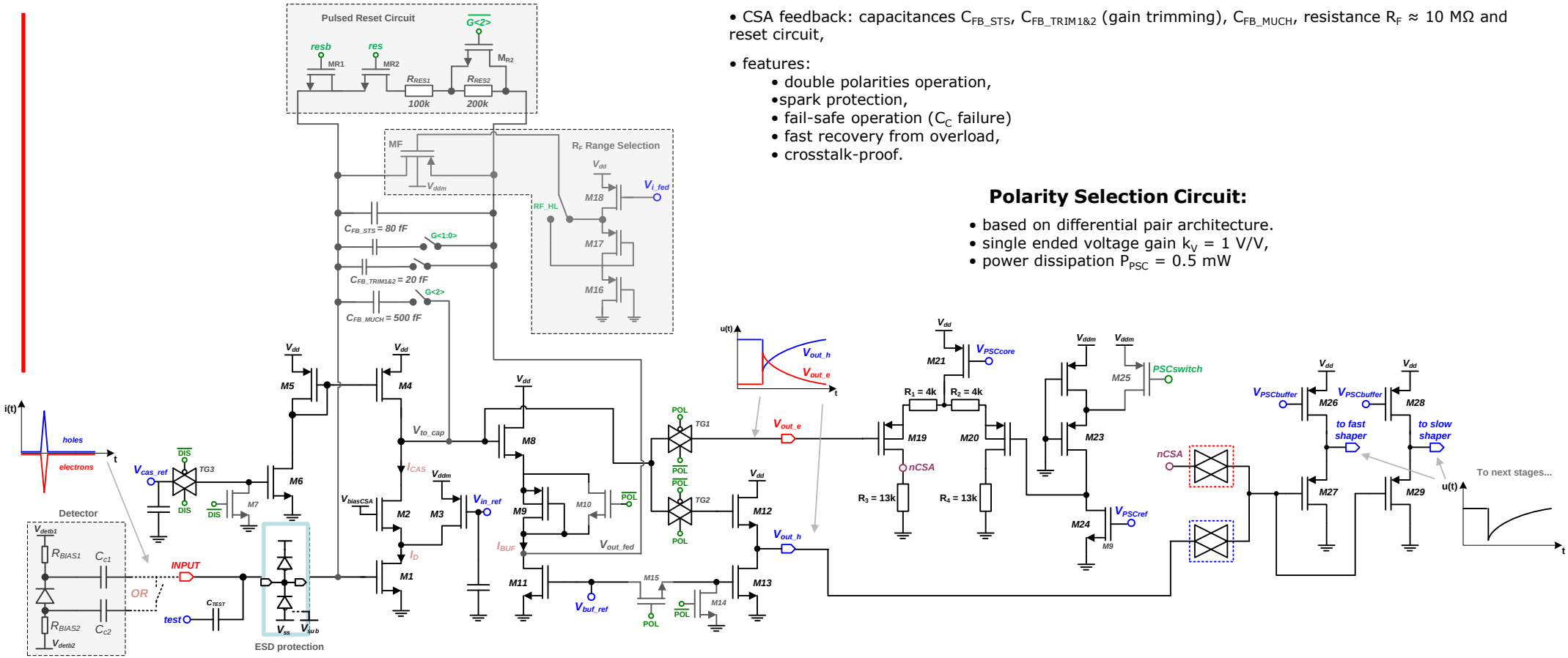
Front-end of the STS/MUCH-XYTER2.2

Charge Sensitive Amplifier:

- based on the direct cascode architecture:
  - input branch current range 0 – 3.9 mA (def. 2 mA),
  - cascode branch current range 0 – 70 μA (def. 30 μA)
  - parameters for default settings: voltage gain k_V = 4.8 kV/V, GBW = 9.1 GHz, power dissipation P_{CSA} = 2.7 mW,
- charge gain: k_q = 9.4 mV/fC for STS mode and k_q = 1.67 mV/fC for MUCH mode,
- CSA feedback: capacitances C_{FB_STS}, $C_{FB\_TRIM1\&2}$ (gain trimming), C_{FB_MUCH}, resistance $R_F \approx 10$ MΩ and reset circuit,
- features:
  - double polarities operation,
  - spark protection,
  - fail-safe operation (C_C failure)
  - fast recovery from overload,
  - crosstalk-proof.

Polarity Selection Circuit:

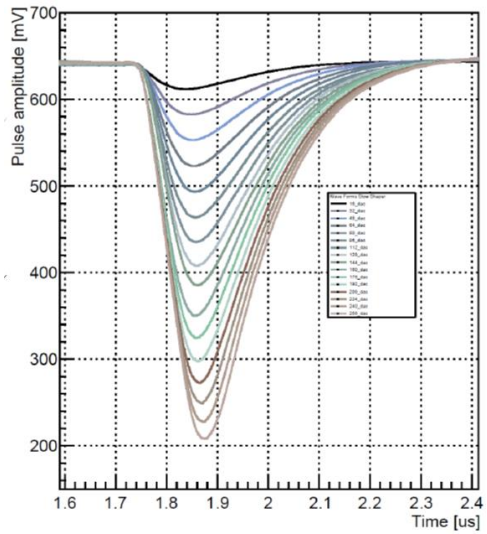
- based on differential pair architecture.
- single ended voltage gain k_V = 1 V/V,
- power dissipation P_{PSC} = 0.5 mW

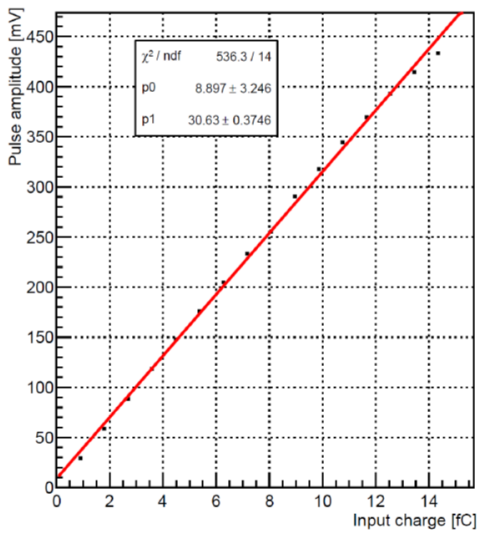


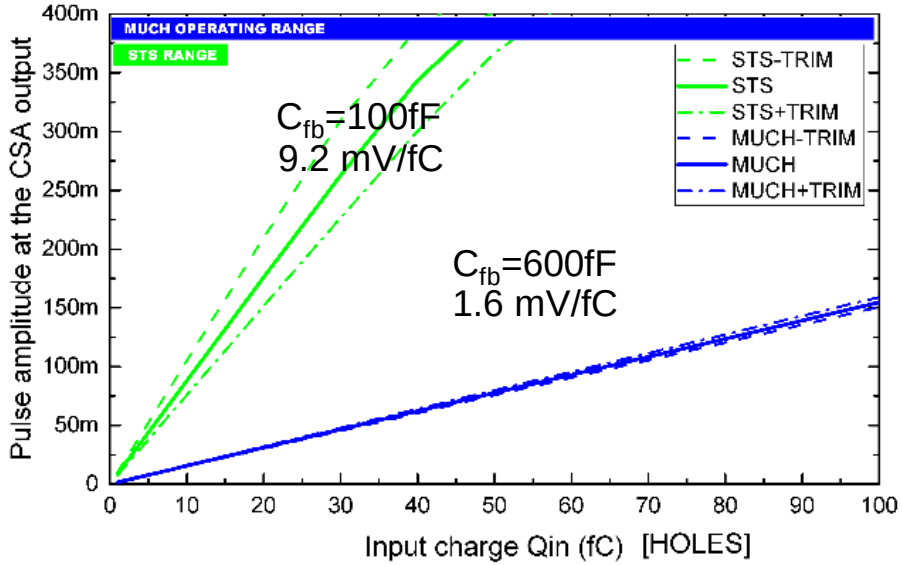
The input stage architecture details: Charge Sensitive Amplifier (CSA) + Polarity Selection Circuit (PSC).

Measurements: Analog waveforms

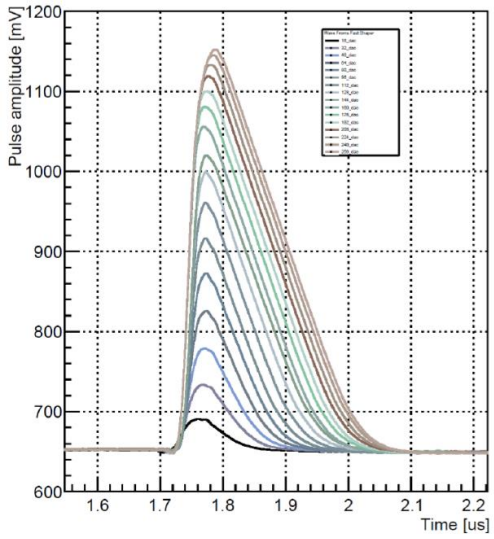
Slow shaper (STS mode)

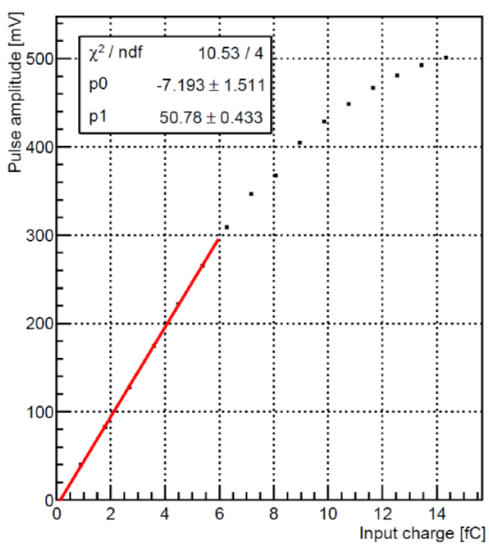




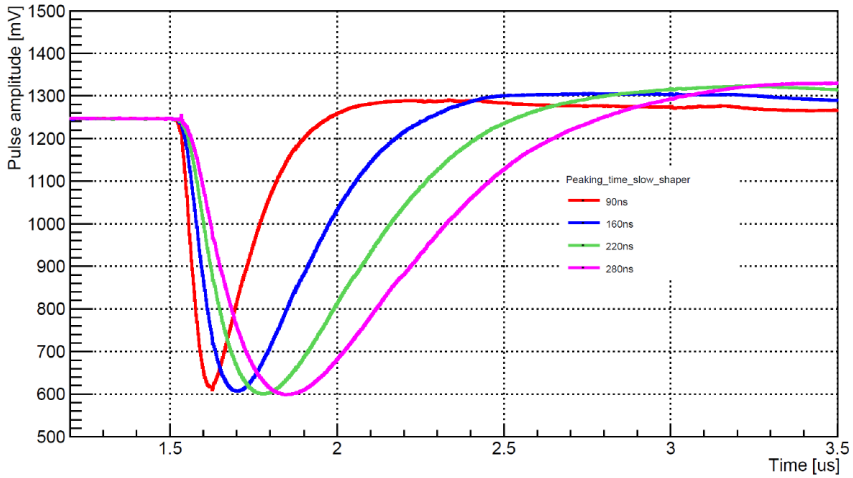


Fast shaper (STS mode)





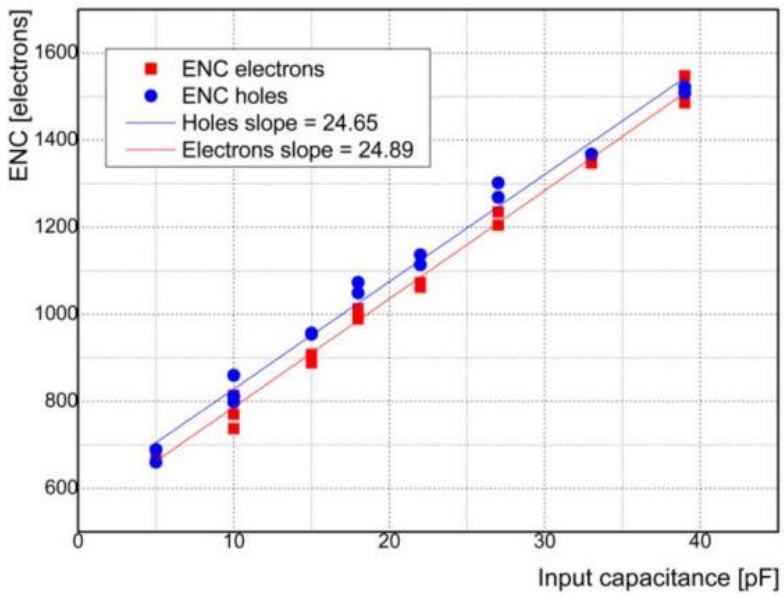
Selectable peaking time: 90 ns – 280 ns

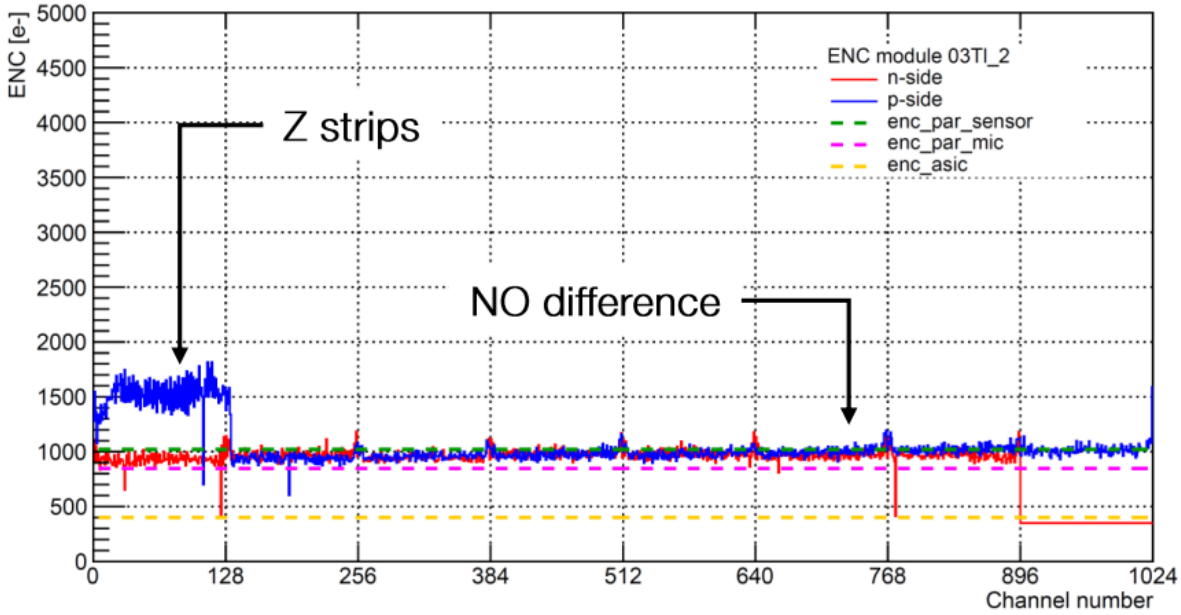


Optimization towards varying dominant noise contributors.

Measurements: selectable peaking times and fast reset

ENC vs Input Capacitance



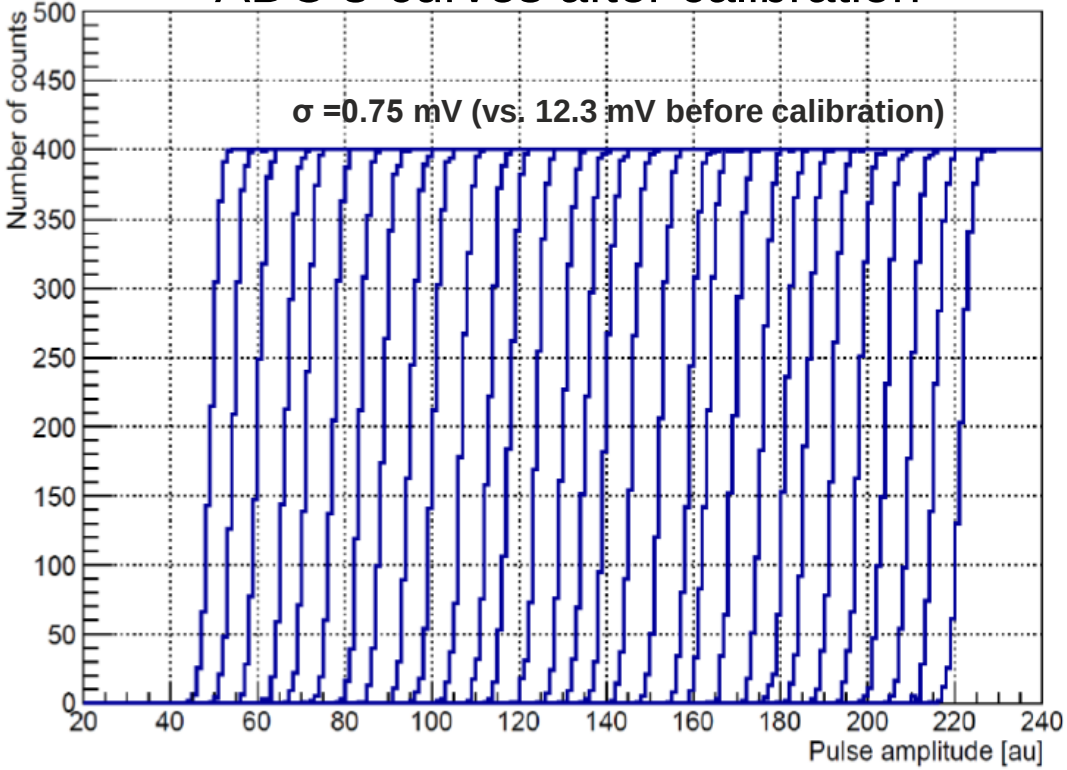


LADDER

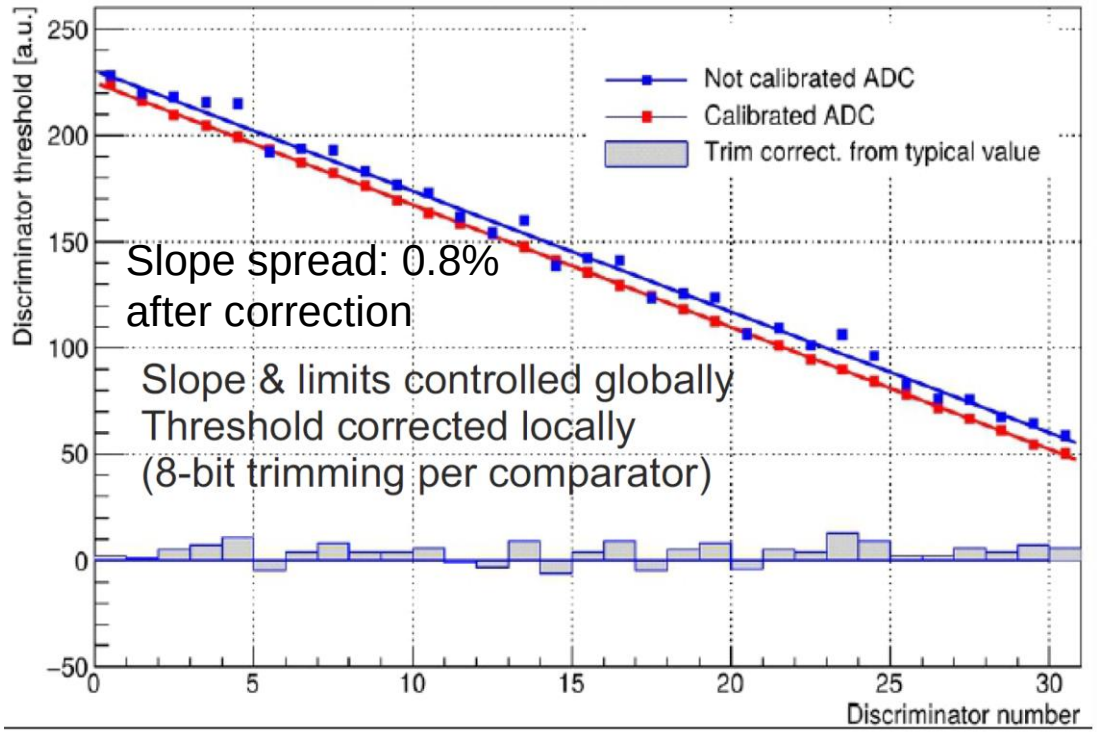
Baseline: 300e-
Slope: 25 e-/pF
Noise@ 10pF: 800e-
Noise in the system: 1000e- RMS

Measurements – in-channel 5-bit ADC

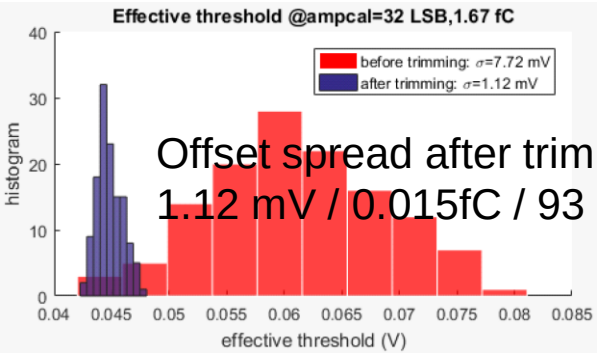
ADC s-curves after calibration



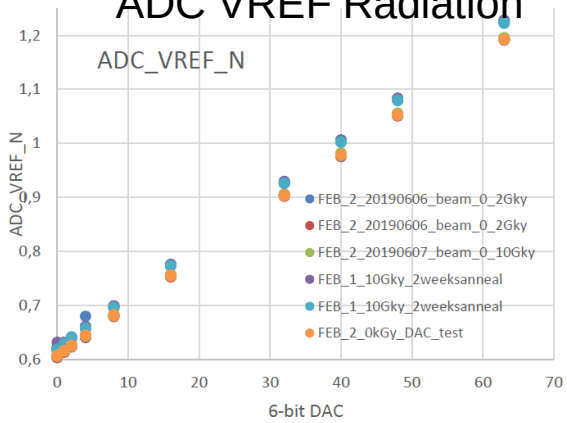
ADC Linearity



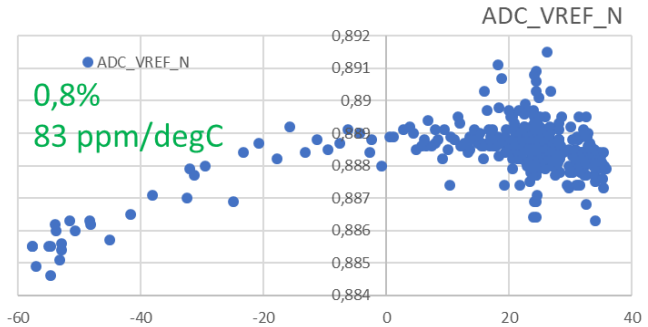
Fast comparator offset calibration



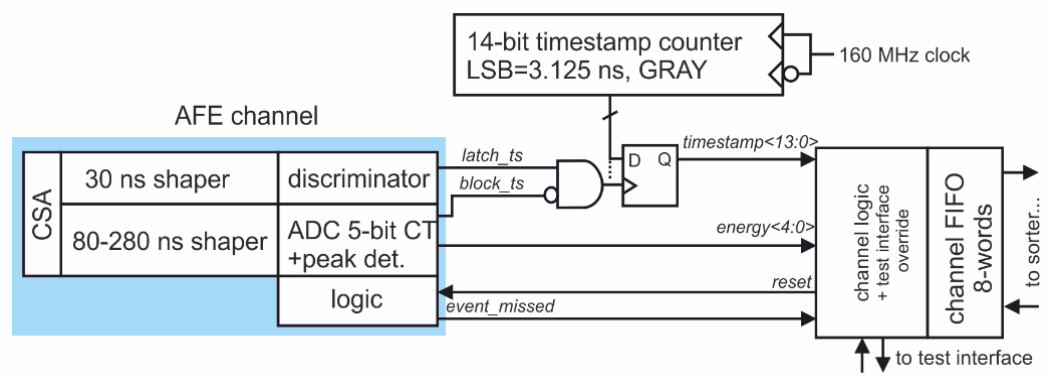
ADC VREF Radiation



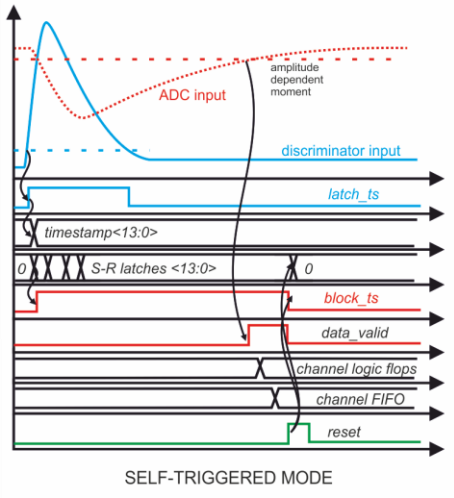
ADC VREF Tempco

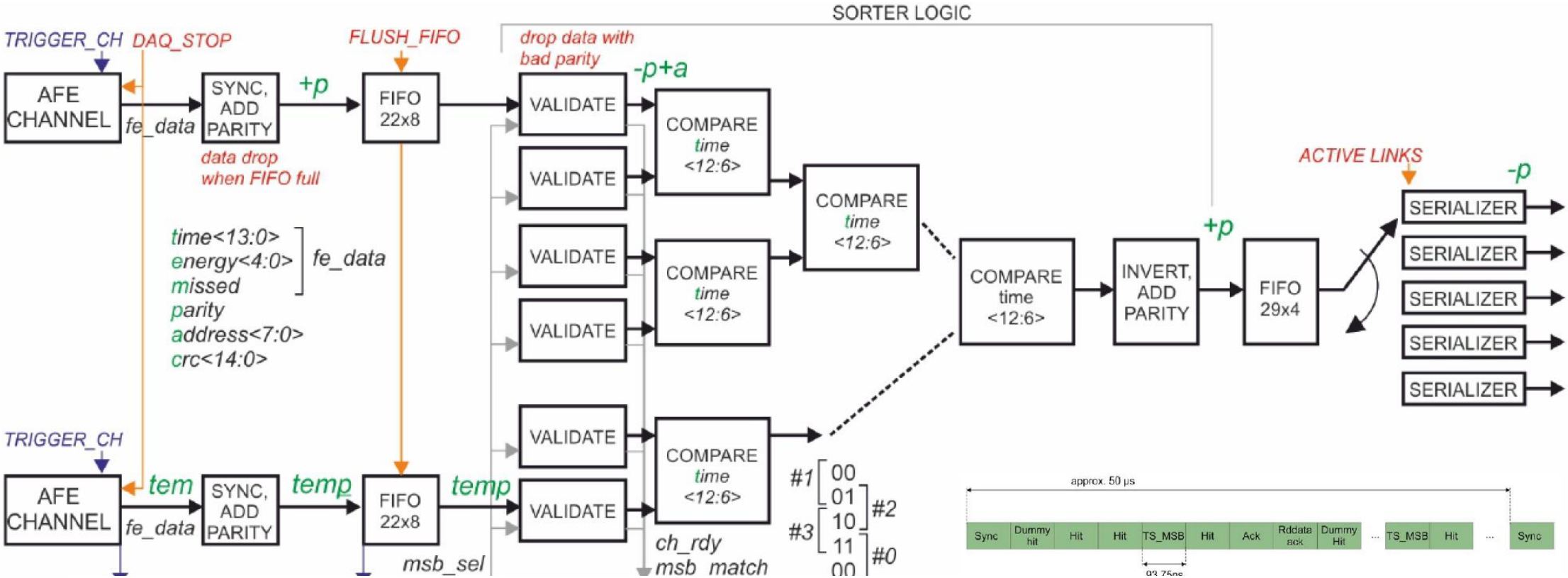


Back-end, data path



Hit data: 27 bits
7-bit channel address
5-bit energy
14-bit timestamp
1-bit event_missed flag





Hit data throughput: 9.41 Mhit/s/link
(Up to 47 Mhit/s/ASIC ; 320 Mbps/link)

Summary

- STS-XYTER series was thoroughly tested during recent years.
- Production candidate, SMX2.2 (2020) has implemented mostly cosmetic changes.
  - Key features:
    - Switchable gain to support silicon and GEM sensors
    - Continuous-Time 5-bit ADC with digital peak detector
    - Triggerless Read-out with custom protocol
    - Baseline restoration using pulsed reset

Thank you for your attention

JOURNAL PAPERS:

K. Kasinski, R. Szczygiel, W. Zabolotny, Back-end and interface implementation of the STS-XYTER2 prototype ASIC for the CBM experiment, Journal of Instrumentation, 2016 vol. 11 art. no. C11018.

K. Kasinski, R. Szczygiel, W. Zabolotny, J. Lehnert, C.J. Schmidt and W.F.J. Müller, A protocol for hit and control synchronous transfer for the front-end electronics at the CBM experiment, Nucl. Instrum. Meth. A 835 (2016) 66.

K. Kasinski, P. Koczon, S. Ayet, S. Löchner, C.J. Schmidt, System level considerations for the front end readout ASIC in the CBM experiment from the power supply perspective, J. Instrum. 12 (2017) C03023. http://stacks.iop.org/1748 0221/12/i=03/a=C03023

W. Zubrzycka, K. Kasinski, Leakage current induced effects in the silicon microstrip and gas electron multiplier readout chai n a nd their compensation method, Journal of Instrumentation, 2018 vol. 13 art. no. T04003, s.s.[2], 1 10.

K. Kasinski, A. Rodriguez Rodriguez, J. Lehnert, W. Zubrzycka, R. Szczygiel, P. Otfinowski, R. Kleczek, C. J. Schmidt Characteri zation of the STS/MUCH XYTER2, a 128 channel time and amplitude measurement IC for gas and silicon microstrip sensors, Nuclear Instruments & Methods in Physics R esearch. Section A,Accelerators, spectrometers, detectors and associated equipment ; 2018 vol. 908, s. 225 235.

P. Otfinowski, P. Grybos, R. Szczygiel, K. Kasinski, Offset correction system for 128 channel self triggering readout chip with in channel 5 bit energy measurement functionality, Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip. 780 (2015) 114 118. doi:http://dx.doi.org/10.1016/j.nima.2015.01.048.

DAQ system:

Wojciech M. Zabołotny, Grzegorz H. Kasprowicz, Adrian P. Byszuk, David Emschermann, Marek Gumiński, Krzysztof T. Poźniak, and Ryszard Romaniuk "Selection of hardware platform for CBM Common Readout Interface", Proc. SPIE 10445, 1044549 (7 August 2017);

W.M. Zabolotny, G. Kasprowicz, A.P. Byszuk, D. Emschermann, M.Gumiński, B. Juszczyk, J. Lehnert, W.F.J. Müller, K. Poźniak and R. Romaniuk "Versatile prototyping platform for Data Processing Boards for CBM experiment", 2016 JINST 11 C02031

W.M. Zabołotny, A.P. Byszuk, D. Emschermann, M. Gumiński, B. Juszczyk, K. Kasiński, G. Kasprowicz, J. Lehnert, W.F.J. Müller, K. Poźniak, R. Romaniuk, R. Szczygieł, Design of versatile ASIC and protocol tester for CBM readout system, J. Instrum. 12 (2017) C02060. http://stacks.iop.org/1748 0221/12/i=02/a=C02060

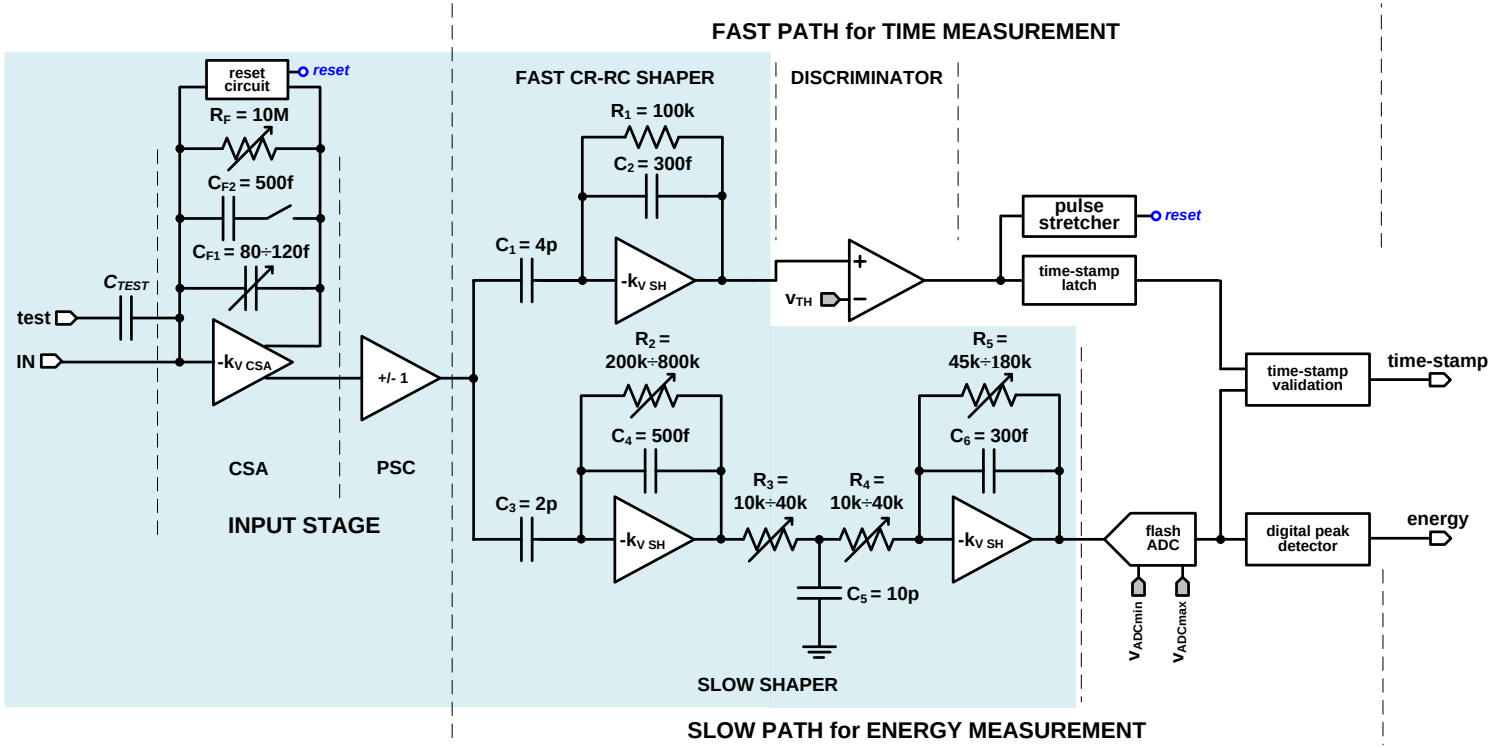
Front-end of the STS/MUCH-XYTER2.2

Main application requirements:

- multichannel self-triggerred architecture (50 μm pitch),
- deposited charge time and energy measurements,
- average rate of input pulses 250 kHz/channel,
- input charge in the range (electrons and holes):
  - 0.5 fC – 15 fC for the STS mode,
  - 1 fC – 100 fC for the MUCH mode,
- detector capacitance at the order of tens pF,
- low noise ENC ~ 1000 e^- rms in STS system,
- limited power consumption < 10 mW/channel
- good uniformity of analog parameters between channel,
- radiation-hardness property.

Readout front-end architecture:

- input stage: Charge Sensitive Amplifier + Polarity Selection Circuit,
- fast path:
  - optimized to determine the input charge arrival time with the resolution of the order of few ns,
  - built of: CR-RC shaper with tp = 40 ns, discriminator, time-stamp latch, pulse stretcher,
- slow path:
  - optimized for accurate energy measurement:
  - built of: CR-$(RC)^2$ based shaper with switchable tp = 80, 150, 220, 280 ns, 5-bit flash ADC, digital peak detector.



The simplified architecture of the single readout channel implemented in the STS/MUCH-XYTER2.2 ASIC.