ASIC design for MPGDs

RD51 Topical Workshop on FE electronics for gas detectors June 17, 2021



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SoCs for next-gen MPGD readout

- The ALCOR concept: a timing/ToT engine easily adaptable to different kind of detectors
- scalable matrix and end-of-column architecture with digital-on-top integration flow
- Pixel pitch below 500 µm, current version 32-pixel matrix

Col 2

Ch 0

Col 2

Ch 1

Col 2

Ch 2

Col 2

Ch 3

Col 3

Ch 0

Col 3

Ch 1

Col 3

Ch 2

Col 3

Ch 3

- the chip performs amplification, signal conditioning and event digitisation, and features fully digital I/O.
- Pixel hosts dual-polarity configurable gain VFE+shaper, 2 LE discriminators, 4 TDCs, digital control and interface
- 64-bit (32-bit on time tagging mode) event and status data is generated on-pixel and propagated down the column
- ✤ 4 LVDS TX data links, SPI configuration and SEU protection on FSM and configuration registers

Col 4

Ch 0

Col 4

Ch 1

Col 4

Ch 2

Col 4

Ch 3

End of column

32 input ports of sensor signals

operation up to 320 MHz (TDC binning down to 50 ps and event rate exceeding 500 kHz per channel)

Col 5

Ch 0

Col 5

Ch 1

Col 5

Ch 2

Col 5

Ch 3

Col 6

Ch 0

Col 6

Ch 1

Col 6

Ch 2

Col 6

Ch 3

Col 7

Ch 0

Col 7

Ch 1

Col 7

Ch 2

Col 7

Ch 3





Coarse counter TDC1 Fine count

TDC2 Fine coun

TDC3 Fine

TDC4 Fine cou

TDC

Contro logic

TIA1

TIA2

ode/cathoo

RCGs

TDC 1



ayloads generato

FIFO

32bit x 4

Data con

Data to bot

Data from

up channe



Col 0

Ch 0

Col 0

Ch 1

Col 0

Ch 2

Col 0

Ch 3

Col 1

Ch 0

Col 1

Ch 1

Col 1

Ch 2

Col 1

Ch 3

RD51 Collaboration Meeting and Topical Workshop on FE electronics for gas detectors, June 17th 2021

Thanks for your attention.



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