Experience on μRWELL with 2D-Strip Readout — For RD51 Tracker

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On behalf of the Resistive DLC Collaboration

RD51 Collaboration Meeting, 18-06-2021

µRWELL tracking system for RD51

- RD51 collaboration will upgrade the existing tracking systems (GEM and resistive mm based) adding a **µRWELL base telescope**.

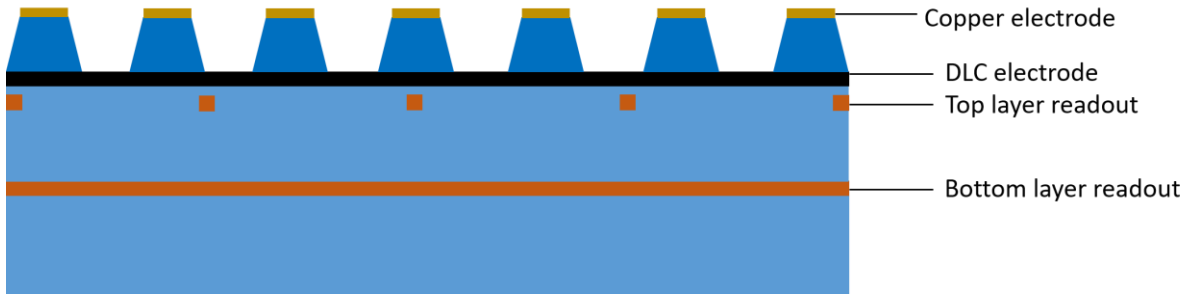
- **Requirements**:
  - 4 detectors (3+1)
  - Active area 10cm x 10cm
  - XY readout 50/50 sharing (256 X, 256 Y)
  - High Rate (assuming 1～10MHz/cm^2)

- **Timeline**
  - **Prototype for October Test Beam**
  - Full telescope for 2022 beams

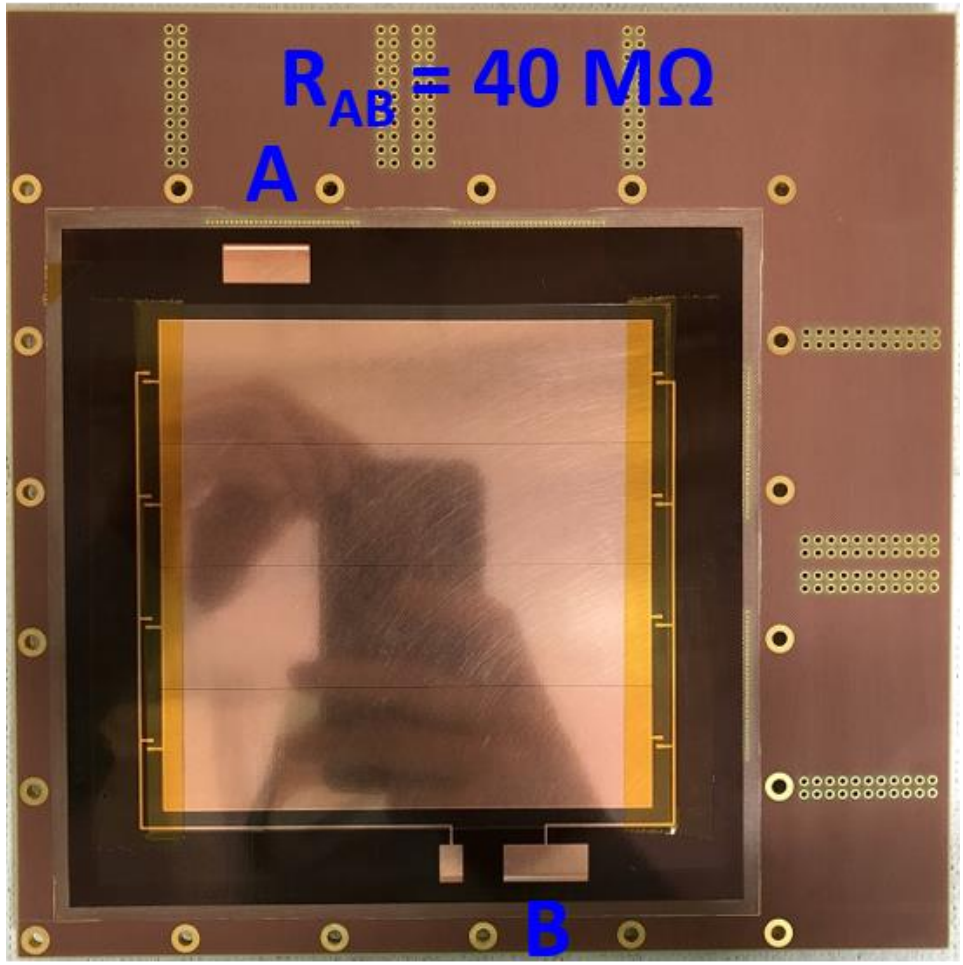
Geometry of the 1st 2D-strip µRWELL

➢ µRWELL PCB with 2D readout strip

- Sensitive area: 10cm×10cm divided into 4 sectors
- Readout strip pitch: 400 µm
- Top layer: 80 µm
- Bottom layer: 350 µm
- Readout strip channel: 512



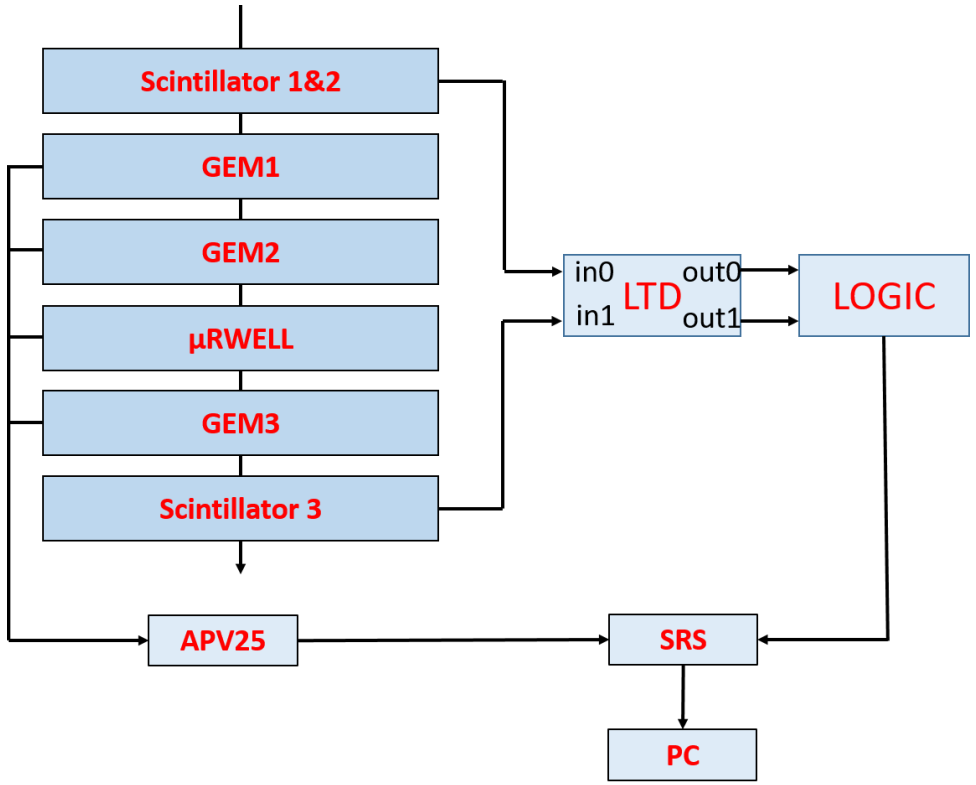
The thickness of APICAL between Top layer and Bottom layer is 50 µm.



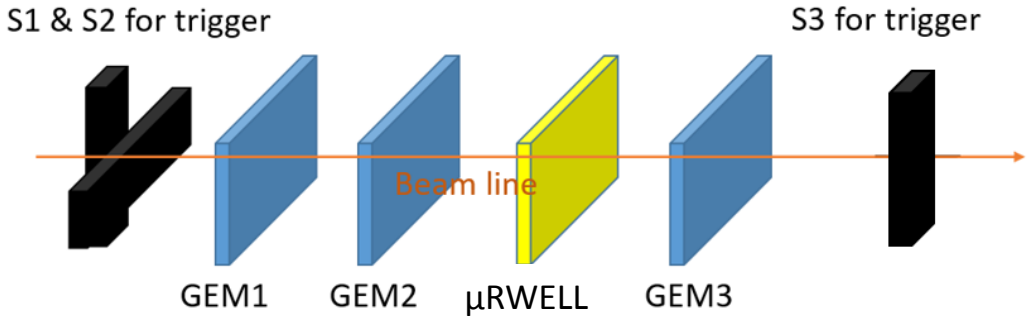
Setup of Beam test at CERN

➢ **Tracker system setup**

- Scintillator(S1, S2, S3) for trigger (10cm × 10cm)
- RD51 GEM (10cm × 10cm) Tracker
- RD51 SRS DAQ: 1024 channel (APV25 readout chip)
- 150GeV muon

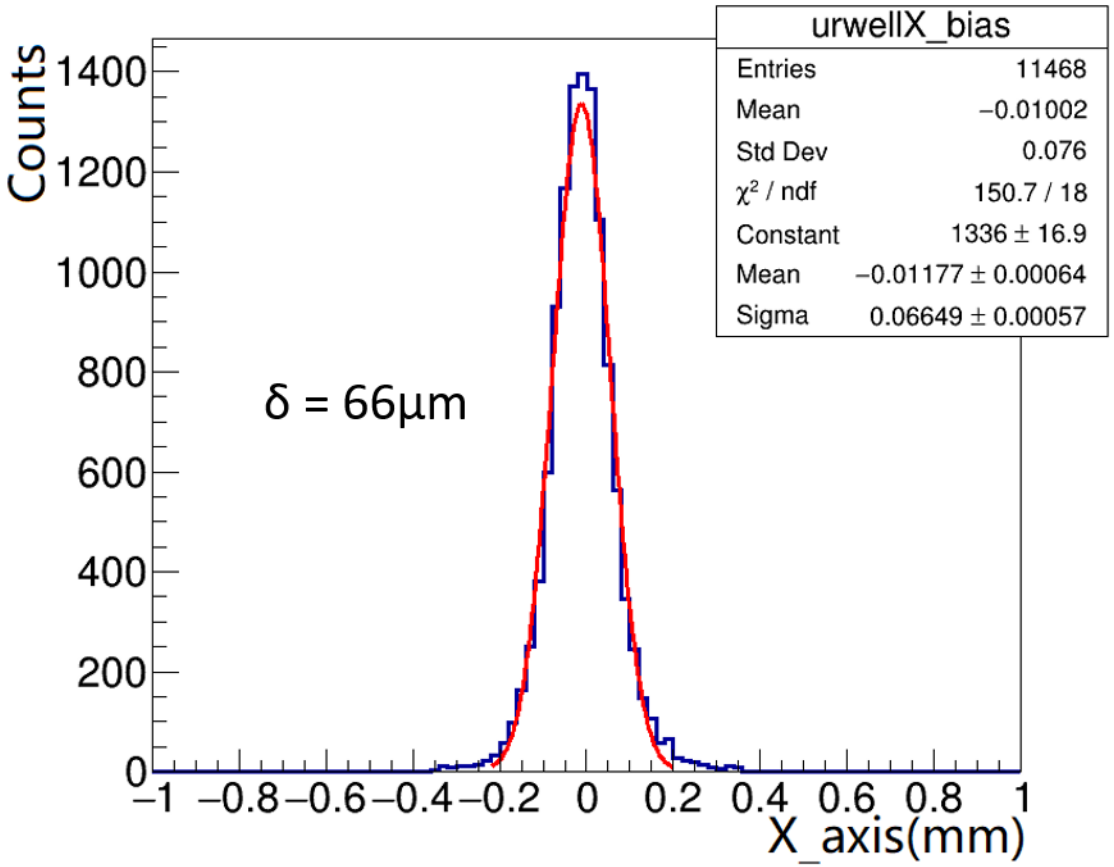


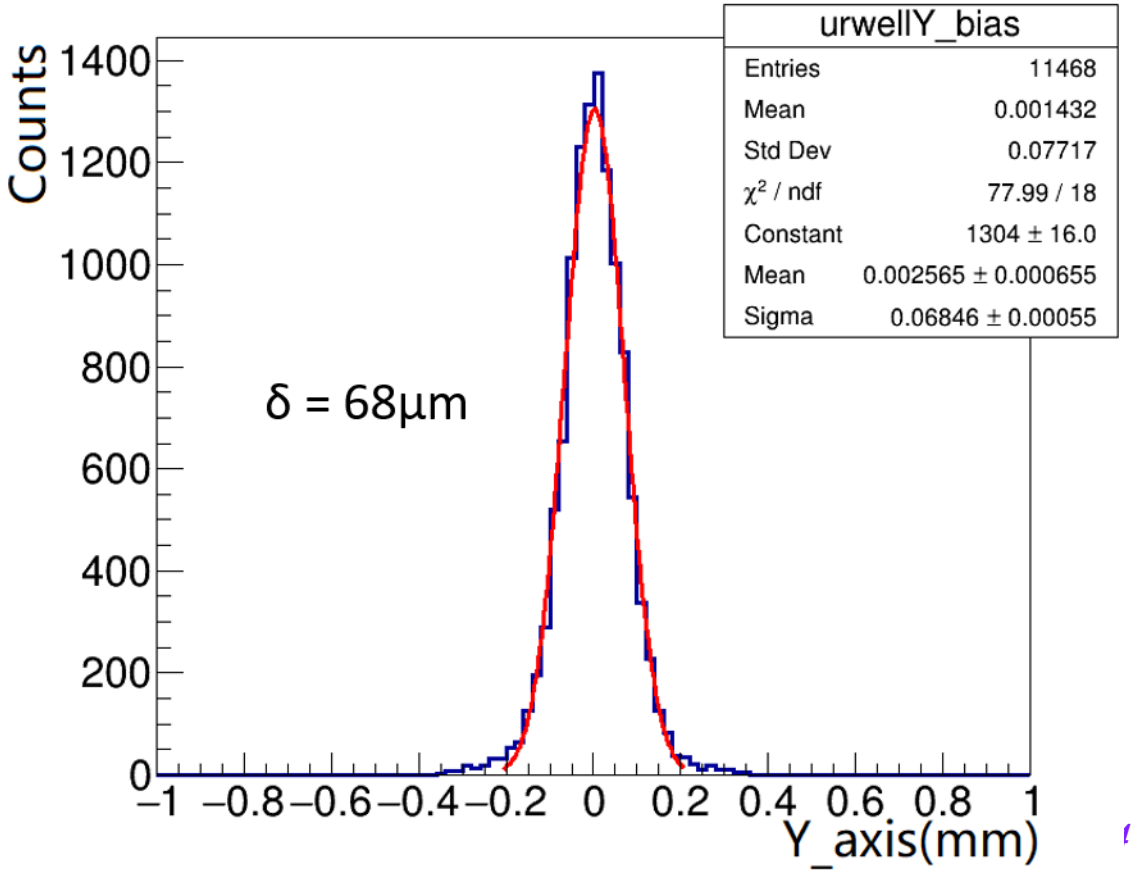
CERN SPS-H4 beam area



Position resolution

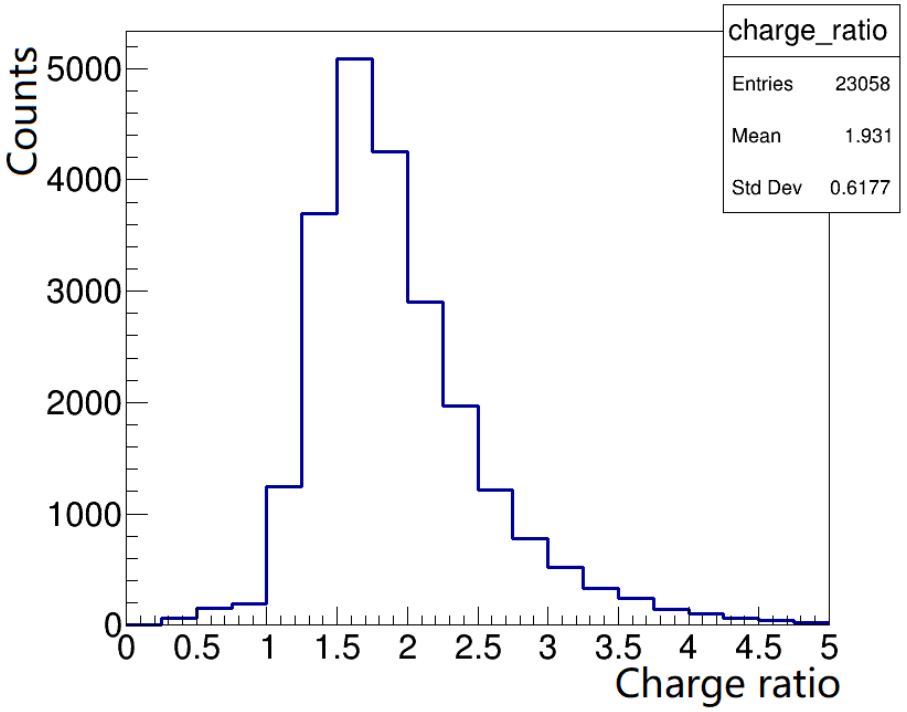
- **Position efficiency:** Charge-weighted center of gravity (COG) method
- Position resolutions better than 70 microns are achieved on both readout directions of the µRWELL prototype



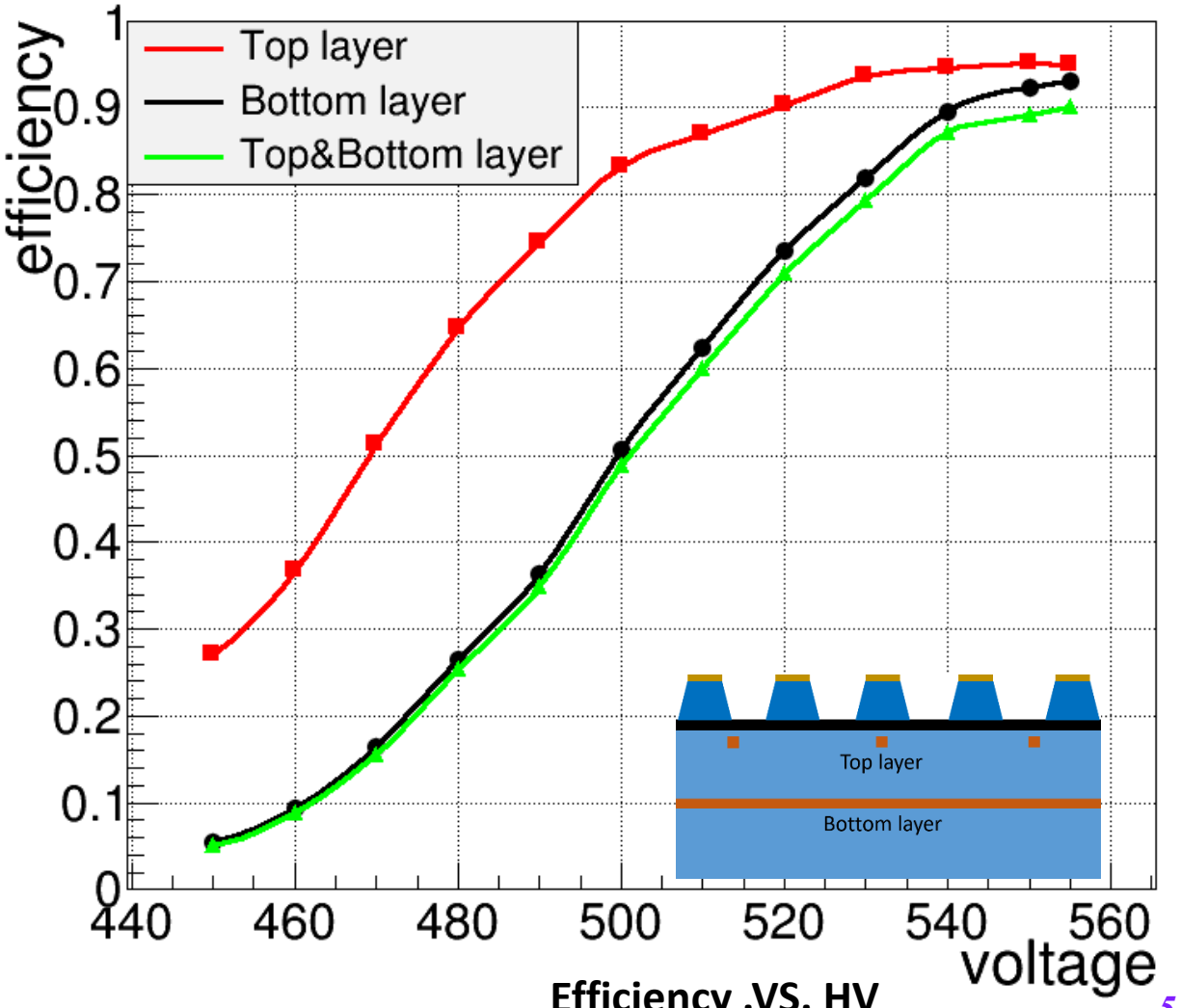


Detection efficiency

- **Detection efficiency .VS. Voltage**
  - **Top layer: ~95%, Bottom layer: ~92%**
  - **Top & Bottom efficiency: ~90%**
  - **Top layer induced charge is 1.9 times of Bottom layer**



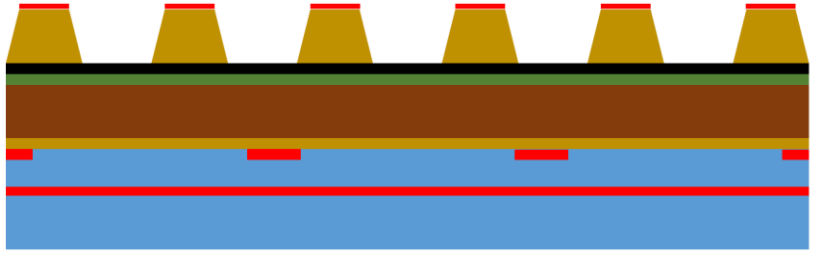
Top layer Charge/Bottom layer charge



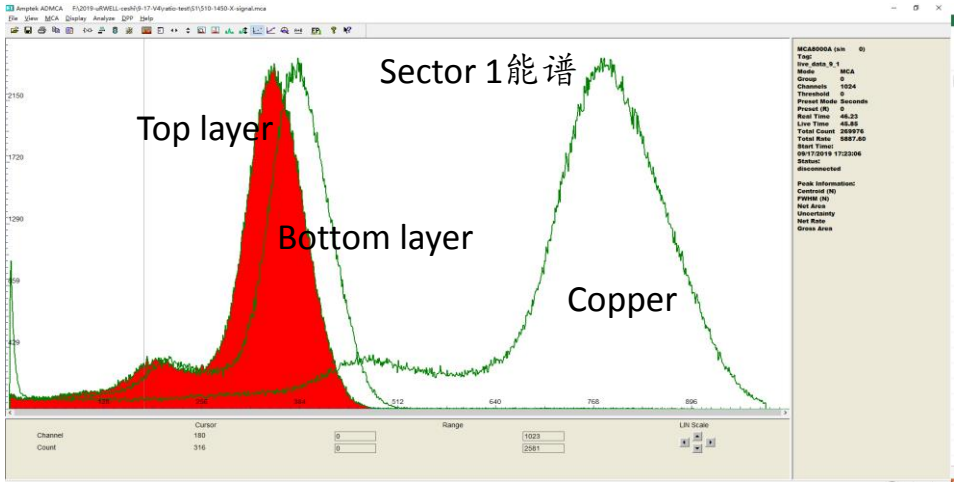
Efficiency .VS. HV

Optimization of the geometry of the readout strips

2nd 2D-strip µRWELL



Copper
APICAL
DLC
Epoxy glue
Prepreg
Insulator layer



Top strips: 60um (80)
Bottom strips: 350um (350)
Pitch: 400um (400)

Insulator layer between Top & Bottom readout strips: 25um (50)
DLC resistivity: R_{AB}=40MΩ

Insulating layer between DLC and readout strip: 50um Prepreg+12um Kapton+10um epoxy glue

	Top	Bottom	Copper	Bottom/Top	Copper/Bottom
Sector 1	354	386	785	1.09	2.03
Sector 2	322	358	698	1.11	1.95
Sector 3	329	375	771	1.14	2.06
Sector 4	336	374	728	1.11	1.95

The spectrums of X and Y are tested independently, not at the same time, we will use two MCA to measure them at the same time soon.

Conclusions of the geometry of XY strips

- Insulating layer between DLC and top readout strip should be as thin as possible, to achieve larger induce signal amplitude;

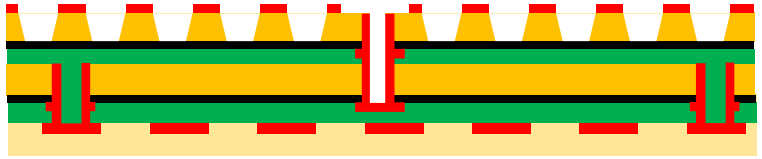
- We want the signal amplitudes on X and Y are the same due to the APV25 is used; if another kind of chip with larger dynamic range is used, we will have better tolerance for the charge sharing.

Alignment problems in SG2++ and SBU

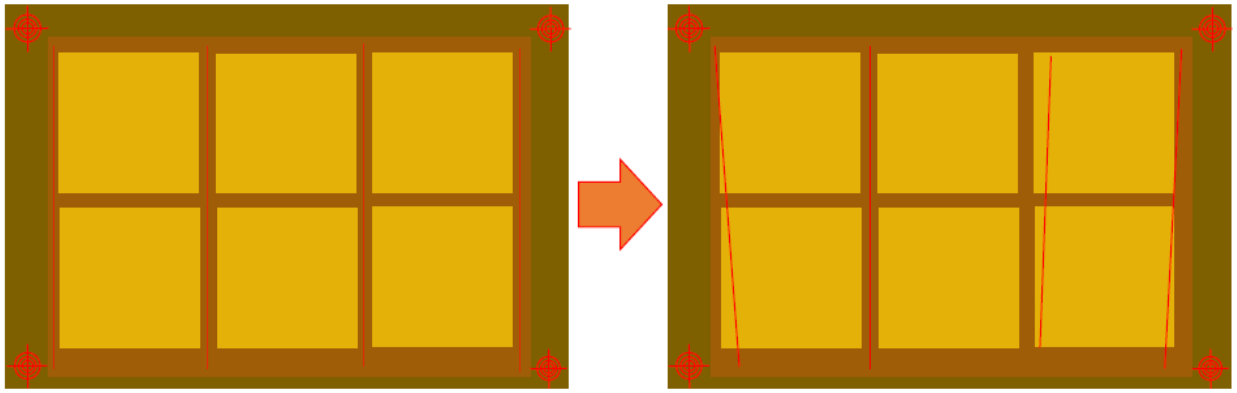
1. SG2++ type (Cu grid): The copper clad on the DLC is etched to conductive grounding lines by photo-lithography.

2. SBU type (Sequential Build Up): Current evacuation achieved by two stacked DLC layers.
Matrix of conductive vias manufactured with SBU technology are used to connect DLC layer to grounding.

SG2++ type



SBU type



Ideal Reality

- For SG2++, after gluing the APICAL substrate onto the readout PCB, it is impossible to see the fast grounding lines, so it is impossible to align the mask for APICAL etching.
- For SBU, still have same alignment problems when making the conductive Vias.

Bring the pattern to the top layer

PEDF: Patterning , Etching , Drilling & Filling

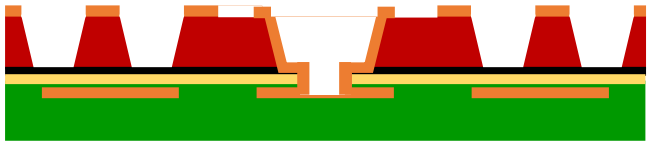
Step1: Copper & APICAL etching, to make a big hole, with DLC on bottom.

Step2: Drill a small hole, the copper of the readout pad expose to air.

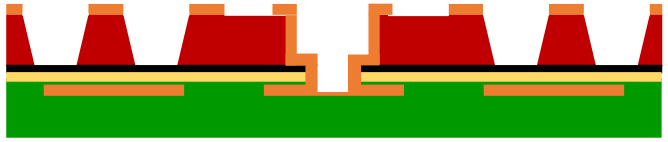
Step3: Use silver glue to connect the DLC to readout pad.

Step4: Make µRWELL structure and remove the copper around silver glue.

PEDP: Patterning , Etching , Drilling & Plating



DEP: Drilling , Etching & Plating



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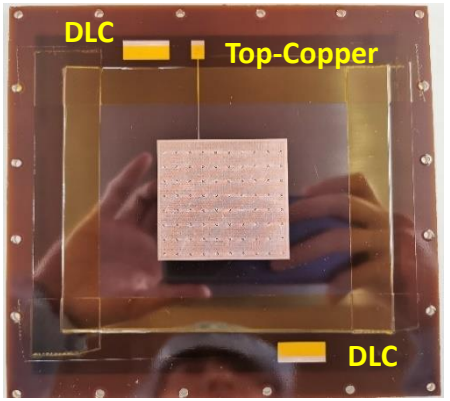
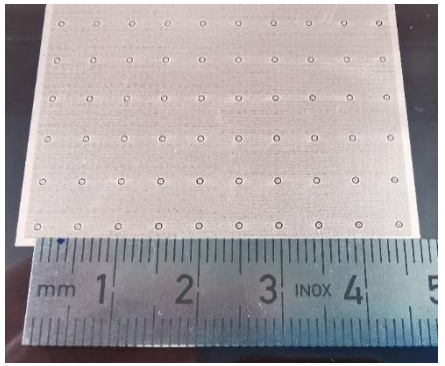


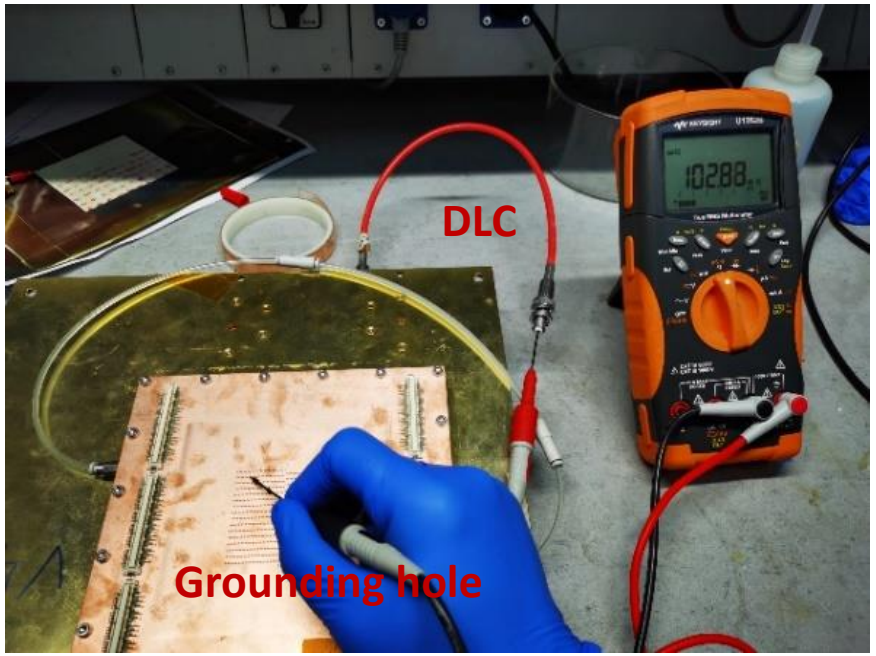


Advantages:

1. **No copper-coated DLC needed, better resistivity control;**
2. **No alignment problems even goes to large area;**

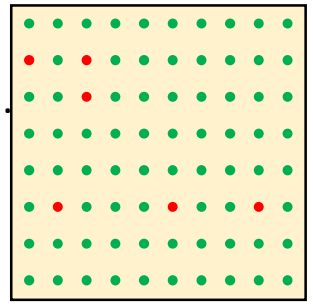
GND connection measurement

Measuring the resistivity between DLC and fast-grounding holes.

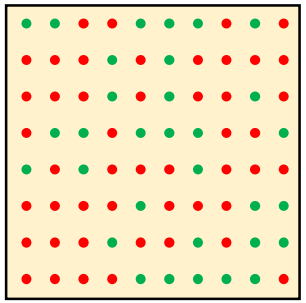


PEDP

6 holes disconnected.
90 to 110 MΩ



PEDF

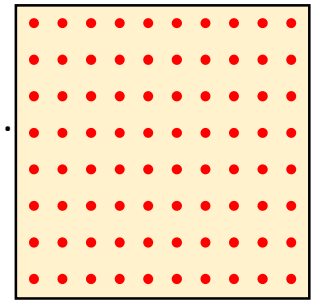


32 holes connected.
350 to 450 MΩ

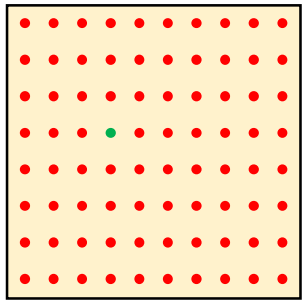
• Connected

• Out of range (>500 MΩ)

All holes disconnected.



DEP



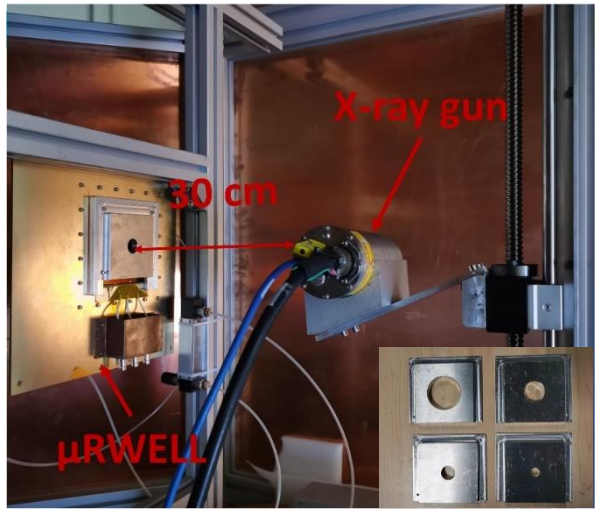
DEF

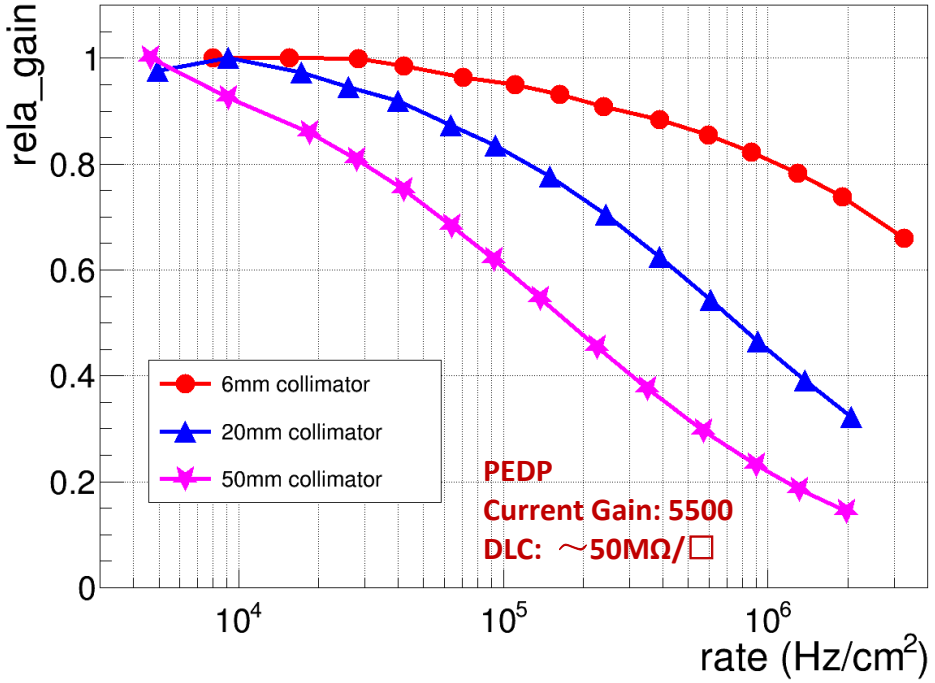
holes connected.
380 MΩ

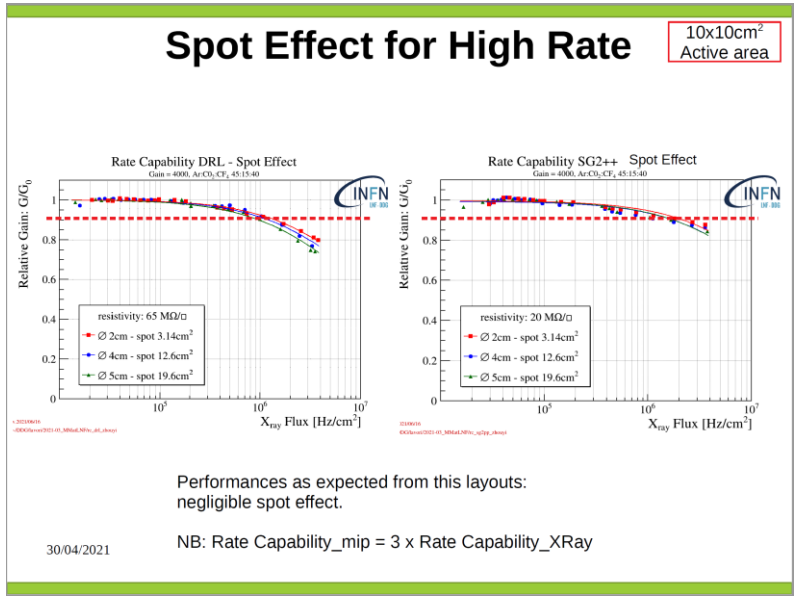
- For DEP and DEF, it is uncontrollable when etching the grounding holes due to that no pattering before etching process. Bad connection between DLC and grounding holes.

The PEDP shows the best connection between DLC and grounding holes.

Rate capability of PEDP





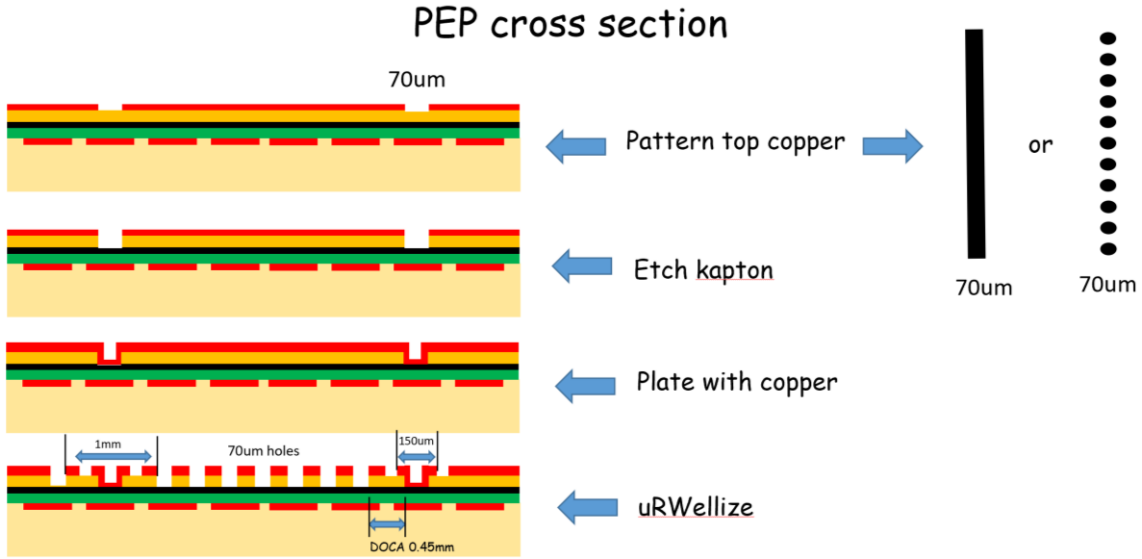


- Spot size effect is clearly observed on PEDP(and also PEDF, DEF) @USTC
- Spot size effect is negligible on double-layer, SG1, SG2++ μRWELLs @LNF

M. Giovannetti,
Resistive DLC CP Meeting, 30-04-2021

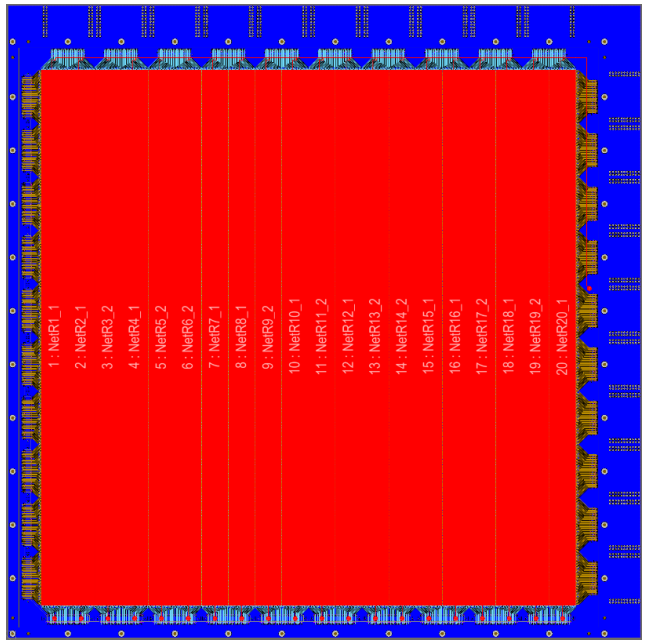
The reason of spot size effect on PEDP is still not very clear, we decide to change the DOT to LINE

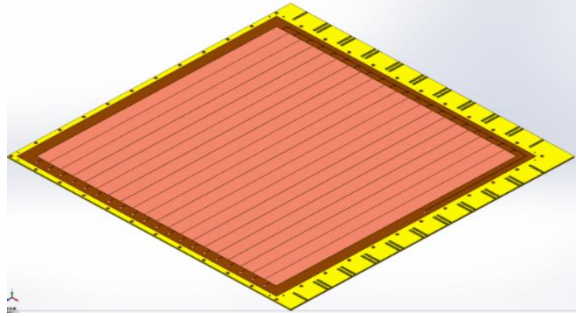
PEP(Patterning, Etching, Plating) method

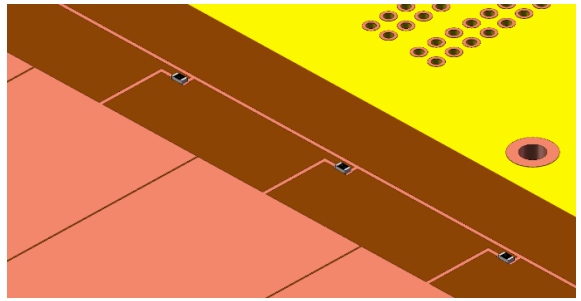


Any pattern can be created to connect the DLC , row of dots but also line.
No alignment problem for large size.
Do not need drilling with Z axis control (simpler than previous structures).

3







- PEP method(Rui's idea) can provide similar GND structures as SG2++, and much simpler than PEDP;
- First batch of PEP µRWELLs for LNF is delivered, detailed measurements are in progress;
- A 50cm×50cm PEP µRWELL with 2D-strip readout for USTC will be fabricated soon;

The possible configurations for RD51 µRWELL tracker

- Top strips: 60µm
- Bottom strips: 350 µm
- Pitch: 400 µm
- Insulator between Top & Bottom readout strips: 25 µm
- Insulator between DLC and readout strip: 20 µm in total
- 256 Channels on Both X & Y
- DLC resistivity: 50～100MΩ/□(depends on the final goal of rate capability)
- Active area: 10cm×10cm
- Detection efficiency: >95% if the pitch of GND line is 12mm (～97% in SG2++);
- SG2++ or PEP technique(Depends on the test results of PEP)