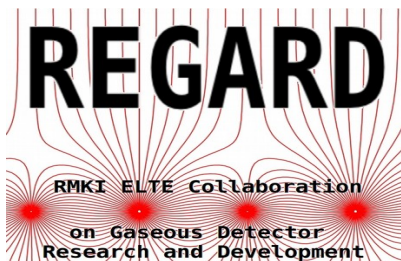


Power and cost efficient FEE for development-stage and mobile outdoor systems

Dezső Varga, Gergő Hamar, Sz. Balogh, G. Galgóczi
Wigner Research Centre for Physics, RMI NFO



RD51 Collaboration Meeting
June 2021 (Online)

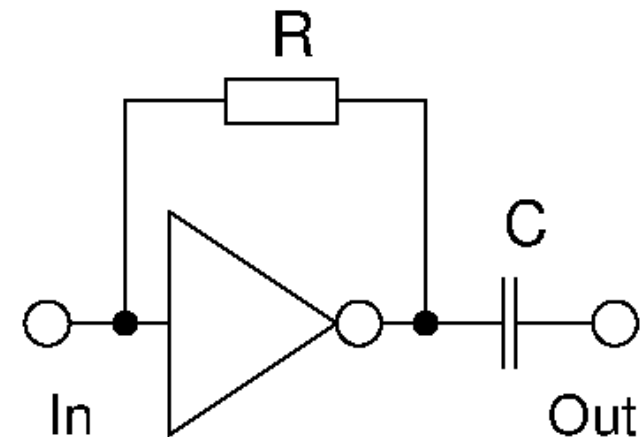
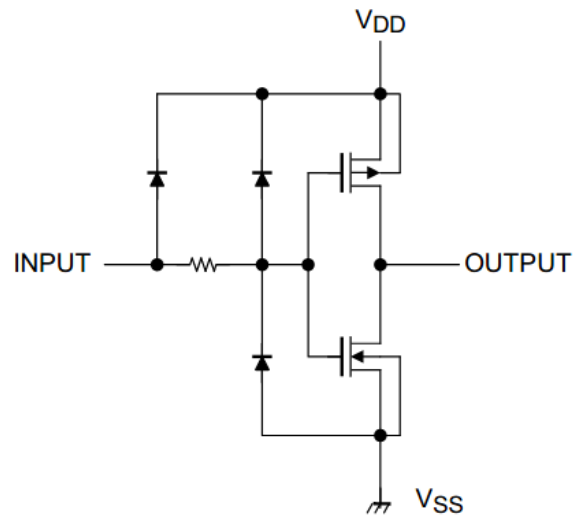
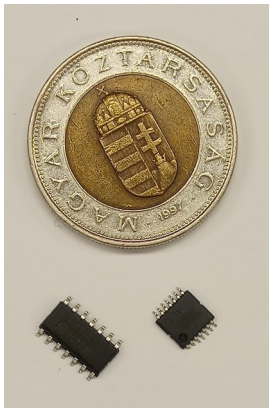


Basic concept: off-the-shelf CMOS components

- CMOS digital gates in analog mode with feedback resistor
- Gain, shaping time and total DC current strongly depends on supply voltage: needs good filtering

4069U-type inverter

Single stage (gain 5 – 10)



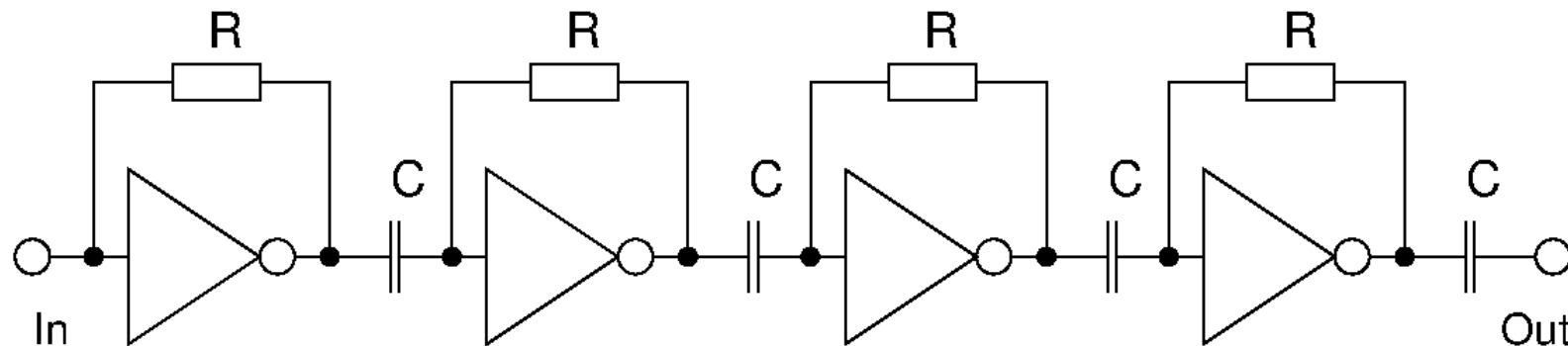
(Notes about the measurements)

- **Input impedance**: effective series input resistance R_{input} and capacitance C_{input}
- Detector-like **input charge** signals: input through high series impedance R_s , where $R_s \gg R_{\text{input}}$
- Equivalent Input Noise (**EIN**): effective output charge, referred to input charge integrated over shaping time. Measured either on test bench or on realistic detector
- Scope images: averaged over 64 shots
- **Good shielding** and input filtering is mandatory

Typical circuitry for gaseous detector

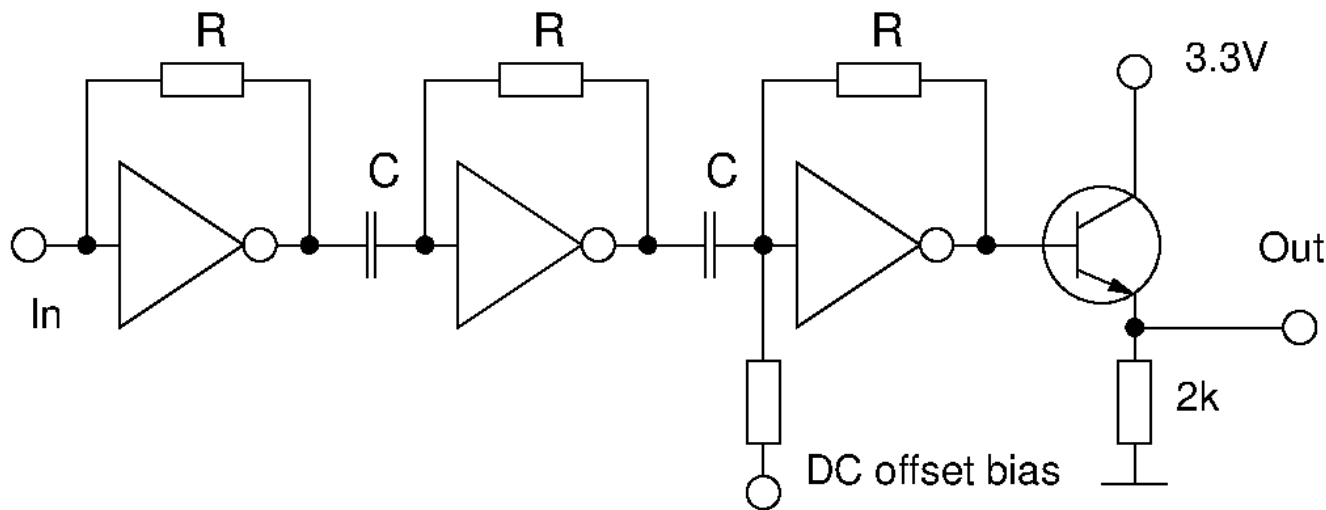
- 4 stage example (no buffer on output): low power, high gain
- Input impedance typical 5 – 10 kOhm, 10pF
- Gain: 0.2 – 1V output for 100ke (16 fC) input
- Shaping time 0.5 – 3 microsec
- High output impedance, 3 – 6 kOhm

$$R = 100k - 1M$$
$$C = 0.5nF - 2nF$$



Typical circuitry for gaseous detector

- Buffered output example (inverting for odd stage number)
- Same as previous except for 0.2 kOhm output impedance (fixed DC offset)

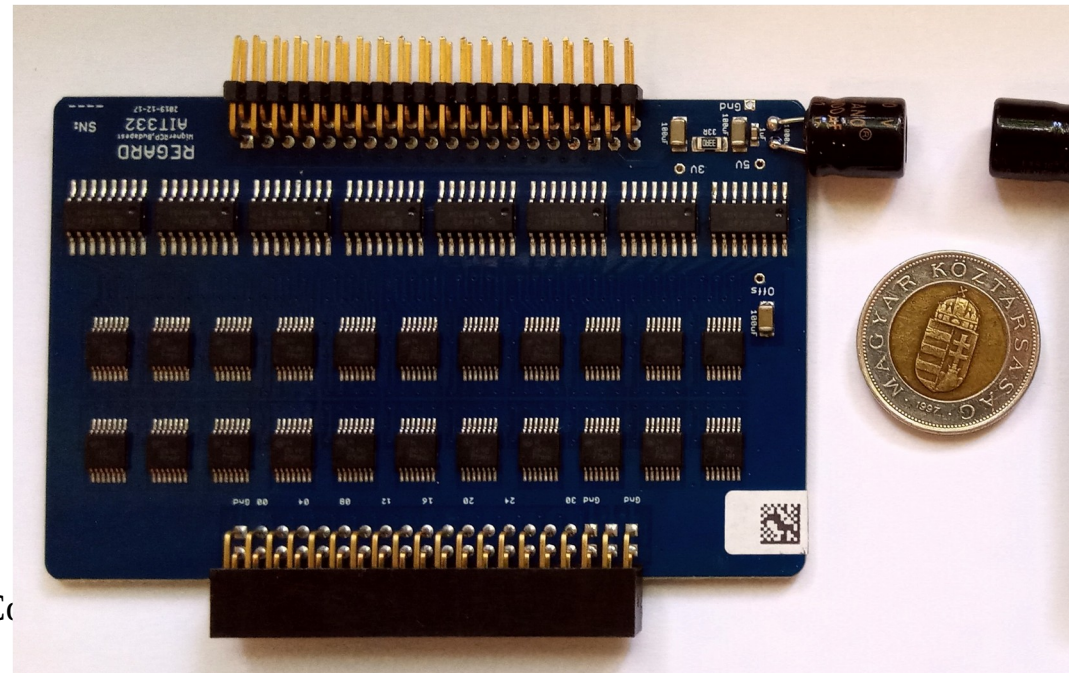
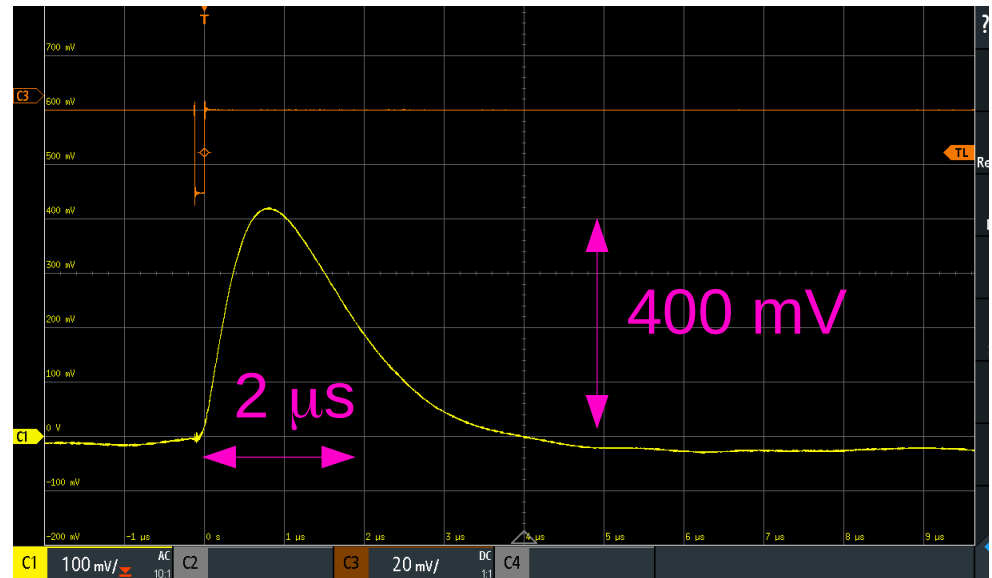


Practical implementations

- 32-channel FEE buffered output (to be read with a digitizer)
- 32-channel FEE, with discriminated (“1 bit ADC”) output
- Single channel FEE with buffered analog output, TTL trigger output and ADC-ed output
- Integrated to DAQ

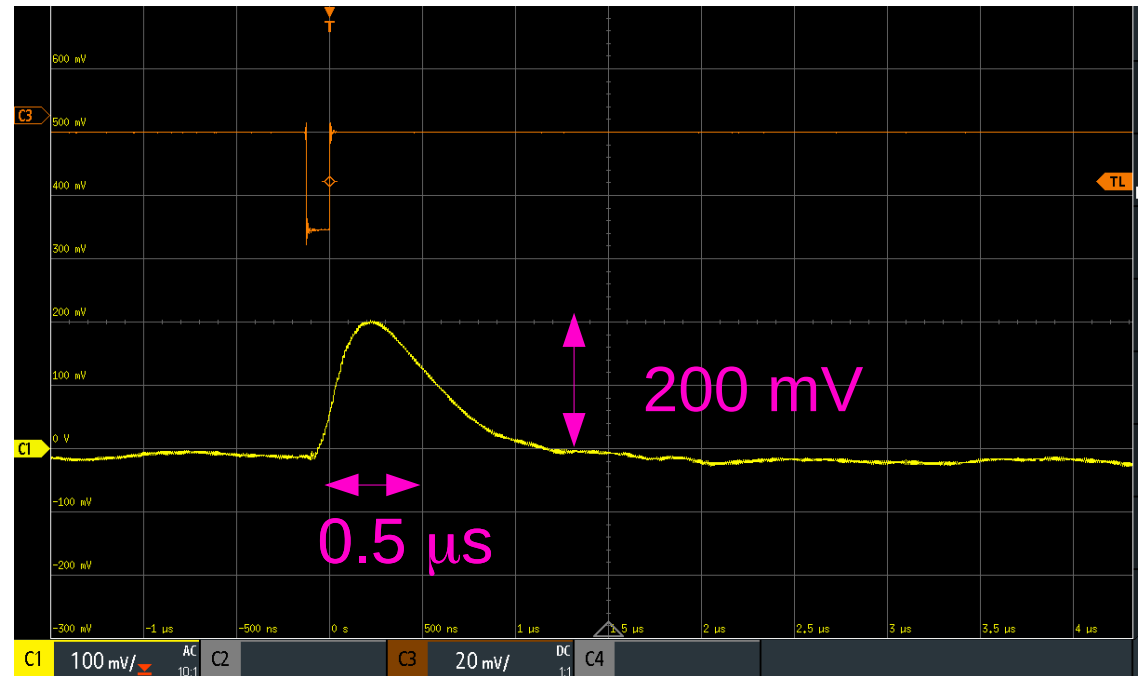
Buffered output 3-stage amplifier

- 32 channels, inverting (positive output for GEM pad readout detector), $R=330\text{ k}\Omega$
- Test input: 125 ns, 30mV, $R_s=390\text{ k}\Omega$ (60ke, **10fC**)
- Output: 400mV, **2 microsec FWHM**
- Noise: 10 mV RMS (1.5 ke, 0.25 fC)



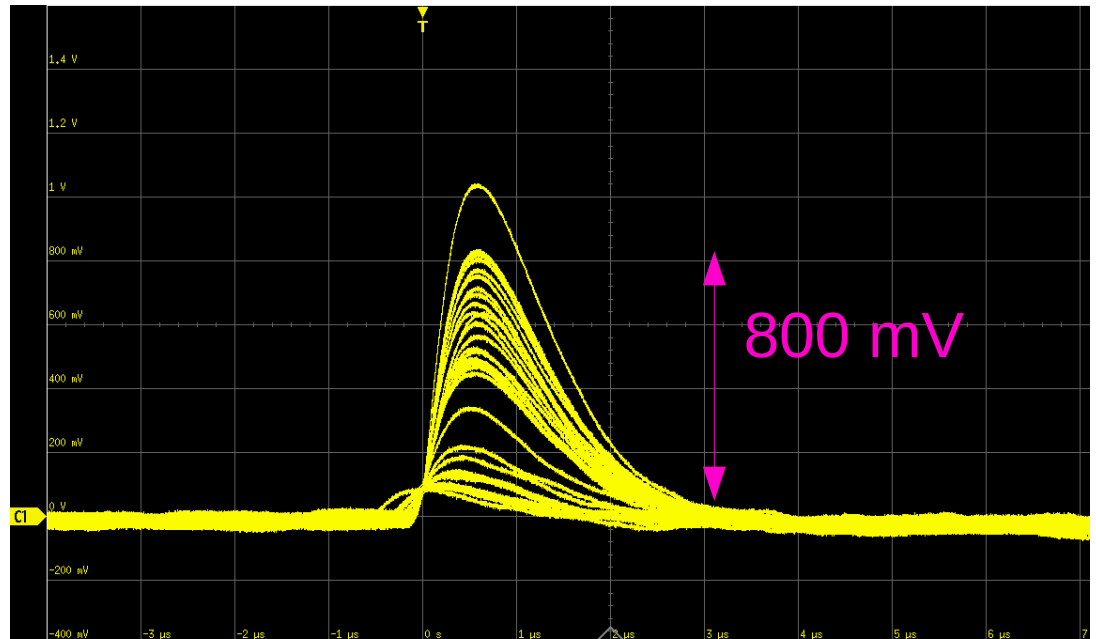
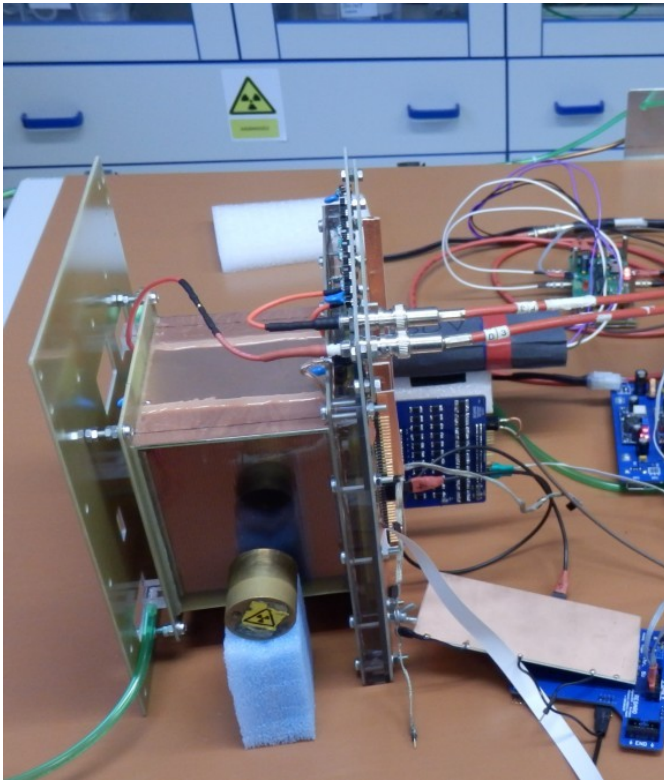
Buffered output 3-stage amplifier

- 32 channel, inverting, **faster**: $R = 100 \text{ k}\Omega$, 7V supply voltage (20 mW/ channel)
- Test input: 125 ns, 30mV, $R_s = 390 \text{ k}$ (60ke, **10fC**)
- Output: 200mV, **0.5 microsec FWHM**



Performance on GEM detector

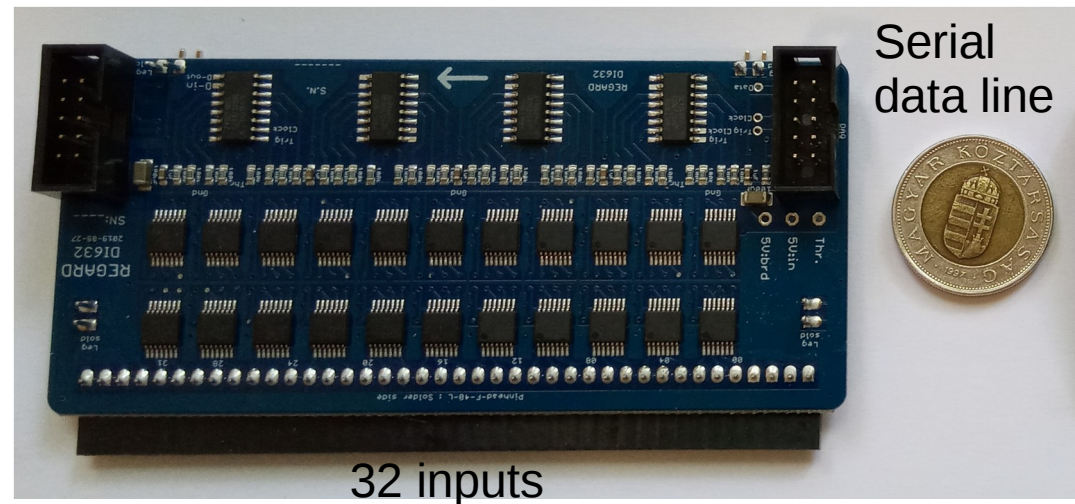
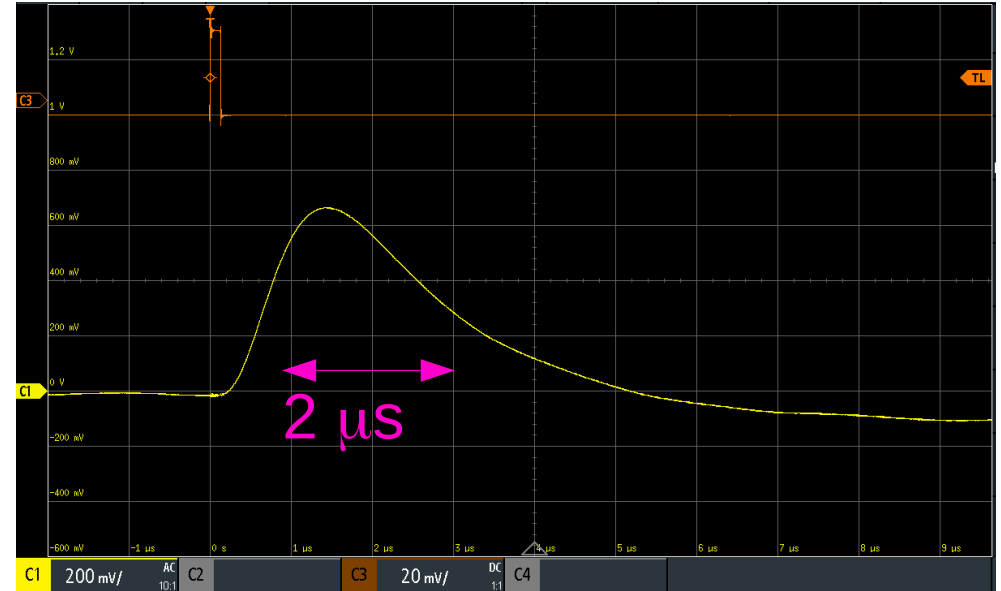
- 32-channel buffered inverting,
Fe-55 (6keV) source on small pads (1.5 mm x 16mm)
- Peak signal 800mV (120ke, gain around 800)
- Noise (EIN on detector!) 10mV, **1.5 ke, 0.25 fC**



G. Galgóczi, JINST Proc. 15 , C08027 (2020)

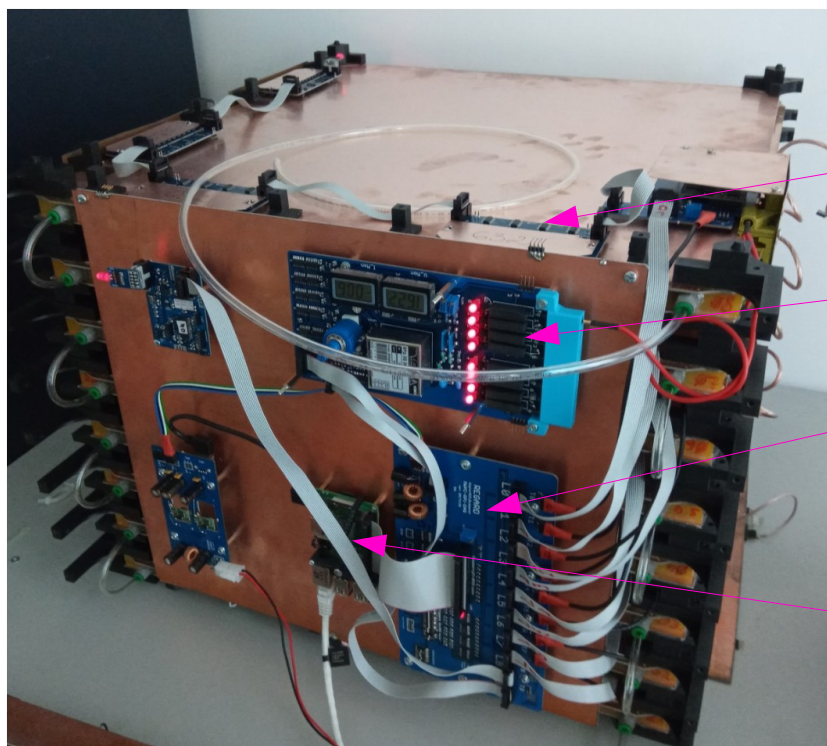
Low power 32-channel amplifier: 4-stage non-buffered

- Supply current at 5V:
12 mA (**2 mW / channel**)
- Test input: 125 ns, 30mV,
 $R_s=390k$ (60ke, 10 fC)
- Output: 650mV,
2 microsec FWHM
- Noise (on detector!):
25 mV (2 ke, 0.3 fC)



Performance on MWPC tracker

- 8 tracking layers, total 1024 channels
- 0.5m x 0.5m, 64 + 64 channel (wire + strips)
- **FEE power consumption 2W**, cost 1k EUR



FEE cards

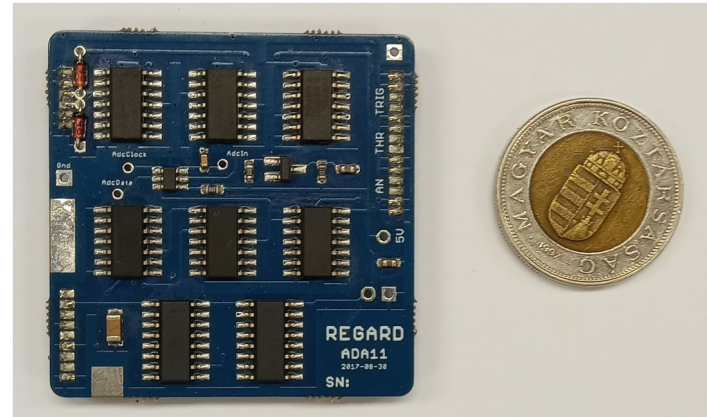
HV supply unit

DAQ unit

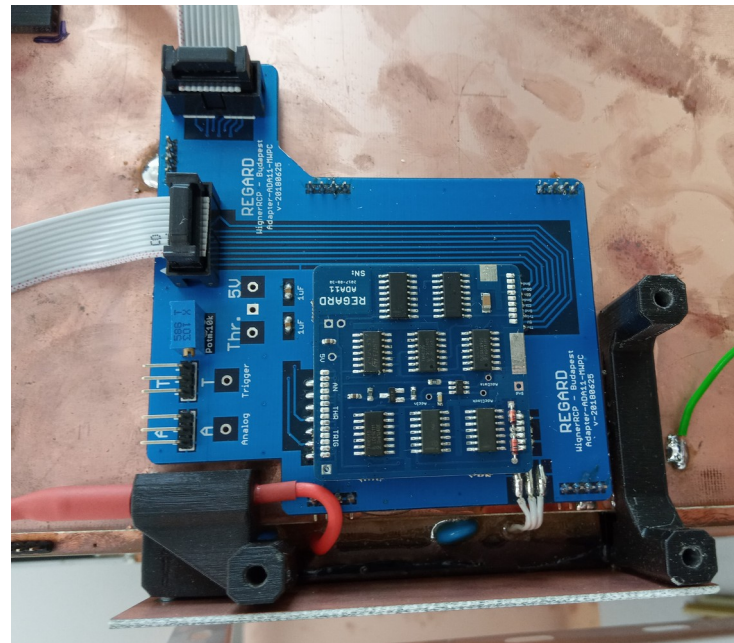
RPi

Integrated analog, trigger, ADC

- Trigger output + ADC serial



- Best practice:
integrate on detector!
HV input, HV filter,
Trigger and ADC
Shielding, mechanics



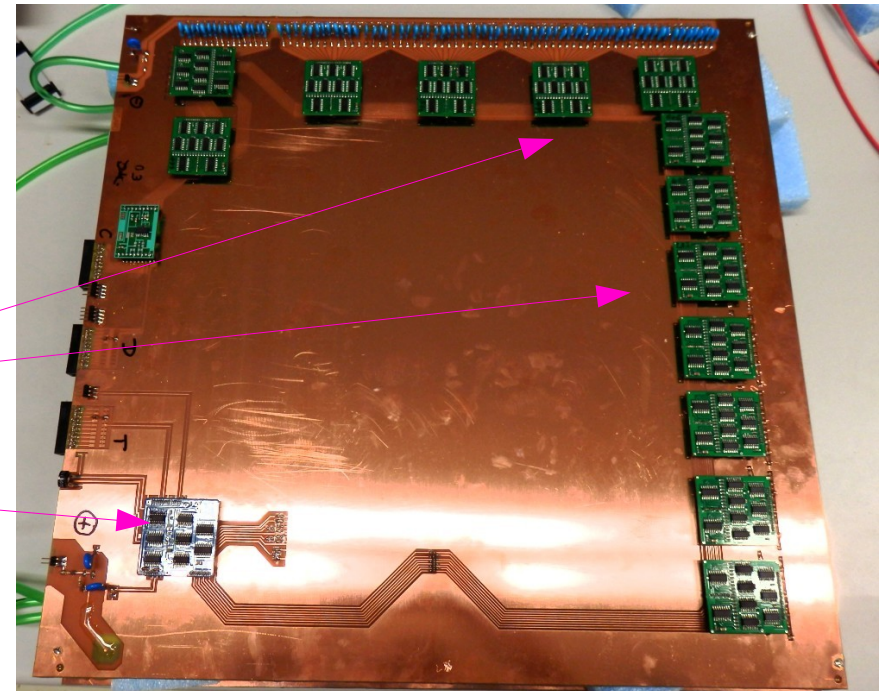
Smaller footprint version (16 channels)

- Here an “OR” gate with higher gain is used as second stage, thus smaller package count
- Example: all integrated at the backside of the detector

FEE-s

Trigger / ADC

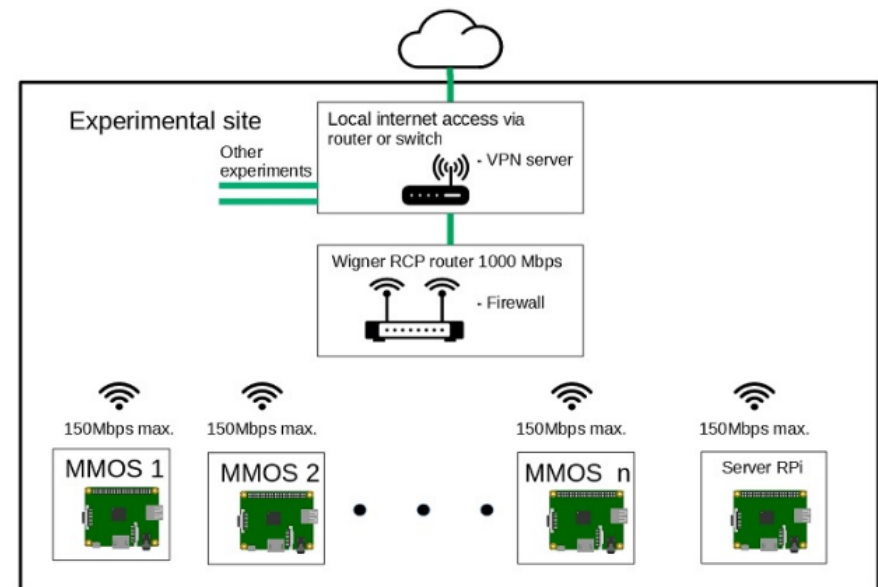
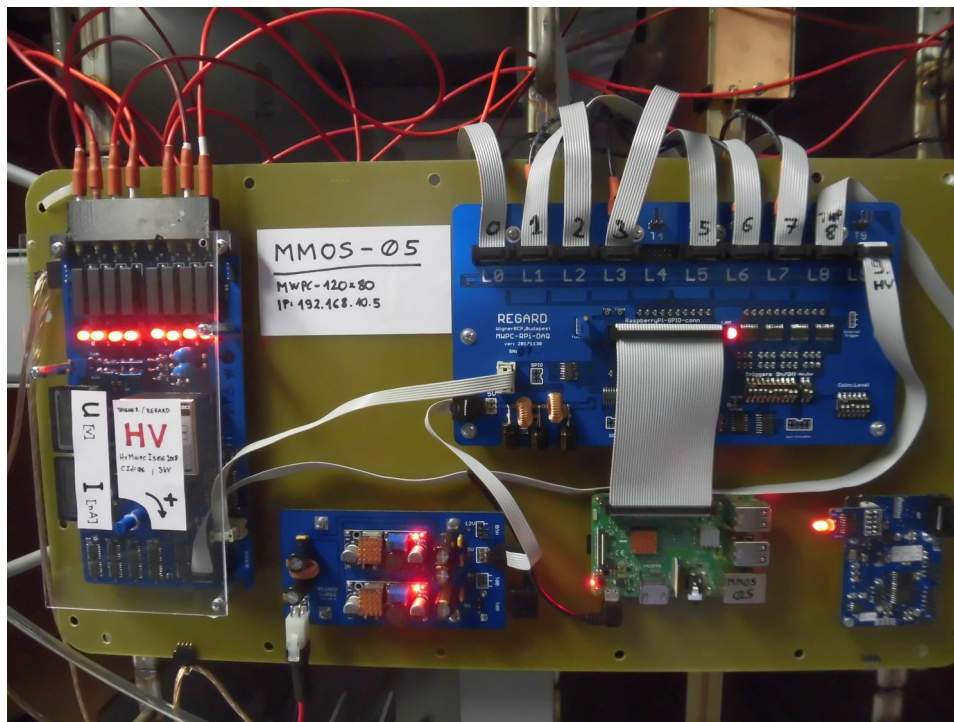
HV input



40cm

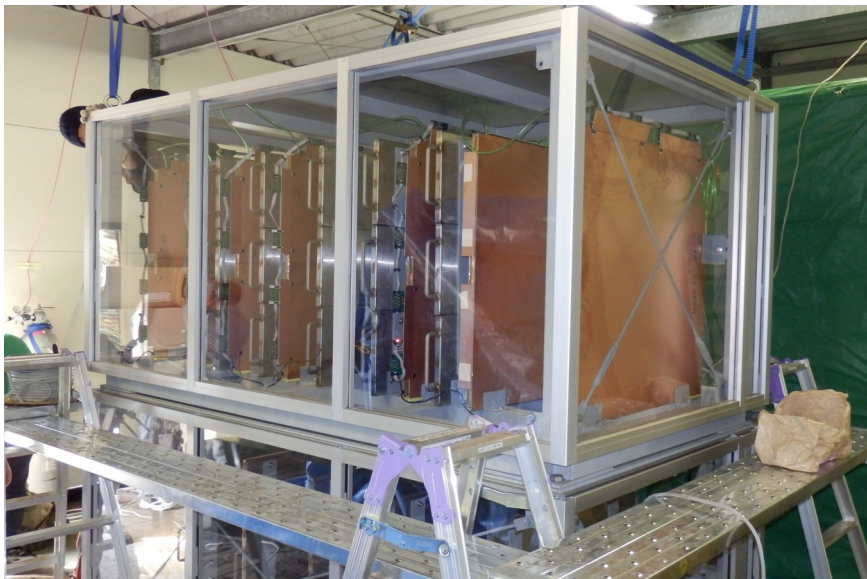
Mobile, modular DAQ system

- Controlled by a single Raspberry Pi
- Integrated trigger logic, serial data acquisition, power supply (LV, HV), and environmental monitoring



Sakurajima Muography Observatory

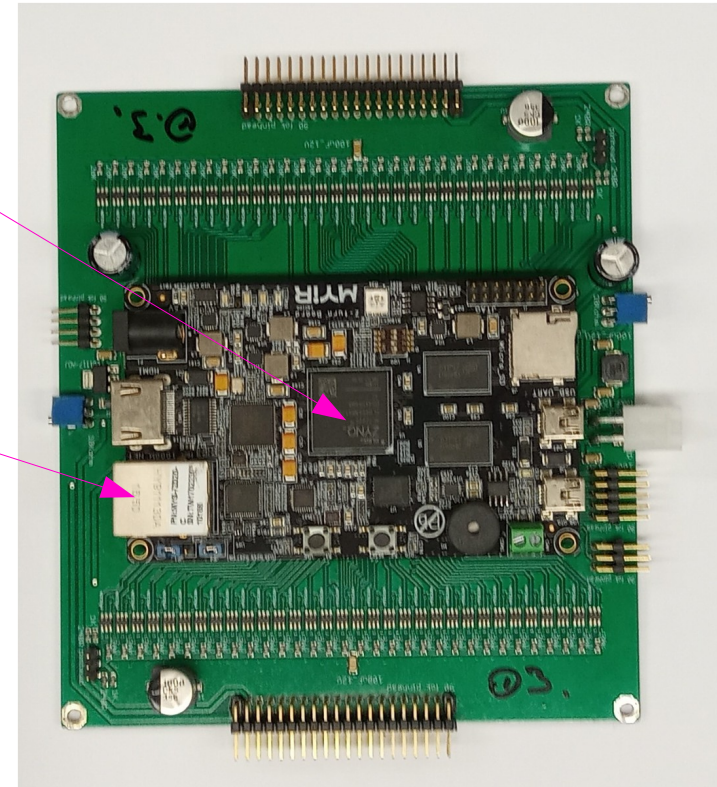
- Total **8 m² tracking system** (largest volcano imaging in the world), in 11 modules (0.6 or 0.9 m² per module, 6 – 8 chambers per module)
- Collaboration between The University of Tokyo and Wigner RCP
- Around 20k FEE channels, running for 3 years in Kyushu, Japan, in ambient conditions



Scientific Reports, Volume 8, Article number: 3207 (2018)

FPGA-controlled ADC-s

- 64 channels: FPGA card runs 12-bit, 3 MS/s ADC-s continuously
- Firmware selects from data stream to Ethernet (via ARM), then directly to PC
- Earlier development with ESS



Conclusions

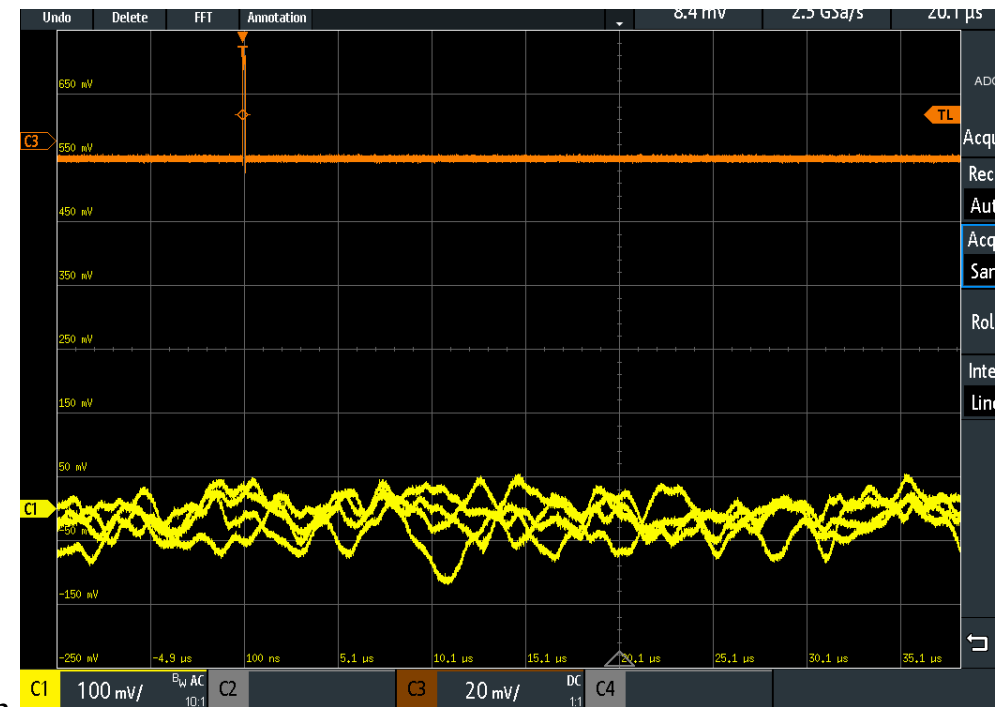
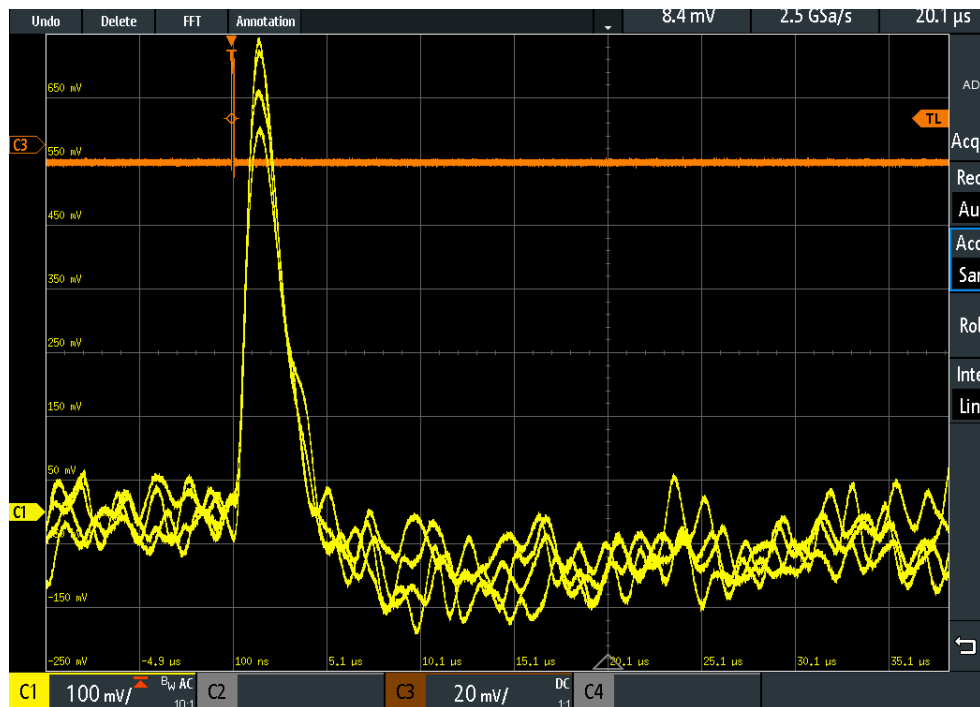
- Cost- and power efficient FEE with off-the-shelf components (few mW/channel, few Eur/channel)
- Covers a wide range of (non-highend) gaseous detector needs
- Tuneable parameters (shaping time, gain)
- Can be an optimal choice where channel numbers between 0.1k – 10k are needed

Backup slides

- Noise on test bench: scope images (low power 4-stage non-buffered), 10 fC input (60 ke)

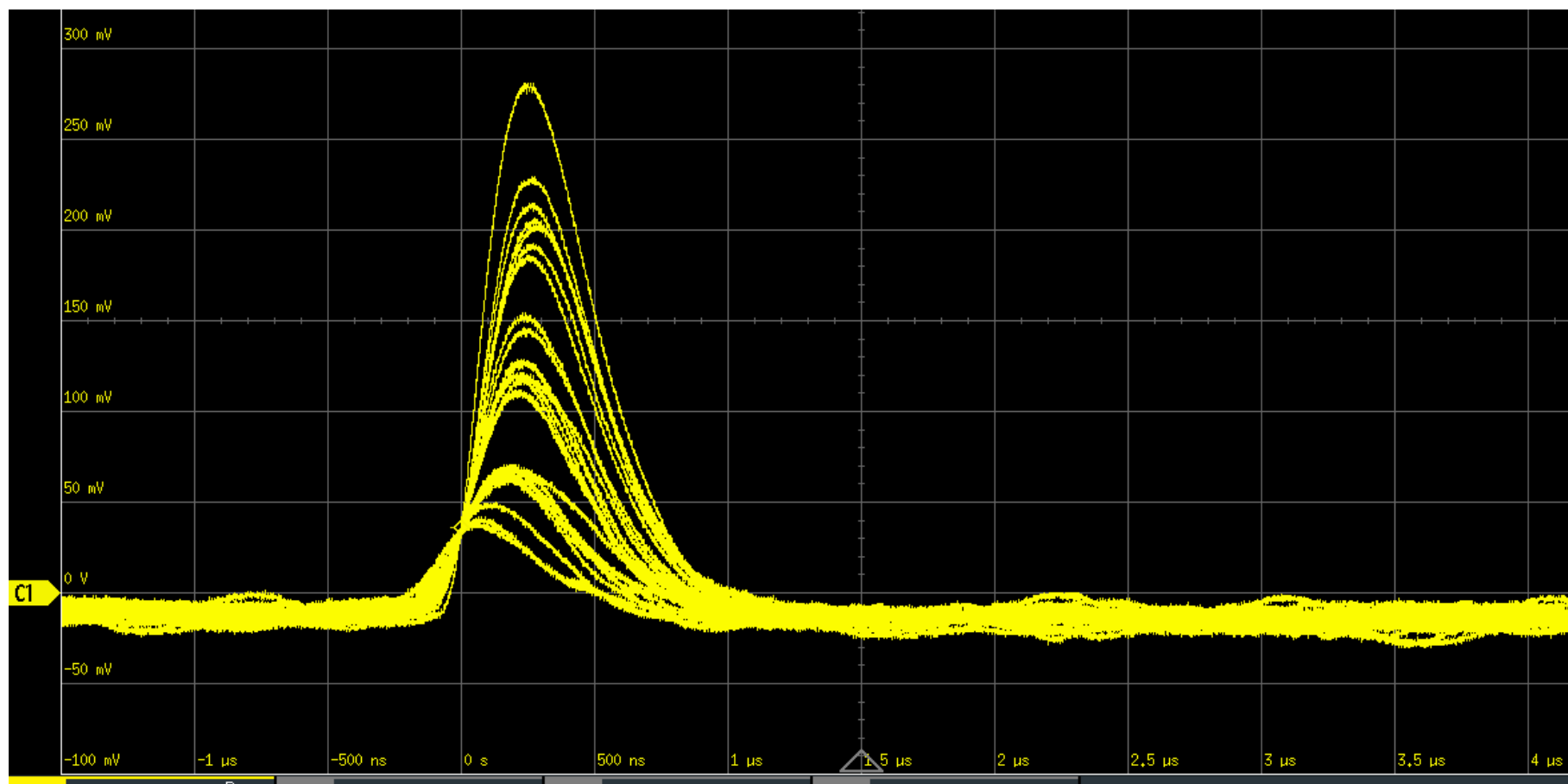
Signal

Noise



GEM detector, faster signals

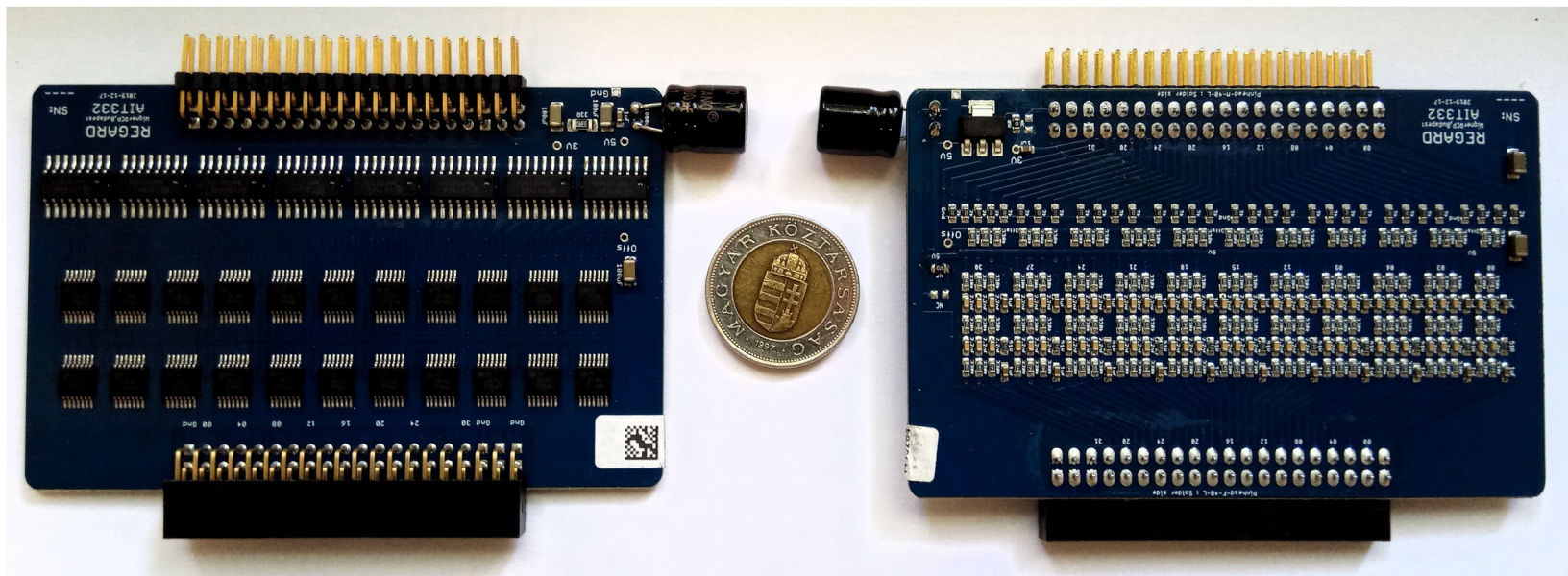
- Buffered output, 500ns FWHM configuration, 5V (Fe55 signals, gain around 800, 120ke on pad)



Electrical parameters cont'd

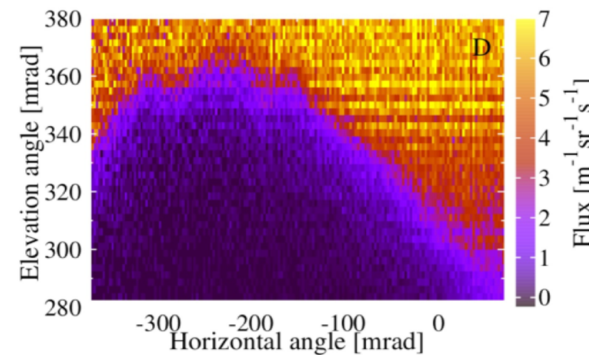
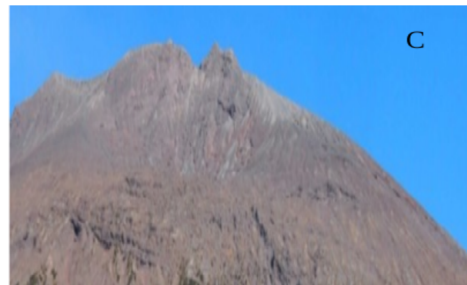
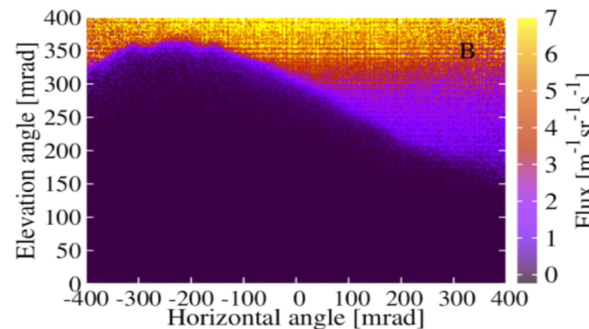
- Dynamic range: nearly full supply range, but linear only in the middle 50%

Buffered output: good linearity from 0 – 3.3V, adjustable DC offset



High performance muon imaging

- Sakurajima Muography Observatory: 3mrad angular resolution, very low background



Scientific Reports, Volume 8, Article number: 3207 (2018)