BIS2: CIBM Reliability Analysis for the LHC

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Beam Interlock System II

Controls Interlocks Beam Manager

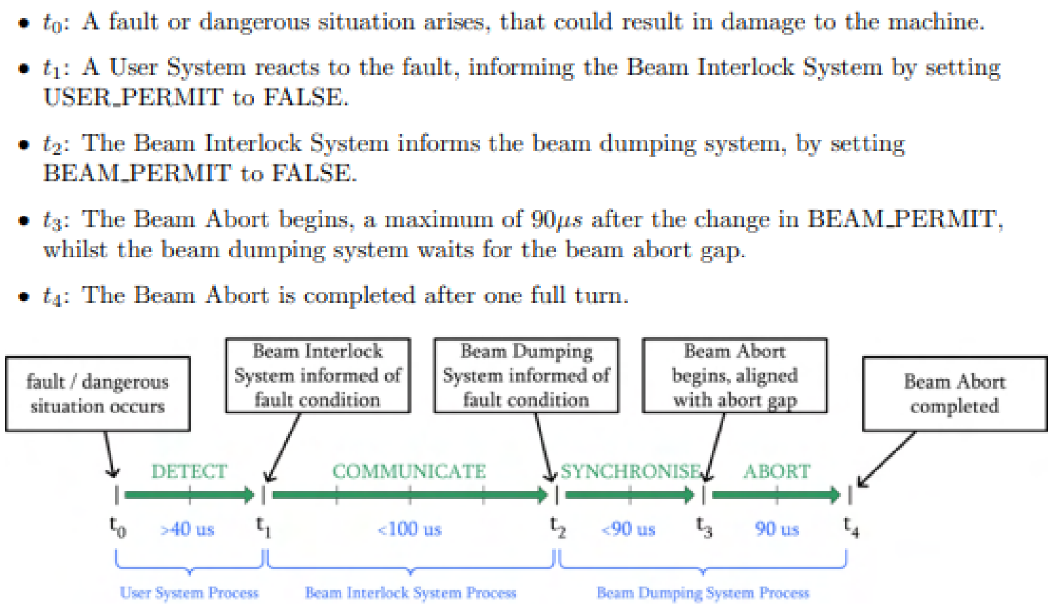
Provisional Results for the Analysis of the CIBM for the Second Version of the BIS in the LHC

Background

- **Beam Interlock System II is the second version of the current BIS, and the plan is to install it in the Long Shutdown 3.**

- **The BIS is installed in not only the LHC, but many more machines. The LHC was looked at first as it is the most stringent.**

- **The BIS takes inputs from User Systems spread around the LHC and prevents beam operation if a User System indicates that there is a problem, or that it is not ready for beam operation.**



- t_0: A fault or dangerous situation arises, that could result in damage to the machine.
- t_1: A User System reacts to the fault, informing the Beam Interlock System by setting USER_PERMIT to FALSE.
- t_2: The Beam Interlock System informs the beam dumping system, by setting BEAM_PERMIT to FALSE.
- t_3: The Beam Abort begins, a maximum of 90μs after the change in BEAM_PERMIT, whilst the beam dumping system waits for the beam abort gap.
- t_4: The Beam Abort is completed after one full turn.

Figure 1: Breakdown of the BIS Reaction Time (B.Todd, 2007)

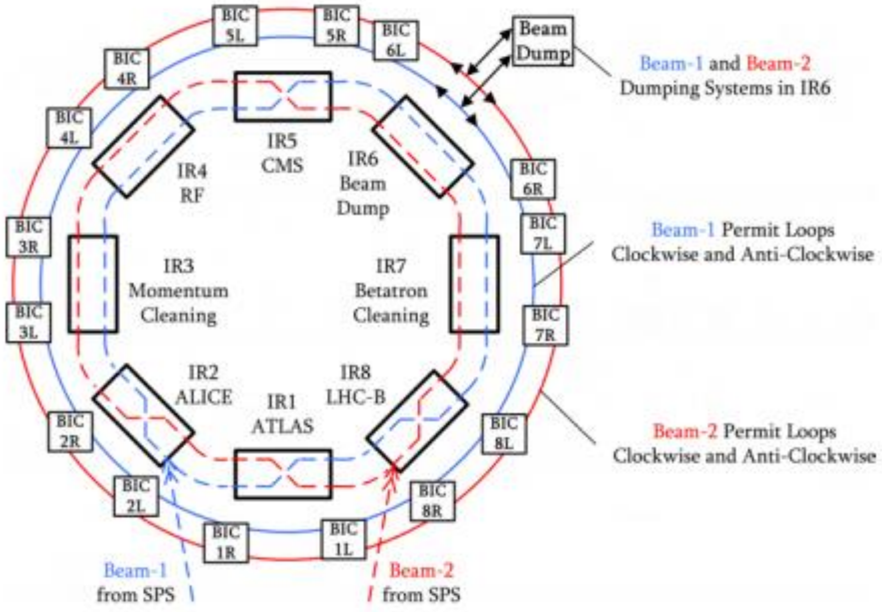
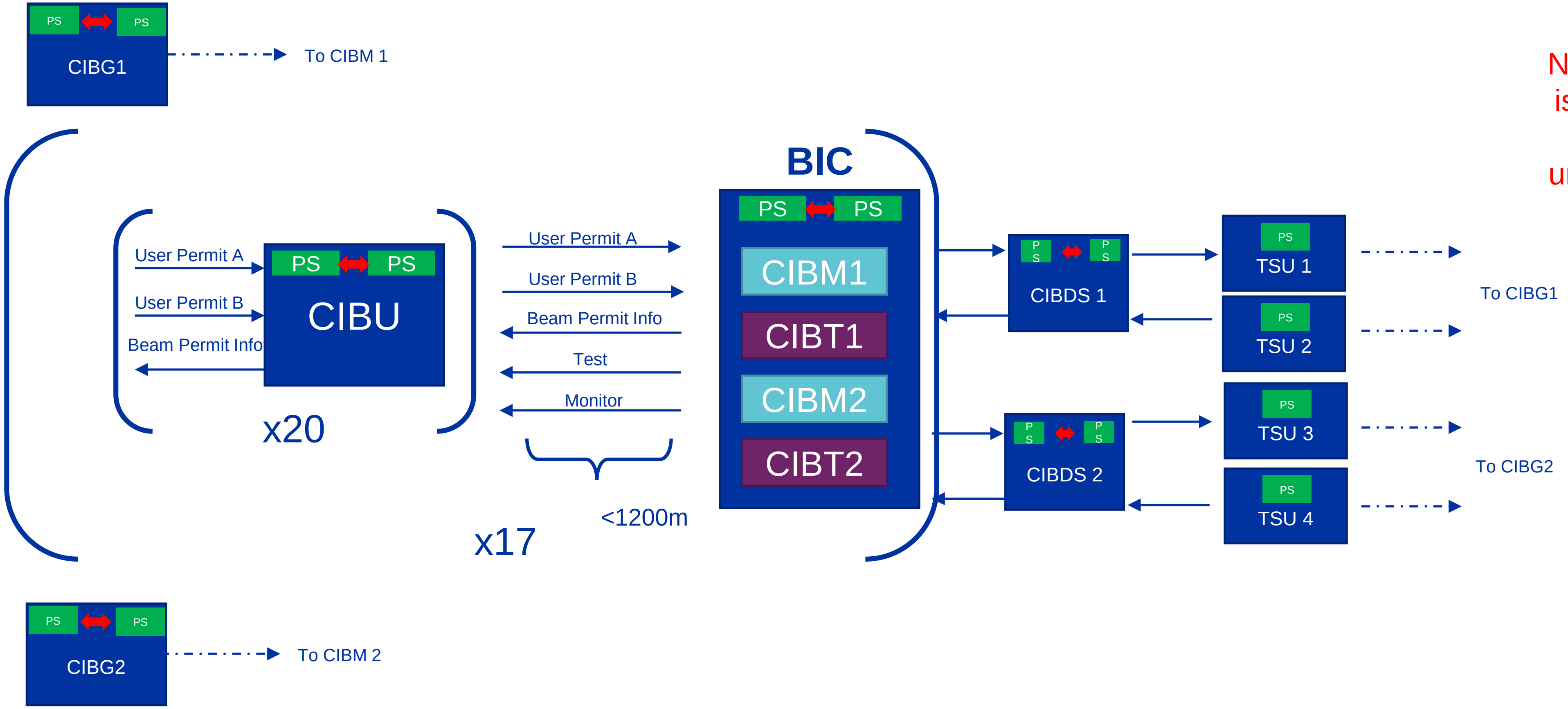


Figure 2: LHC with Permit Loops, Controllers & Dumping System (B.Todd, 2007)

Block Diagram of the Current BIS

- **In order to understand the BIS2 and how the system works, an initial look at the current BIS was carried out.**

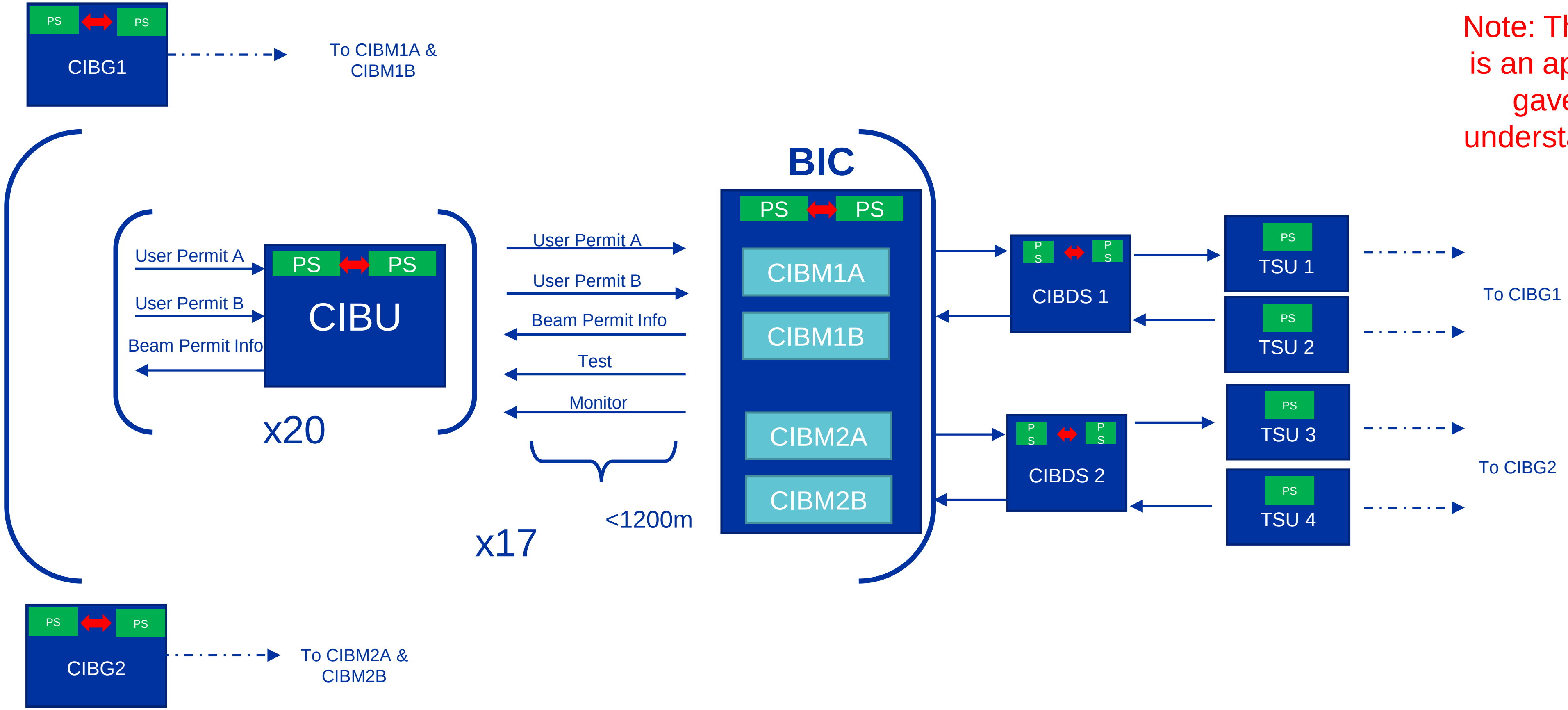
- **This also allowed for a familiarisation of it's functionality and the role of the sub-systems.**



Note: This block diagram is an approximation and gave me an initial understanding of the BIS

Block Diagram of BIS2

- A block diagram of the proposed BIS2 can be drawn up which helps to highlight the high-level differences between the two systems.



Note: This block diagram is an approximation and gave me an initial understanding of the BIS

Approach

- **Initially determining the overall reliability target for the BIS as a system.**

- **Data compiled in the AFT will be used, alongside the "Risk Matrices for CERN Accelerators" document, to determine an acceptable failure rate.**

There are 2 main failure modes of interest that can be identified for the BIS:

- False Dump – Beam dump initiated when no failure occurs.
- Blind Failure – BIS does not initiate a beam dump when there is a failure.

- **Begin with top-down approach to define reliability requirements.**

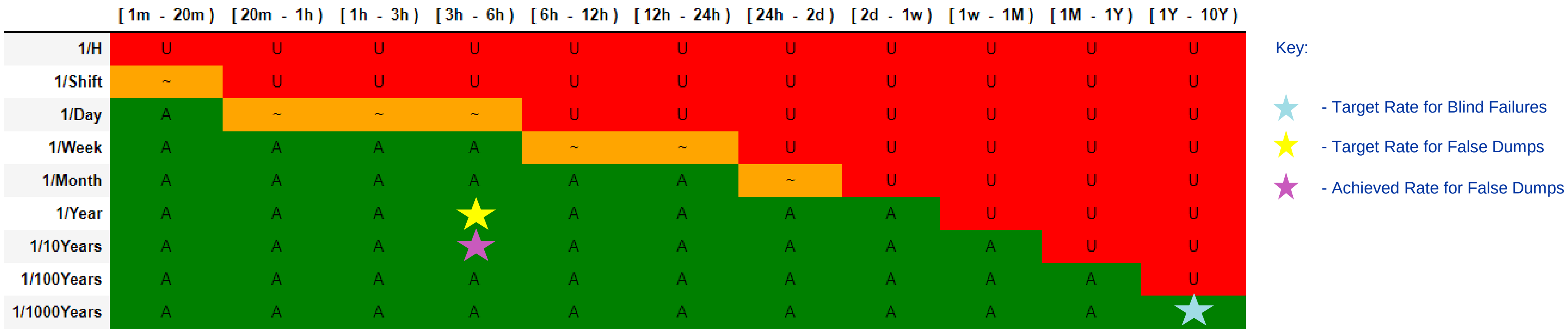
- **Follow this with bottom-up approach (component level analysis) in-line with the top-down requirements.**

- **Using Isograph, we plan to do: Prediction Analysis → FMECA → Fault Tree Analysis.**

- **AvailSim4 to also be used to carry out further analysis and comparison.**

- **Note: This analysis is for the BIS2 present in the LHC. The BIS is also present in the other accelerators and studies will be also be carried out for them.**

Reliability Target for the LHC (Courtesy of Thomas Cartier-Michaud, et al.)



	[1m - 20m)	[20m - 1h)	[1h - 3h)	[3h - 6h)	[6h - 12h)	[12h - 24h)	[24h - 2d)	[2d - 1w)	[1w - 1M)	[1M - 1Y)	[1Y - 10Y)
1/H	U	U	U	U	U	U	U	U	U	U	U
1/Shift	~	U	U	U	U	U	U	U	U	U	U
1/Day	A	~	~	~	U	U	U	U	U	U	U
1/Week	A	A	A	A	~	~	U	U	U	U	U
1/Month	A	A	A	A	A	A	~	U	U	U	U
1/Year	A	A	A	★	A	A	A	A	U	U	U
1/10Years	A	A	A	★	A	A	A	A	A	U	U
1/100Years	A	A	A	A	A	A	A	A	A	A	U
1/1000Years	A	A	A	A	A	A	A	A	A	A	★

Key:

★ - Target Rate for Blind Failures

★ - Target Rate for False Dumps

★ - Achieved Rate for False Dumps

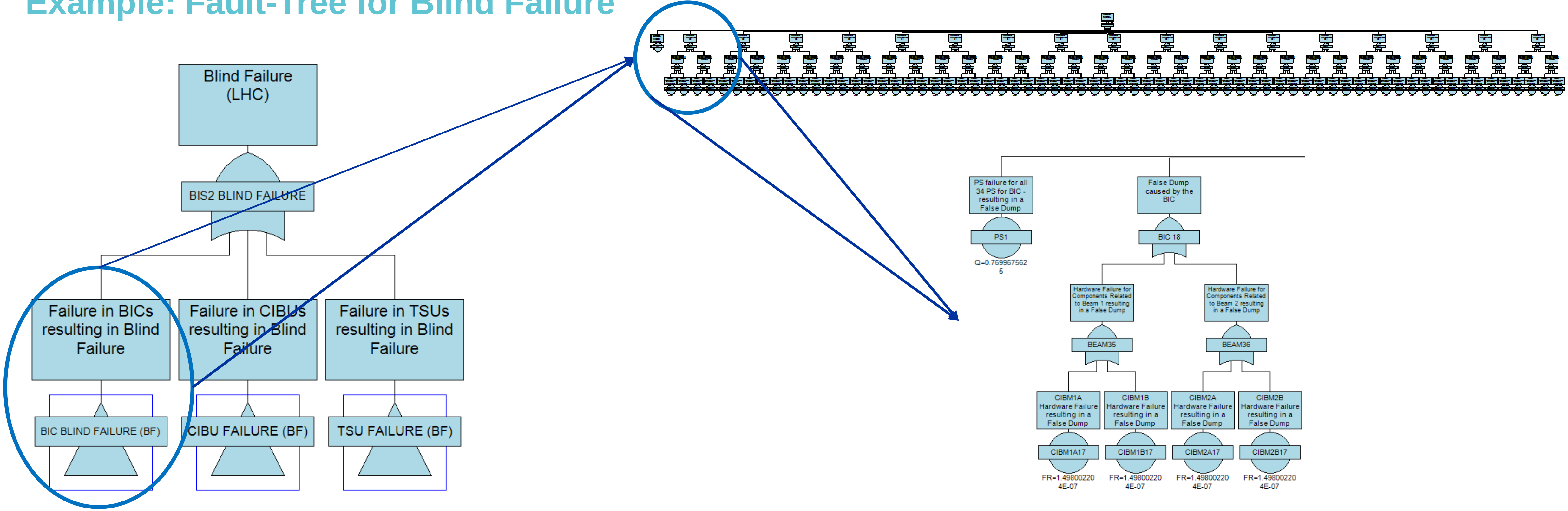
- Using the Risk Matrix above based on AFT data, the rate achieved for the current BIS in operation can be highlighted.
- Achieved rate for False Dumps is covering the period from 2010 – 2018 (there was a 2 year shut down in this period).
- Following this, and the recovery time for the LHC, the reliability target for the BIS2 in the LHC can also be highlighted.

Top-Down Approach to Create a High-Level Fault-Tree in Order to Determine System Reliability

High-Level Fault-Tree Using Isograph

Begun with a top-down approach to identify the causes of the 2 **main** Failure Modes:

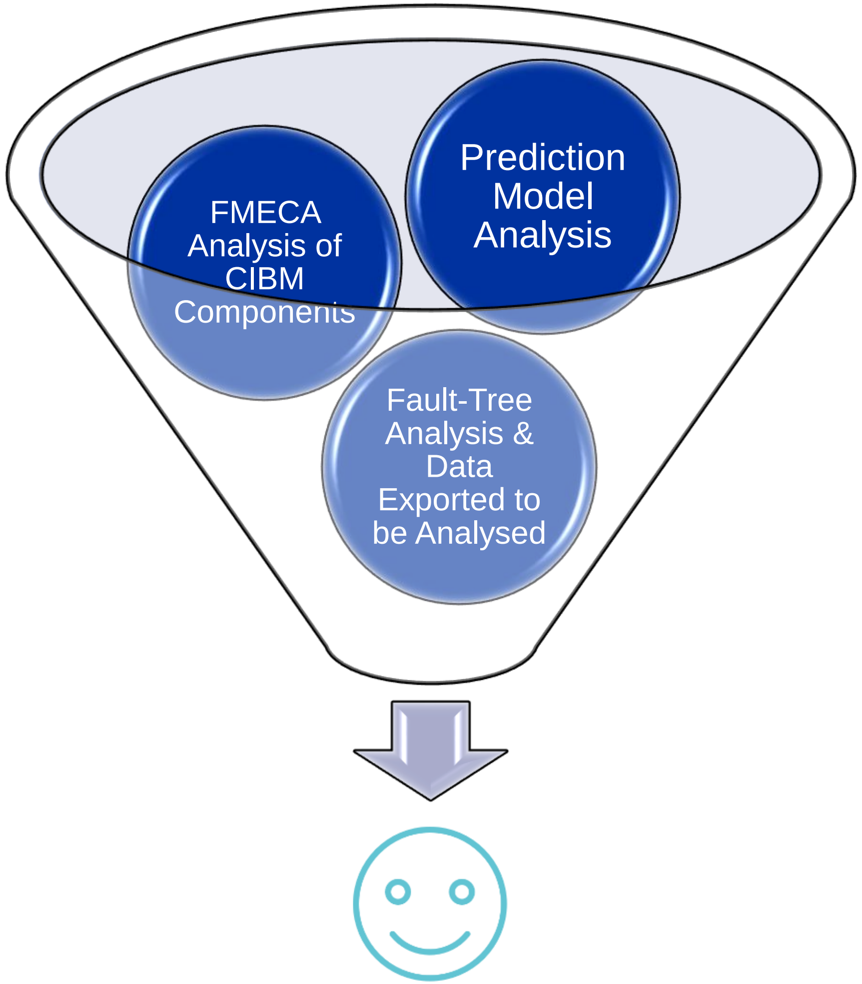
Example: Fault-Tree for Blind Failure



- The aim of the bottom-up approach is to calculate the failure rates of the individual sub-systems belonging to the fault-tree.
- These can then be inputted into the fault-tree above. This presentation is showing the failure rate calculation of the CIBM.

Bottom-Up Approach to Determine the Reliability of the CIBM

Approach Taken using Isograph

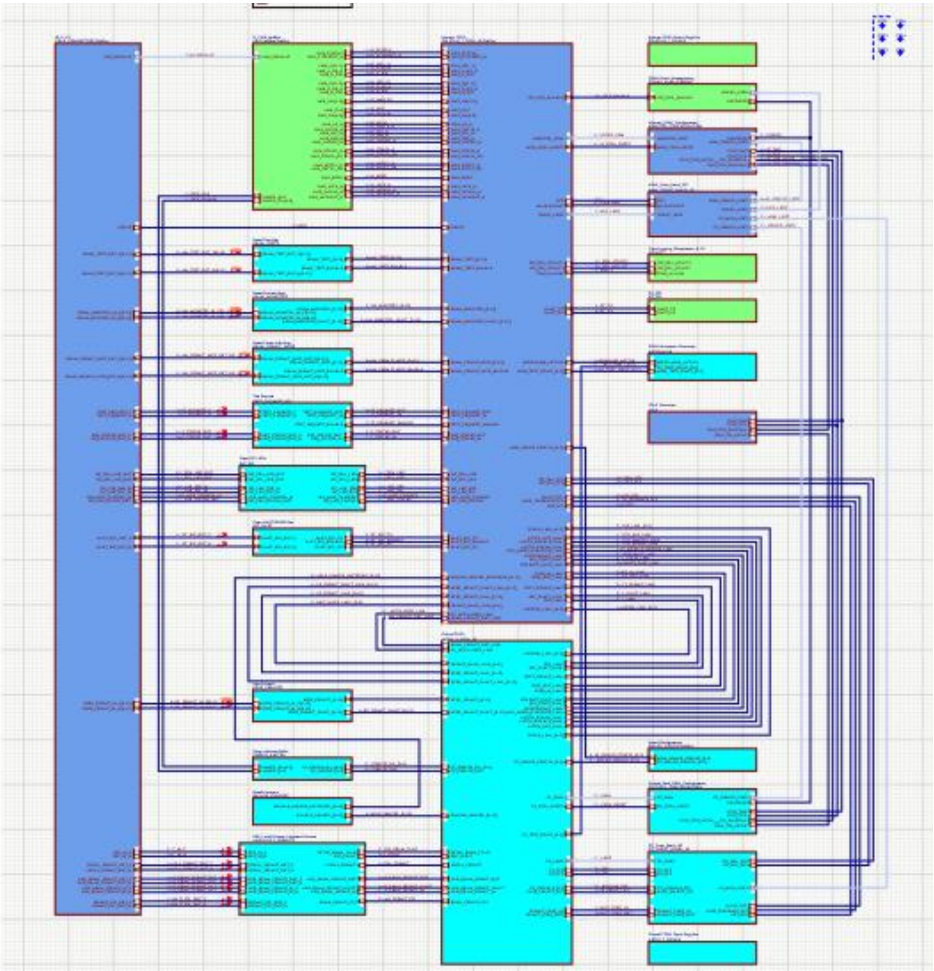


FMECA Analysis of CIBM Components

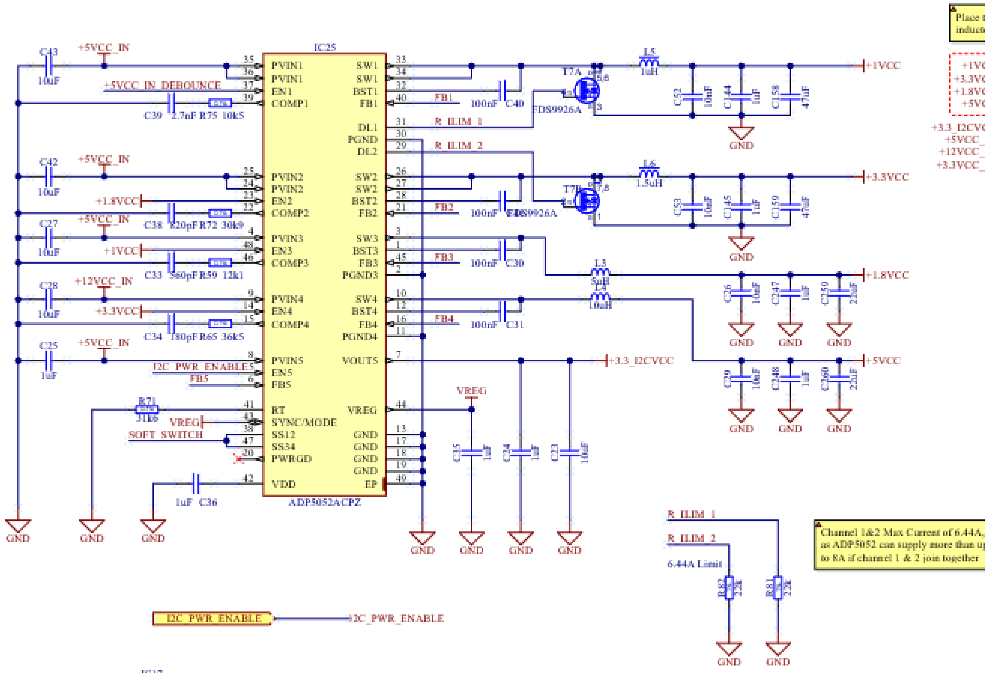
Prediction Model Analysis

Fault-Tree Analysis & Data Exported to be Analysed

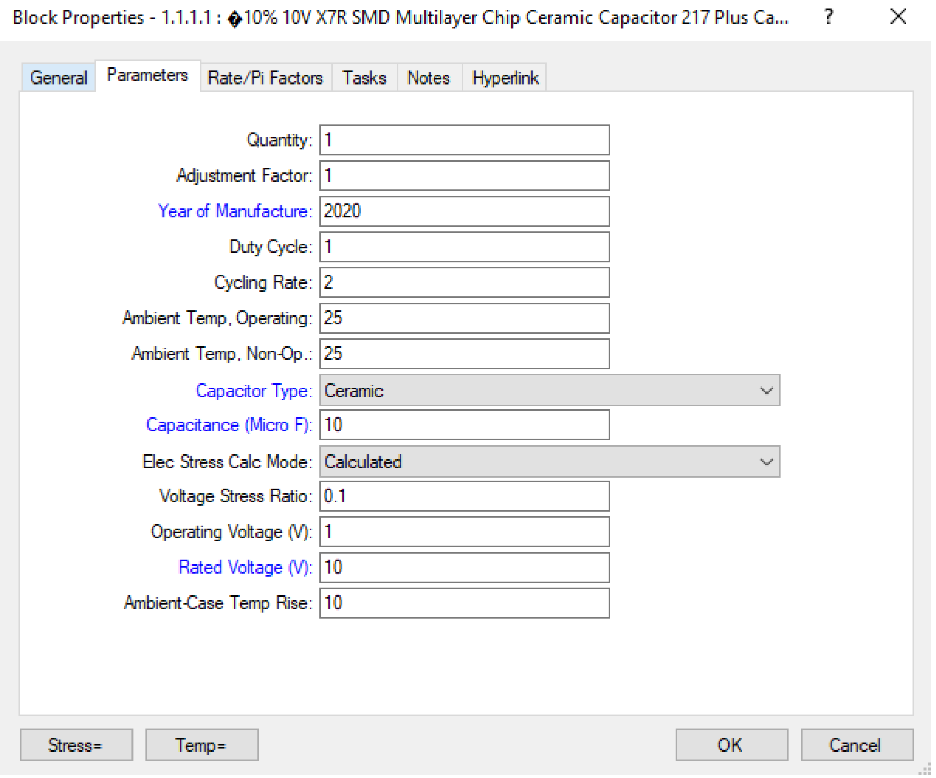
Controls Interlocks Beam Manager



- **In total, there are 347 individual components that need to be individually analysed:**
  - Failure rates determined
  - FMECA analysis

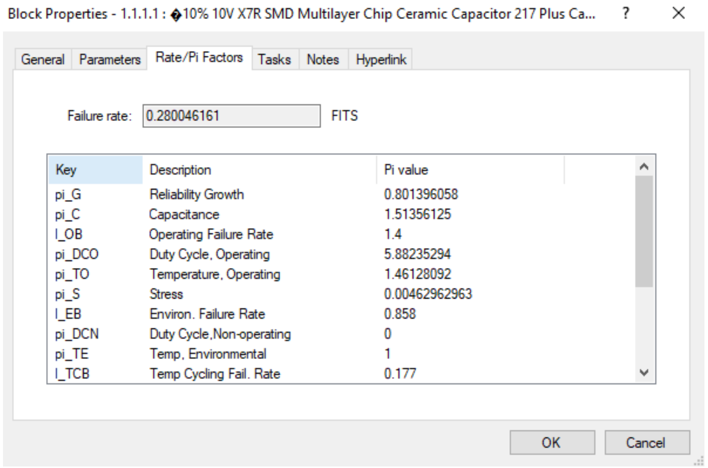


Prediction Model Analysis



Block Properties - 1.1.1.1 : �10% 10V X7R SMD Multilayer Chip Ceramic Capacitor 217 Plus Ca...

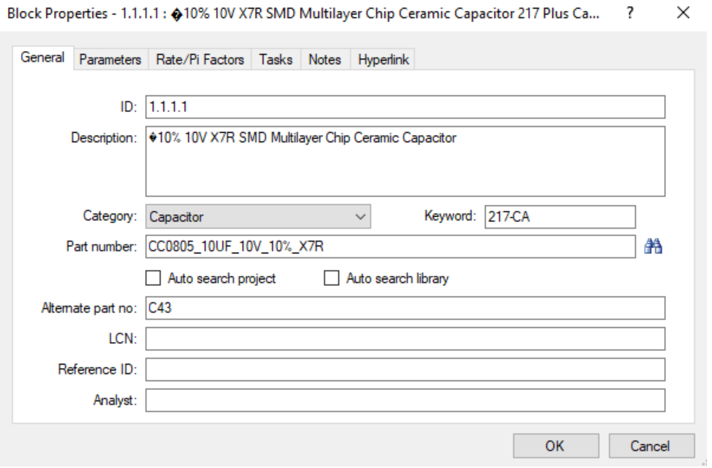
Quantity: 1
Adjustment Factor: 1
Year of Manufacture: 2020
Duty Cycle: 1
Cycling Rate: 2
Ambient Temp, Operating: 25
Ambient Temp, Non-Op.: 25
Capacitor Type: Ceramic
Capacitance (Micro F): 10
Elec Stress Calc Mode: Calculated
Voltage Stress Ratio: 0.1
Operating Voltage (V): 1
Rated Voltage (V): 10
Ambient-Case Temp Rise: 10



Block Properties - 1.1.1.1 : �10% 10V X7R SMD Multilayer Chip Ceramic Capacitor 217 Plus Ca...

Failure rate: 0.280046161 FITS

Key	Description	Pi value
pi_G	Reliability Growth	0.801396058
pi_C	Capacitance	1.51356125
l_OB	Operating Failure Rate	1.4
pi_DCO	Duty Cycle, Operating	5.88235294
pi_TO	Temperature, Operating	1.46128092
pi_S	Stress	0.00462962963
l_EB	Environ. Failure Rate	0.858
pi_DCN	Duty Cycle,Non-operating	0
pi_TE	Temp, Environmental	1
l_TCB	Temp Cycling Fail. Rate	0.177



Block Properties - 1.1.1.1 : �10% 10V X7R SMD Multilayer Chip Ceramic Capacitor 217 Plus Ca...

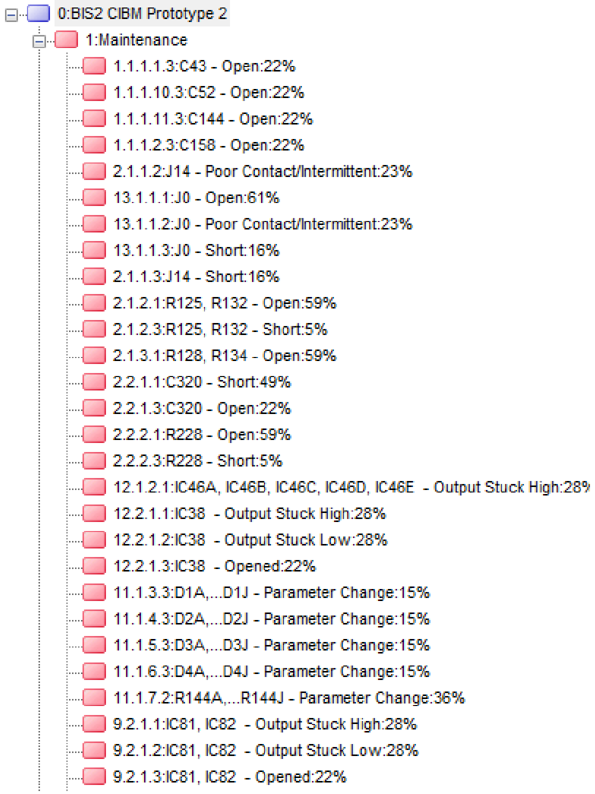
ID: 1.1.1.1
Description: �10% 10V X7R SMD Multilayer Chip Ceramic Capacitor
Category: Capacitor
Keyword: 217-CA
Part number: CC0805_10UF_10V_10%_X7R
☐ Auto search project ☐ Auto search library
Alternate part no: C43
LCN:
Reference ID:
Analyst:

- For each component in the CIBM we estimate the failure rate with the **Military Handbook 217+.**
- When the military handbook doesn't provide any data, we take the manufactures failure rate and input that directly in the Isograph.

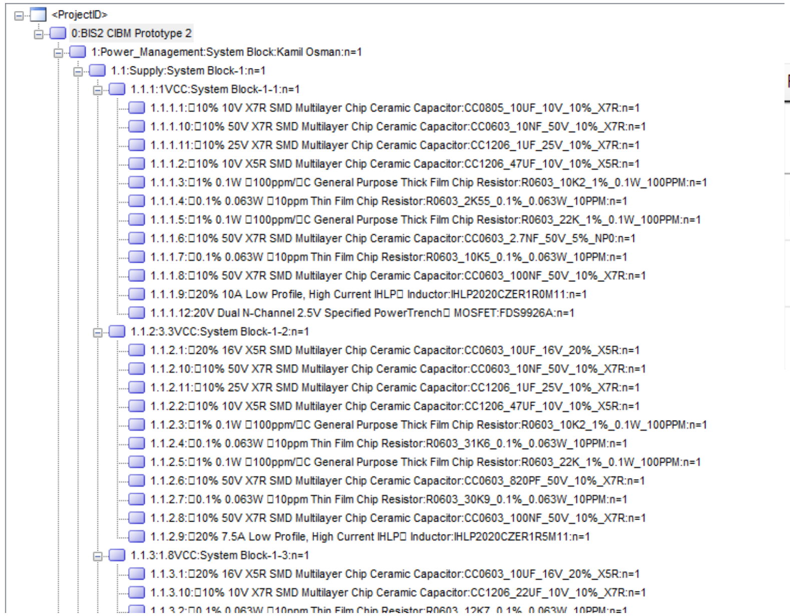
- Assumptions taken:
  - Duty Cycle = 1
  - Cycling Rate = 2
  - Ambient Case Rise 10
  - Relative Humidity Factor = 1
  - Inputs for the Voltage Stress Ratio was taken from the schematics of the CIBM in Altium.
- Time invested ~ 4 weeks.

FMECA Analysis

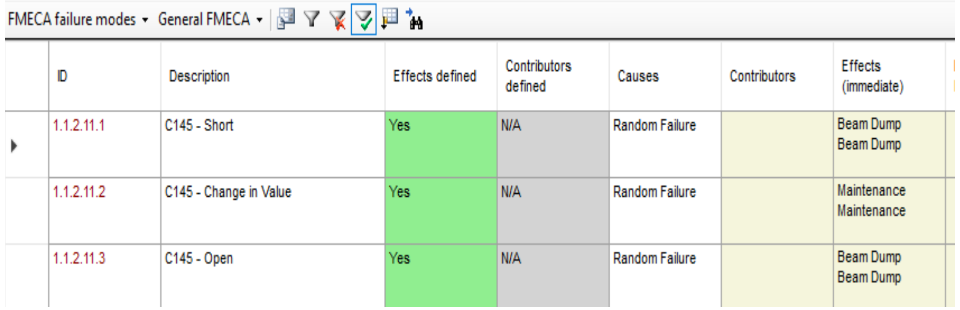
- **This analysis was done together with the BIS team. Every failure mode for every component was looked at to determine the failure effect.**
- **Used the Military Handbook 338 to determine the apportionment failure rate of component types.**
- **Time invested ~ 8 weeks.**



- 0:BIS2 CIBM Prototype 2
  - 1:Maintenance
    - 1.1.1.1.3:C43 - Open:22%
    - 1.1.1.10.3:C52 - Open:22%
    - 1.1.1.11.3:C144 - Open:22%
    - 1.1.1.2.3:C158 - Open:22%
    - 2.1.1.2:J14 - Poor Contact/Intermittent:23%
    - 13.1.1.1:J0 - Open:61%
    - 13.1.1.2:J0 - Poor Contact/Intermittent:23%
    - 13.1.1.3:J0 - Short:16%
    - 2.1.1.3:J14 - Short:16%
    - 2.1.2.1:R125, R132 - Open:59%
    - 2.1.2.3:R125, R132 - Short:5%
    - 2.1.3.1:R128, R134 - Open:59%
    - 2.2.1.1:C320 - Short:49%
    - 2.2.1.3:C320 - Open:22%
    - 2.2.2.1:R228 - Open:59%
    - 2.2.2.3:R228 - Short:5%
    - 12.1.2.1:IC46A, IC46B, IC46C, IC46D, IC46E - Output Stuck High:28%
    - 12.2.1.1:IC38 - Output Stuck High:28%
    - 12.2.1.2:IC38 - Output Stuck Low:28%
    - 12.2.1.3:IC38 - Opened:22%
    - 11.1.3.3:D1A,...D1J - Parameter Change:15%
    - 11.1.4.3:D2A,...D2J - Parameter Change:15%
    - 11.1.5.3:D3A,...D3J - Parameter Change:15%
    - 11.1.6.3:D4A,...D4J - Parameter Change:15%
    - 11.1.7.2:R144A,...R144J - Parameter Change:36%
    - 9.2.1.1:IC81, IC82 - Output Stuck High:28%
    - 9.2.1.2:IC81, IC82 - Output Stuck Low:28%
    - 9.2.1.3:IC81, IC82 - Opened:22%

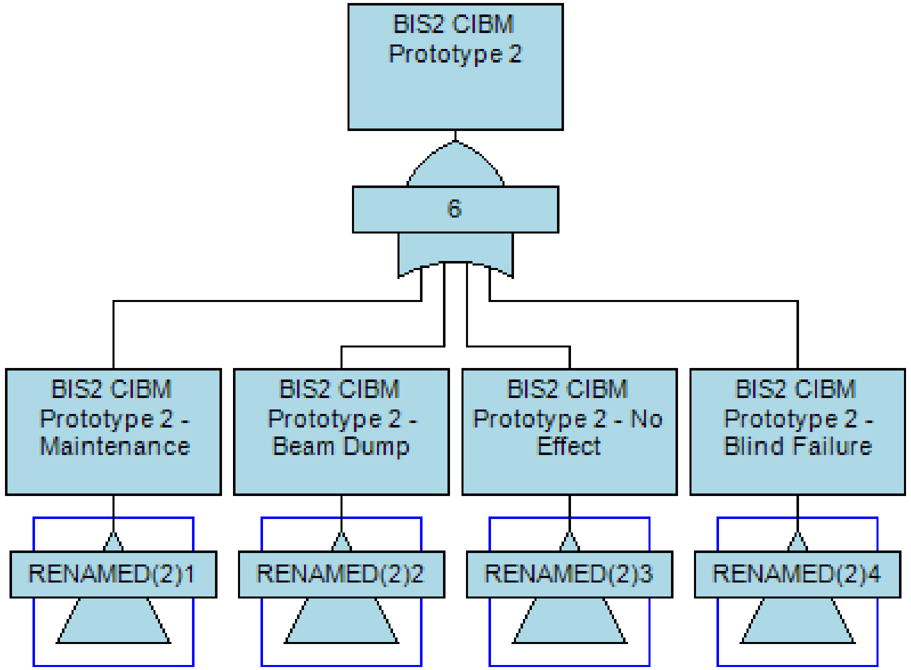


- <ProjectID>
  - 0:BIS2 CIBM Prototype 2
    - 1:Power_Management:System Block:Kamil Osman:n=1
      - 1.1:Supply:System Block-1:n=1
        - 1.1.1:1VCC:System Block-1-1:n=1
          - 1.1.1.1:□10% 10V X7R SMD Multilayer Chip Ceramic Capacitor:CC0805_10UF_10V_10%_X7R:n=1
          - 1.1.1.10:□10% 50V X7R SMD Multilayer Chip Ceramic Capacitor:CC0603_10NF_50V_10%_X7R:n=1
          - 1.1.1.11:□10% 25V X7R SMD Multilayer Chip Ceramic Capacitor:CC1206_1UF_25V_10%_X7R:n=1
          - 1.1.1.2:□10% 10V X5R SMD Multilayer Chip Ceramic Capacitor:CC1206_47UF_10V_10%_X5R:n=1
          - 1.1.1.3:□1% 0.1W □100ppm/□C General Purpose Thick Film Chip Resistor:R0603_10K2_1%_0.1W_100PPM:n=1
          - 1.1.1.4:□0.1% 0.063W □10ppm Thin Film Chip Resistor:R0603_2K55_0.1%_0.063W_10PPM:n=1
          - 1.1.1.5:□1% 0.1W □100ppm/□C General Purpose Thick Film Chip Resistor:R0603_22K_1%_0.1W_100PPM:n=1
          - 1.1.1.6:□10% 50V X7R SMD Multilayer Chip Ceramic Capacitor:CC0603_2.7NF_50V_5%_NP0:n=1
          - 1.1.1.7:□0.1% 0.063W □10ppm Thin Film Chip Resistor:R0603_10K5_0.1%_0.063W_10PPM:n=1
          - 1.1.1.8:□10% 50V X7R SMD Multilayer Chip Ceramic Capacitor:CC0603_100NF_50V_10%_X7R:n=1
          - 1.1.1.9:□20% 10A Low Profile, High Current IHLP□ Inductor:IHLP2020CZER1R0M11:n=1
          - 1.1.1.12:20V Dual N-Channel 2.5V Specified PowerTrench□ MOSFET:FDS9926A:n=1
        - 1.1.2:3.3VCC:System Block-1-2:n=1
          - 1.1.2.1:□20% 16V X5R SMD Multilayer Chip Ceramic Capacitor:CC0603_10UF_16V_20%_X5R:n=1
          - 1.1.2.10:□10% 50V X7R SMD Multilayer Chip Ceramic Capacitor:CC0603_10NF_50V_10%_X7R:n=1
          - 1.1.2.11:□10% 25V X7R SMD Multilayer Chip Ceramic Capacitor:CC1206_1UF_25V_10%_X7R:n=1
          - 1.1.2.2:□10% 10V X5R SMD Multilayer Chip Ceramic Capacitor:CC1206_47UF_10V_10%_X5R:n=1
          - 1.1.2.3:□1% 0.1W □100ppm/□C General Purpose Thick Film Chip Resistor:R0603_10K2_1%_0.1W_100PPM:n=1
          - 1.1.2.4:□0.1% 0.063W □10ppm Thin Film Chip Resistor:R0603_31K6_0.1%_0.063W_10PPM:n=1
          - 1.1.2.5:□1% 0.1W □100ppm/□C General Purpose Thick Film Chip Resistor:R0603_22K_1%_0.1W_100PPM:n=1
          - 1.1.2.6:□10% 50V X7R SMD Multilayer Chip Ceramic Capacitor:CC0603_820PF_50V_10%_X7R:n=1
          - 1.1.2.7:□0.1% 0.063W □10ppm Thin Film Chip Resistor:R0603_30K9_0.1%_0.063W_10PPM:n=1
          - 1.1.2.8:□10% 50V X7R SMD Multilayer Chip Ceramic Capacitor:CC0603_100NF_50V_10%_X7R:n=1
          - 1.1.2.9:□20% 7.5A Low Profile, High Current IHLP□ Inductor:IHLP2020CZER1R5M11:n=1
        - 1.1.3:1.8VCC:System Block-1-3:n=1
          - 1.1.3.1:□20% 16V X5R SMD Multilayer Chip Ceramic Capacitor:CC0603_10UF_16V_20%_X5R:n=1
          - 1.1.3.10:□10% 10V X7R SMD Multilayer Chip Ceramic Capacitor:CC1206_22UF_10V_10%_X7R:n=1
          - 1.1.3.2:□0.1% 0.063W □10ppm Thin Film Chip Resistor:R0603_12K7_0.1%_0.063W_10PPM:n=1



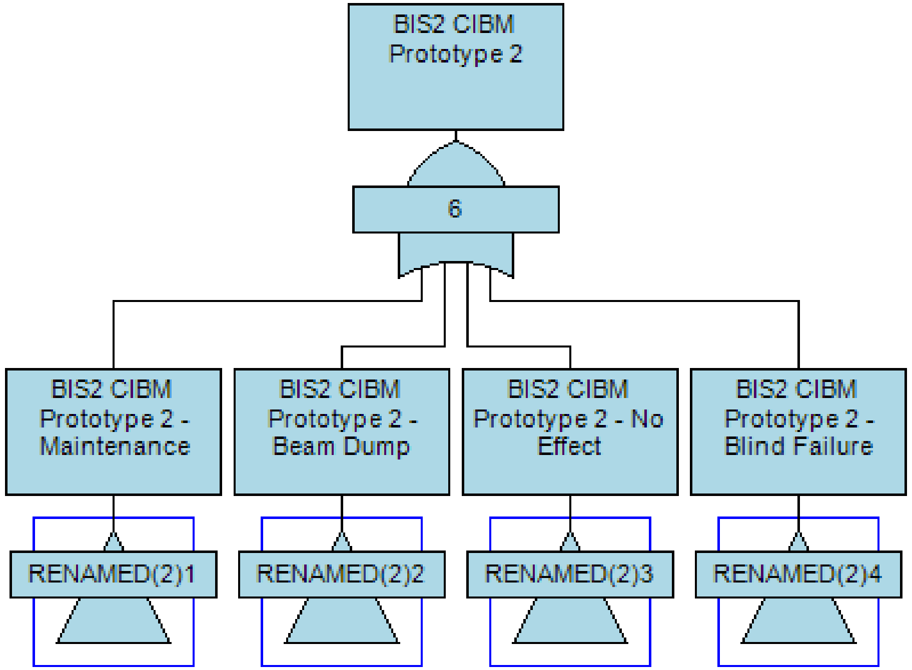
	ID	Description	Effects defined	Contributors defined	Causes	Contributors	Effects (immediate)
▶	1.1.2.11.1	C145 - Short	Yes	N/A	Random Failure		Beam Dump Beam Dump
	1.1.2.11.2	C145 - Change in Value	Yes	N/A	Random Failure		Maintenance Maintenance
	1.1.2.11.3	C145 - Open	Yes	N/A	Random Failure		Beam Dump Beam Dump

CIBM Analysis – Results for a Single CIBM



- **There are 4 main failure modes that have been identified through the FMECA analysis:**
  - **Blind Failure**
  - **False Dump**
  - No Effect
  - Maintenance
- **This fault-tree is generated automatically through Isograph following the FMECA analysis.**

CIBM Analysis – Results for a Single CIBM

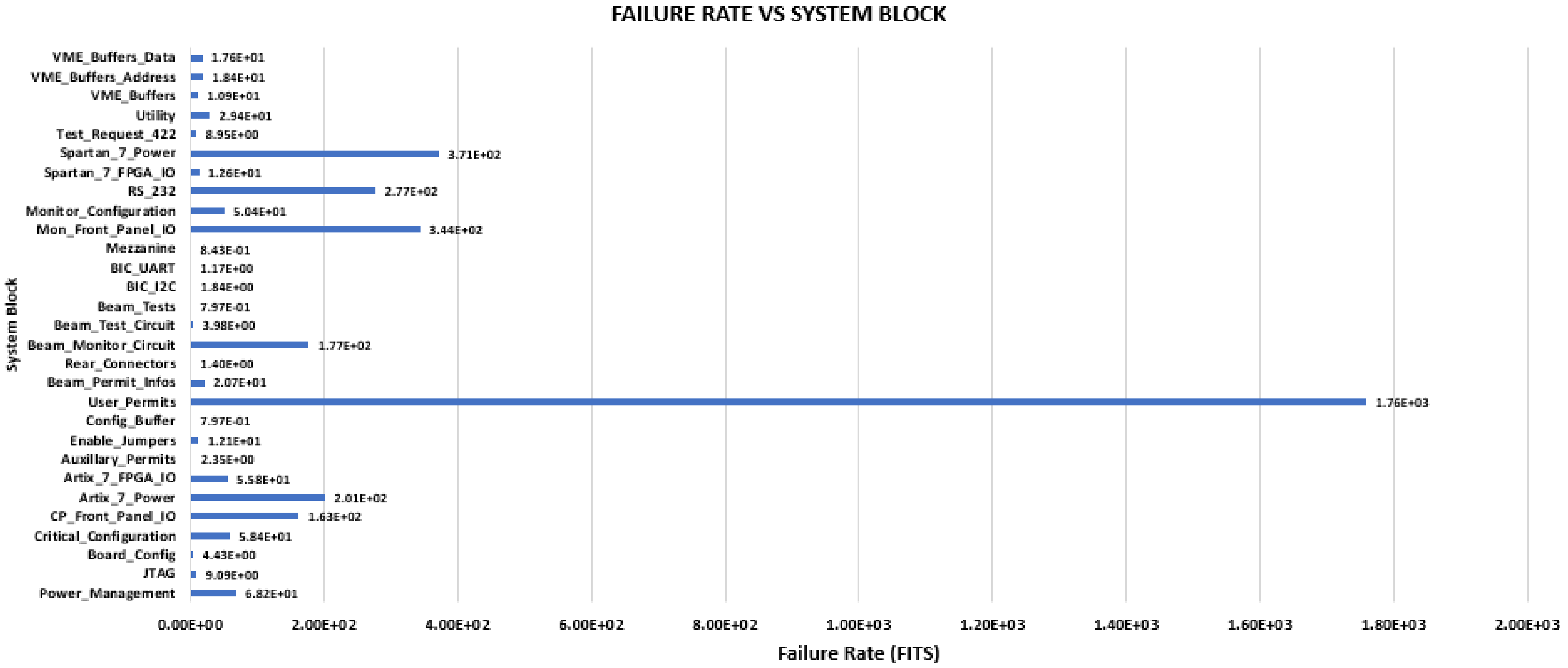


Once the fault-tree is created, Isograph can run a simulation to calculate the reliability of the system depending on the inputted time period.

	Reliability for a 10 Year Period	Reliability for a 1 Year Period	Reliability for a 1 Week Period	Reliability for a 1 LHC Day (20h Fill)	Reliability for a 10 hour fill
Overall	0.9767210826	0.9976473567	0.9999548287	0.9999946224	0.9999973112
Blind Failure	0.9999379863	0.9999937985	0.9999998811	0.9999999858	0.9999999929
False Dump	0.9869632253	0.9986886107	0.9999748339	0.999997004	0.999998502
No Effect	0.9955921688	0.9995583401	0.999991528	0.9999989914	0.9999994957
Maintenance	0.9940656165	0.9994049709	0.9999885852	0.9999986411	0.9999993205

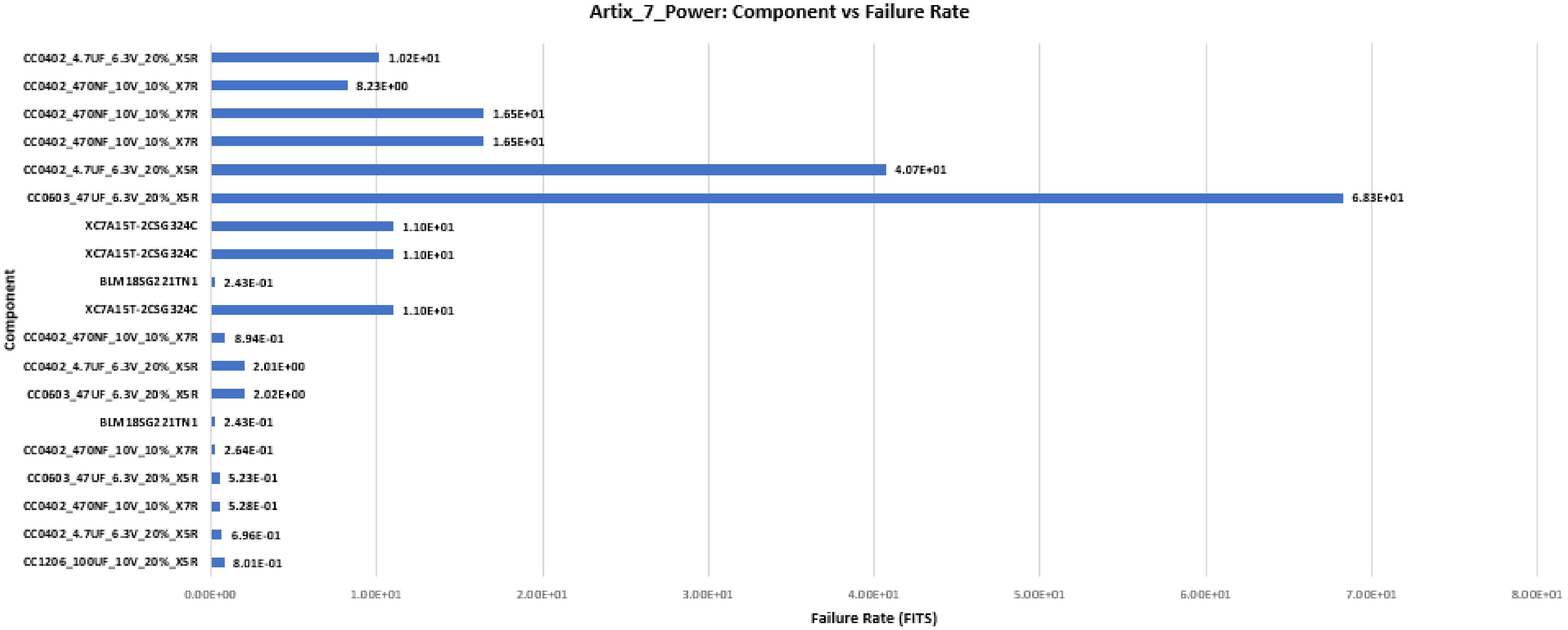
CIBM Analysis – Results for a Single CIBM

On the global CIBM behaviour, the failure rate by sub-system type in the CIBM was identified:

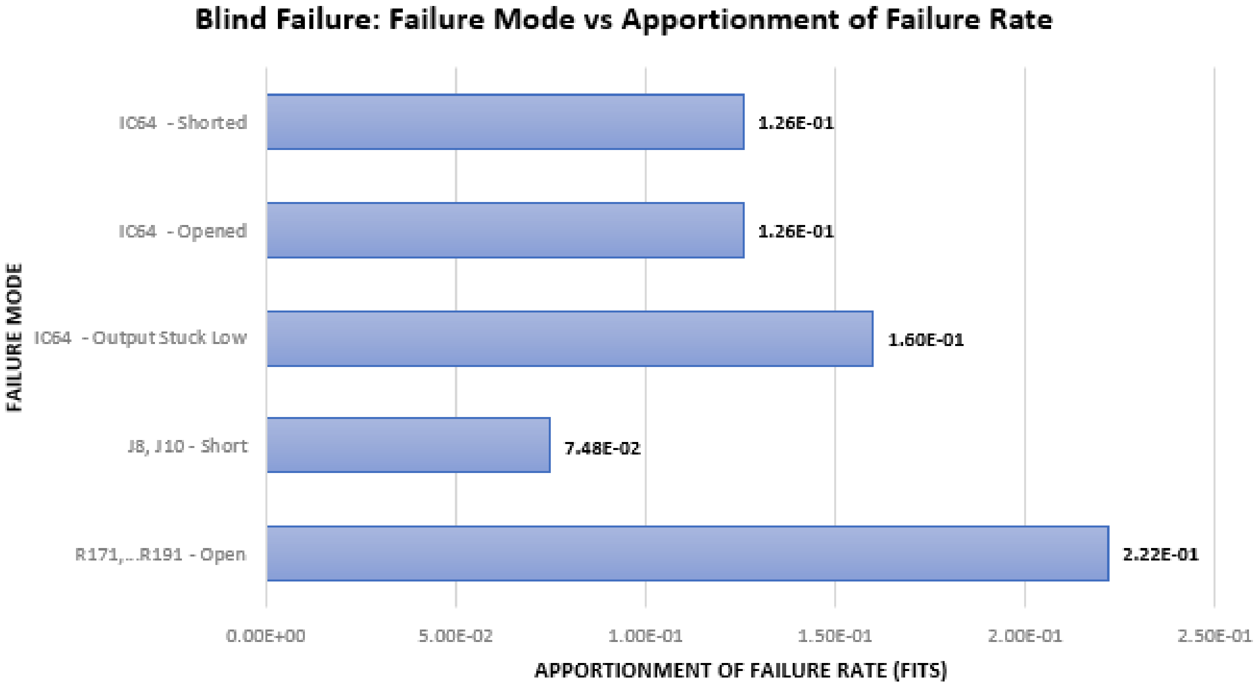


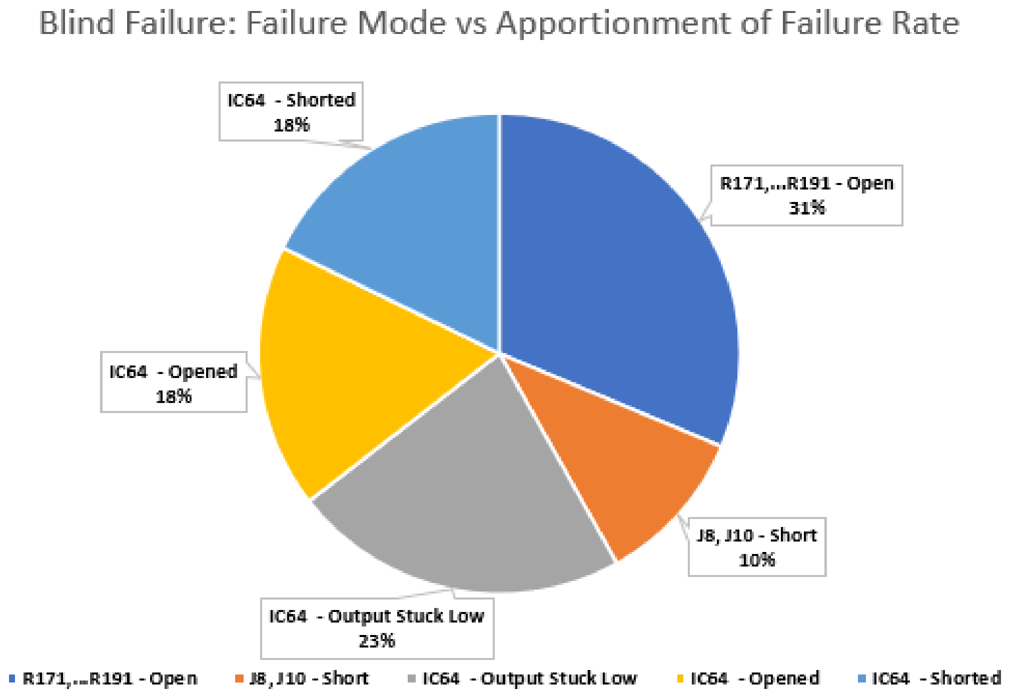
CIBM Analysis – Results for a Single CIBM

Additionally, a breakdown by the sub-system type within the CIBM was provided to the BIS team. A plot below shows the component vs failure rate of the Artix_7_Power, as an example:



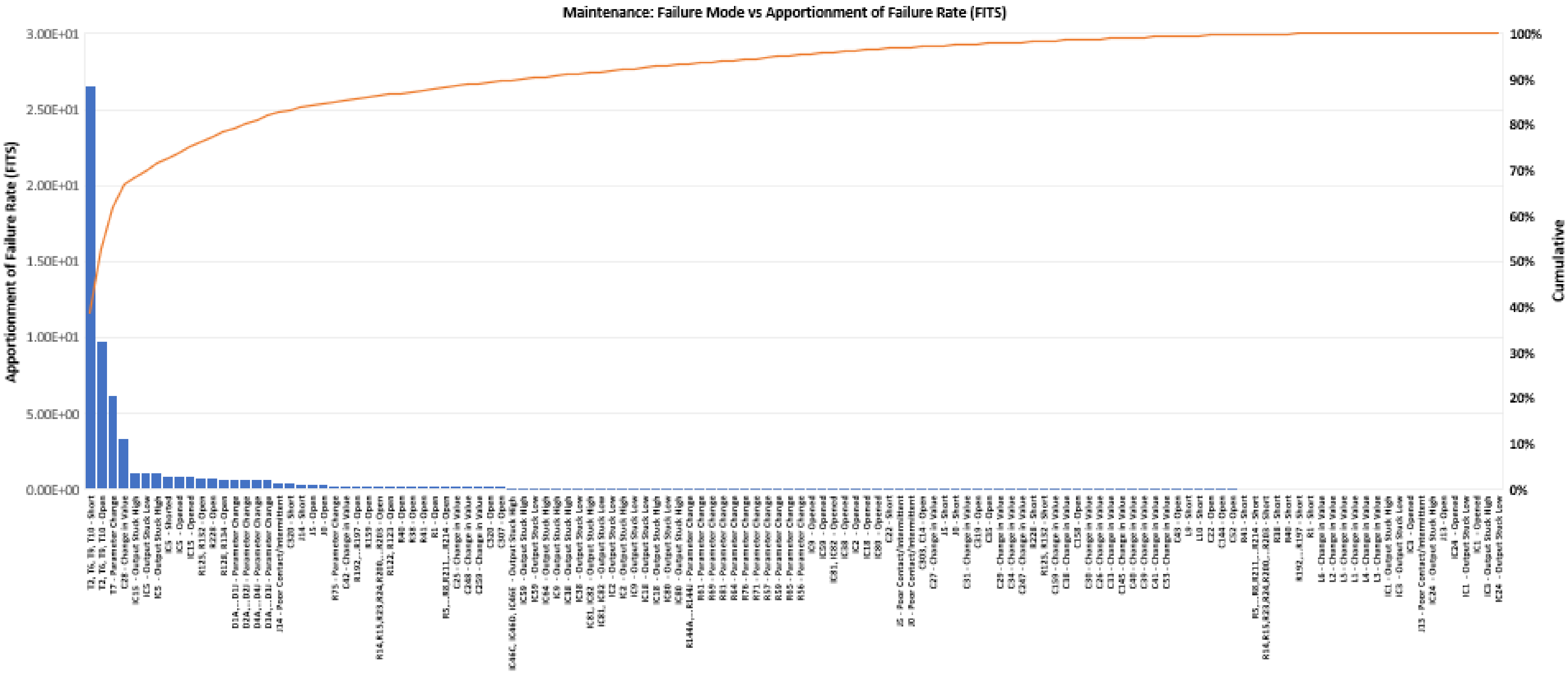
CIBM Analysis – Results for a Single CIBM





- **All the data created through Isograph following the prediction and FMECA analysis was exported out of Isograph to create out further analysis on Excel.**
- **We provided additional detailed results to the system experts for further evaluation. This included failure rates by component types and sub-systems, and by failure effects.**

CIBM Analysis – Results for a Single CIBM

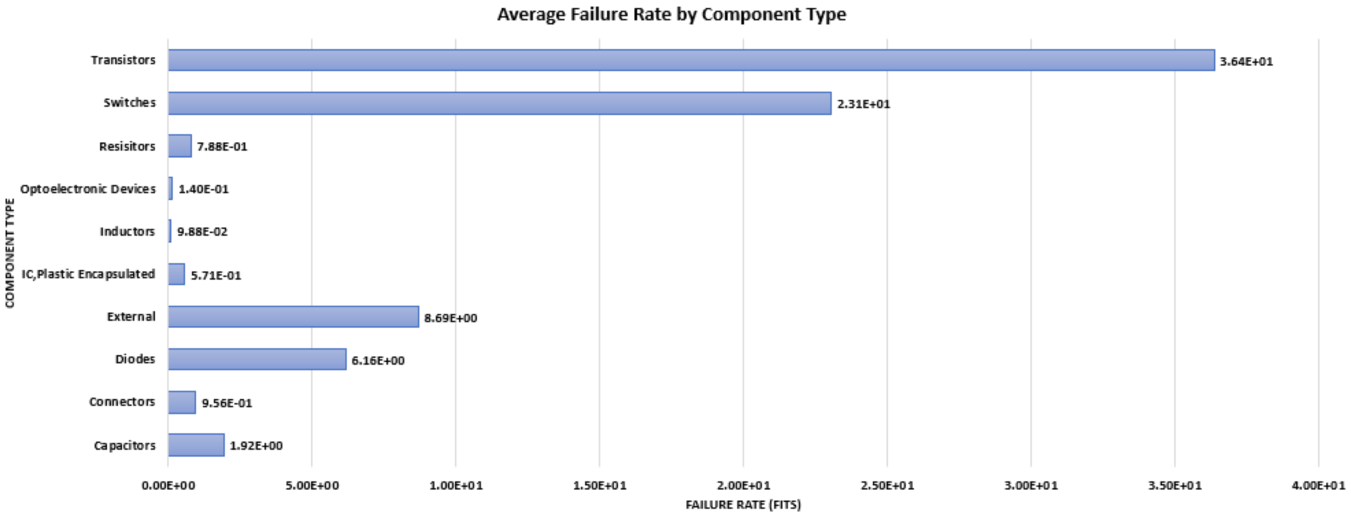


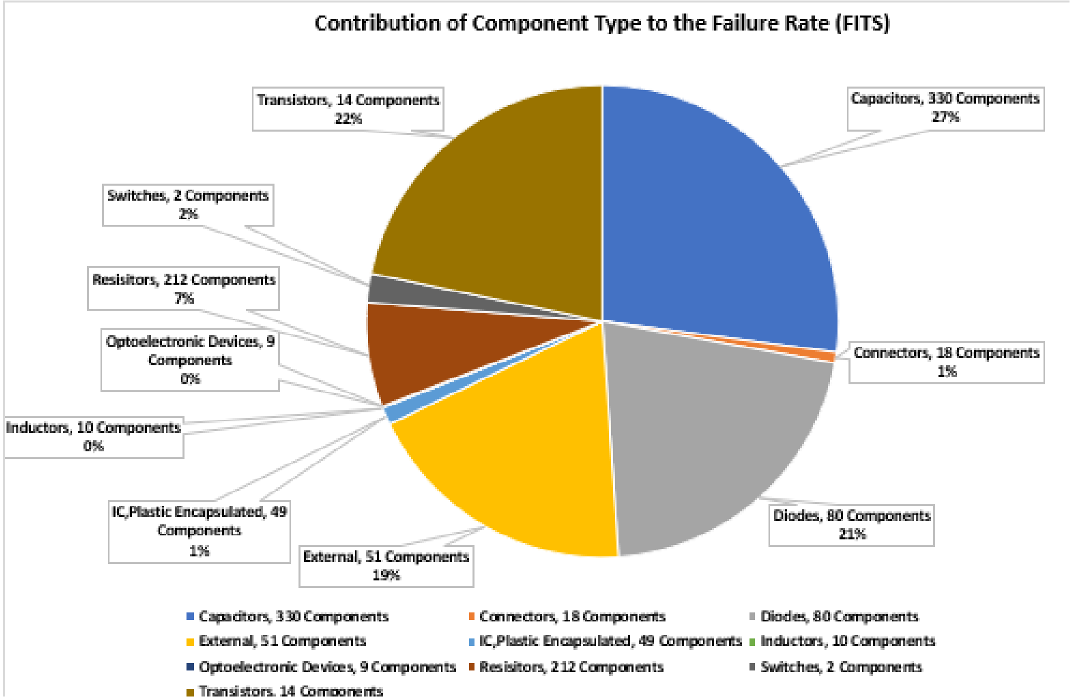
This chart was created for each of the failure modes to show the failure effects. This clearly highlights to the experts the largest contributors to the given failure effects.

CIBM Analysis – Results for a Single CIBM

- **Plots were also created for the CIBM in its entirety.**

- **The system experts were given data on how the chosen component types contributed to the overall failure rate.**





Conclusions & Outlook

- **We have analysed the CIBM prototype for the BIS2 and have used the full chain of tools available on Isograph, from Prediction → FMECA → Fault-Tree Modelling.**
- **The results were provided to the experts for further analysis and feedback.**
- **The analysis of a single CIBM took 3 months to complete, but this has established a clear route on how to carry out the analysis for the remaining sub-systems of BIS2.**
- **The results are only covering a single CIBM. There are 68 CIBMs that all need to be analysed. The next step is to begin the analysis of the CIBU with the system experts, which there are 200. When all the sub-systems have been analysed, a model for the entire BIS needs to be completed.**

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