The CMS Endcap Timing Layer

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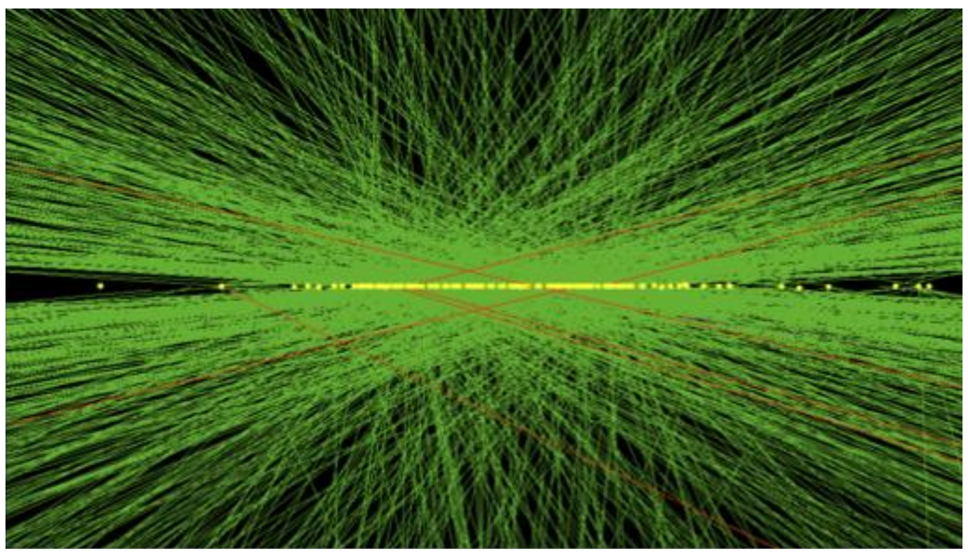
Outline

- Why is timing important for LHC experiments?
- Challenges in the endcap region of CMS
- Sensor technology, design and performance
- Modules, readout and services
- Putting everything together: the ETL detector
- Outlook

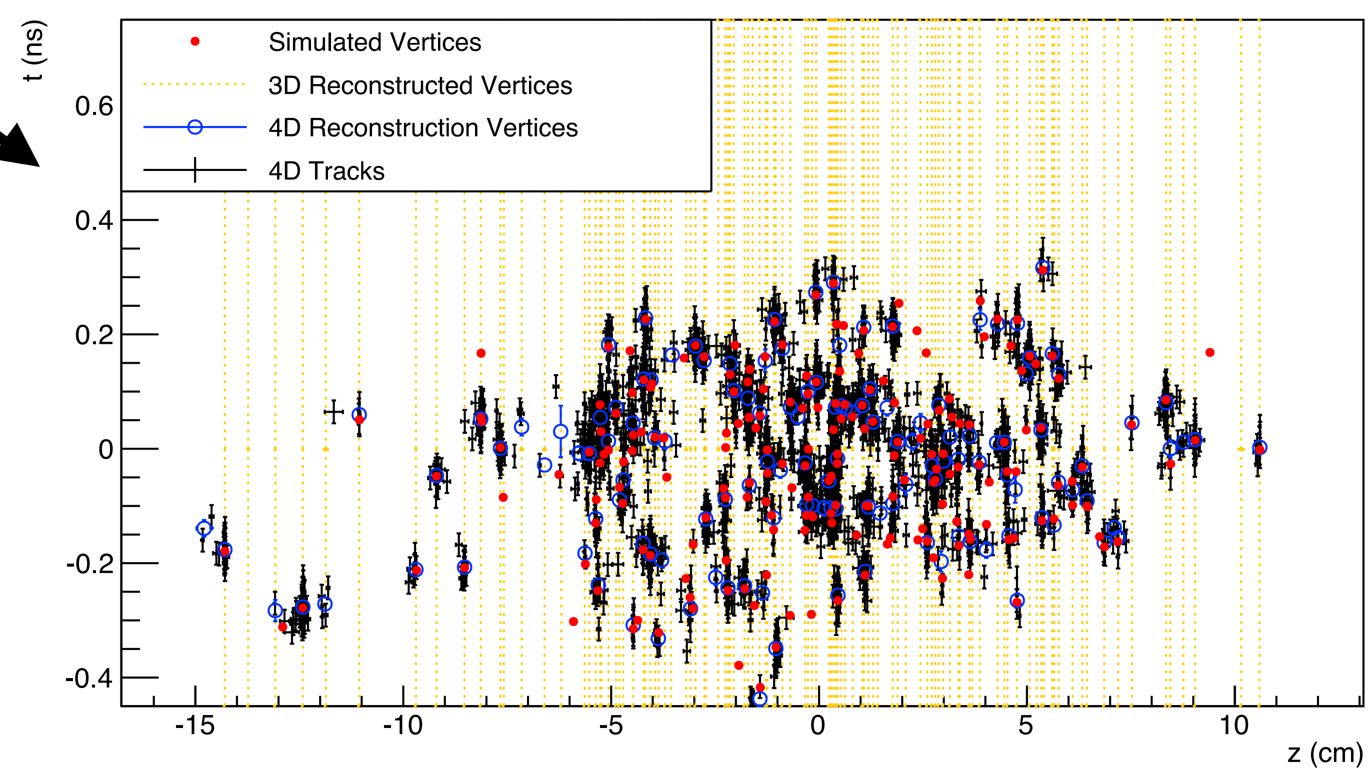
Why timing, why now?

- High Luminosity ➞ large number of pileup interactions, from <μ>=38 at the end of Run 2 to <μ>=200
- Precision timing information for tracks and vertices helps **maintaining physics performance**
- CMS target: **time stamps with 30-50ps resolution for every track**
- HL-LHC to start in 2029 ➞ 7 years from now!



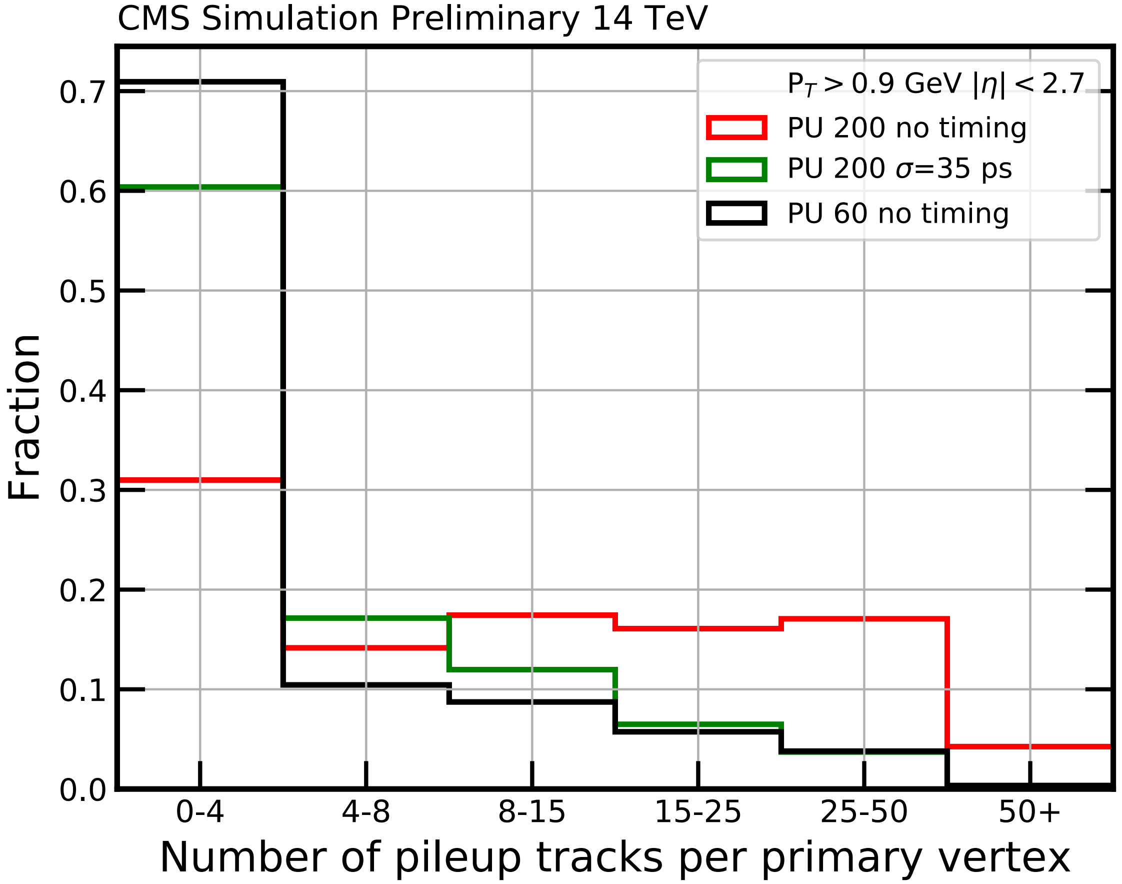
Tracks and vertices at the HL-LHC, the (probably) most shared illustration about high pileup

Timing allows to distinguish vertices at same x, y, z. Not attempting to improve spatial resolution!

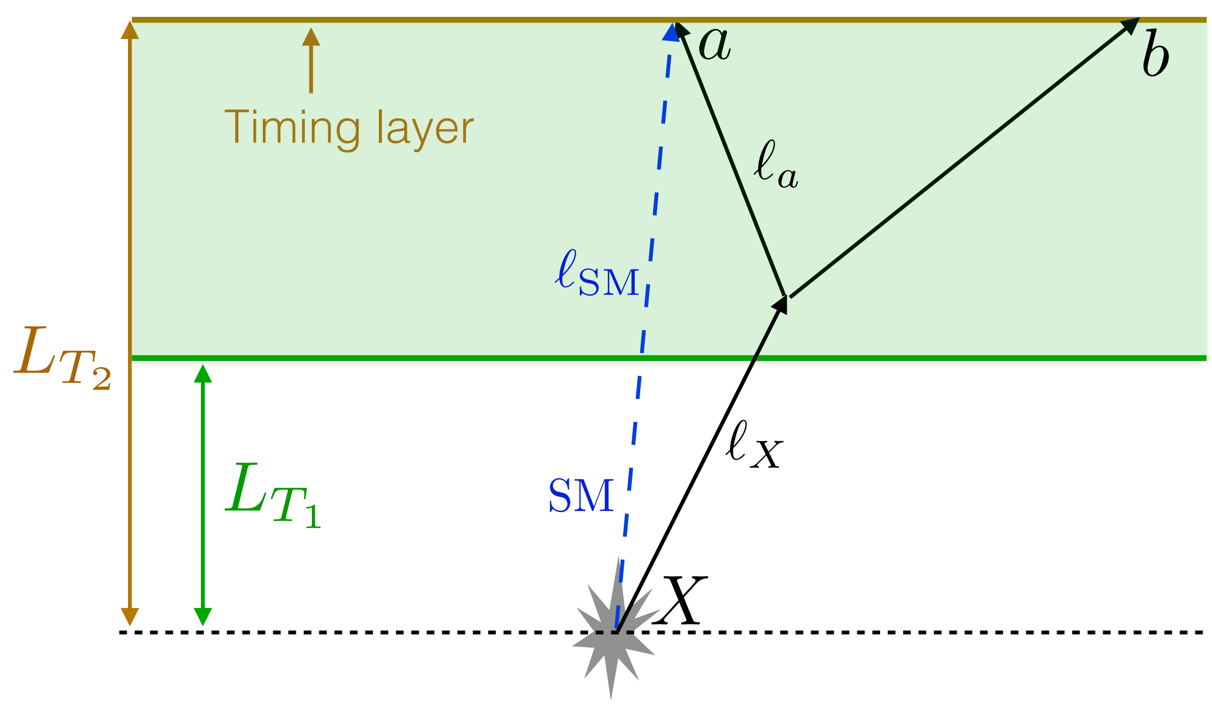


Physics impact

- Target: Detector with 50ps single hit resolution → **~35ps average time resolution** with **two hits per track** (two layer design)
- Two physics benefits:
  - **Pileup mitigation** → increase of effective integrated luminosity
  - 4D tracks over large η range → **new handles e.g. on long lived particles**



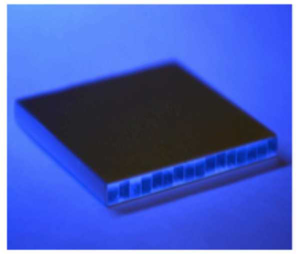
PRL 122.131801



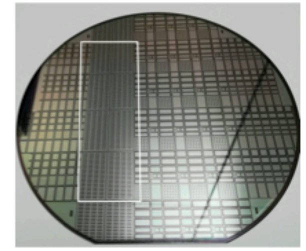
$$\Delta t^i_{\mathrm{delay}} = \frac{\ell_X}{\beta_X} + \frac{\ell_i}{\beta_i} - \frac{\ell_{\mathrm{SM}}}{\beta_{\mathrm{SM}}}$$

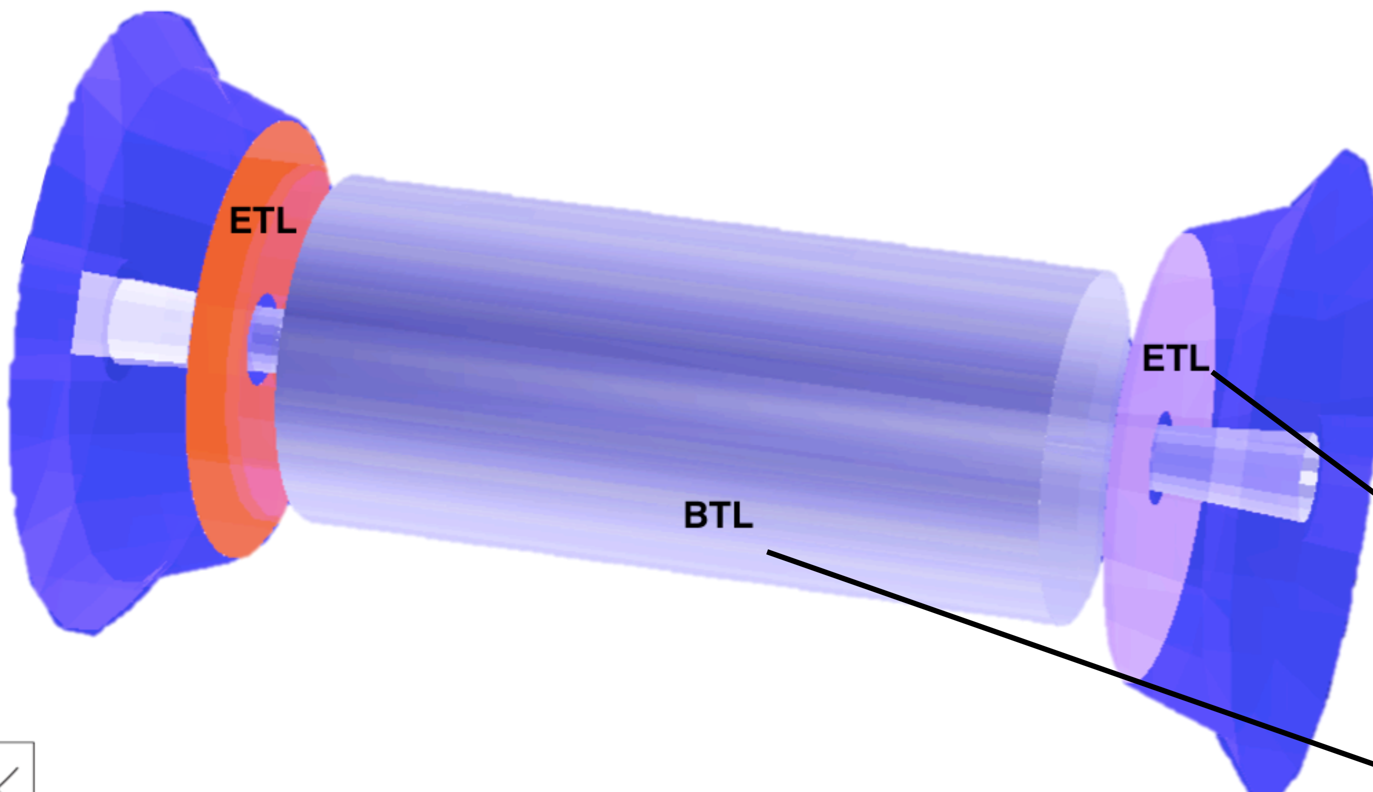
Get yourself oriented

BTL: LYSO bars + SiPM readout:
- TK / ECAL interface: $|\eta| < 1.45$
- Inner radius: 1148 mm (40 mm thick)
- Length: ±2.6 m along z
- Surface ~38 m^2; 332k channels
- Fluence at 4 ab^{-1}: 2×10^{14} n_{eq}/cm^2

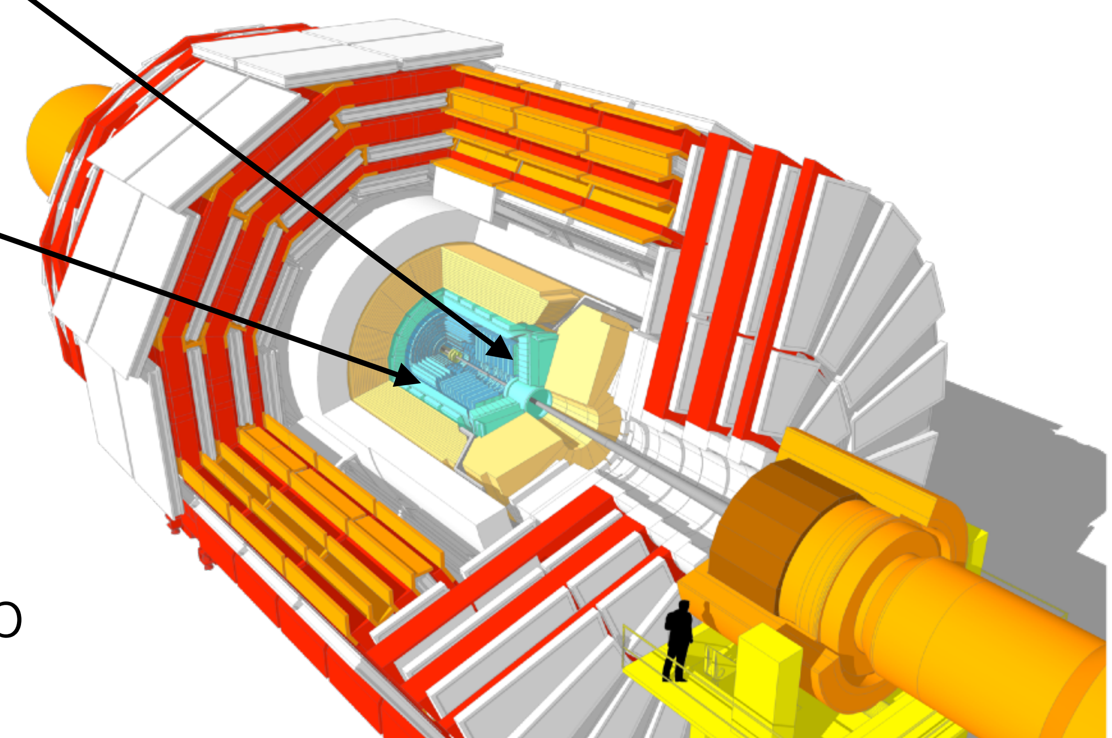


ETL: Si with internal gain (LGAD):
- On the CE nose: $1.6 < |\eta| < 3.0$
- Radius: $315 < R < 1200$ mm
- Position in z: ±3.0 m (45 mm thick)
- Surface ~14 m^2; ~8.5M channels
- Fluence at 4 ab^{-1}: up to 2×10^{15} n_{eq}/cm^2





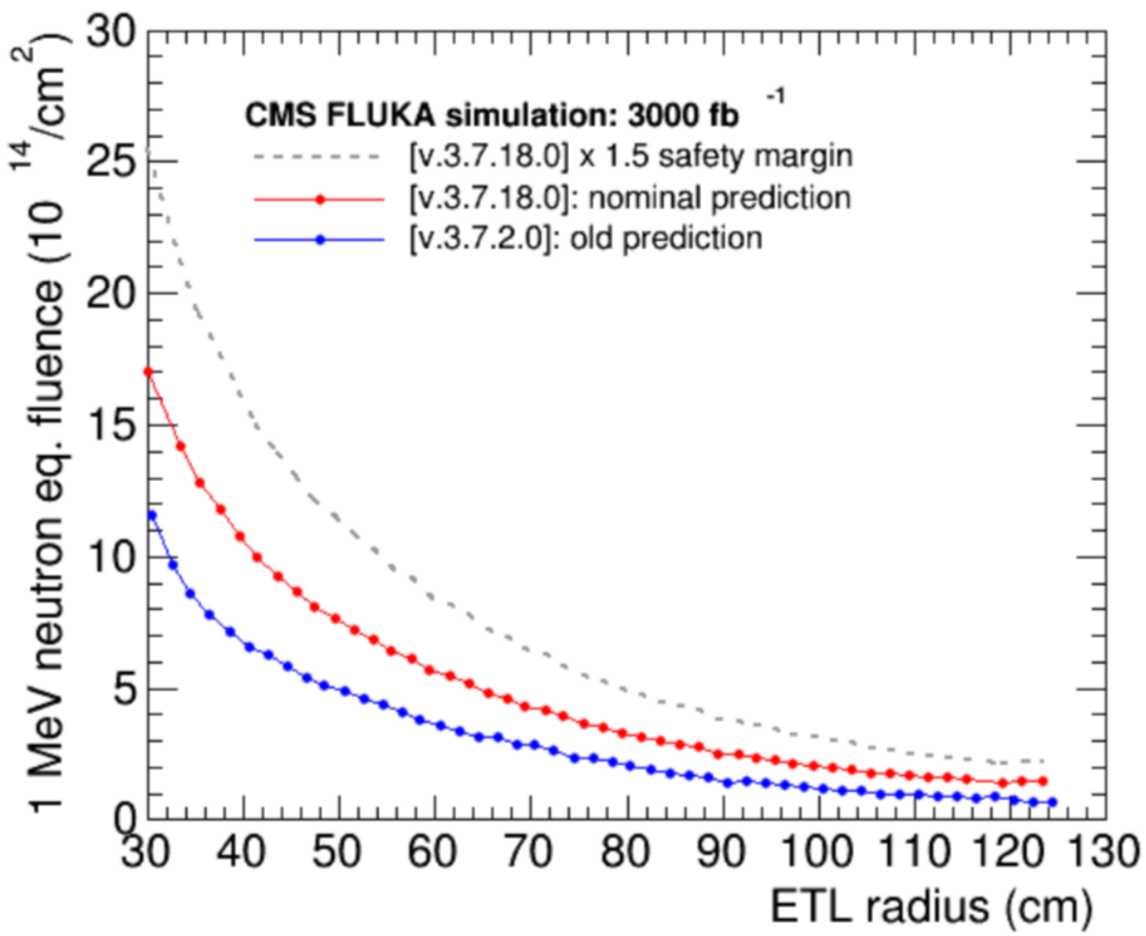
(Almost) hermetic coverage up to $|\eta|<3.0$



Two different detector technologies for barrel and endcap:
- LYSO crystals with SiPM in barrel: Barrel Timing Layer (BTL)
- Ultrafast silicon detectors in endcap: Endcap Timing Layer (ETL)

Challenges in the CMS Endcap

- **Occupancy and radiation** in the forward parts of CMS ➞ silicon detector
    - Expected dose in forward region almost 30x higher than in barrel
- Up to 1.6×10^{15} n_{eq}/cm^2 after 3000/fb at highest η (lowest r) of ETL
- **Very limited space available** on the CE nose, coverage $1.6 < |\eta| < 3.0$
    - Allowed z-space (without services) ~45mm

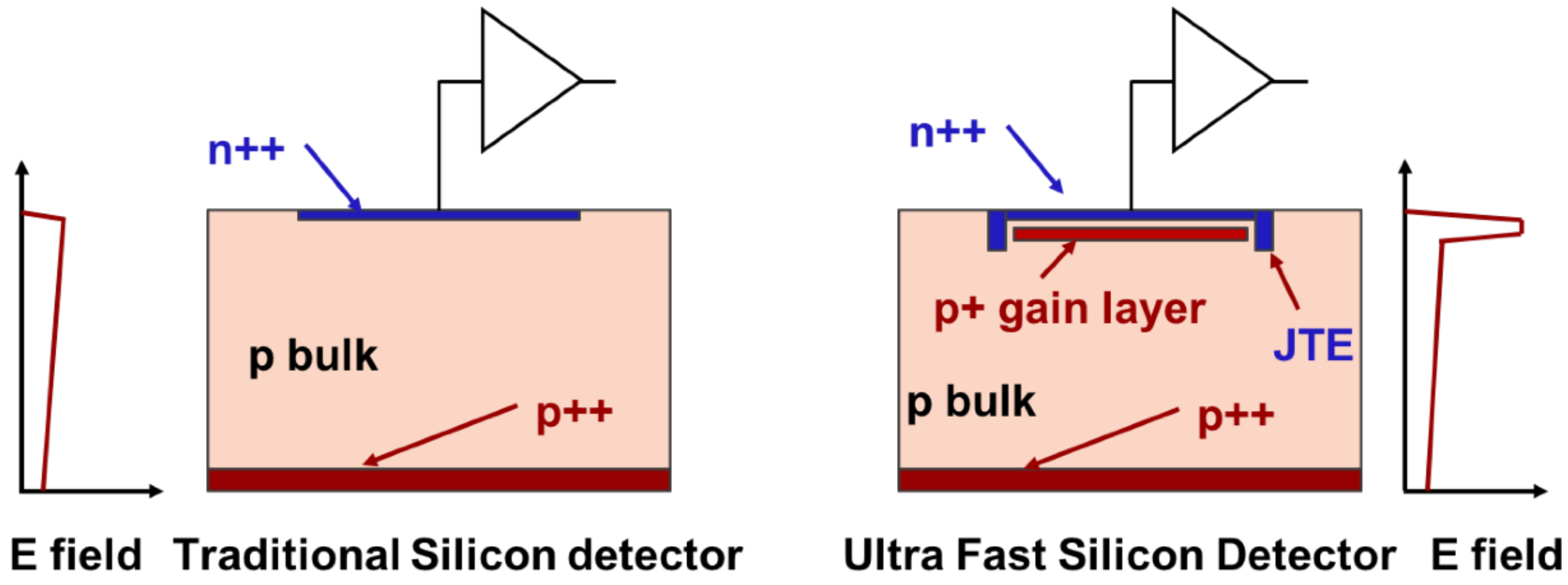


Radiation dose and fluences for barrel and endcap timing layers

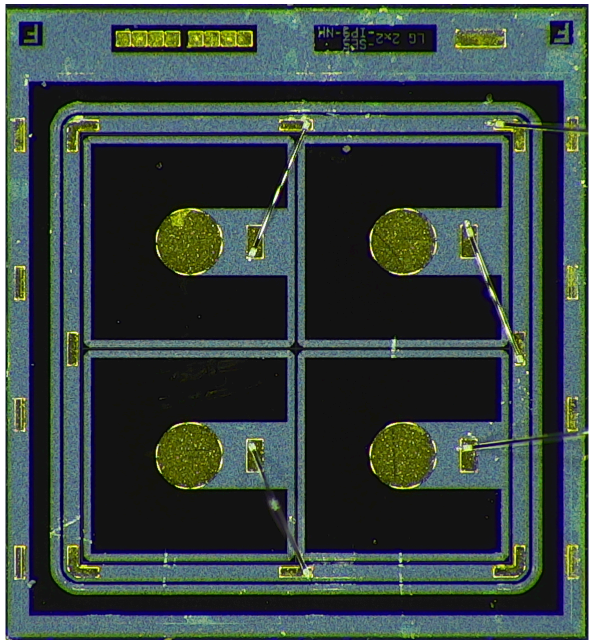
Region	$\|\eta\|$	r (cm)	z (cm)	3000 fb^{-1} n_{eq}/cm^2	3000 fb^{-1} Dose (kGy)	1.5×3000 fb^{-1} n_{eq}/cm^2	1.5×3000 fb^{-1} Dose (kGy)
Barrel	0.0	116	0	1.65×10^{14}	18	2.48×10^{14}	27
Barrel	1.15	116	170	1.80×10^{14}	25	2.70×10^{14}	38
Barrel	1.45	116	240	1.90×10^{14}	32	2.85×10^{14}	48
Endcap	1.6	127	303	1.5×10^{14}	19	2.3×10^{14}	29
Endcap	2.0	84	303	3.0×10^{14}	50	4.5×10^{14}	75
Endcap	2.5	50	303	7.5×10^{14}	170	1.1×10^{15}	255
Endcap	3.0	31.5	303	1.6×10^{15}	450	2.4×10^{15}	675

Ultrafast Sensors

- **Low Gain Avalanche Diodes** (LGAD): Additional gain layer (multiplication implant)
  - Internal gain proportional to bias voltage
  - Low / moderate gain ~10: **low noise, fast slew-rate and fast rising pulse**
  - Thin sensors: **50μm depletion region**
  - Junction Termination Extension (JTE) reduces electric field at perimeter of pads, resulting in **no-gain inter-pad gaps**. Need to be sufficiently small for large coverage.
- 1.3 x 1.3 mm^2 pixels: moderate capacitance
- Moved from 16x32 pixel sensor to 16x16 to increase production yield



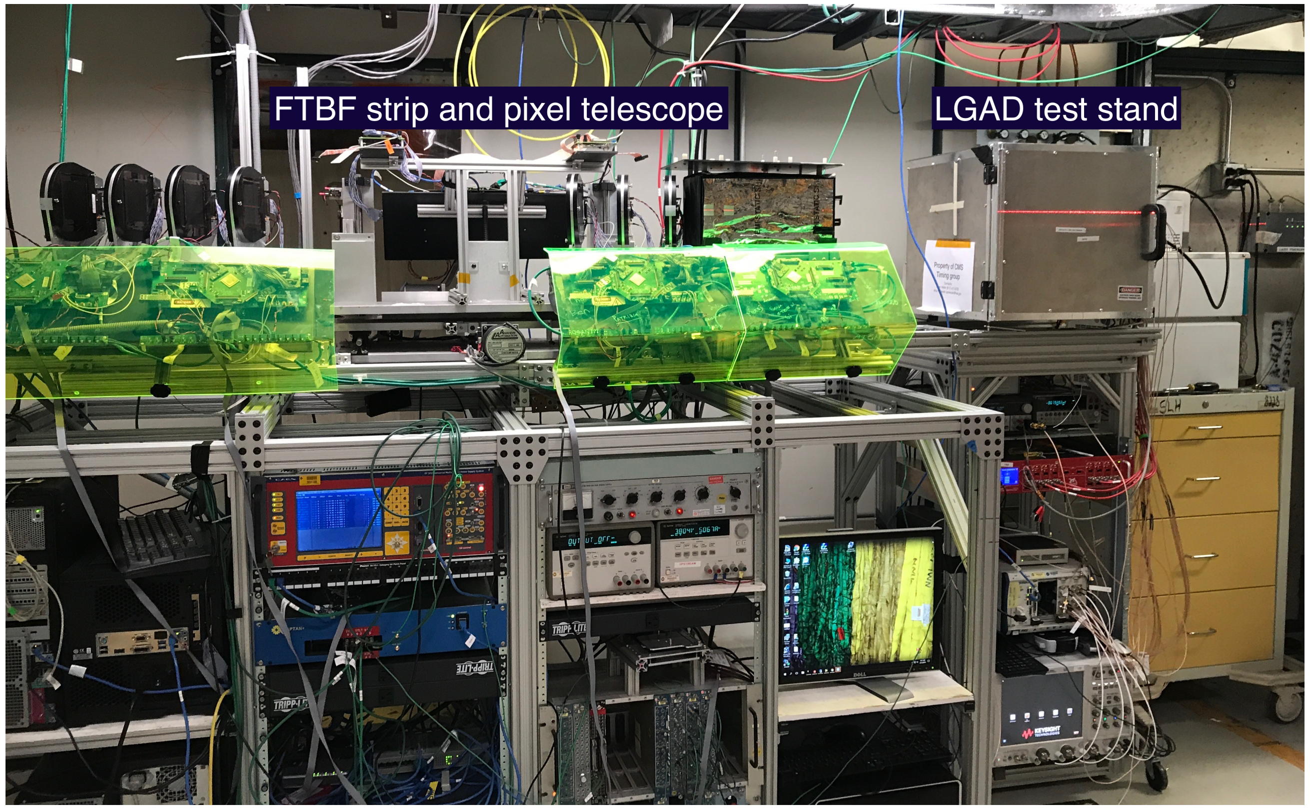
4x4 pixel prototype, Hamamatsu

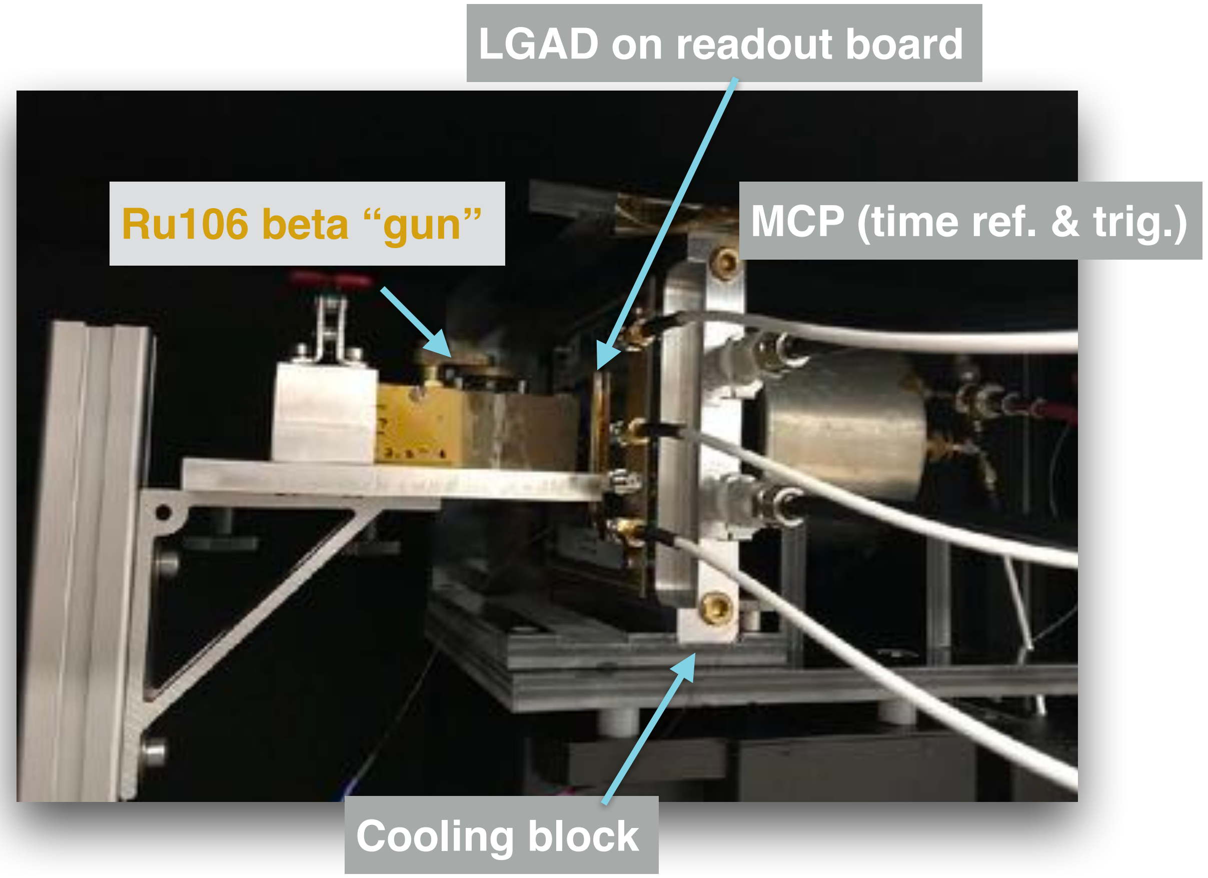


Sensor performance evaluation

- Several facilities at institutes around the world used to study performance and sensor characteristics. ETL is a global collaboration!
  - Fermilab test beam (120 GeV protons)
  - Beta source for high volume testing
  - Probe stations for waver-scale uniformity studies and larger scale, fast QC

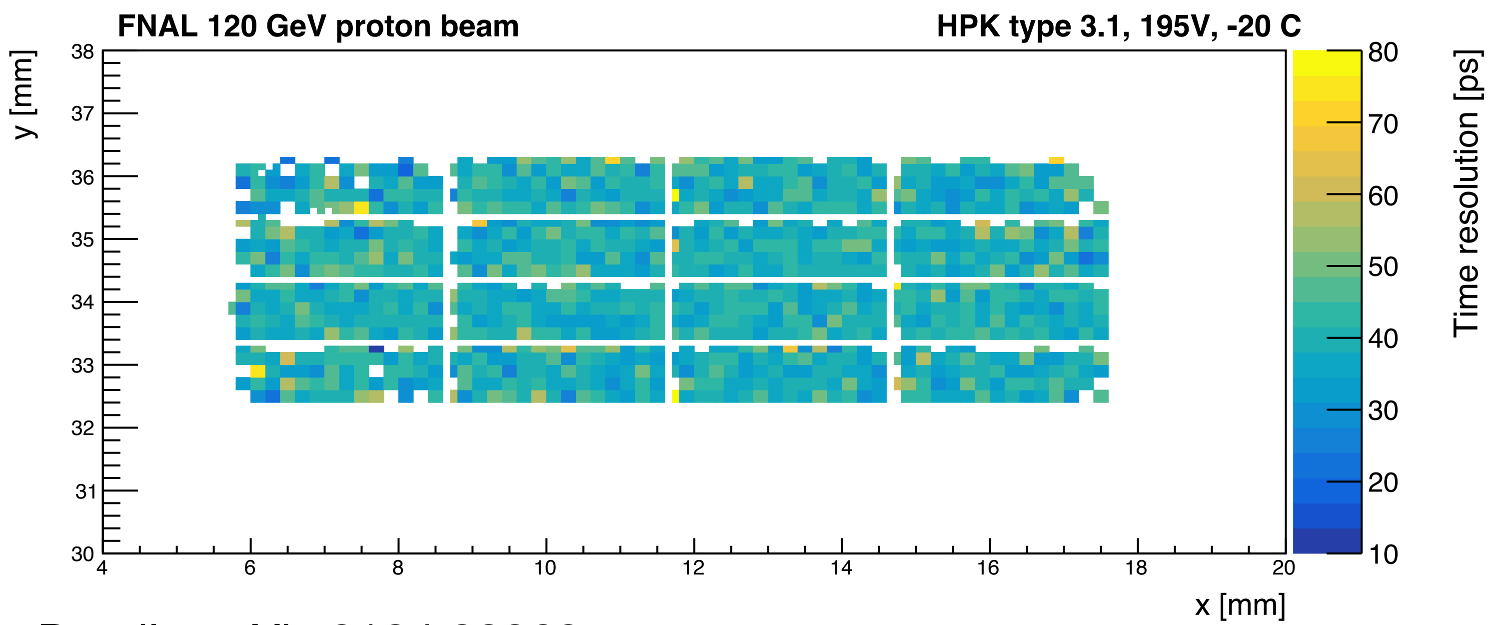
Details: arXiv:2104.08369





Sensor performance

- HBK prototypes, 4x4 pixel arrays with 1x3mm² pixel size
- **Uniform time resolution** for entire active area of pads observed in test beam
  - Intrinsic **sensor resolution 30ps**
- Remarkable good agreement of collected charge measurements in test beam and beta source
- Test beam measurements **confirm laser TCT measured size of inter-pad gap** (non-active area), gaps < 80μm specified for ETL
- Verified that **MIP response can be predicted from CV probe station measurements** → highly important for large scale production uniformity testing!



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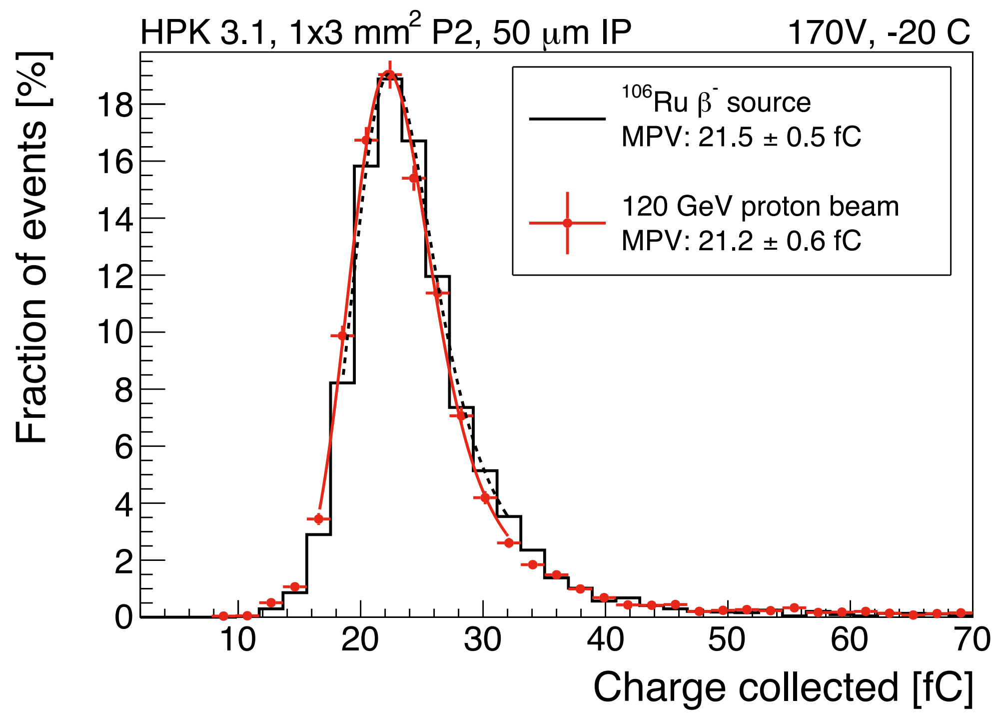
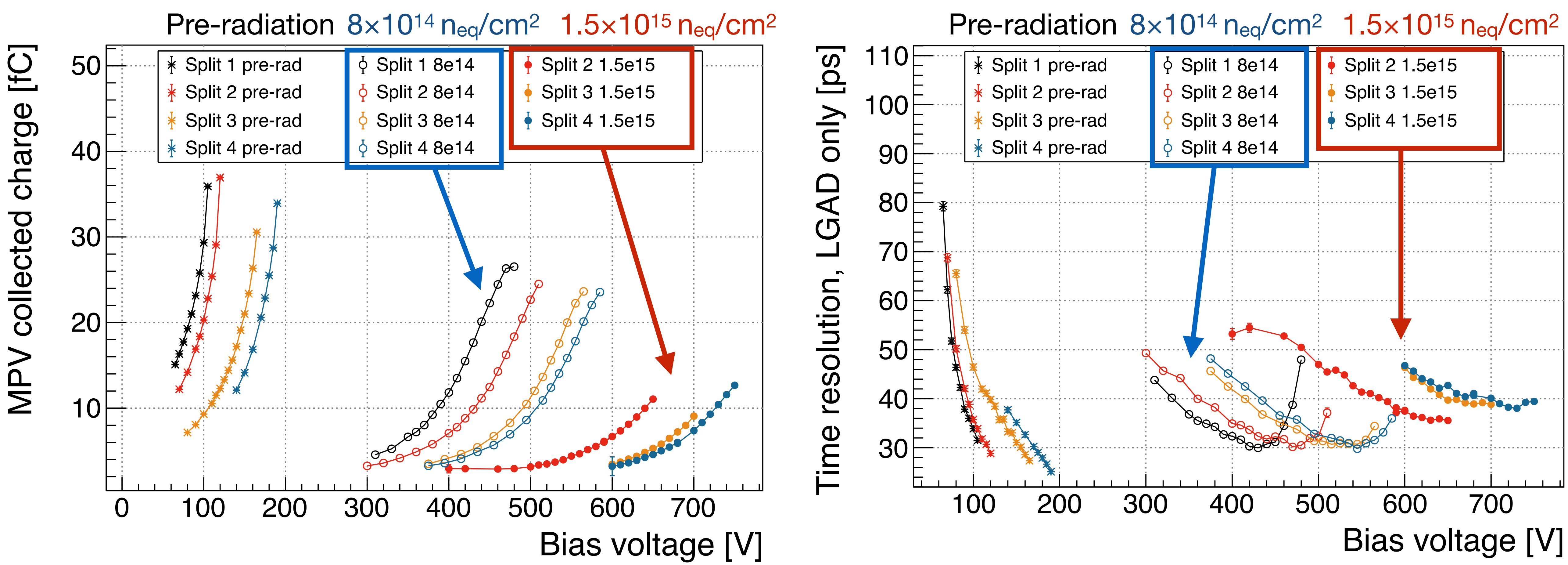


LGAD radiation tolerance

- Irradiated sensors to 8×10^{14} and 1.5×10^{15} n_{eq}/cm^2 (expected after $3000fb^{-1}$)
- Bias voltage needs to be increased to maintain gain after irradiation
- Characterization of irradiated sensors shows 40ps time resolution until expected end of life at the end of HL-LHC
- Safe operations according to specs possible with bias <12V/µm, verified in test beam



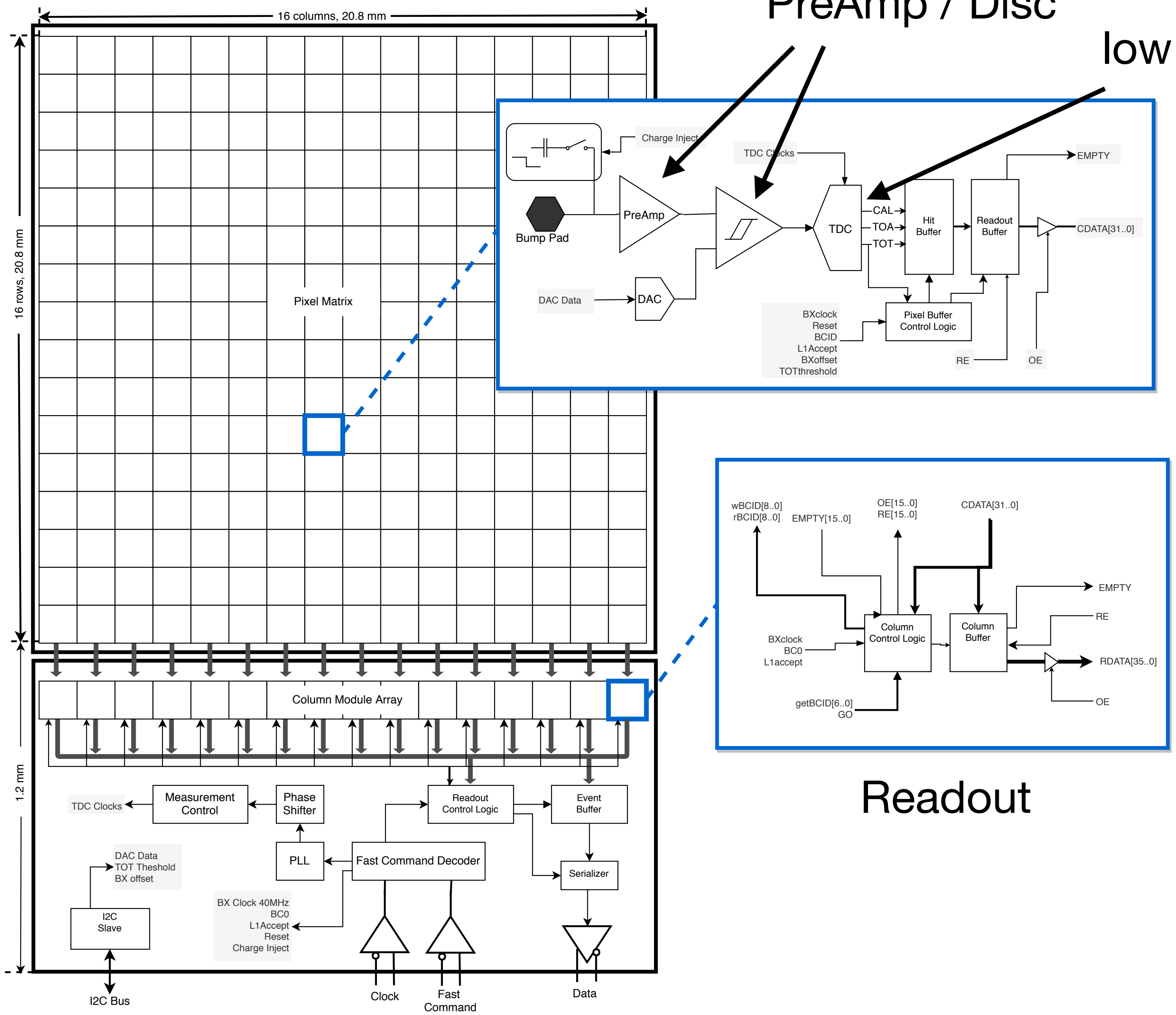
Endcap Timing ReadOut Chip (ETROC)

- Extract precision timing from small LGAD signal (~5fC at end of life)
- Low power budget of 1W/chip, ~3 mW/channel → low power TDC
- ASIC contribution to time resolution < 40ps

16x16 pixel array

PreAmp / Disc

low power TDC

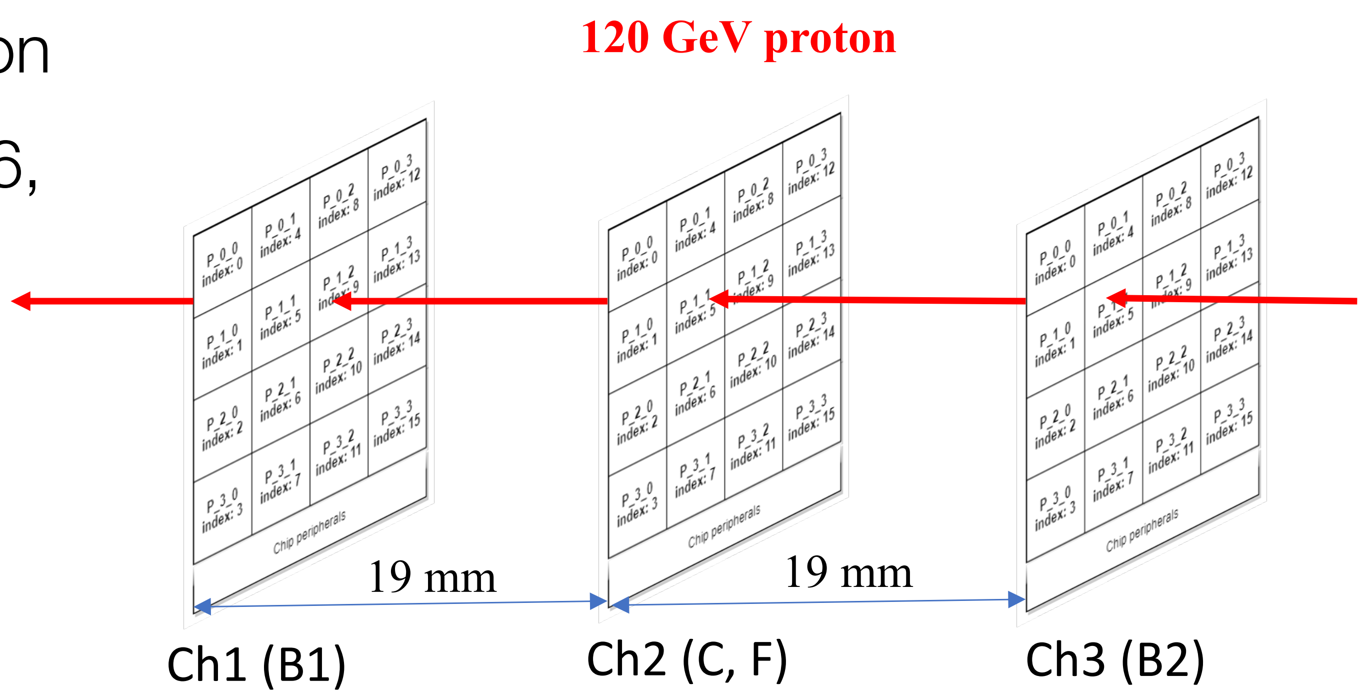


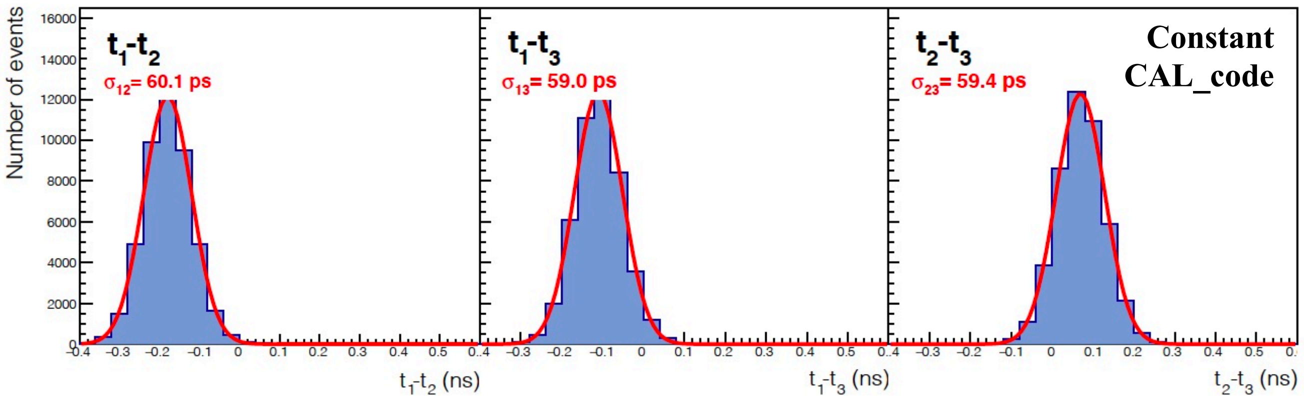
Readout

Details: arXiv:2011.01222

ETROC prototypes

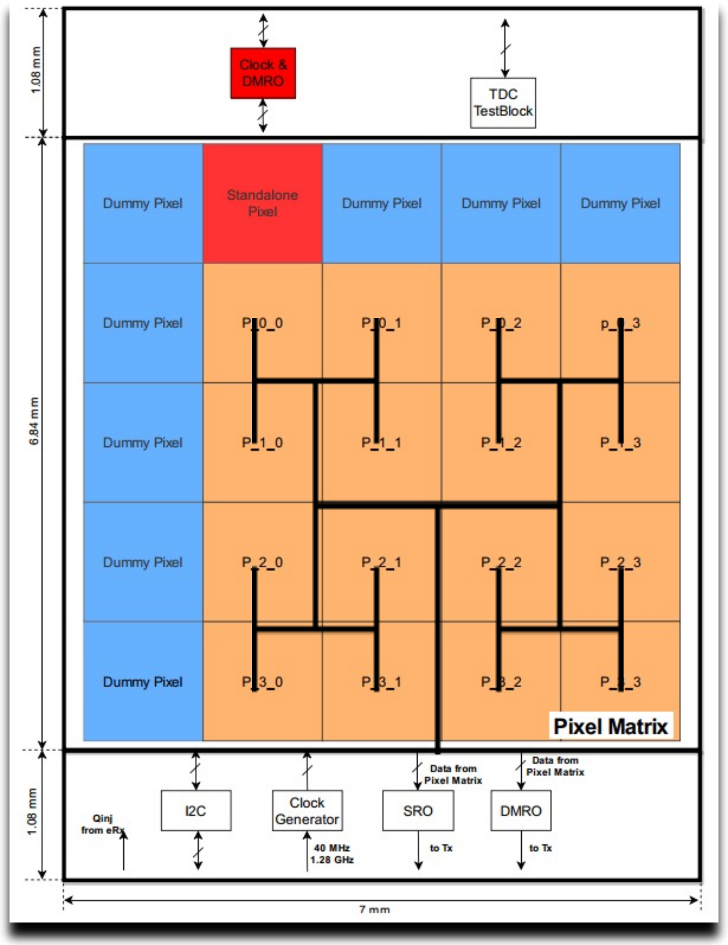
- ETROC0: single analog channel to test core front-end analog performance
- ETROC1 (4x4 pixels, ETROC0 + TDC) + LGAD sensor tests in test beam during first half of 2021
  - 70M triggered events
  - ~42ps single-hit timing resolution
- Upcoming ETROC2: full size 16x16, full functionality





ETROC1 test beam

ETROC1 4x4 H-tree
clock distribution within chip



ETL Time resolution (unit: ps)

	ETROC1 simulation	TDR specification
LGAD+ preamp/discriminator + TDC bin	35	
Time-walk correction residual	< 10	
Internal clock distribution	< 10	
System clock distribution	< 15	
Per hit total time resolution	41	50 ps
Per track (2 hits) total time resolution	29	35 ps

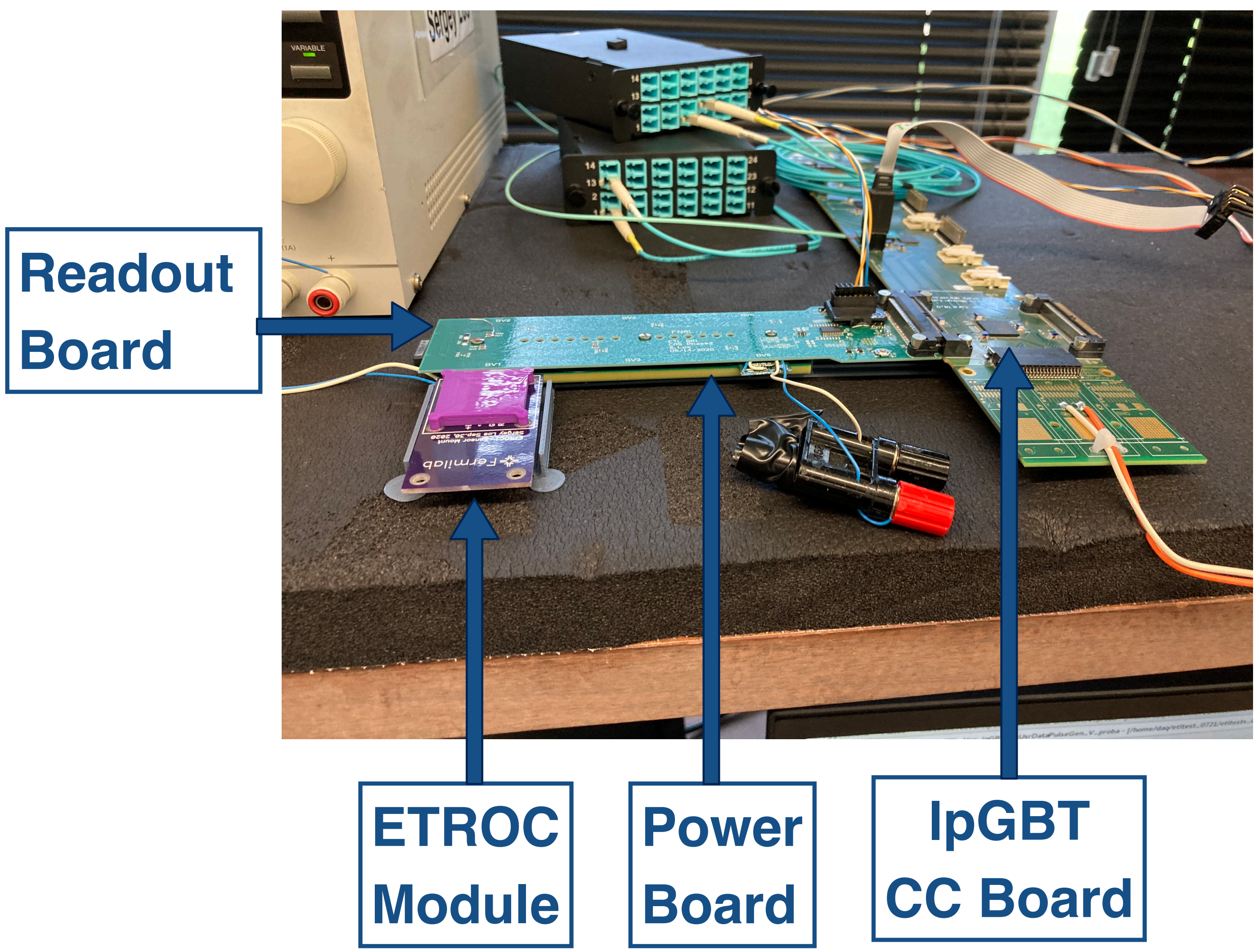
$$\sigma_i = \sqrt{0.5 \cdot (\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2)}$$ ~ 42 – 46 ps

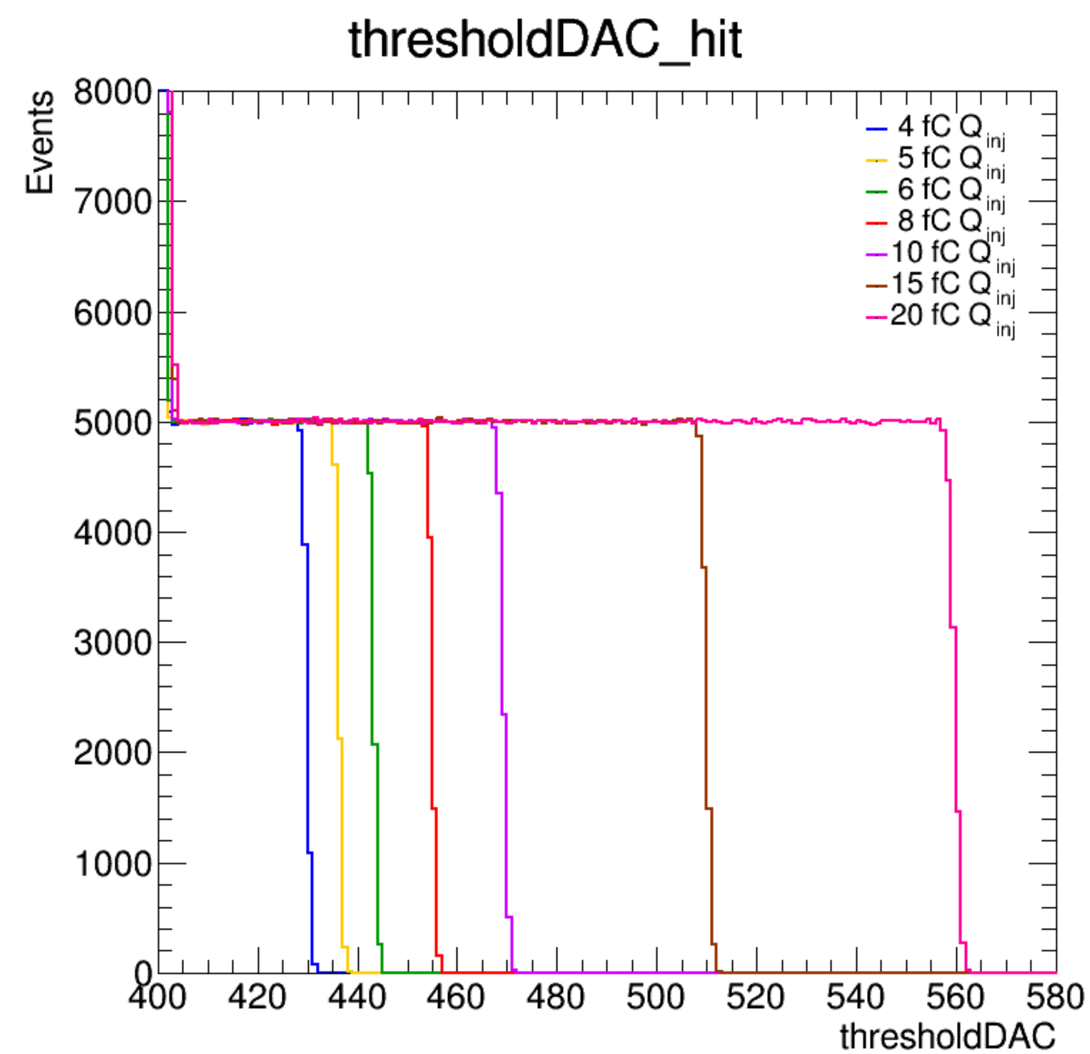
(with LGAD HV=230V for all three channels)

includes all 4 contributions from the table → in good agreement with simulation and specs!

ETROC1 readout tests

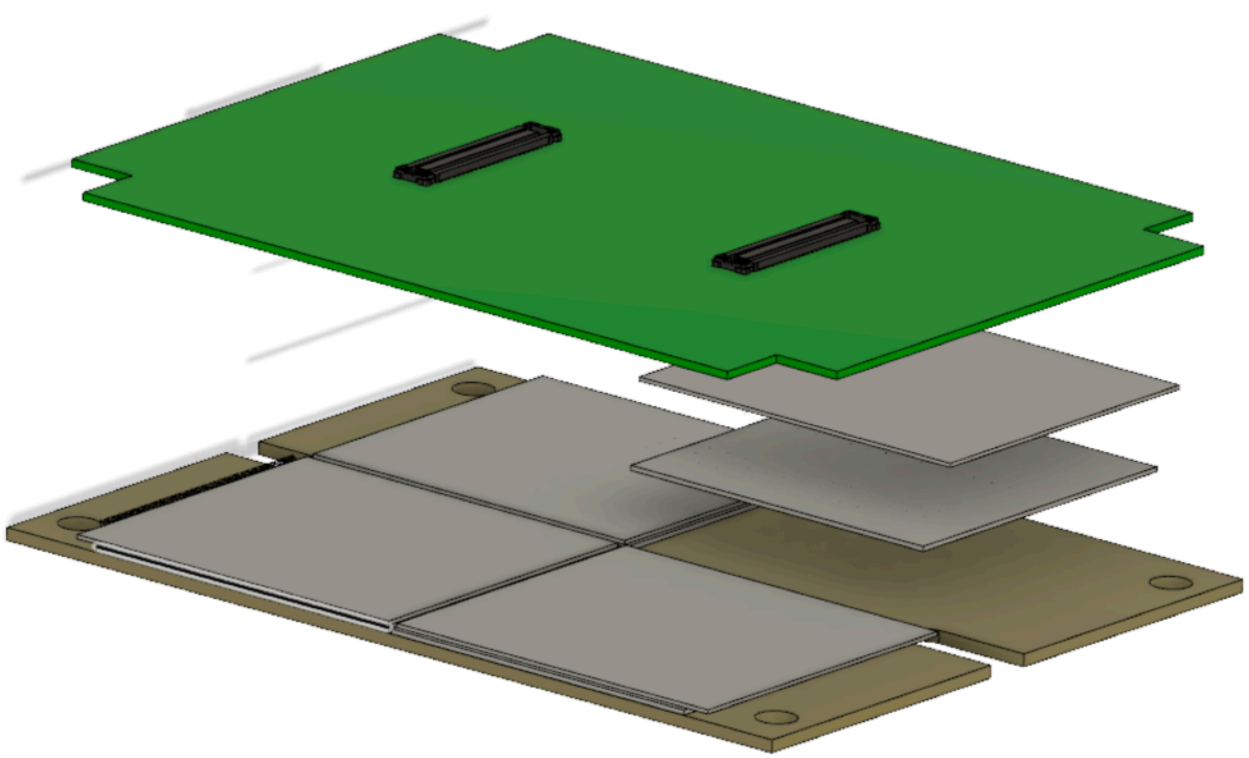
- ETROC1 module used with realistic readout chain through BTL based board
- Use charge injection to produce S-curves, see similar behavior to initial ETROC1 tests
- TOA jitter introduced by power board prototype under control with proper filters





Modules

- Modules are based on 4 16x16 pixel LGAD sensors, bump bonded to one ETROC each
- Sensors are glued on AlN baseplate and in thermal contact with the cooling disk at -20°C
- Studying a “flipped” design of sensor and ETRC wrt initial proposal, wire bonds to PCB
- Modules are directly connected to multi-module readout board that sits on top



PCB with connectors to ETL readout board

ETROC, bump bonded to sensor

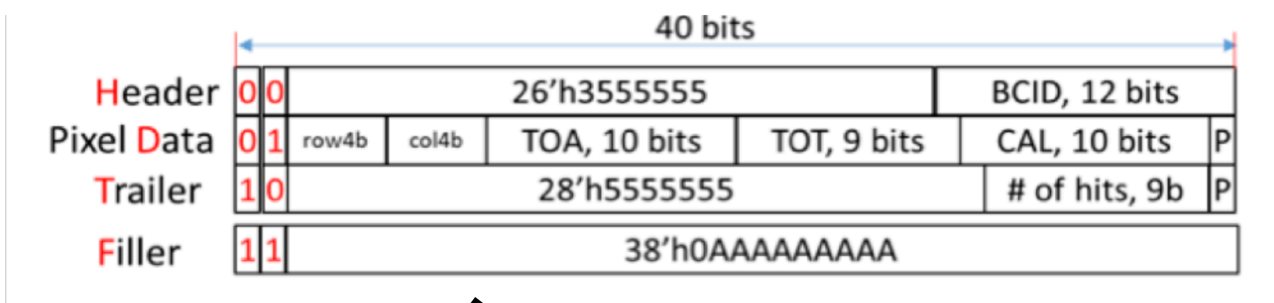
16x16 pixel LGAD sensor

AlN baseplate

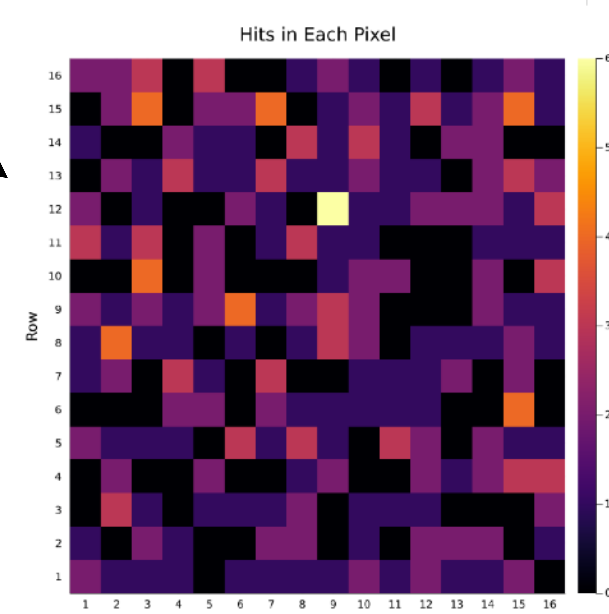
Services

- Readout board based on CERNs rad-hard Low Power Gigabit Transceiver (lpGBT) and Optical Link Module (VTRx+)
- Prototype v1 (first in realistic form factor) works with ETROC2 emulator, can test full readout chain

Preliminary data format

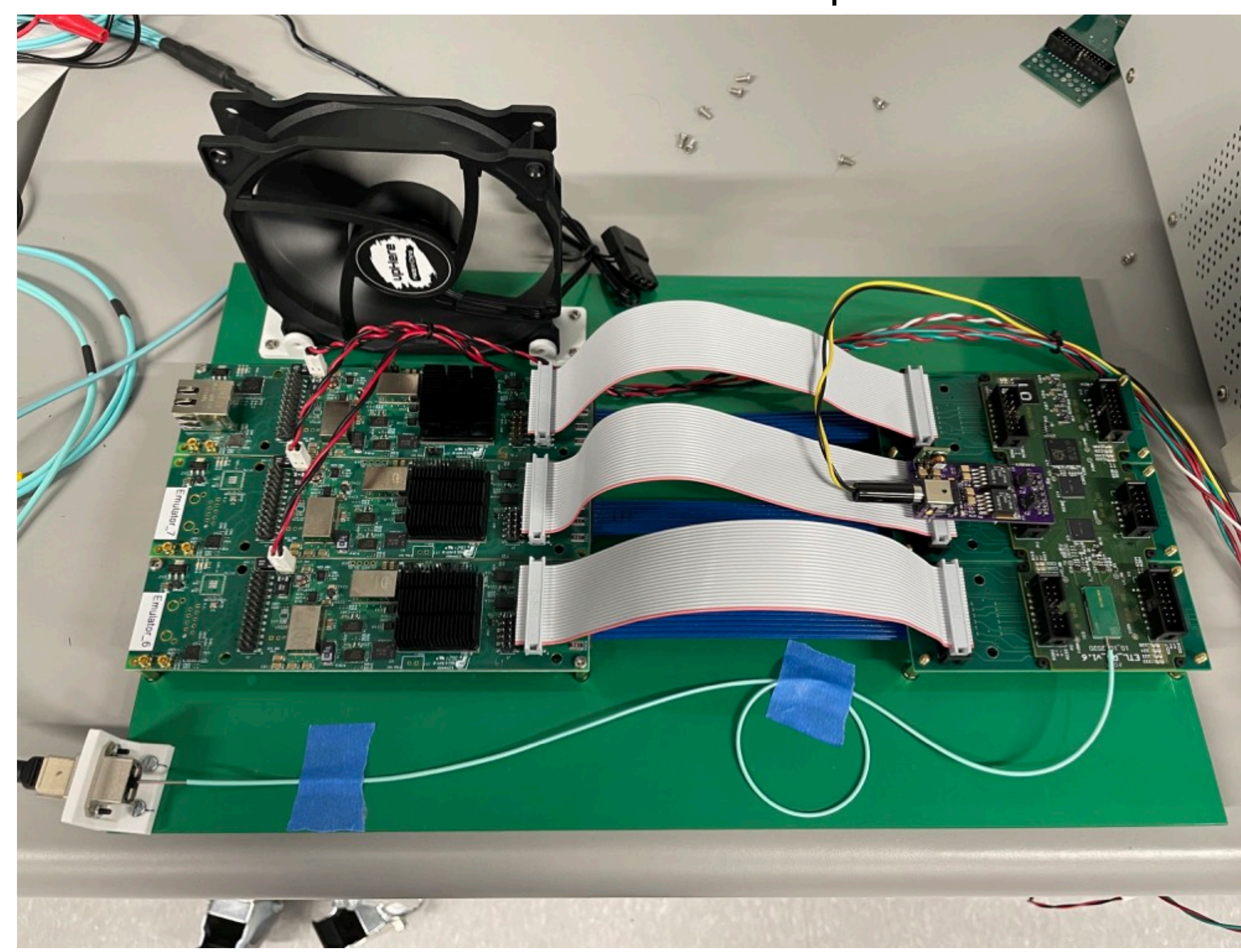


Random hit pattern generated in ETROC2 emulator, read out through readout board, software based data unpacker



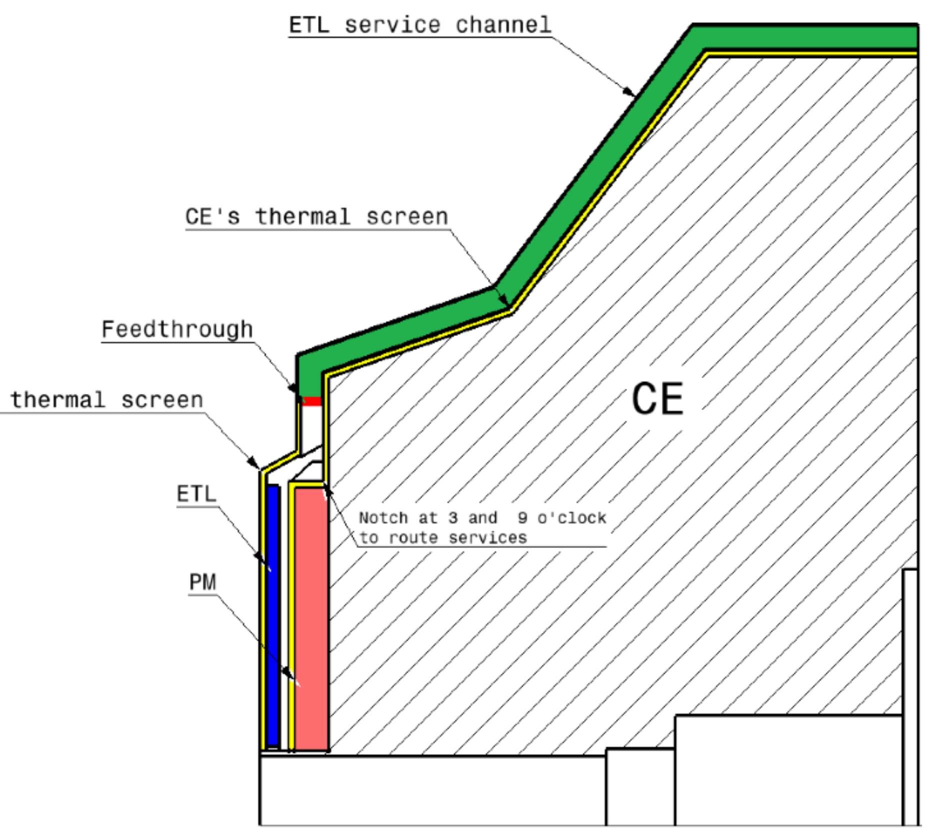
ETROC2 emulators: "modules"

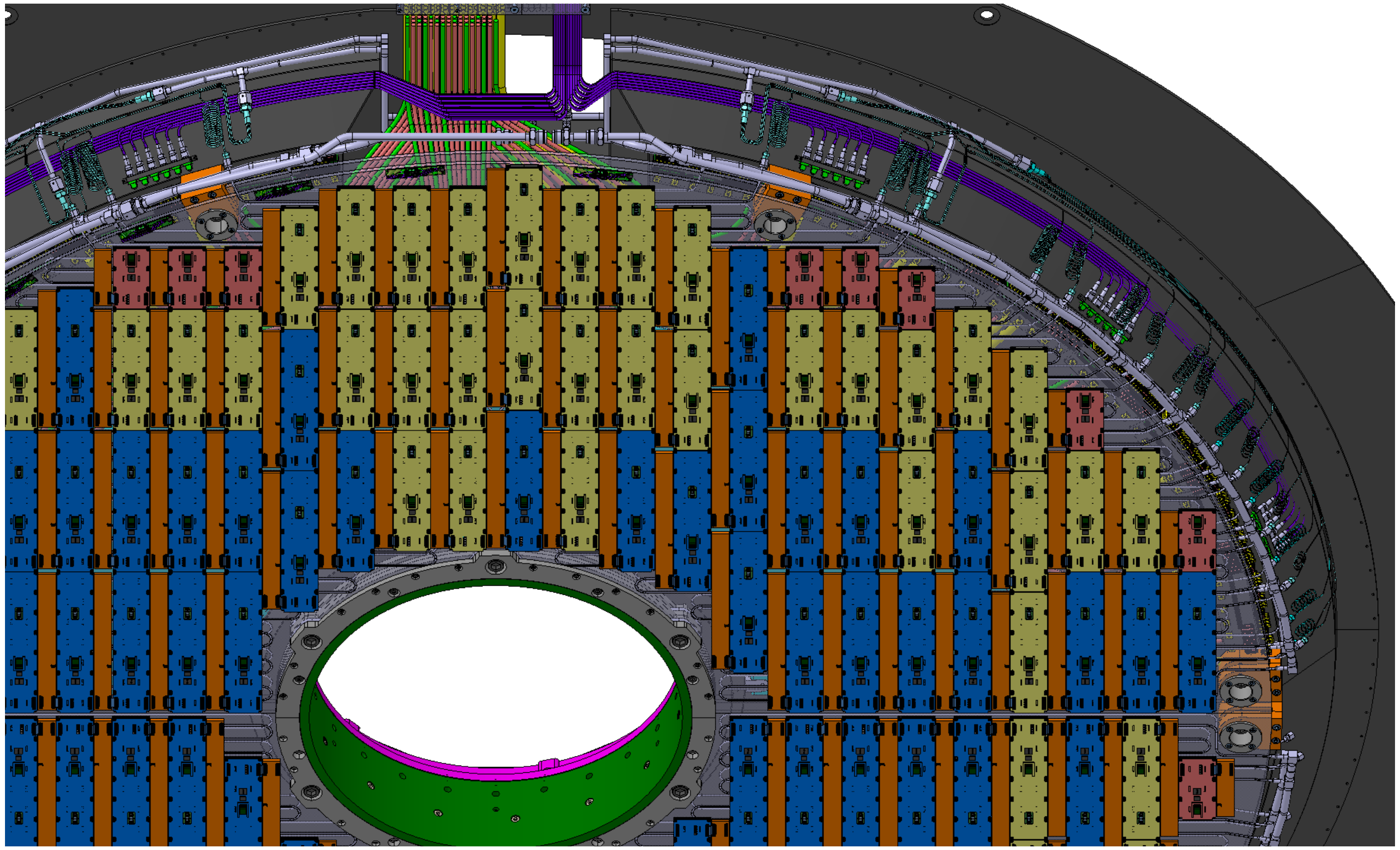
Readout board prototype on interposer boards



The ETL detector

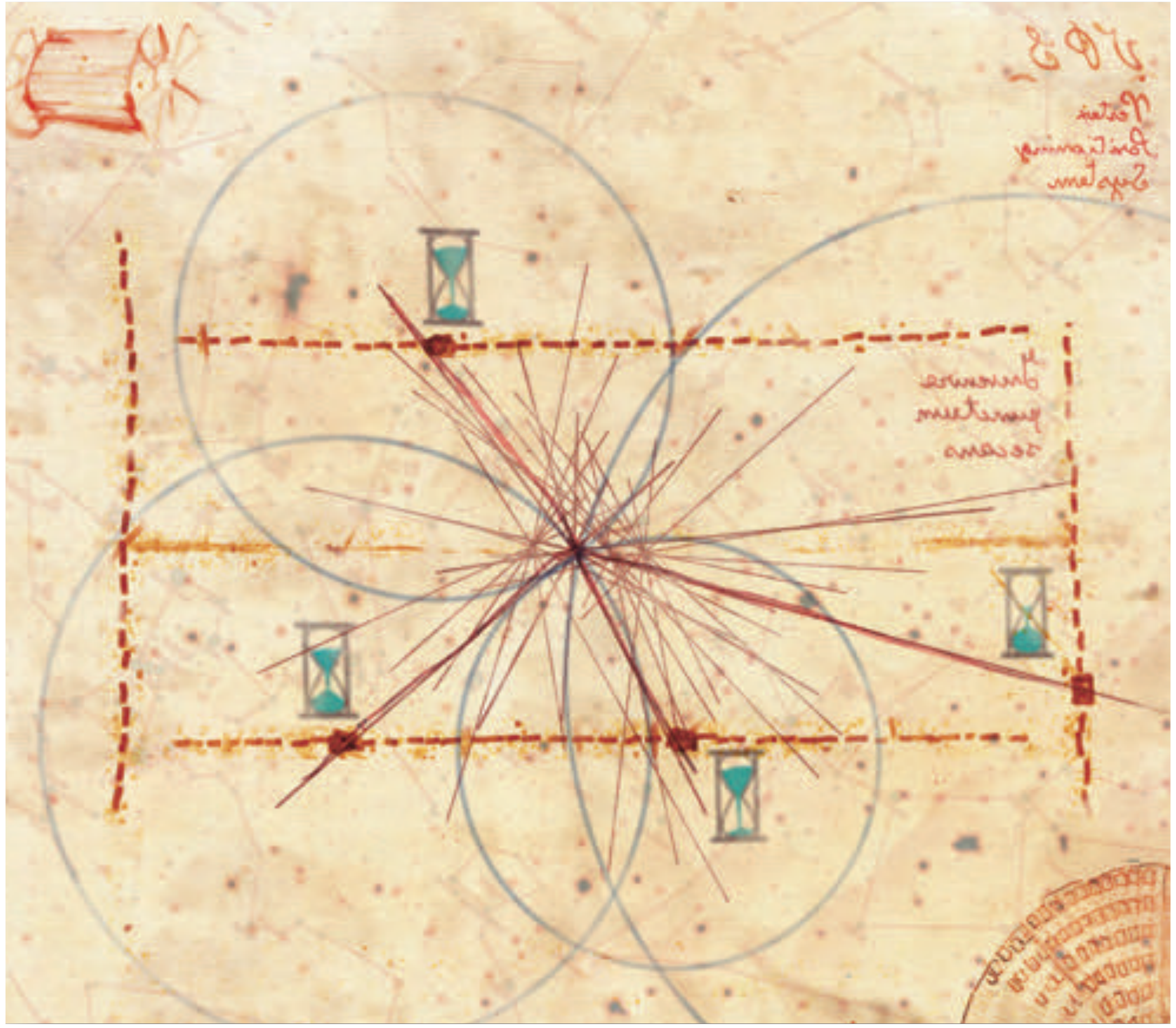
- Strong effort to combine inputs from studies into a complete detector design and layout: ~8000 modules (4 sensors each) on 2 endcaps. ~8M channels in total
  - Each detector consists of 2 disks with front and back face instrumented
  - Modules + front end electronics and services need to fit in very tight mechanical envelope!





Summary and Outlook

- LGAD sensors well suitable for CMS timing in the endcap layer
  - Intrinsic LGAD time resolution of 30ps
  - Time resolution according to specs until end of life
- ETROC prototypes and emulators have been extensively tested, development of fully functional ETROC2 currently being finalized
- Front end electronics based on radiation hard CERN components well advanced
- Challenging mechanical engineering of the full detector system is progressing well
- Common MTD DAQ system is being developed together with barrel detector



BACKUP