

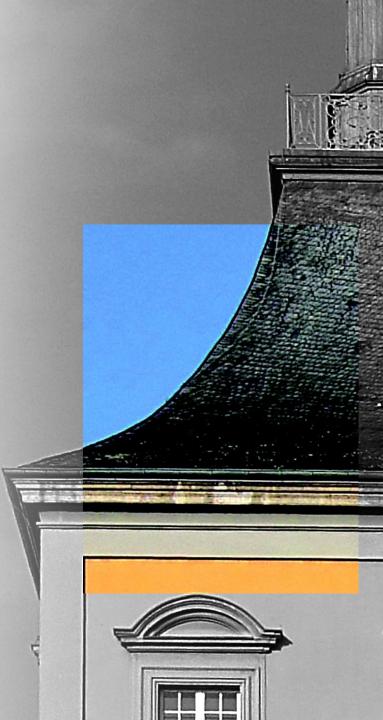
Development and testing of a radiation-hard large electrode DMAPS design in a 150 nm CMOS process.

Ivan Caicedo*, C. Bespin, J. Dingfelder, T. Hemperek, T. Hirono, F. Huegging, H. Krueger, P. Rymaszewski, L. Schall, T. Wang, N. Wermes (University of Bonn)

M. Barbero, P. Barrillon, P. Breugnon, P Chabrillat, N. Destaing, A. Habib, P. Pangaud, A. Rozanov (Aix Marseille University, CNRS/IN2P3, CPPM)

Y. Degerli, F. Guilloux, P. Schwemling (IRFU CEA-Saclay)

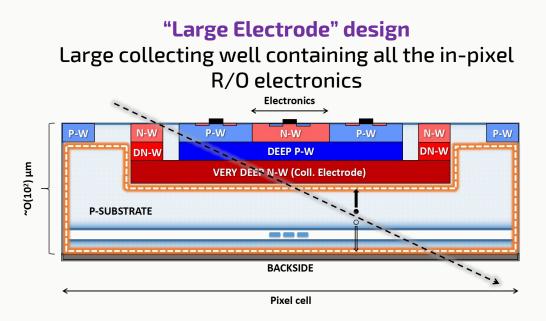
*caicedo@physik.uni-bonn.de





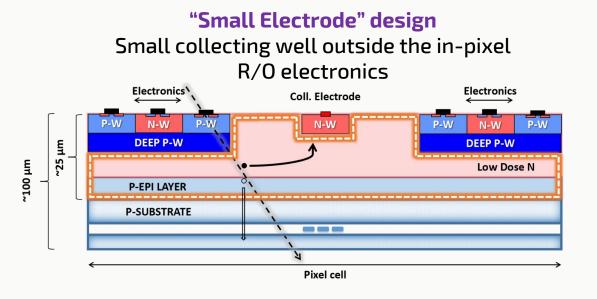
DEPLETED MONOLITHIC ACTIVE PIXEL SENSORS (DMAPS)

- Developed in commercial CMOS processes: Multiple wells to shield electronics and avoid hybridization.
 - Considerable depleted regions in highly resistive substrates: Fast charge collection by drift.



PROS: Short drift distances, strong E-field (Rad-hard). **CONS:** Large sensor capacitance, high analog power.

---> Requires design efforts to optimize timing and minimize cross-coupling into the collection node.



PROS: Small sensor capacitance, low power and noise. **CONS:** Weak electrical field compromises rad-hardness.

---> Requires process modifications and small pixel pitch to optimize charge collection.





DMAPS FOR HIGH ENERGY COLLIDER EXPERIMENTS

Taking the ATLAS iTK upgrade

requirements as benchmark:

	ITk Outer Layer
Occupancy	1 MHz/mm ²
Time Res.	25 ns
NIEL	10 ¹⁵ n _{eq} /cm ²
TID	80 Mrad
Area	O(10m²)

DMAPS would offer:

- Reduced material budget compared to hybrids.
- Cheaper and less complex module production.

The Monopix DMAPS developments

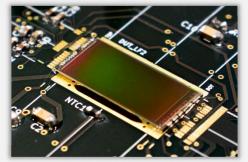
Column-Drain ("FE-I3 like") synchronous R/O architecture and fast front-end implementations

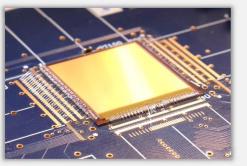
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Design optimization to preserve charge collection after irradiation

LF-Monopix: Large electrode DMAPS in LFoundry 150 nm CMOS

TJ-Monopix: Small electrode DMAPS in Tower 180 nm CMOS





(Talk by C. Bespin)





caicedo@physik.uni-bonn.de



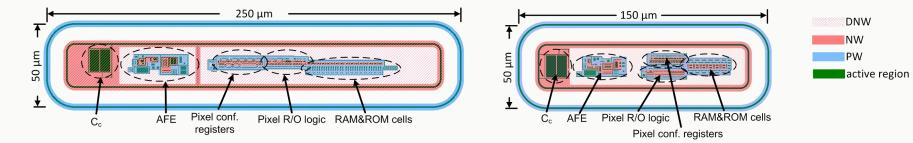
THE LF-MONOPIX PROTOTYPES

LF-Monopix1

- Full-size (~cm²) large electrode DMAPS.
- Functional columndrain R/O architecture.
- In-pixel electronics in >2 kOhm-cm resistive substrates.



Pixel layouts (Top view):



DAQ system: Bonn's Multi-I/O 3 ("MIO3") and General Purpose Analog Card ("GPAC")



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LF-Monopix2



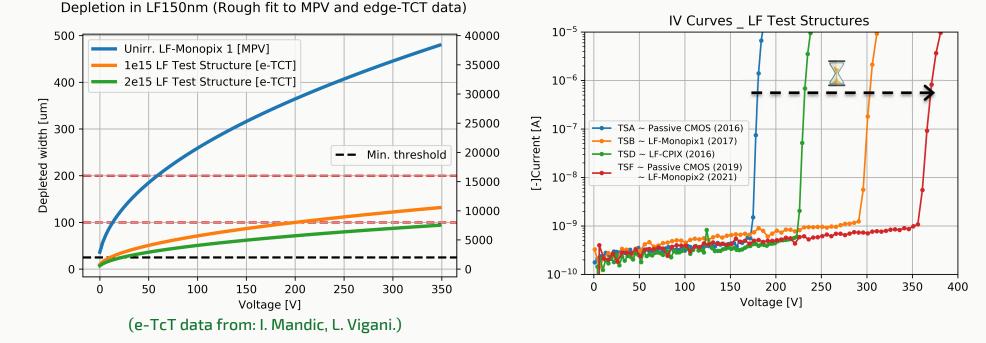
DEPLETION IN LFOUNDRY HR-SUBSTRATES

CMOS DMAPS aim to deplete the silicon bulk and collect charge mainly by drift

In order to do so, the **LF-Monopix** chips use:

- A highly resistive substrate:
- ~7 kOhm-cm, Czochralski processed

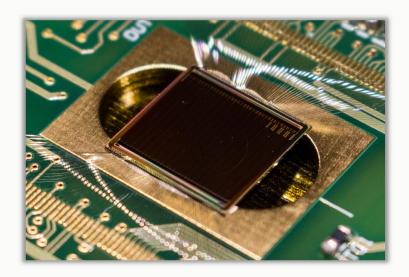
• Large reverse bias voltages: Improved across LF150 prototypes







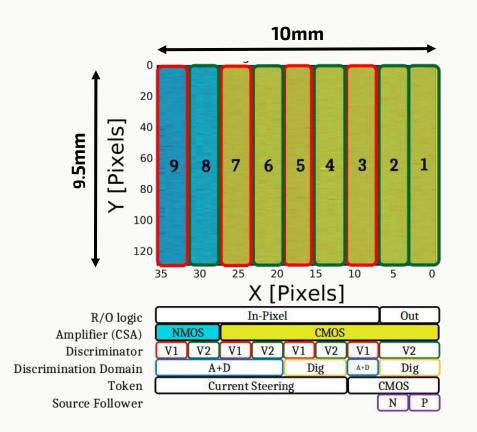
LF-MONOPIX1



- Functional in-pixel R/O logic.
- Large 50 x 250 μm² pixel array (129 rows x 36 cols)
- Bunch-crossing clock frequency (40MHz clock)
- 40 MHz/160MHz CMOS or LVDS serial output.
- Timestamping: 8-bit LE/TE (ToT) @ 25 ns.
- Power: 55 µW/pixel (~1.7W/cm²)

Noise: ~150-200e-

Tuned Thr: ~1600 ± 100e-



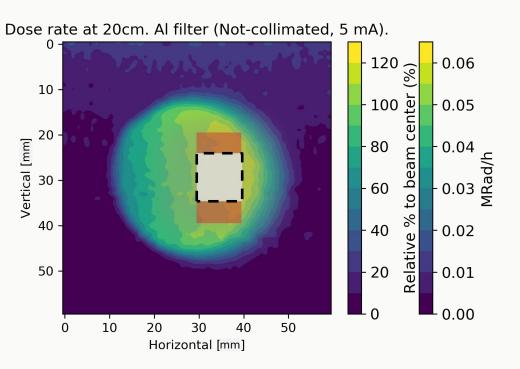




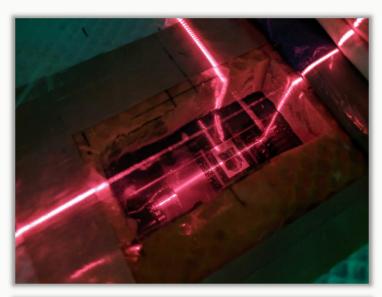


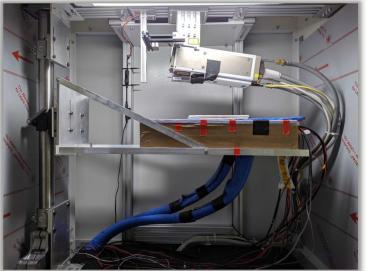
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TID IRRADIATION @ SILAB BONN



- **Sample:** 100 µm thick LF-Monopix1 (Powered on)
- X-ray tube settings: 40 kV, 50 mA ---> 0.6 MRad/h
- **Temperature:** Cooled down with chiller through plate. **0**±**2 C** in **NTC**
- 15 steps up to 100 MRad

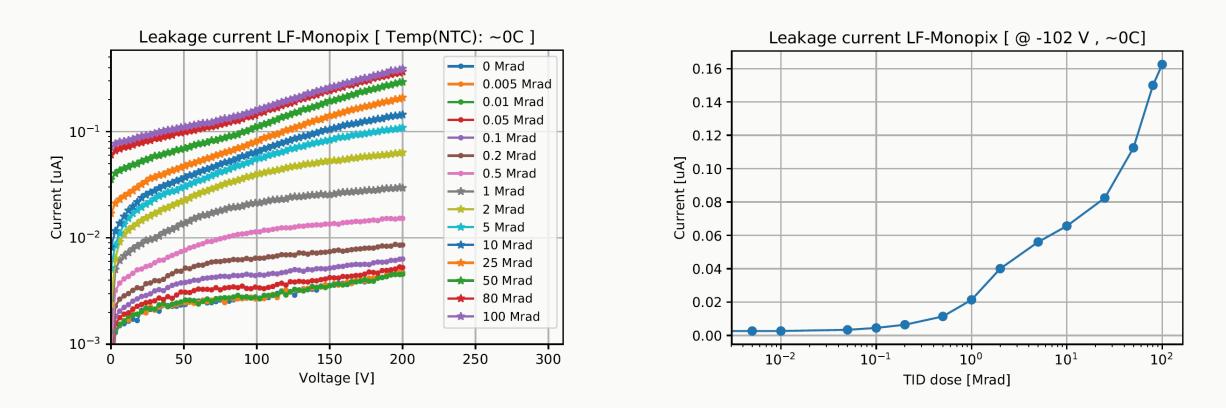








TID IRRADIATION: LEAKAGE CURRENT



Increase of 2 orders of magnitude after 100 Mrad at 0 ± 2C temperature



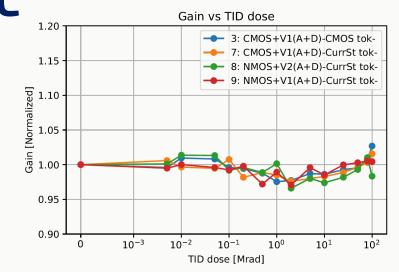
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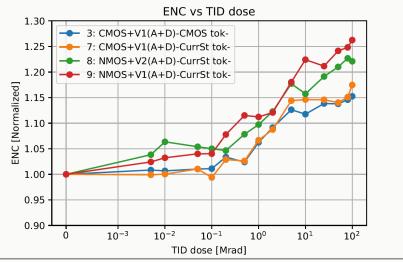


TID IRRADIATION: GAIN & ENC

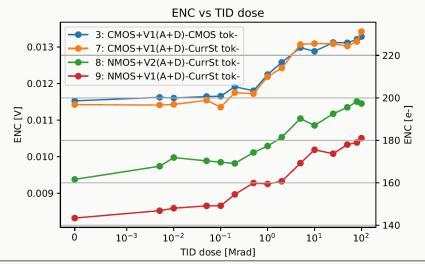
• **Relative Gain variation**: <3%



• **Relative ENC increase:** NMOS (25%) > CMOS (15%)



• Nominal ENC: CMOS > NMOS







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TID IRRADIATION: DACS & DIGITAL PERFORMANCE

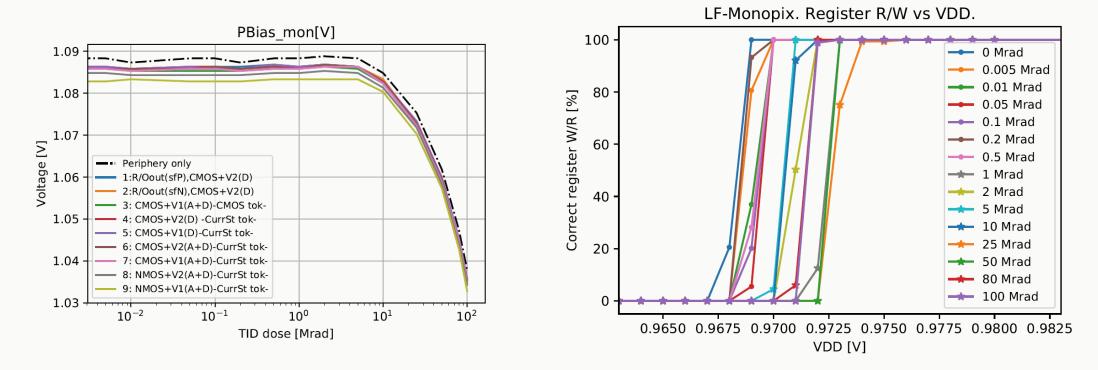
• DAC Reference Current:

Drop of 5% from 5 to 100 MRad

• Shift register R/W:

Variation < 0.5% in whole matrix

Default VDD: 1.8V



No degradation of digital performance



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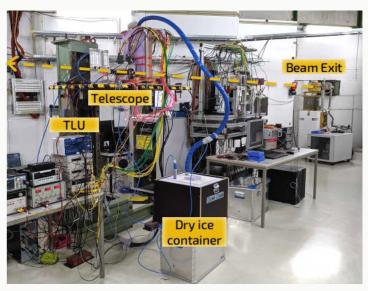


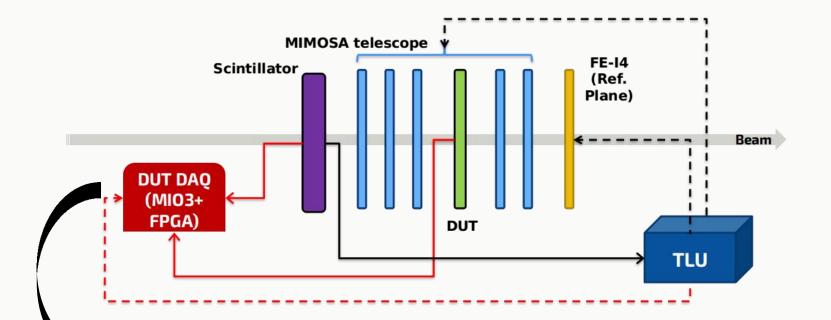
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TB DATA ACQUISITION AND SAMPLING @ ELSA/DESY

Telescope setup:

- 1 LF-Monopix1 DUT (200/100 μm thickness),
- 5 MIMOSA26 tracking planes
- 1 FE-I4 timing reference plane.
- Triggered by a plastic scintillator through a Trigger Logic Unit.
- **Beam:** 5 GeV e- at DESY TB21 2.5 GeV e- at ELSA (Bonn)





Scintillator, TLU and DUT (Token) timestamps sampled with a **640 MHz** clock in the MIO3 FPGA.

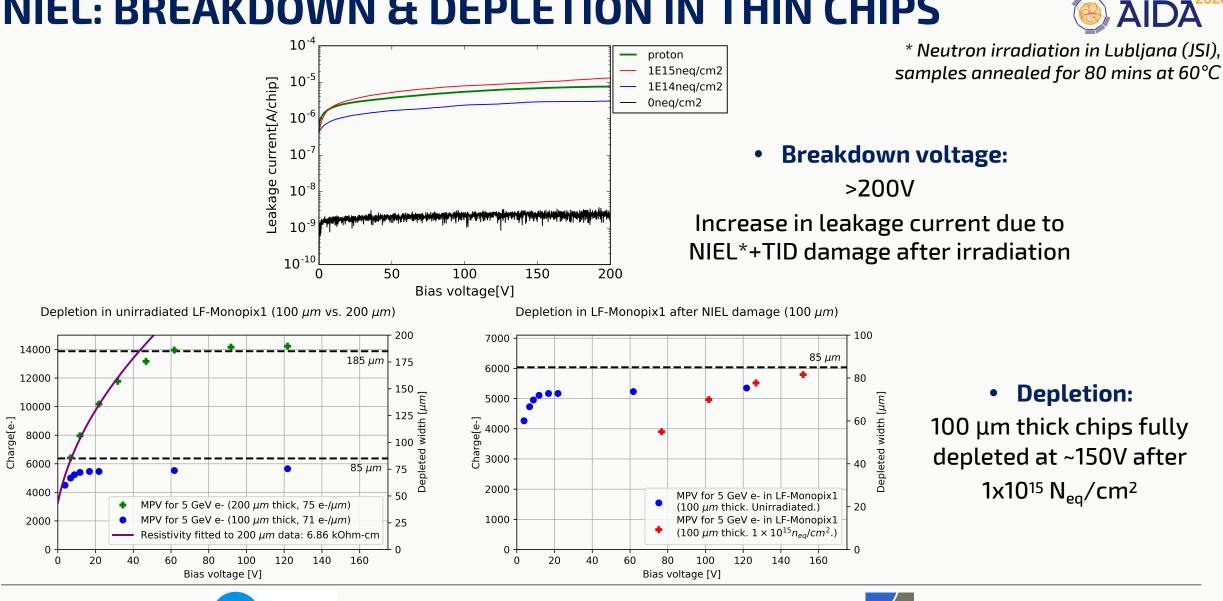
TB data analysis carried out using: https://github.com/SiLab-Bonn/beam_telescope_analysis



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NIEL: BREAKDOWN & DEPLETION IN THIN CHIPS

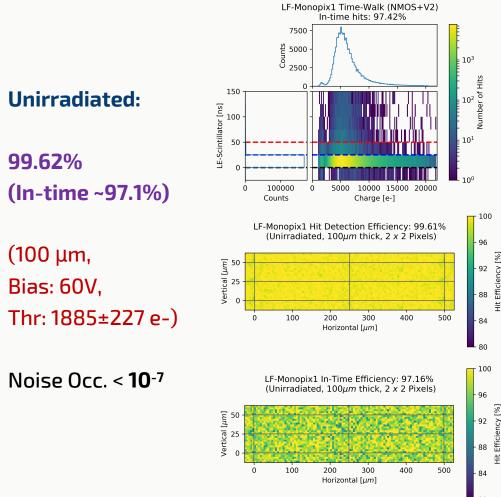


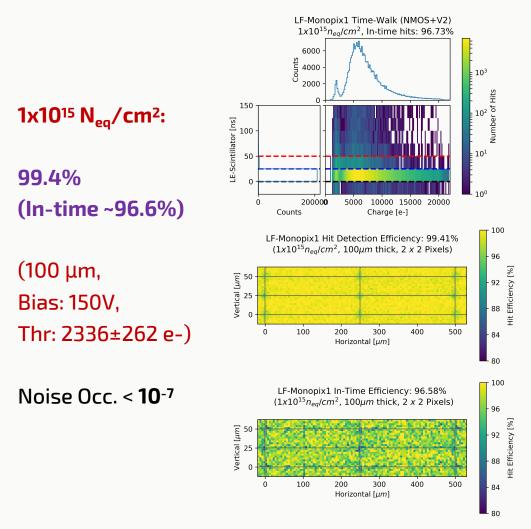






DETECTION EFFICIENCY





The chip's sensor and front-end still performed well after a NIEL fluence of $1 \times 10^{15} N_{eq}/cm^2$

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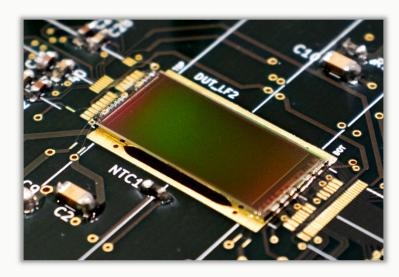
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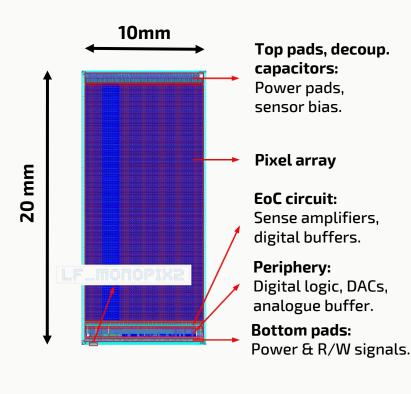




LF-MONOPIX2



- Smaller pixel pitch than LF-M1: 50 x 150 μm^2
 - → Reduced C_{det}
 (ergo: lower noise & power)
 → Larger pixel array
 - (340 rows x 56 cols)
- 40 MHz/160MHz CMOS or LVDS serial output.
- Timestamping: 6-bit LE/TE (ToT) @ 25 ns.
- Power: ~30 µW/pixel
- Injection & HitOr: Digital, at pixel level.



Column-drain R/O in
a 2 centimeter long
column, with full in-
pixel electronicsImproved pixel
layout for further
cross-coupling
mitigation

 \checkmark

Most of the matrix (57%) employs the rad-hard front-end that performed best in LF-M1

New features tested in other columns:

• Bidirectional discrimination circuitry.

- CSA designs with increased gain.
- Smaller $C_f(1.5 \text{ fF})$







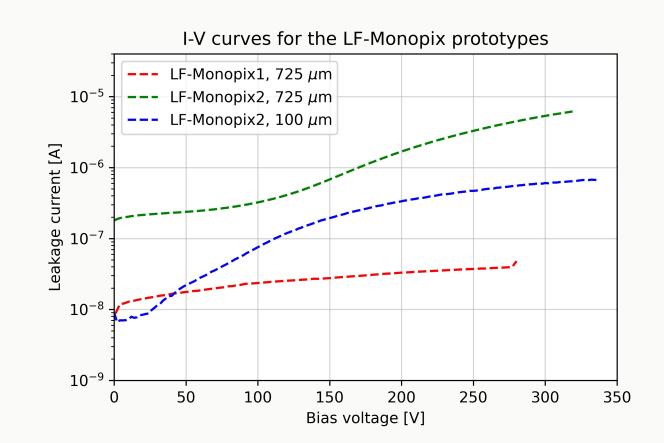
LF-MONOPIX2: SENSOR BREAKDOWN AND LEAKAGE

There was a significant improvement (>30%) in breakdown voltage from LF-M1 to LF-M2

Mainly due to guard-ring optimisation

Breakdown voltage >350V

Valid also after thinning and backside processing

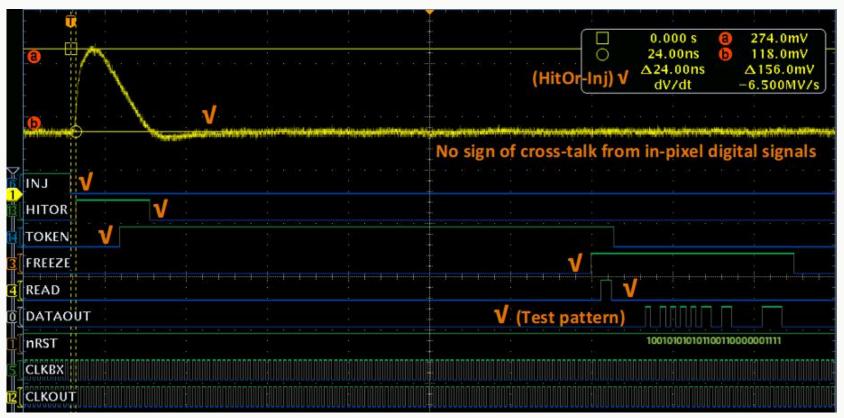




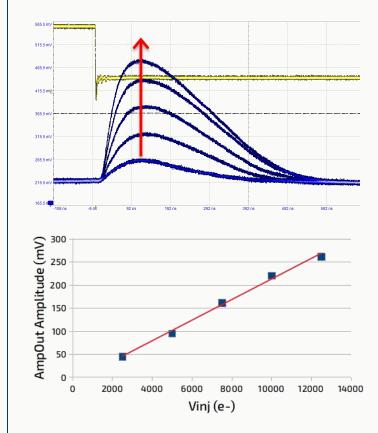


FUNCTIONAL FRONT-END, R/O AND INJECTION.

• Correct R/O architecture operation and data output.



• Linear CSA response.



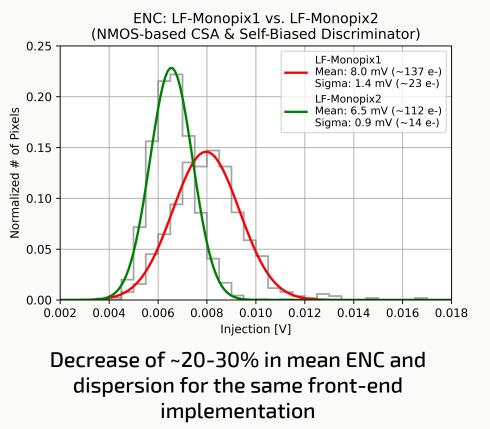
Injection of 1V pulse to a single monitored pixel - 40 MHz R/O enabled





LF-MONOPIX2: ENC

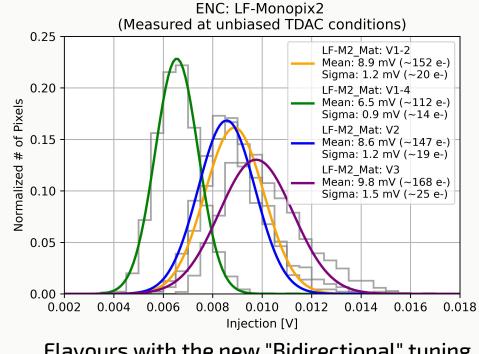
• From LF-Monopix1 to LF-Monopix2:



(As expected from reduced pixel pitch ~ C_d)

• Between LF-Monopix2 flavours:

Ν	[atrix	Column	CSA	Feedback cap.	Discriminator	Logic
	1-1	55 - 52	V1	$1.5\mathrm{fF}$	Bidirectional tuning	Falling
	1-2	51 - 48	V1	$5\mathrm{fF}$	Bidirectional tuning	Falling
\square	1-3	47 - 40	V1	$5\mathrm{f}$	unidirectional tuning	Rising
	1-4	39 - 16	V1	$5\mathrm{f}$	unidirectional tuning	Falling
	2	15 - 8	V2	$1.5\mathrm{fF}$	Bidirectional tuning	Falling
	3	7 - 0	V3	$1.5\mathrm{fF}$	Bidirectional tuning	Falling



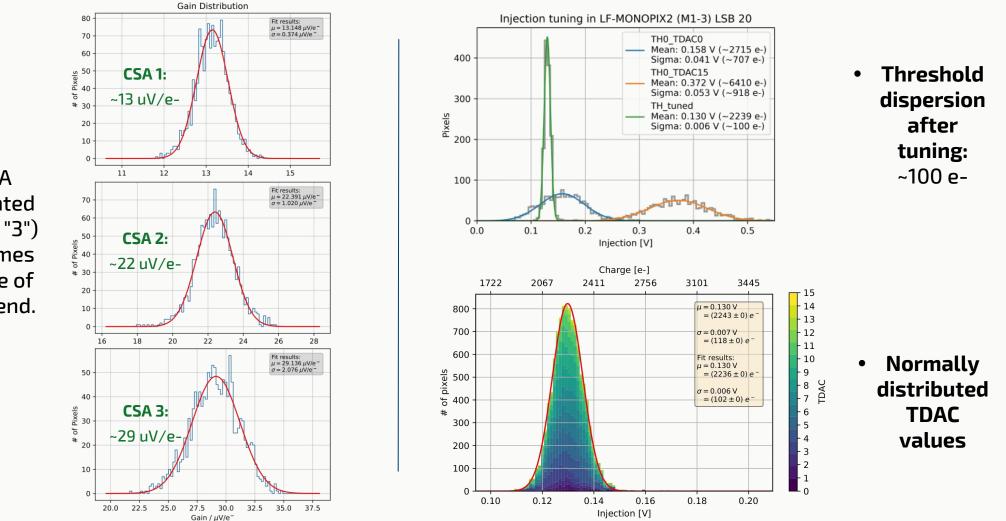
Flavours with the new "Bidirectional" tuning circuitry show a larger ENC and dispersion.







LF-MONOPIX2: FRONT-END GAIN AND TUNING



The two new CSA variants implemented in the chip ("2" and "3") show a gain 2-3 times larger than the one of the original front-end.

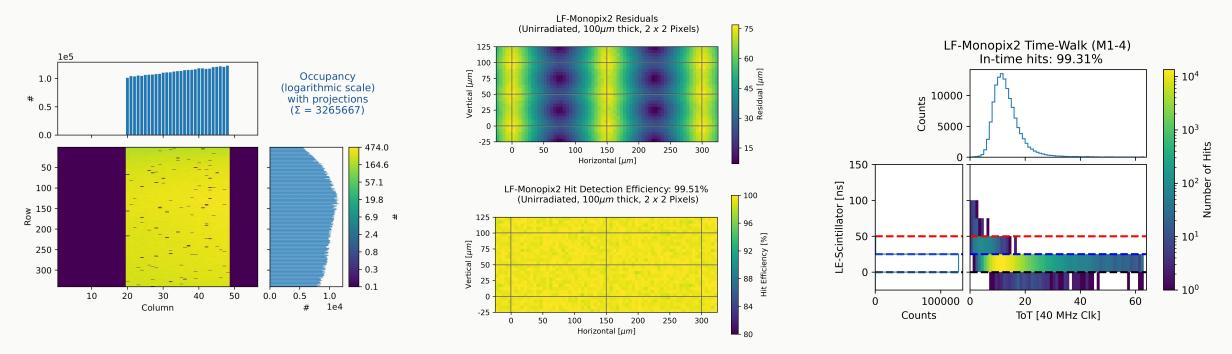




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LF-MONOPIX2: (PRELIMINARY) HIT EFFICIENCY

 Unirradiated chip exposed to 5 GeV electrons @ DESY: Data from matrices with CSA1 and unidirectional tuning. (100 μm thick, Bias: 60V, Thr: 2236±102 e-) Noise Occ. < 10⁻⁷



Our first test beam measurement results with LF-Monopix2 are encouraging, both in terms of hit detection efficiency and in-time hits (>99%)

> Upcoming: Proton irradiation and two weeks of test beam campaigns @DESY



2/24/2022



CONCLUSIONS

- Fully implemented fast R/O architecture in two large electrode DMAPS chips designed in a 150nm CMOS process and highly resistive wafers.
- X-ray irradiation and measurements in neutron irradiated samples have demonstrated that <u>the</u> <u>LF-Monopix1 prototype is radiation-hard</u>:
 - Small analog and digital degradation after 100 MRad TID dose
 - Full depletion of thinned sensors after neutron fluences of $1 \times 10^{15} \, N_{eq} / cm^2$
 - Hit detection efficiency after 1x10¹⁵ N_{eq}/cm² > 99% (In-time >96%)
- <u>A long column design (LF-Monopix2) with reduced pixel size is functional</u> and shows:
 - Increased breakdown voltage (>350V).
 - Improved cross-coupling mitigation.
 - Improved default front-end performance, as expected from the reduction in detector capacitance.
 - A uniform hit detection efficiency >99% before irradiation.



2/24/2022





Thank you for your attention.

Questions?

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under GA No. 675587-STREAM, 654168 (AIDA-2020) and 101004761 (AIDA-Innova).

The measurements leading to these results have partially been performed at the Test Beam Facility in DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).