HEPHY
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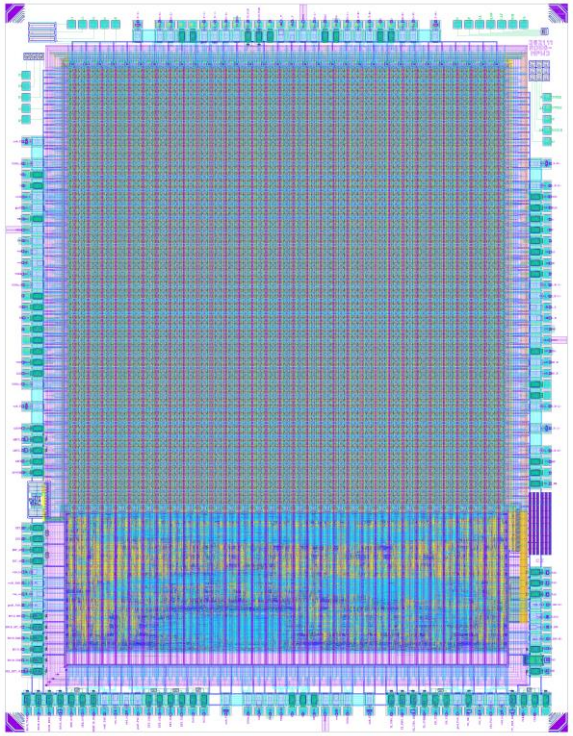
ÖAW

RD50



Design and characterization of depleted monolithic active pixel sensors within the RD50 collaboration

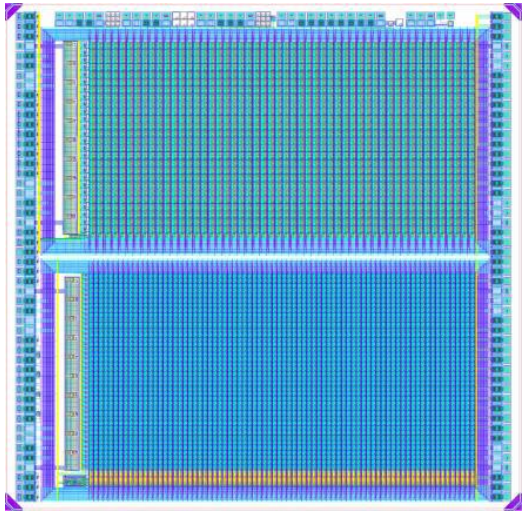
Patrick Sieberer, on behalf of the RD50 CMOS working group

CERN-RD50 CMOS

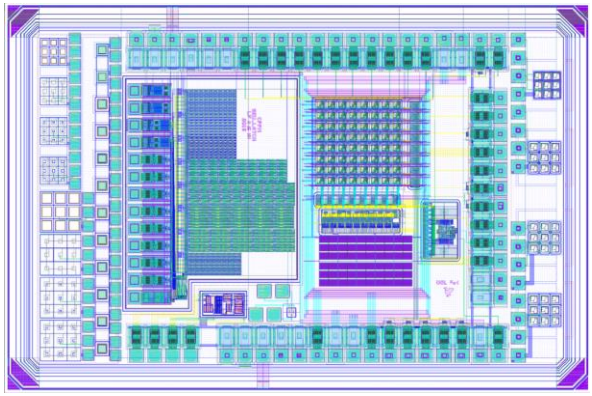
- CERN-RD50 collaboration
  - Radiation hard semiconductor devices for very high luminosity colliders
  - >400 people
  - 63 institutes
- CERN-RD50 CMOS Working Group
  - Program to study and develop monolithic CMOS sensors with
    - High granularity
    - High radiation tolerance
    - LFoundry 150nm HV-CMOS
  - Our program includes
    - TCAD simulations
    - ASIC design
    - DAQ development
    - Performance evaluation
  - Involved resources
    - >40 people
    - 17 institutes

RD50 CMOS DMAPS

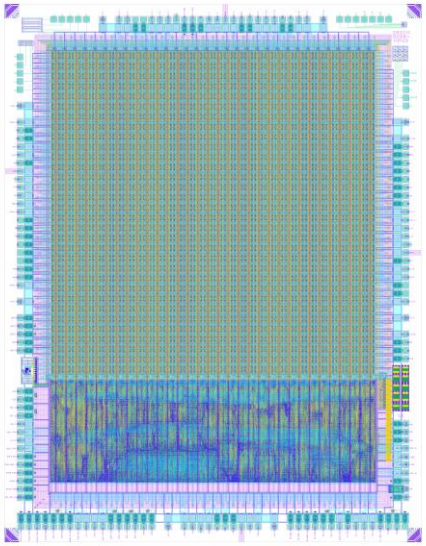
Overview



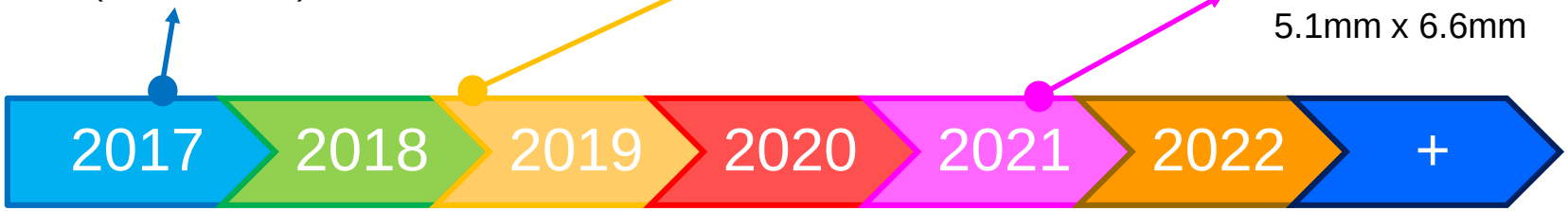
RD50-MPW1
(5mm x 5mm)



RD50-MPW2
(3.211mm x 2.120mm)

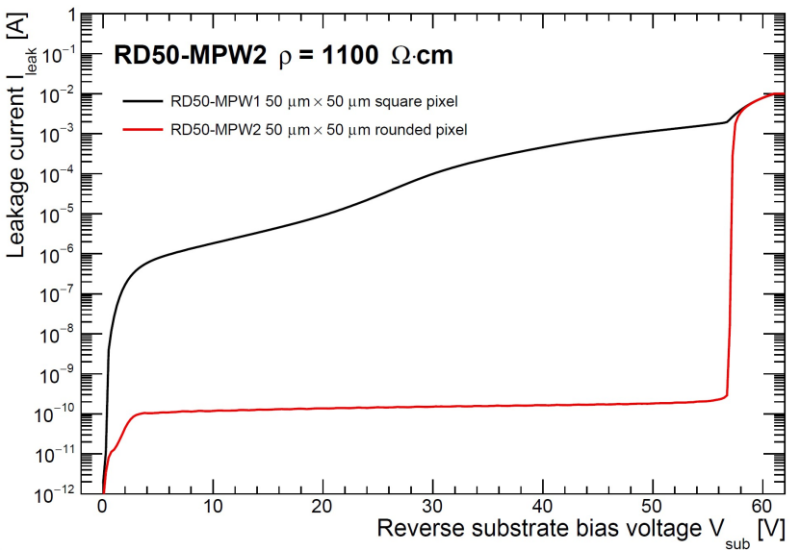


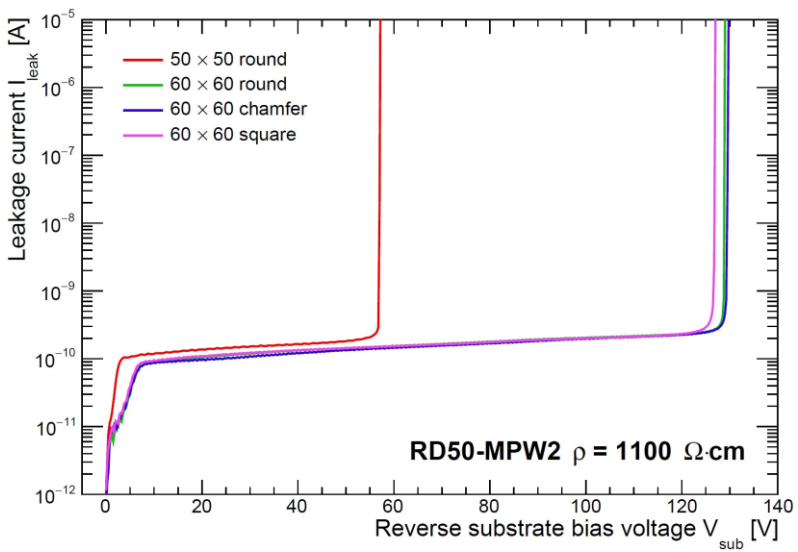
RD50-MPW3
5.1mm x 6.6mm



- 3 Depleted Monolithic Active Pixels Sensors (DMAPS) designed so far
  - submission dates in timeline, chip delivery ~5 months later
- All of them in LFoundry 150nm process
- High resistivity substrates (up to ~2kOhm*cm)

RD50-MPW1 and RD50-MPW2

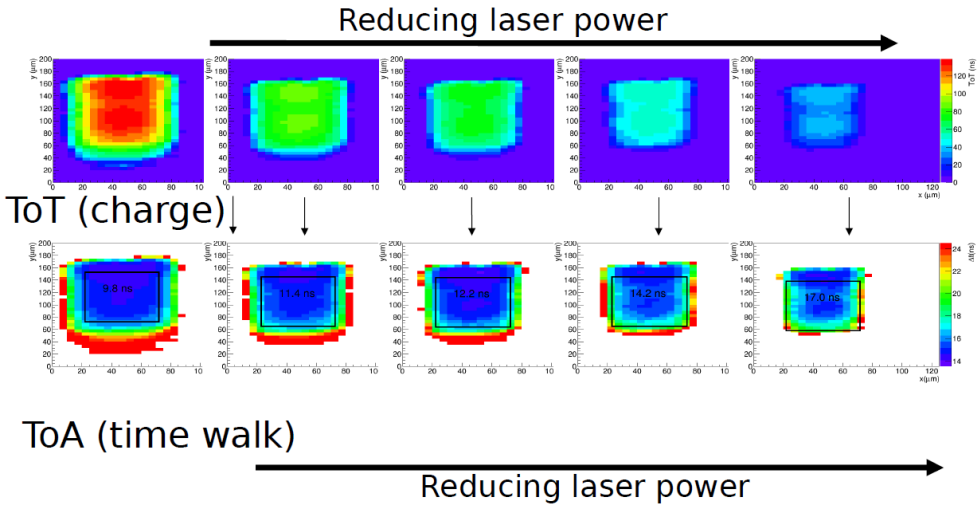




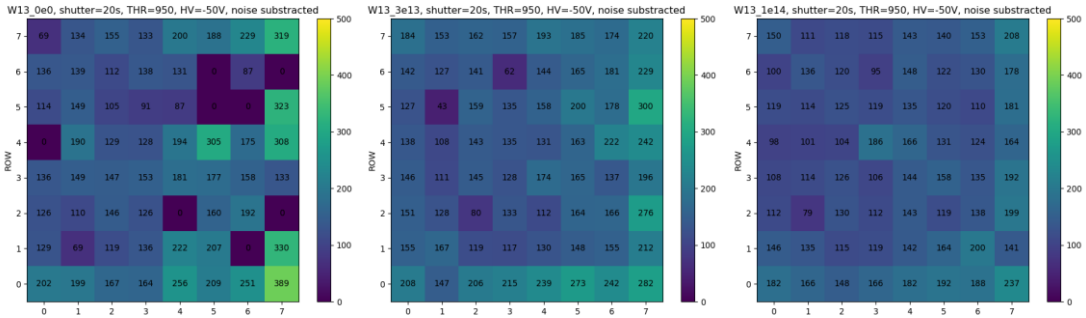
See talk by M. Franks at 36th RD50 workshop

- RD50-MPW1 suffered from high leakage current and low breakdown voltages
- TCAD studies done => RD50-MPW2 as analog-only chip
  - Performs really well ($I_{leak}\downarrow$, $V_{BD}\uparrow$)
  - Detailed tests including timing studies with lasers and testbeams (analog + digital performance)

RD50-MPW2 Laboratory (Highlights)



- TCT and eTCT on passive test structures and active matrix
- Timing performance dependence on decreasing laser power as expected:
  - ToT decreases
  - ToA increases
- Rough calibration ToT → electrons available
- For details, see B. Hiti at 38th RD50 workshop (presented by S. Powell)



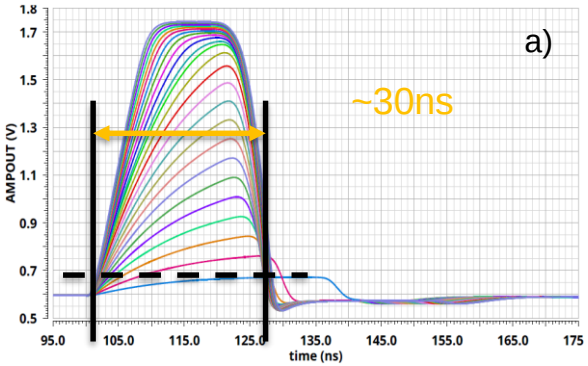
unirradiated | $3e13N_{eq}/cm^2$ | $1e14N_{eq}/cm^2$

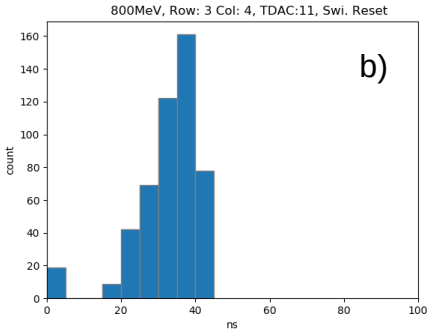
Measurements with Sr90 source (only done for lower irradiated chips)

- Irradiation campaign up to $2e15N_{eq}/cm^2$
- Sr90 tests: Decrease in pixel efficiency seen
- "L" shape at edges observed
  - Might come from biasing scheme
  - Not fully understood

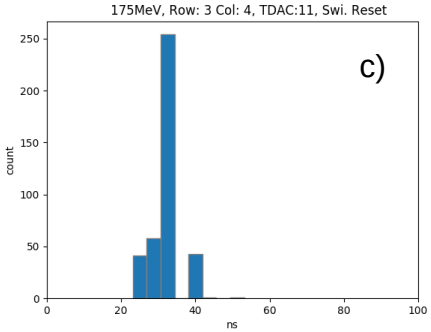
RD50-MPW2 Testbeam (Highlights)

- Testbeams at medical facilities
  - Ruder Boskovic Institute (HR)
    - See talk from R. Palomo at 39th RD50 workshop
  - Rutherford Cancer Center (UK)
    - See talk from S. Powell at 38th RD50 workshop
  - MedAustron (AT)
- Analog performance
  - Pulse width at various beam energies
- Digital performance in a telescope
  - Digital logic in FPGA
  - Synchronization with other detectors possible
  - Data rate rather low (only one pixel can be activated; analog only chip!)
  - Tracking possible, but limited capabilities (single pixel)
  - ***Lot of lessons learned for RD50-MPW3***





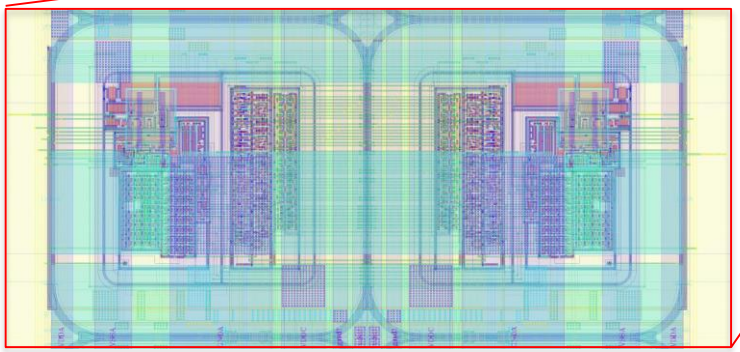
- Simulation a) and testbeam measurements at 800MeV b) and 175MeV c) for a 'switched reset pixel'
- Pulse width of signal independent of beam energy
- Testbeam results agree with simulation

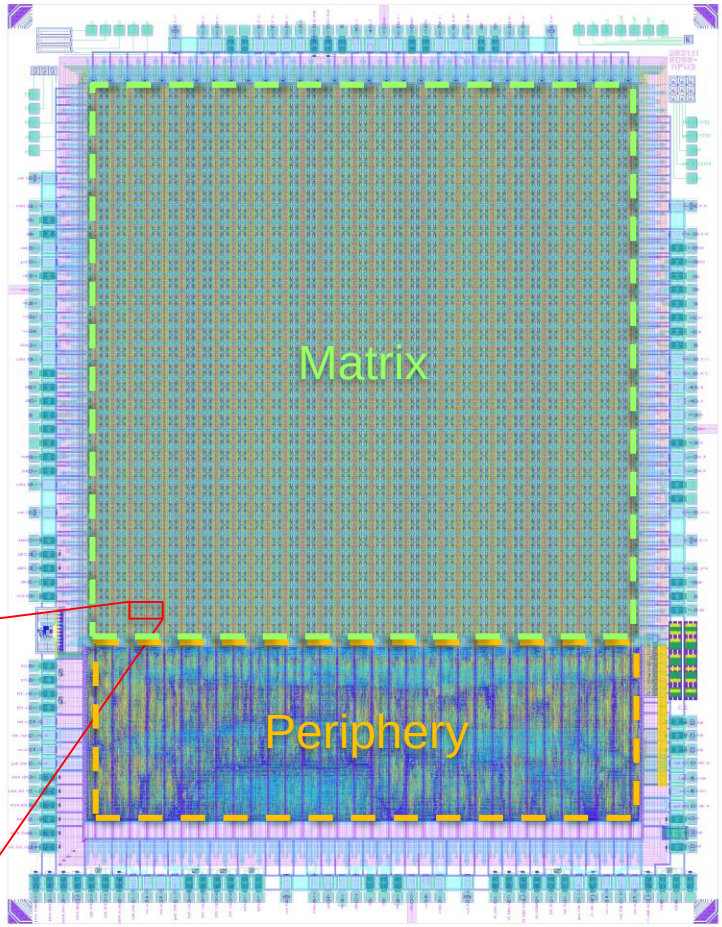


DESIGN OF RD50-MPW3

Overview

- Analog pixel design taken from RD50-MPW2
  - 64 x 64 pixels
  - Pixel size 62µm x 62µm
  - Active area: 3.968mm x 3.986mm
    - Total Size: 5.1mm x 6.6mm
- Digitization in each pixel
  - FEI3-style
  - Increase of pixel size necessary
    60µm x 60µm (RD50-MPW2) to
    62µm x 62µm (RD50-MPW3)
- Complete new design of digital periphery
  - Covering ~15% of total area
  - Focus of this talk

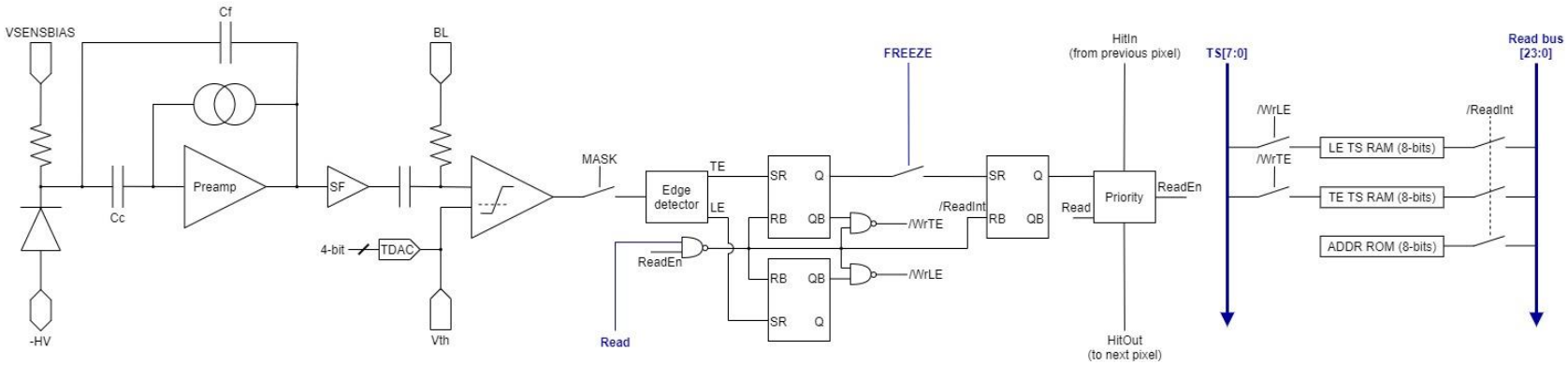




First draft of documentation available

Analog Matrix

- Pixels read out in double columns (DCOLs) with shared digital busses to reduce routing congestions
- Each pixels receives a global (chip-internal) timestamp and returns
  - 8bit leading edge
  - 8bit trailing edge
  - 8bit pixel address
- 8 flip-flops plus logic for configuration <u>implemented in each pixel</u>
  - All pixel from DCOL connected to a shift-register
  - Read-back is possible
  - Not shown in figure below
- Overview of the functionalities of the matrix can be seen in *Development of High Voltage-CMOS sensors within the CERN-RD50 collaboration (E. Vilella, VERTEX2021, submitted to NIM-A)*

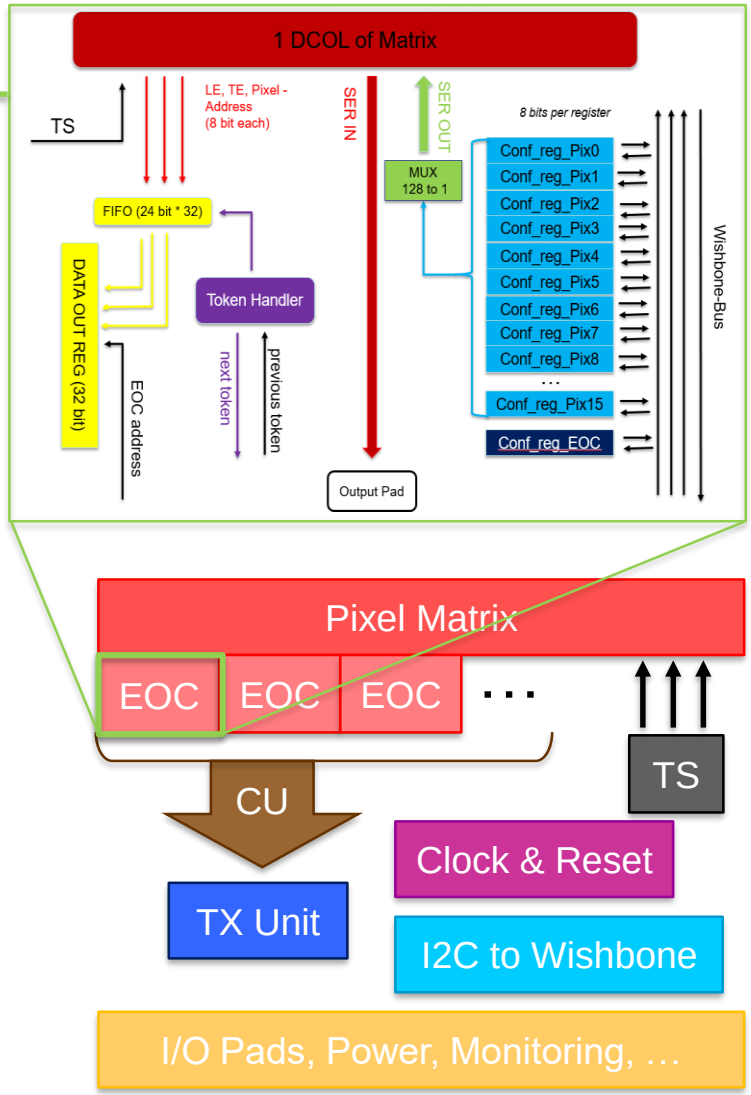


In-pixel readout logic (FEI3 - style)

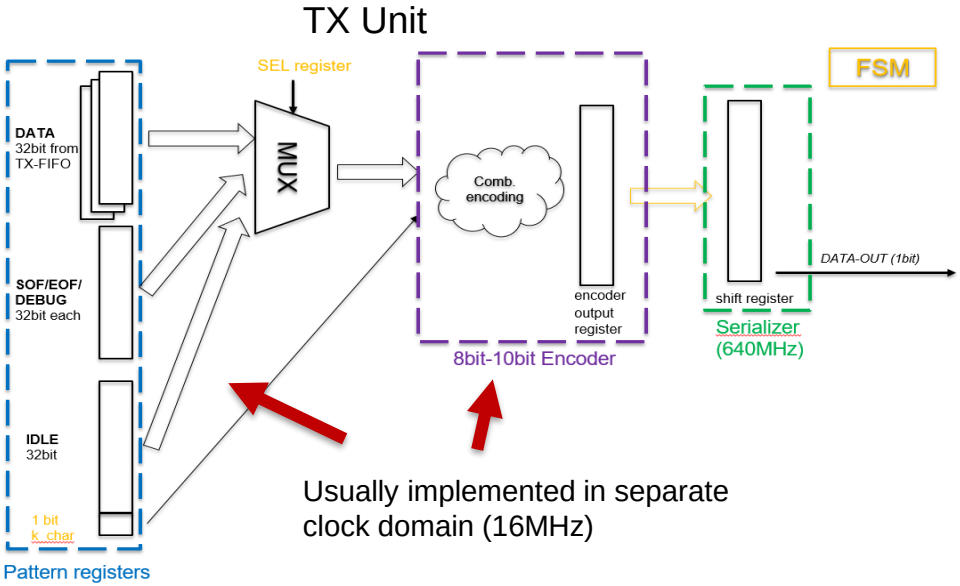
DIGITAL READOUT IMPLEMENTATION

Overview

- One End-Of-Column (EOC) per DCOL
  - Configuration of pixels
  - Pixel data readout + 32 words deep buffer
- Transmission Unit (TX Unit) for data transmission
  - 128 words deep buffer (FIFO)
  - Framing
  - Encoding (Aurora 8bit-10bit)
  - Serialization (Serial stream at 640MHz)
- Control Unit (CU) for reading out EOC buffers
  - Controls data propagation from EOCs to TX Unit
- Global Timestamp (TS) Generator
  - 8bit, running at 40MHz
  - Gray-encoded to minimize activity on bus
- Clock and Reset Generator
  - Dividing a fast (640MHz) clock into a 40MHz clock
  - Clock multiplexer for optional external 40MHz
  - Synchronizing the 2 external reset signals with clock
- I2C to wishbone module
  - Converts external I2C signals to internal wishbone control signals

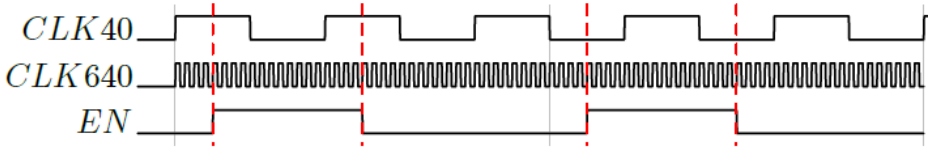


Features of RD50-MPW3



Clock Domain Crossing (CDC)

- Usually, internal clocks are generated using a PLL
  - Not available, complex to design
- Internal 40MHz used
  - generated by a divider from external 640MHz
- Special enable signal (EN, shown below) generated with 640MHz clock
  - 2 different cases, but always exactly 1 rising edge of 40MHz clock within high level of enable
  - Special attention to constraints and clock tree needed



Timing of enable signal (EN)

Internal Buffers

- 2 stage FIFO chain
  - 32 words deep in each DCOL
  - 128 words deep in TX Unit
  - Less high speed buffers in FPGA required

Monitoring

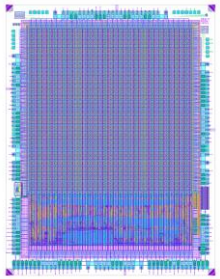
- 10 monitoring outputs for internal signals

External Control

- Parts of internal logic can be controlled with external signals for debugging

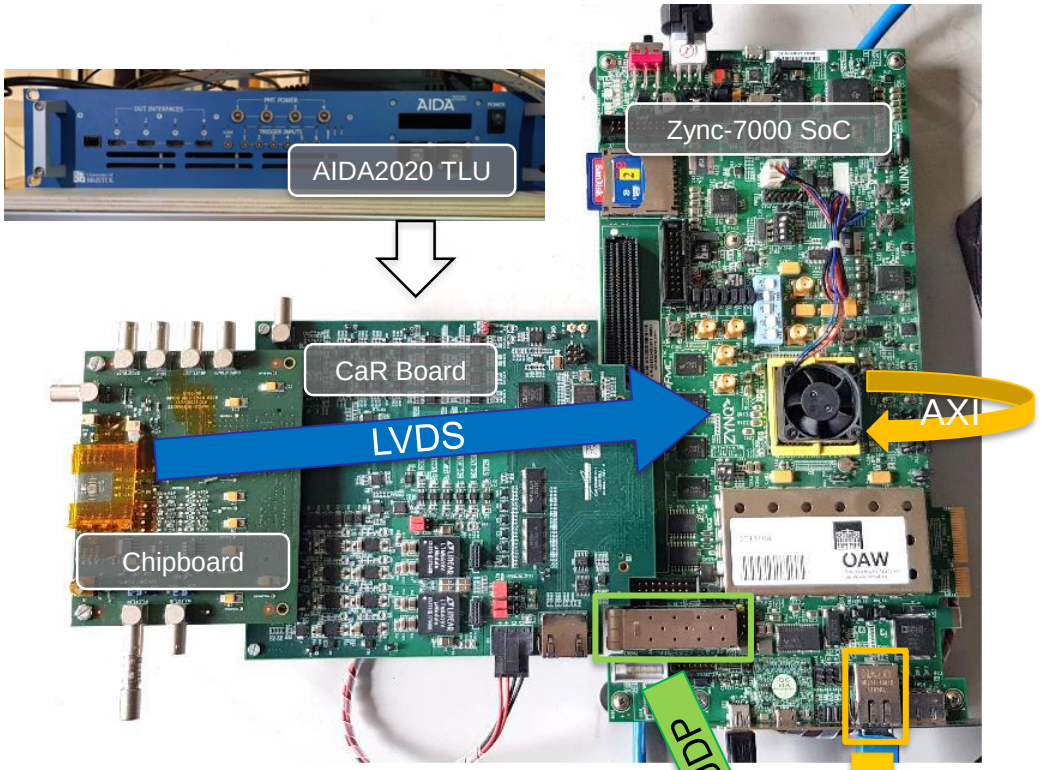
CONCEPTS RD50-MPW3 DAQ

Hardware

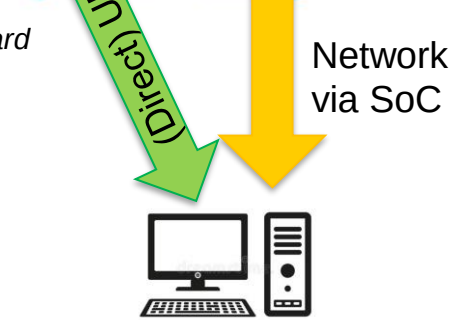


- Incoming data stream (to FPGA)
- High speed data path
- Low speed data path (Monitoring)

Draft of RD50-MPW3 chipboard

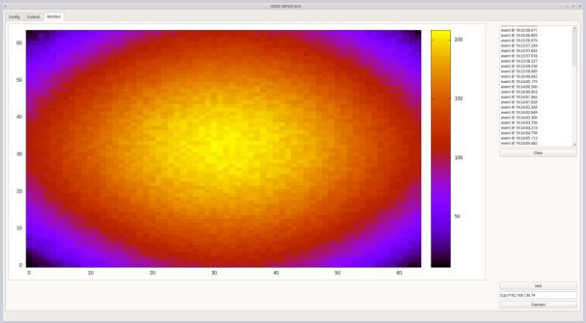


Pictures shows RD50-MPW2 chipboard



- Caribou used as DAQ
- AIDA2020 TLU connected to CaR-board for triggering
- 2-level chipboard to readout 2 chips with one setup
- 2 data paths (next slide)

Data Flow and Software

	Fast data path	Slow data path
Purpose	Data taking	Monitoring, Spy Data (small percentage of data)
Data flow	SFP port + UDP (Jumbo frames) for fast, firmware-controlled readout	AXI Bus + Ethernet network for monitoring and slow control
Data storage	Integrated into EUDAQ (EUDAQ raw data files)	EUDAQ + custom data storage possible, Handling of slow control commands
Usage	• data transmission + storage only • easy integration to tracking framework Corryvreckan • Testbeam	• Slow control commands • Monitoring • Standalone tests at laboratory
Current development efforts (examples)	Loopback speed-test at 640MHz implemented • Dummy data generated in FPGA • Data sent to CaRboard, loop-back over FMC connector • Data read by FPGA + sent over UDP to PC (850Mbit/s data rate achieved)	Draft of online monitor: 

Outlook & Summary

End 2020
- Start Design RD50-MPW3

End 2021
- Submission RD50-MPW3

Begin 2022 (now)
- DAQ development
- Chipboard design

April 2022
- Expected Chip delivery

June 2022
- First Laboratory test

October 2022
- Testbeam at CERN SPS

Summary

- RD50-MPW2 very successful chip
  - Analog performance increased a lot compared to RD50-MPW1
- RD50-MPW3 submitted for fabrication in December 2021
  - Analog pixels electronics from RD50-MPW2
  - New digital periphery
- DAQ Design (Hardware, Firmware and Software) of RD50-MPW3 ongoing
  - No show stoppers seen so far
  - Ultimate goal is to build a small telescope demonstrator

Outlook/ToDo

- Triggering/Synchronization with other detectors
  - No internal trigger in RD50-MPW3
  - Synchronous (AIDA-mode) readout with TLU
- "Time bin matching"
  - Order of hits depends a lot on the data rate
    - Due to fast internal readout scheme
  - Time matching tricky when internal timestamp has an overflow (8bit at 25ns -> every 6.4µs)
    - Might be old data in the FIFO chain of the chip
  - Design of a System Verilog based framework ongoing to provide data for different hit rates, occupancies, … for developing a software algorithm

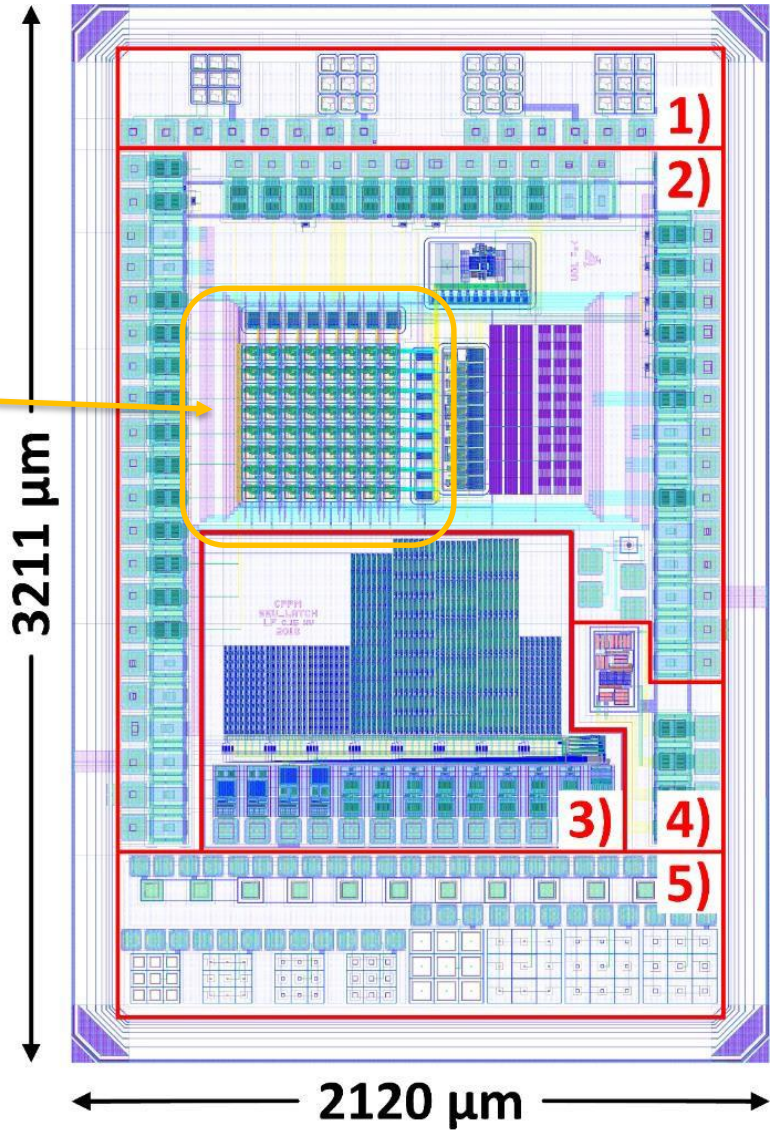
This work has been partly performed in the framework of the CERN-RD50 collaboration. It has received funding from the Austrian Research Promotion Agency (FFG), grant number 878691 and from the European Union's Horizon 2020 Research and Innovation program under grant agreement 101004761 (AIDAinnova).

BACKUP

RD50-MPW2

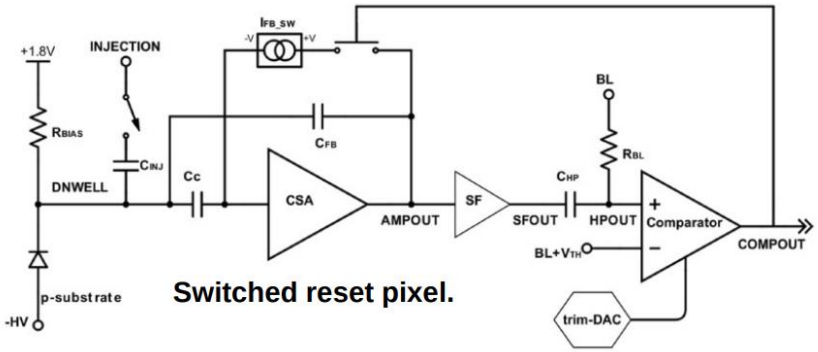
Introduction RD50-MPW2

- LFoundry 150nm process
- Different Wafer resistivities and fluences available
- Passive test-structures 1)
- **Active matrix of DMAPS pixel, including analogue readout 2)**
- SEU tolerant memory array 3)
- Bandgap reference voltage 4)
- Test structures with SPADs 5)
- Details on 3) and 4): See talk from R. Marco Hernandez at 36th RD50 workshop
- Details on 1): See talk from M. Franks at 36th RD50 workshop or from R. Marco Hernandez at VERTEX 2020



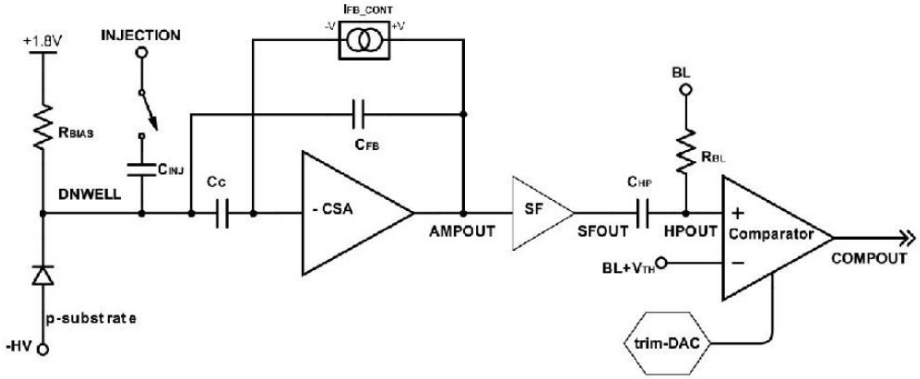
Pixel Flavors

Switched Reset Pixel



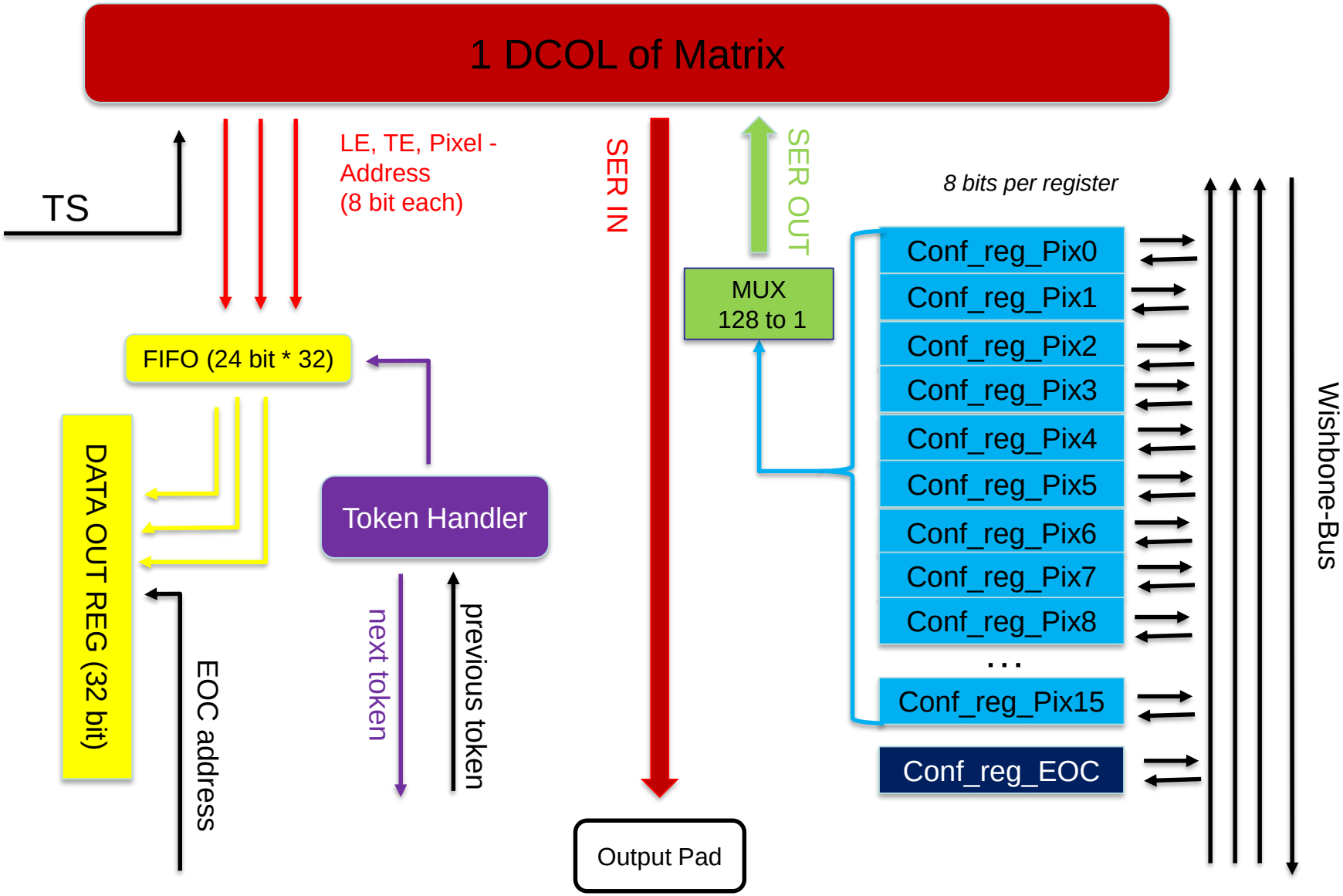
Switched reset pixel.

Continuous Reset Pixel

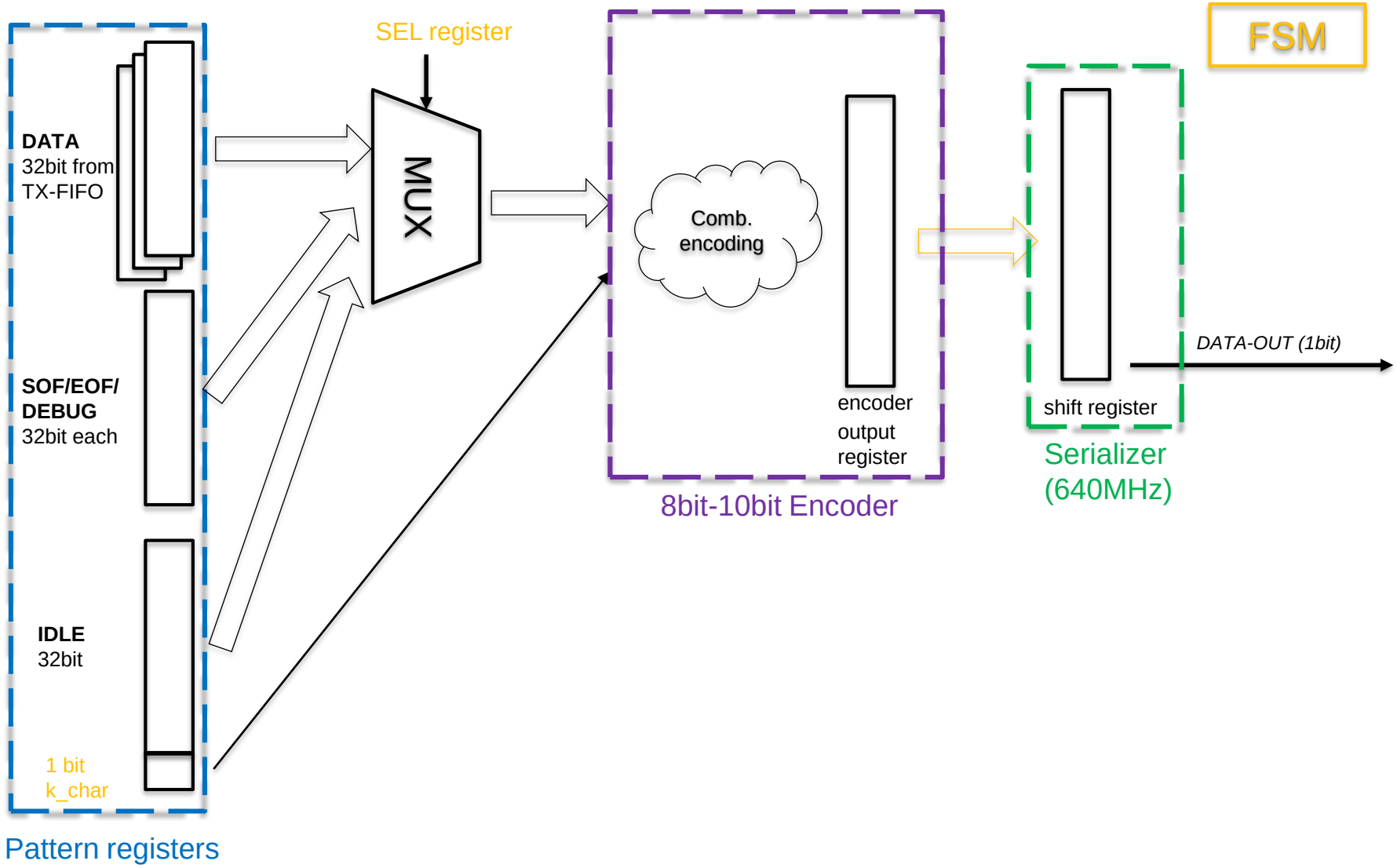


DIGITAL READOUT IMPLEMENTATION

Matrix Readout and Control – End Of Column (EOC)



Novelties of RD50-MPW3



TRIGGERING RD50-MPW3

AIDA TLU

AIDA-TLU with 2 possible DUT interfaces:

- EUDET Mode: Needed for Hephy-telescope and many other older telescope
  - Whenever no (fast or "synchronizable") internal TS is available in the telescope
- AIDA Mode: Needed for RD50-MPW3 and newer telescope (probably at CERN)
  - Whenever internal TS-synchronizing is possible
  - Much faster than EUDET

Trigger/Busy Handshake With Trigger Number

This interface mode is an extension of the Trigger/Busy handshake. After the DUT detects that the TLU has de-asserted the TRIGGER line it can cause the TLU to clock out the current trigger number by toggling the DUT clock line. The number is clocked Least Significant Bit (LSB) first. Figure 4.2 shows the signal timing for this interface mode.

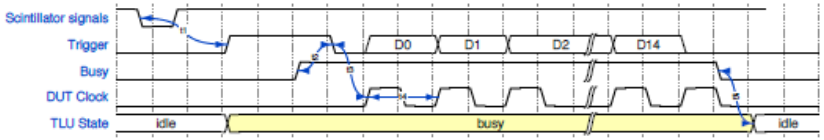


Figure 4.2: Trigger/Busy Interface Mode With Trigger Number

This mode of operations is enabled by setting the DUTMaskMode flag for the specific DUT to 0b00. See section 10.2 for details.

Synchronous (AIDA) Mode

In synchronous mode (also known as AIDA mode) the TLU sends a clock (by default 40MHz) to the DUT.
When the TLU produces a trigger, the trigger line from TLU to DUT is asserted for one cycle of the clock. In order to synchronize time-stamps between TLU to DUT a single cycle timestamp reset signal is issued at the start of each run.
The DUT can veto triggers at any point by asserting the BUSY line.
Figure 4.3 shows the signal timing for this interface mode.

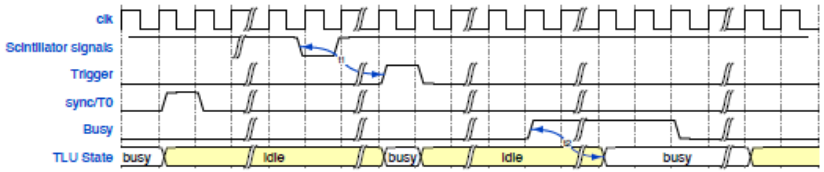


Figure 4.3: Synchronous (AIDA) Interface Mode

This mode of operations is enabled by setting the DUTMaskMode flag for the specific DUT to 0b11. See section 10.2 for details.

Trigger 2

- TLU has two internal, fast FIFOs
  - Trigger Number (TN), 15 bit
  - Fast timestamp (TS-T = TimeStamp-TLU), up to 160MHz, ~16 bit (coarse and fine(?))
- <u>For the EUDET mode, the TN written on the DUT interface after every trigger</u>
  - Trigger input from scintillators needed
- <u>For AIDA mode, TS-C and TS-T are synchronized at the beginning of each run</u> with a special signal on the DUT interface
  - TLU and RD50-MPW3 now have the same TS!
- **EUDAQ Producer available, which reads the two FIFOs of the TLU to match TN with a TS-T (and thus also TS-C)**
  - Event matching must be done offline
  - Data readout over the IPBus, up to **50MHz trigger rate** possible (otherwise, FIFO-overflow)
    - **This determines our max. particle rate we can handle (!)**