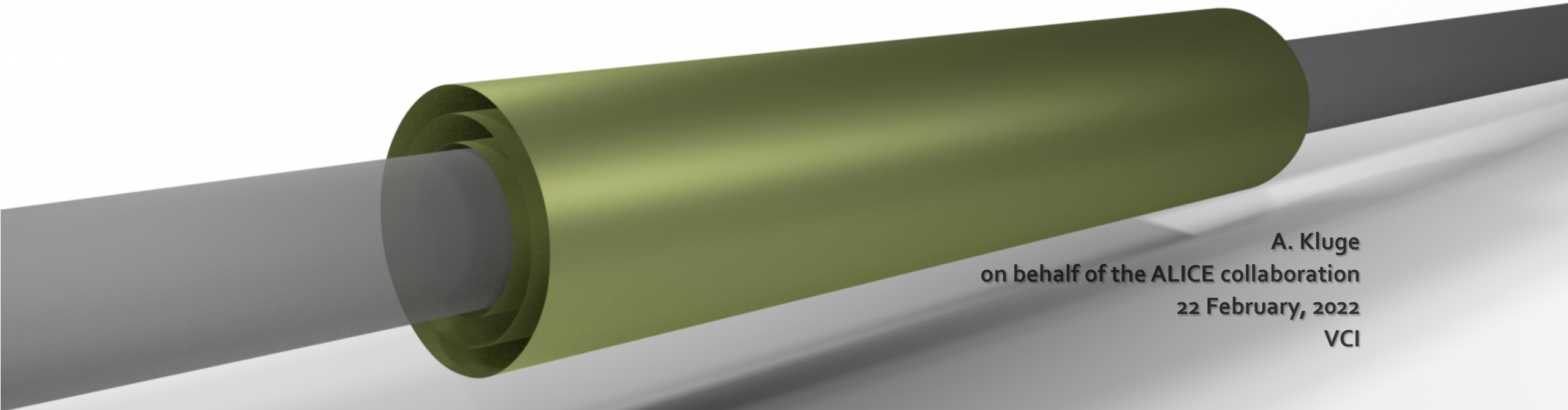
ALICE - ITS3

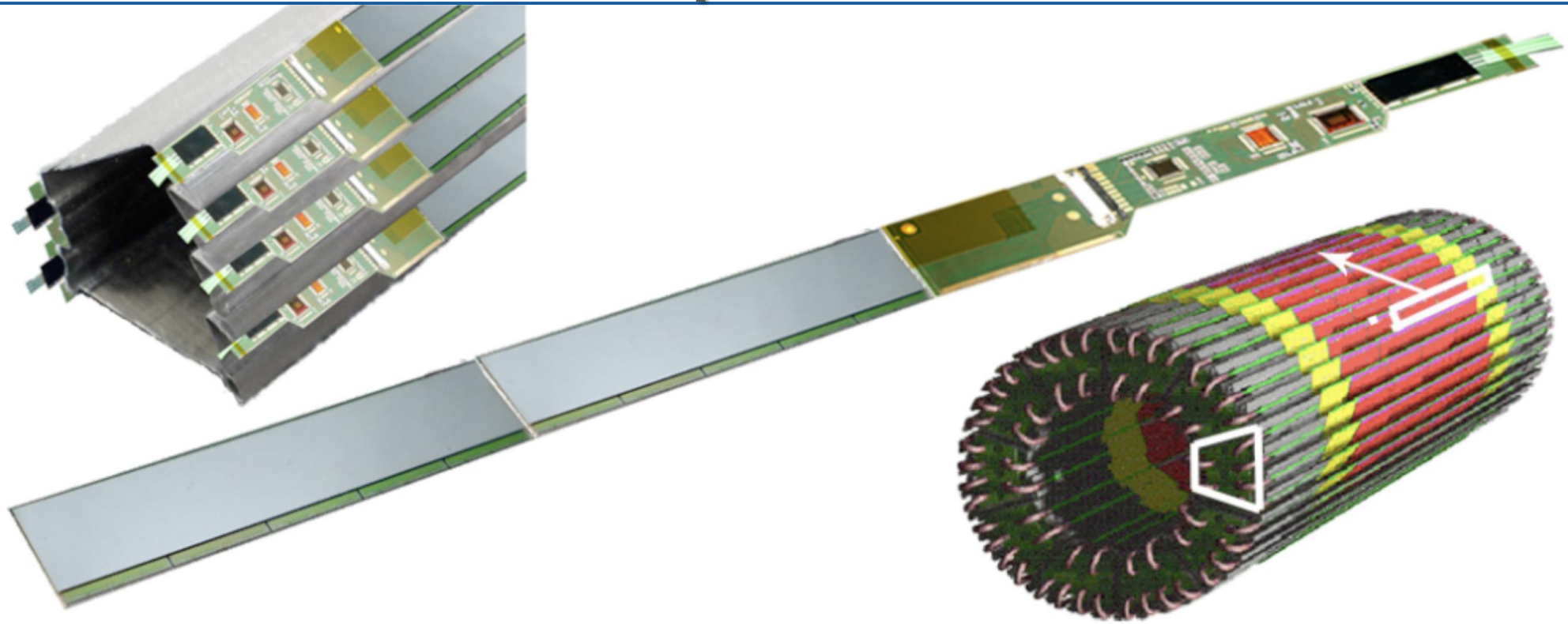
bent, wafer-scale CMOS detector



A. Kluge
on behalf of the ALICE collaboration
22 February, 2022
VCI

ALICE pixel detectors

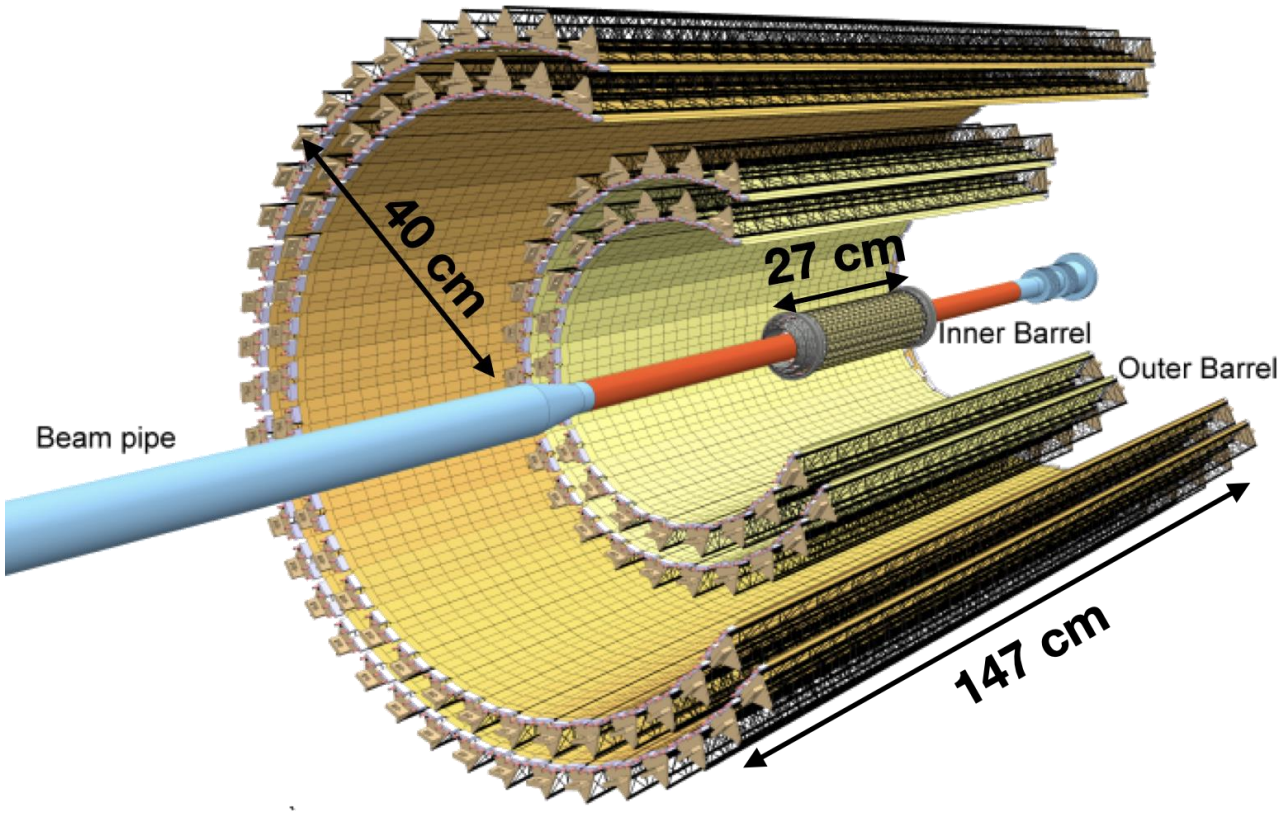
ALICE – silicon pixel detector – Run1/2

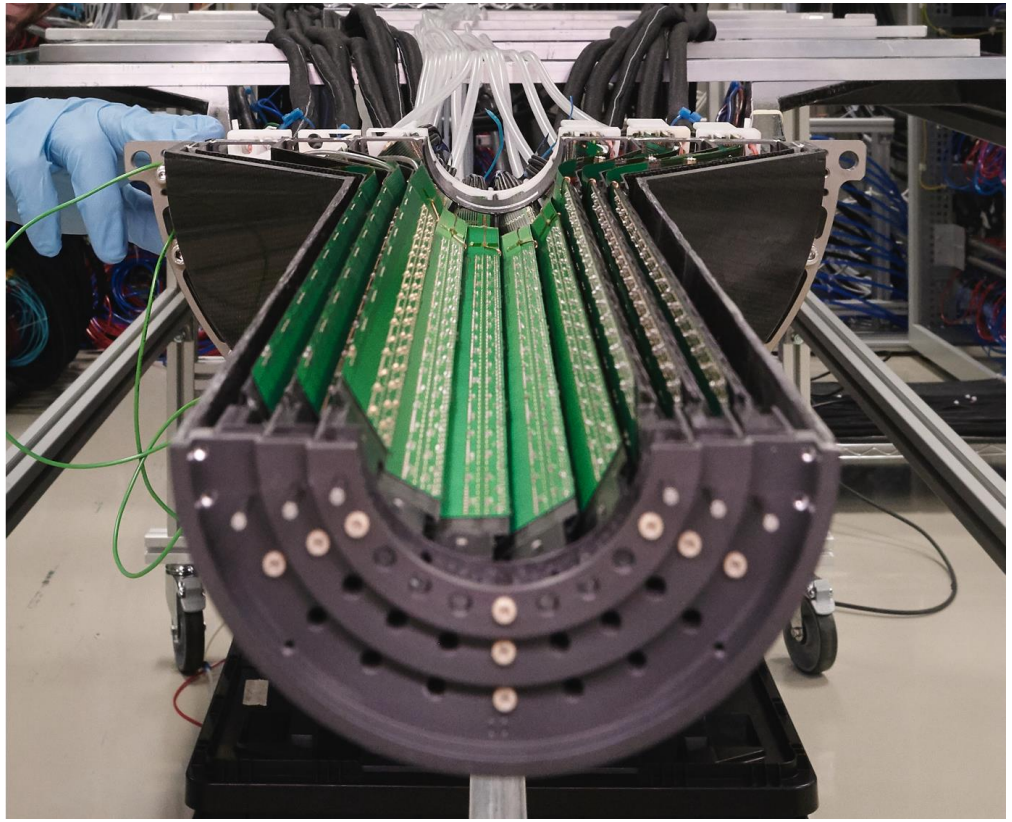


2008 Run1/2
ITS1-SPD hybrid pixel
425 x 50 μm^2 pixel size
1.0% X_0 per layer

hybrid flex HDI
C_4F_{10} cooling
CF support

ALICE – inner tracker 2 – Run 3/4

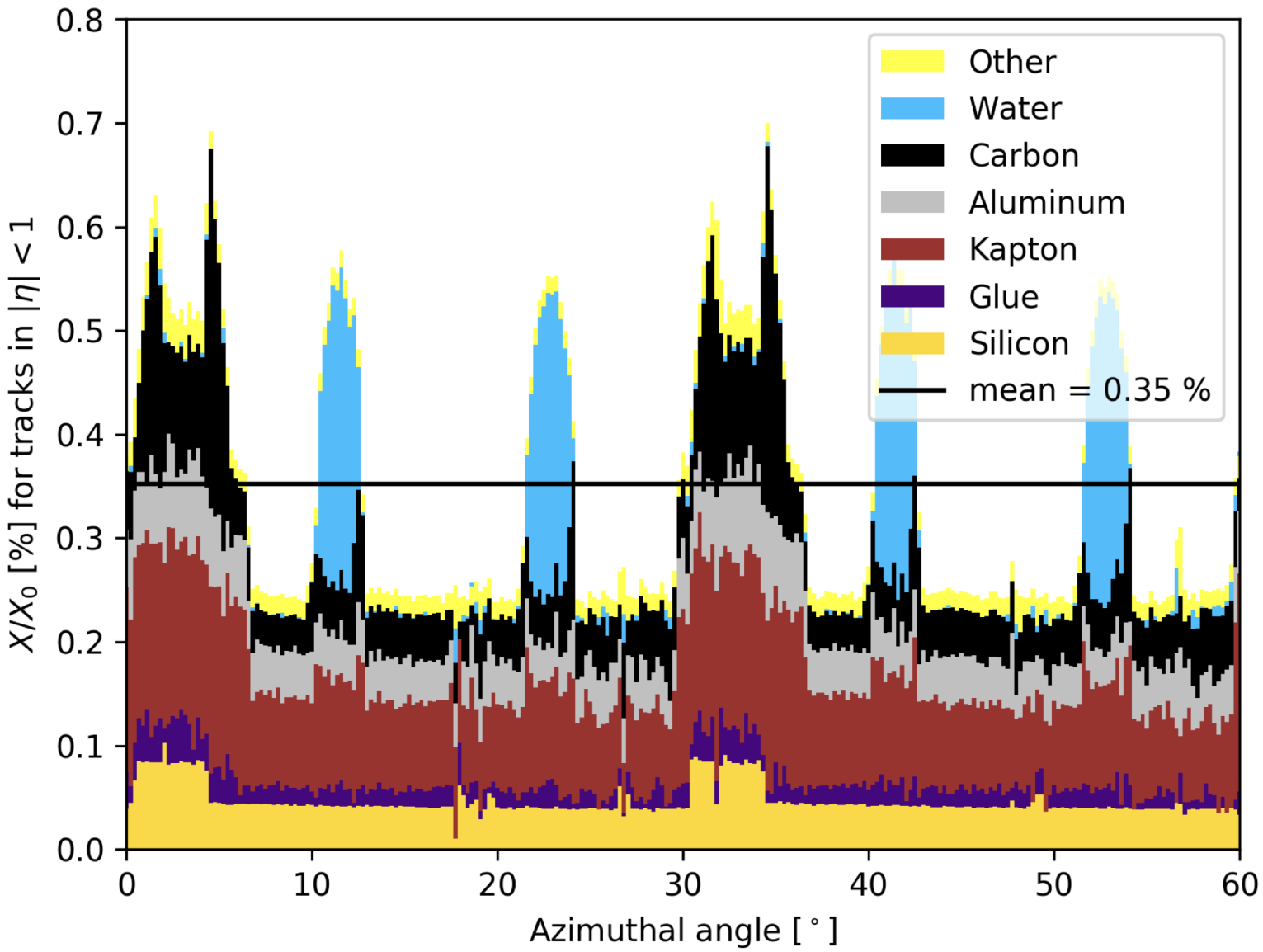




2022 Run3/4
ITS2 MAPS
30 x 30 μm^2 pixel size
0.35% X_0

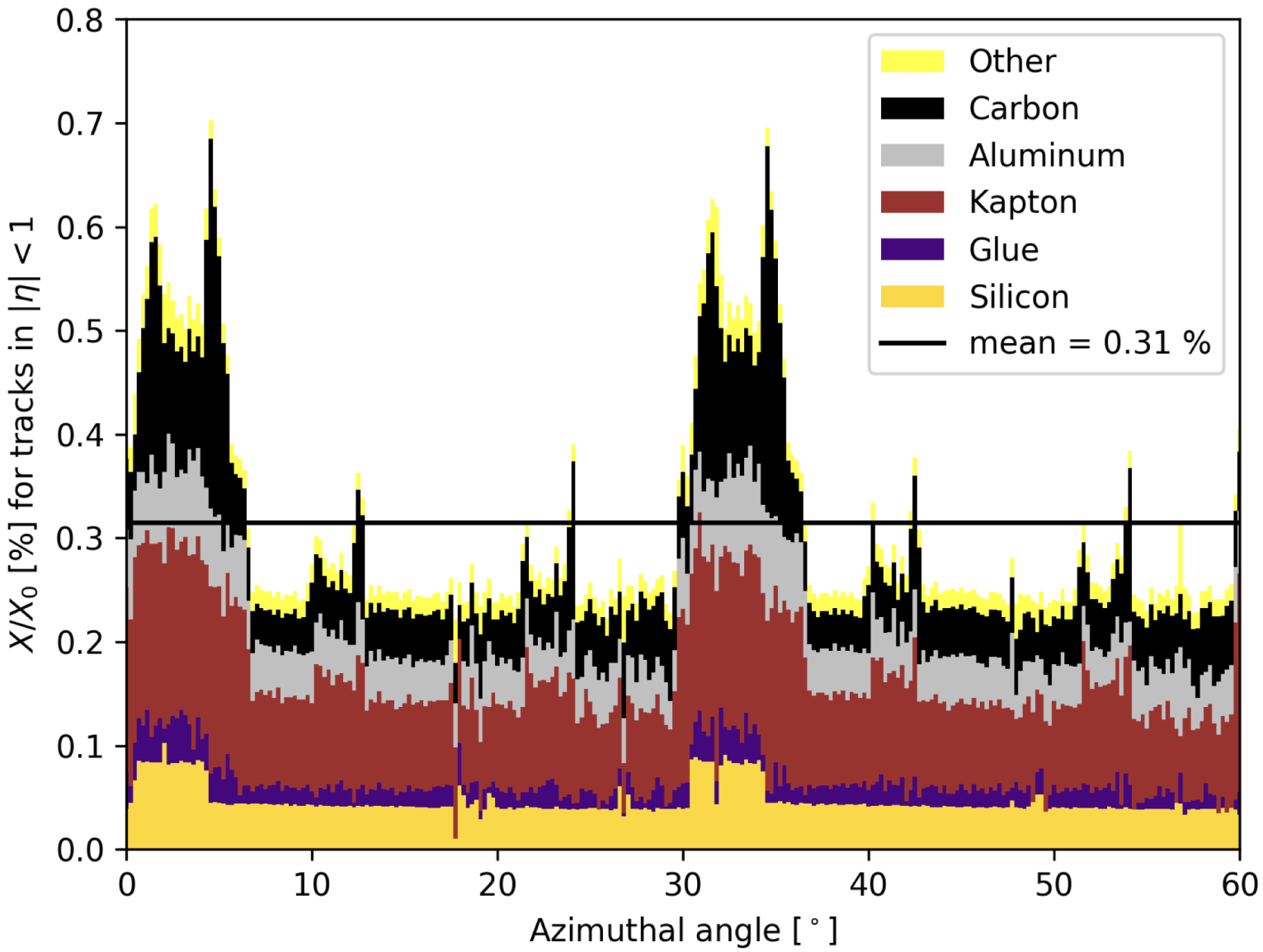
hybrid flex HDI
water cooling
CF support

Material budget ITS2



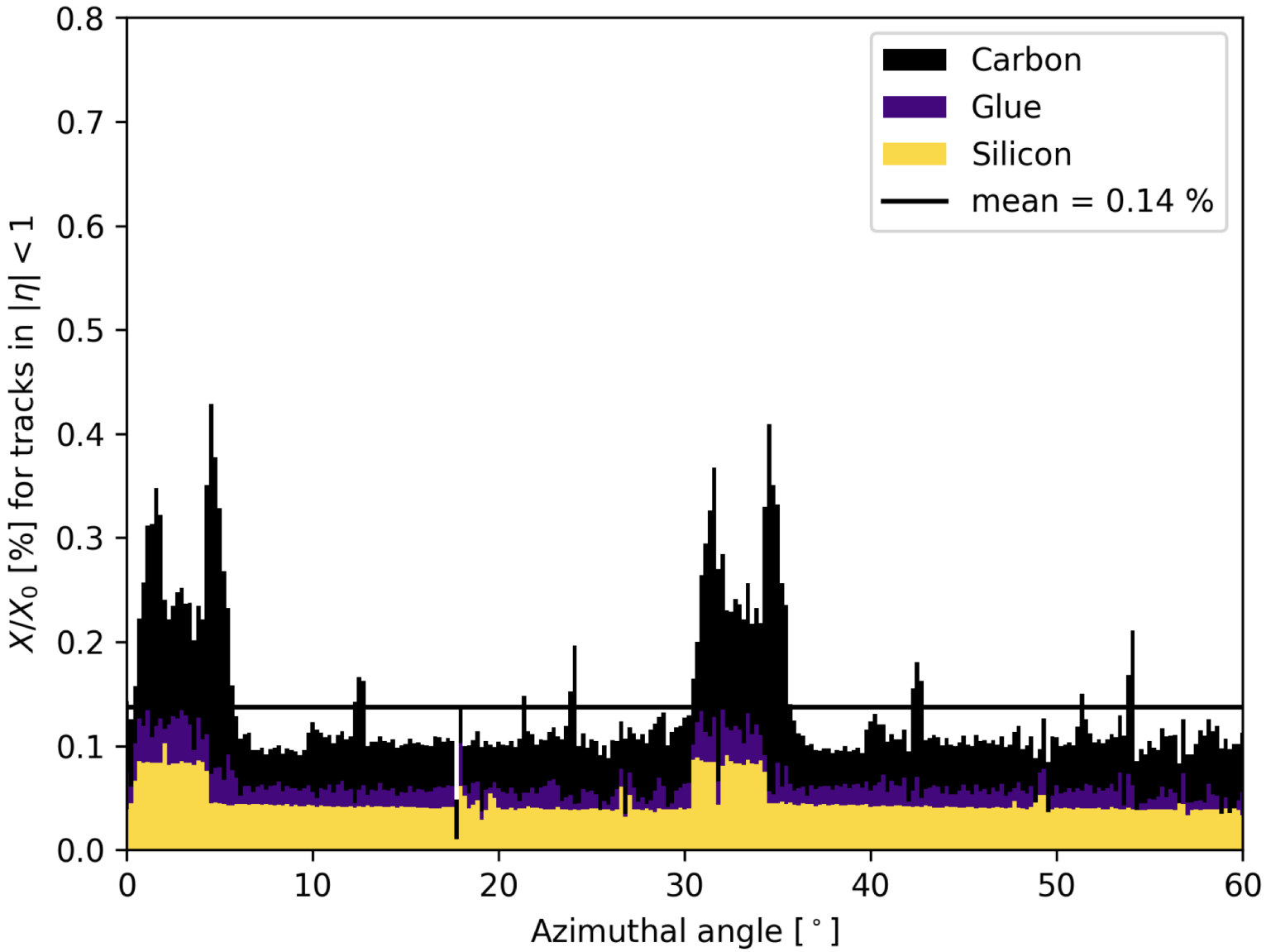
- **ITS2**
  - **0.35% X_0 per layer**
  - **Silicon contributes 15% only**
  - **Irregularities due to support/cooling**

Material budget ITS2



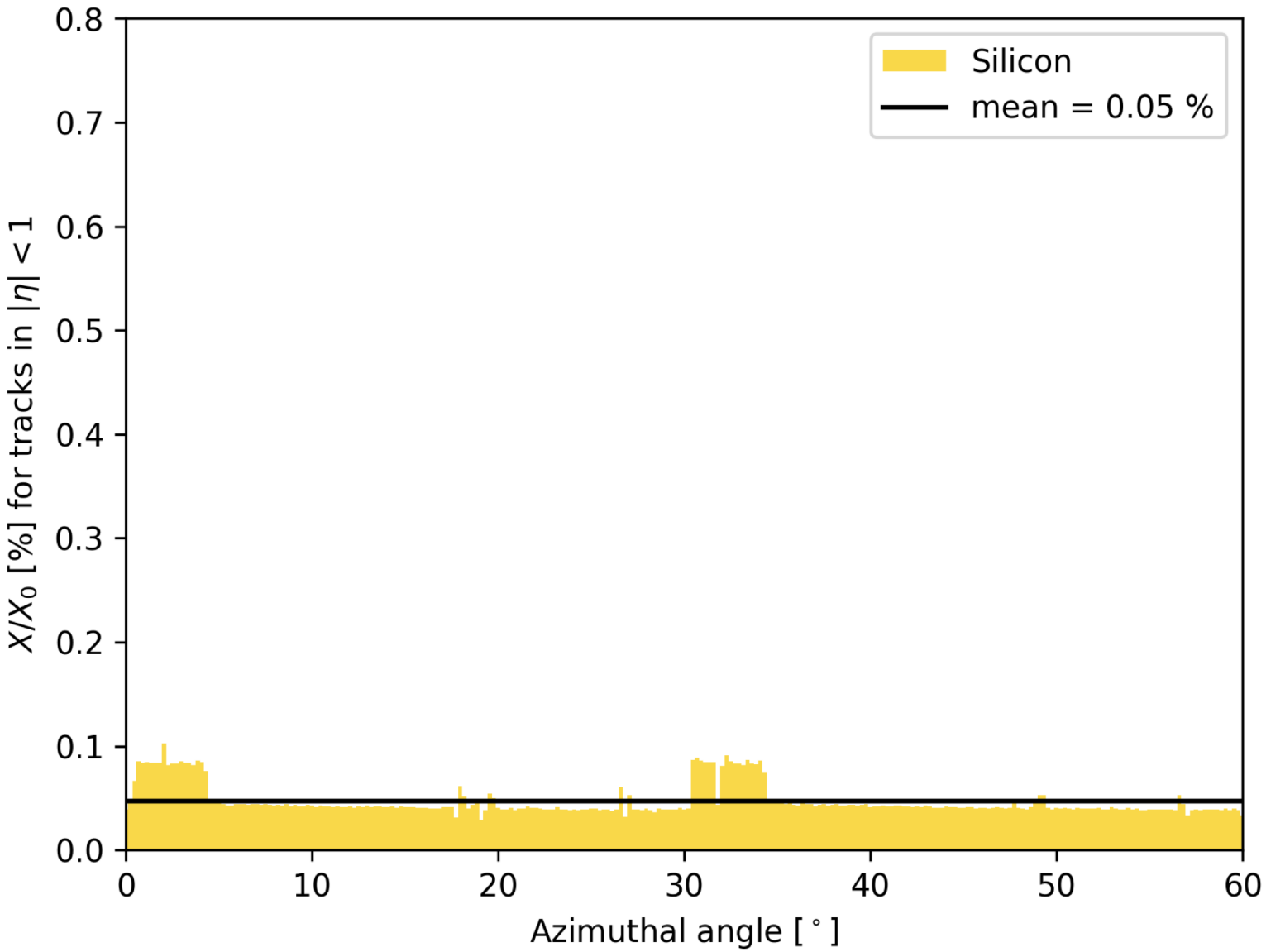
- **ITS2**
  - 0.35% X_0 per layer
  - Silicon contributes 15% only
  - Irregularities due to support/cooling
- **What if ?**
- **Water cooling is removed**
  - Air cooling
  - → 0.31% X_0 per layer

Material budget ITS2



- **ITS2**
  - 0.35% X_0 per layer
  - Silicon contributes 15% only
  - Irregularities due to support/cooling
- **What if ?**
- **Water cooling is removed**
  - Air cooling
  - → 0.31% X_0 per layer
- **Removal of the HDI hybrid flex board (power & data)**
  - If integrated on silicon ASIC
  - → 0.14% X_0 per layer

Material budget ITS2

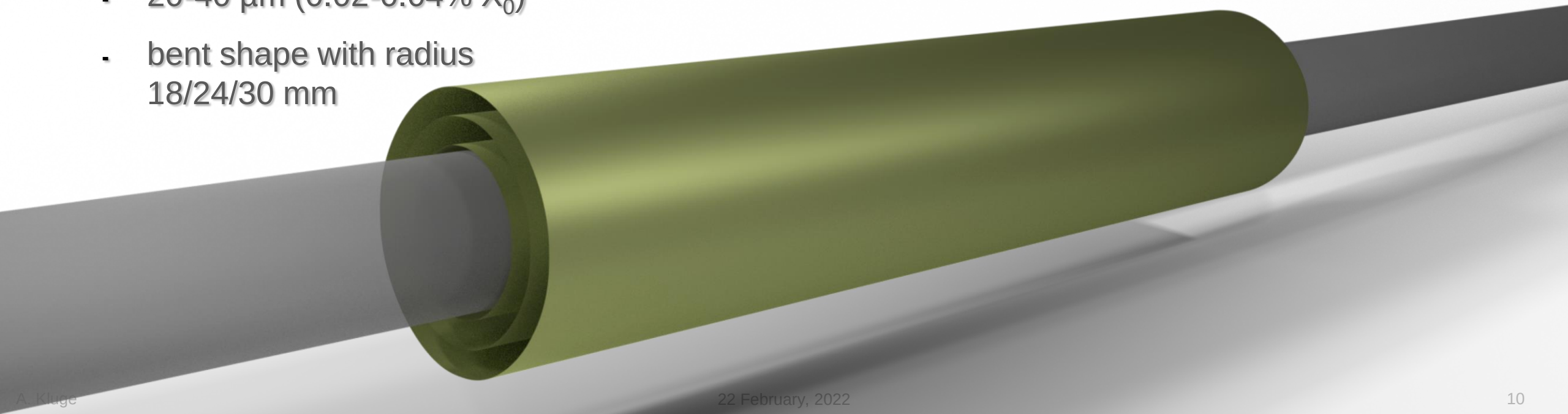


- **ITS2**
  - 0.35% X_0 per layer
  - Silicon contributes 15% only
  - Irregularities due to support/cooling
- **What if ?**
- **Water cooling is removed**
  - Air cooling
  - → 0.31% X_0 per layer
- **Removal of the HDI hybrid flex board (power & data)**
  - If integrated on silicon ASIC
  - → 0.14% X_0 per layer
- **Removal of mechanical support**
  - Stability due to bent silicon wafers
  - → 0.05% X_0 per layer

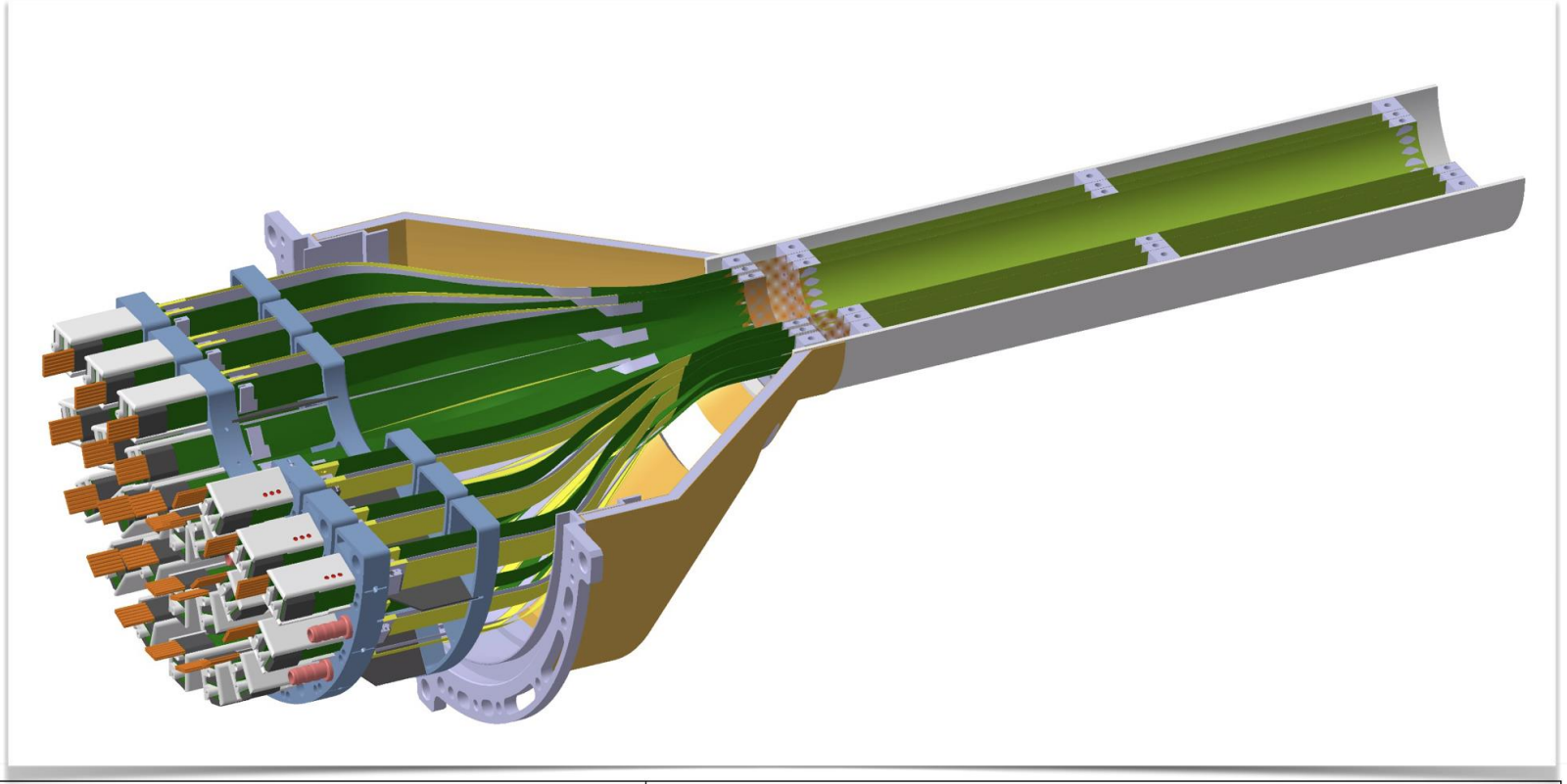
ITS3 Specifications & Layout

ITS3 specifications & layout

- **Concept**
  - **replace inner 3 layers of ITS2 with ITS3**
  - 280 mm long sensor ASICs
  - out of 300 mm long stitched wafers
  - 20-40 µm (0.02-0.04% X_0)
  - bent shape with radius 18/24/30 mm
  - carbon foam rib to hold ASICs in place
  - air cooling
  - homogenous material distribution
- **6 sensor ASICs**
  - **2 halves * 3 layers**



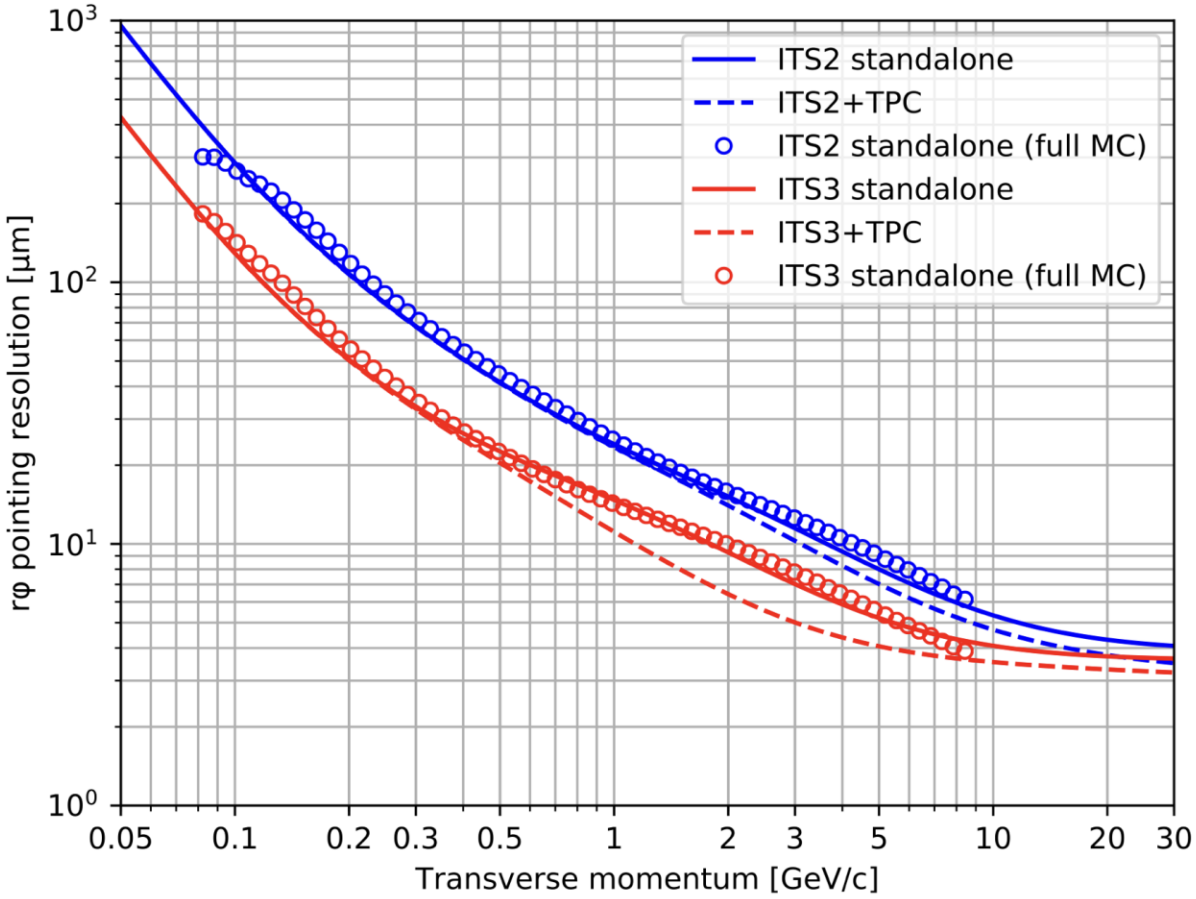
ITS3 specifications & layout



Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	280		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

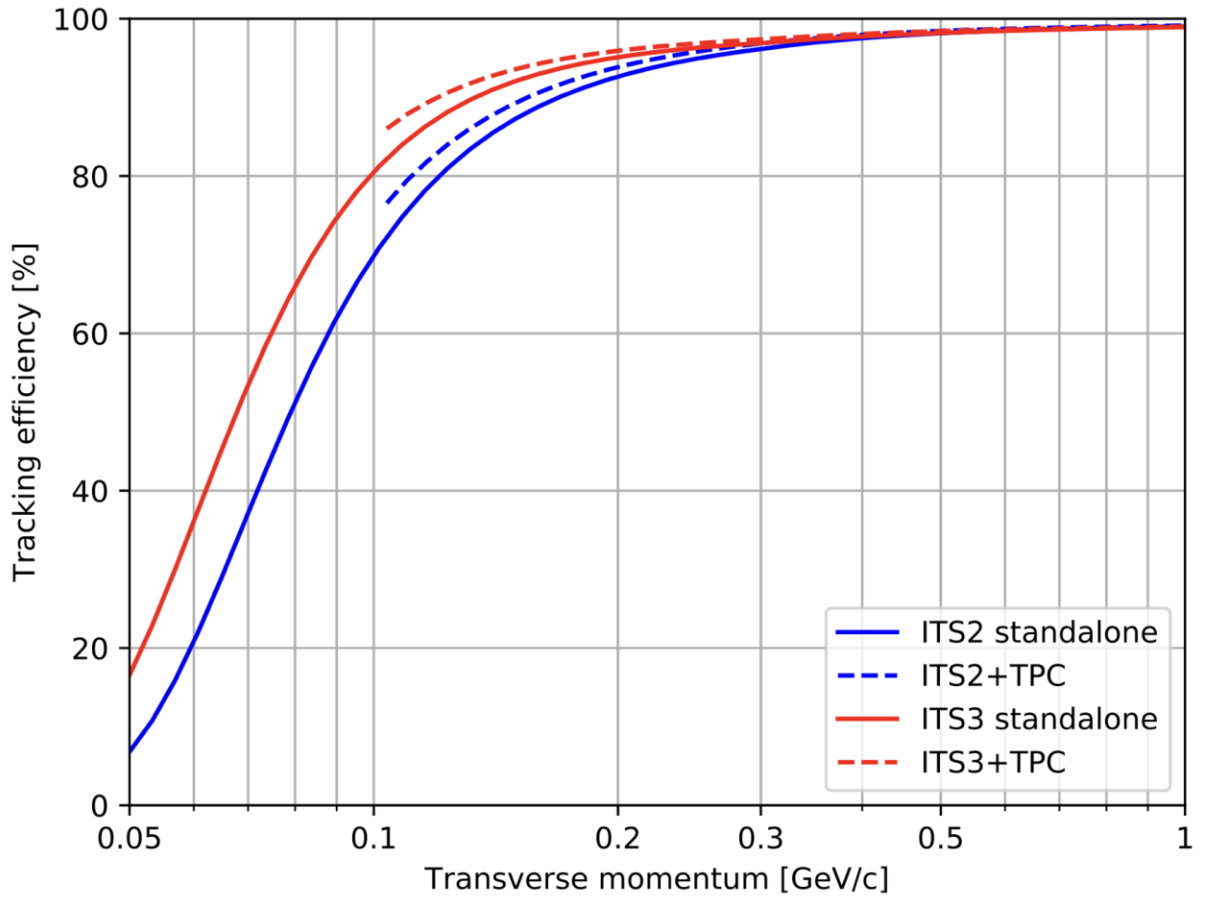
ITS3 performance

pointing resolution



improvement of factor 2 over all momenta

tracking efficiency



large improvement for low transverse momenta

Which questions need to be answered?

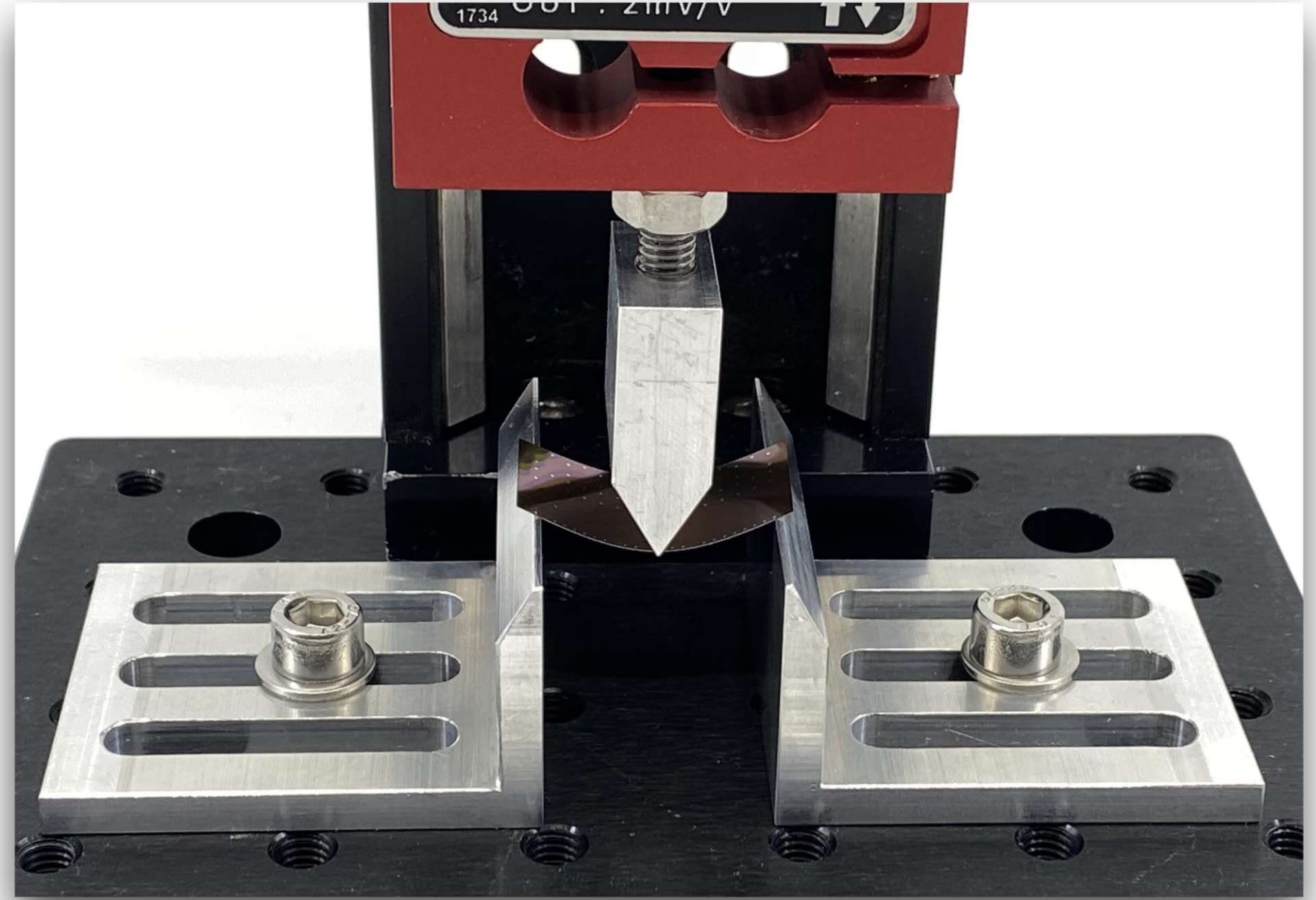
- **Idea**
  - **remove all but the silicon sensor ASIC and**
  - **bend it around beam pipe**

    for increased performance and mechanical stability
- **Questions**
  - **Can thin silicon be bent without breaking?**
  - **Are bent silicon sensor ASICs functional?**
  - **Can long, thinned silicon sensors be integrated without a heavy CF structure?**
  - **Can the sensor be cooled with air only efficiently?**
  - **Can a 280 mm long silicon sensor ASIC be produced?**
  - **Can the sensors be connected without additional HDI?**

Bent sensor ASICs (ALPIDE)

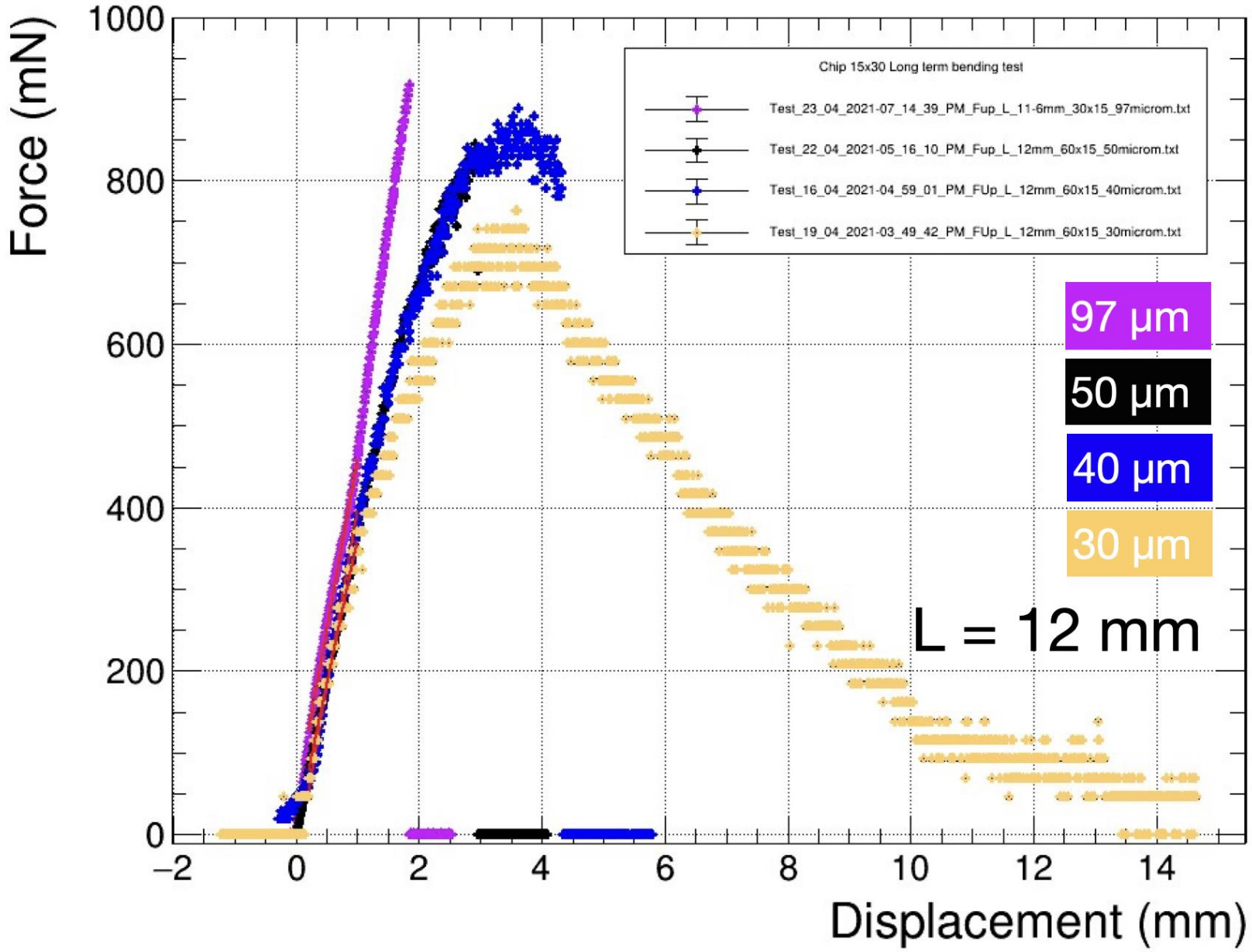
Can thin silicon be bent without breaking?

Bending

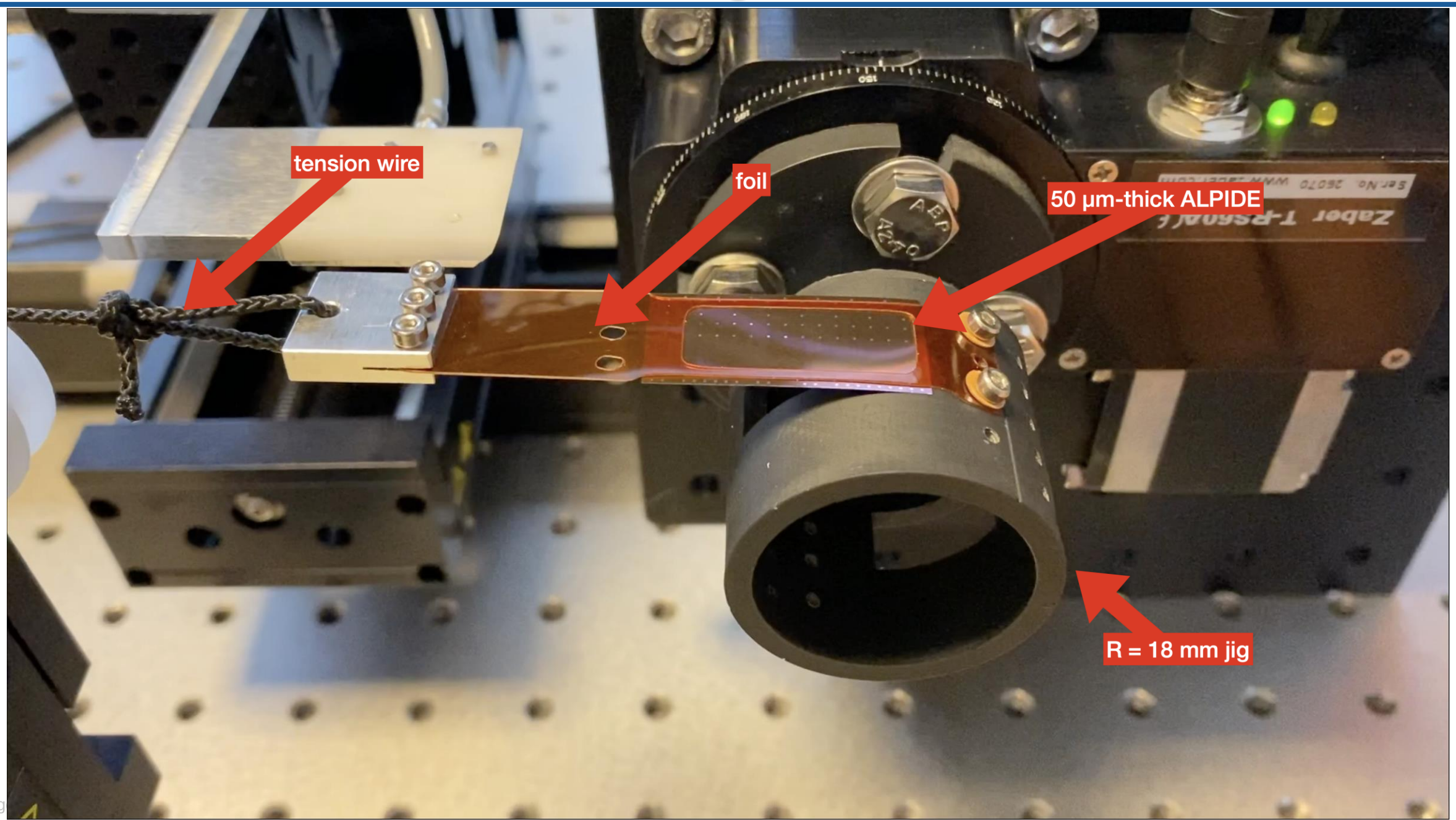


Bending

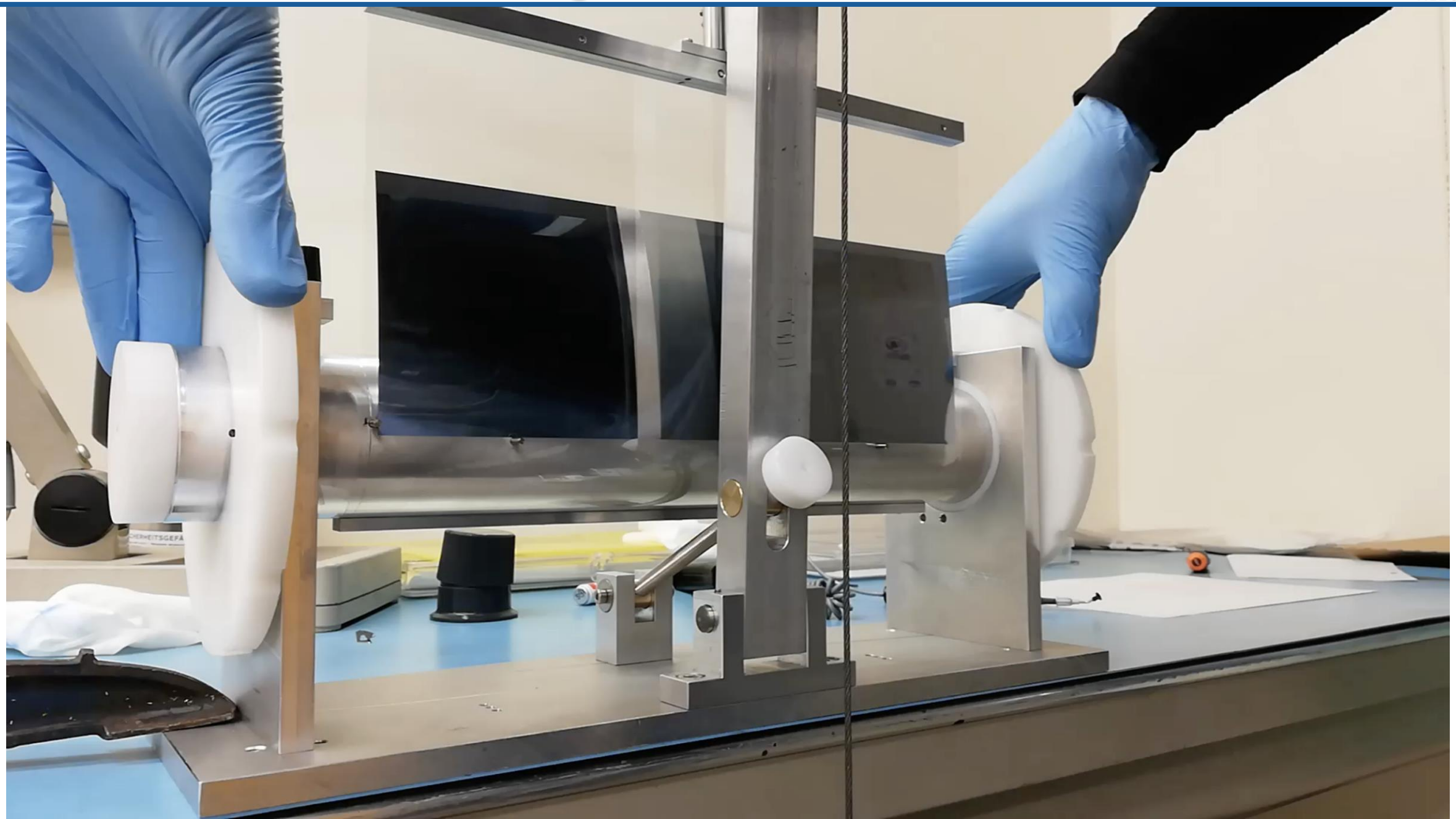
- Thin wafers are very flexible
- ITS3 target radius and thickness very feasible



Bending ALPIDE



Bending wafer scale silicon

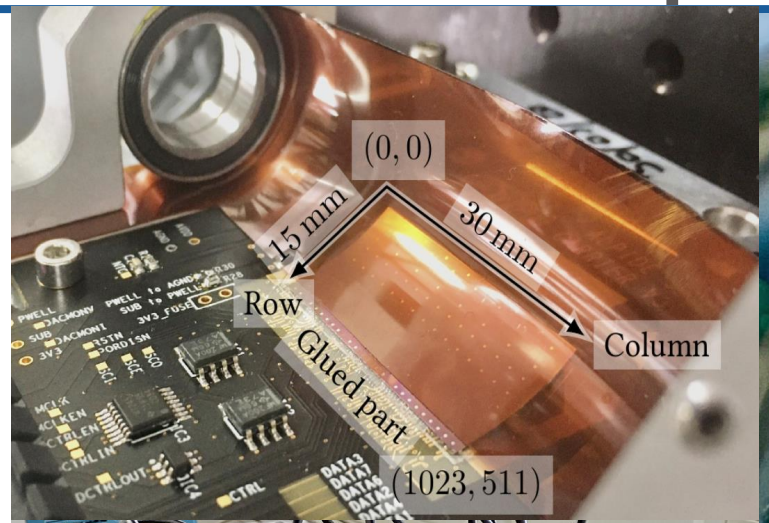


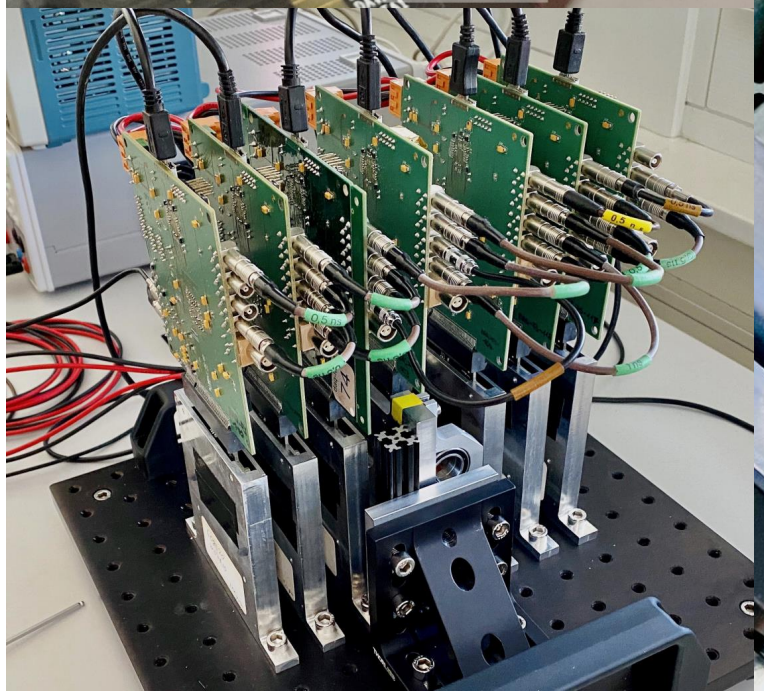
Bent sensor ASICs (ALPIDE) in beam test

Are bent silicon sensor ASIC functional?

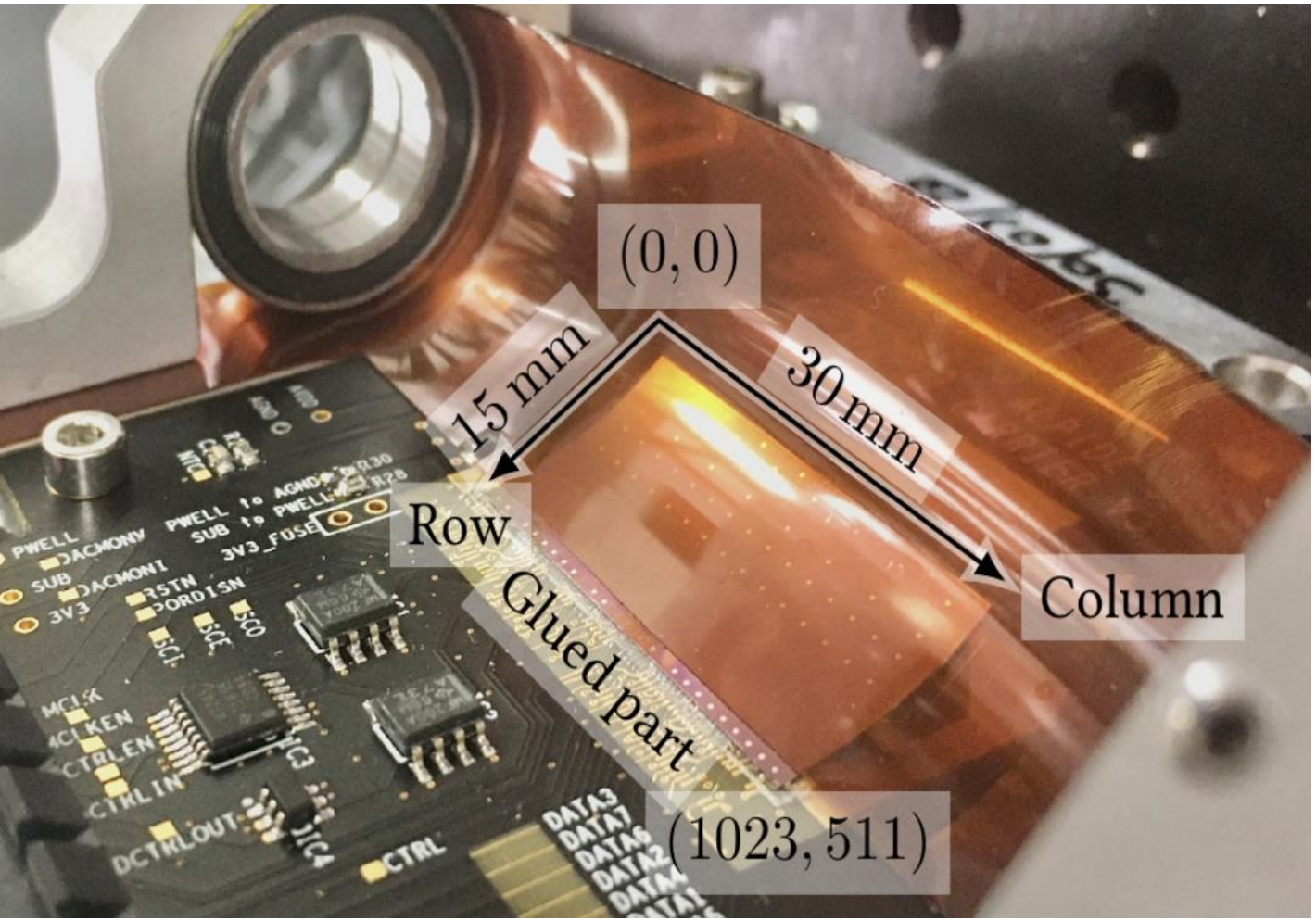
Beam test campaigns

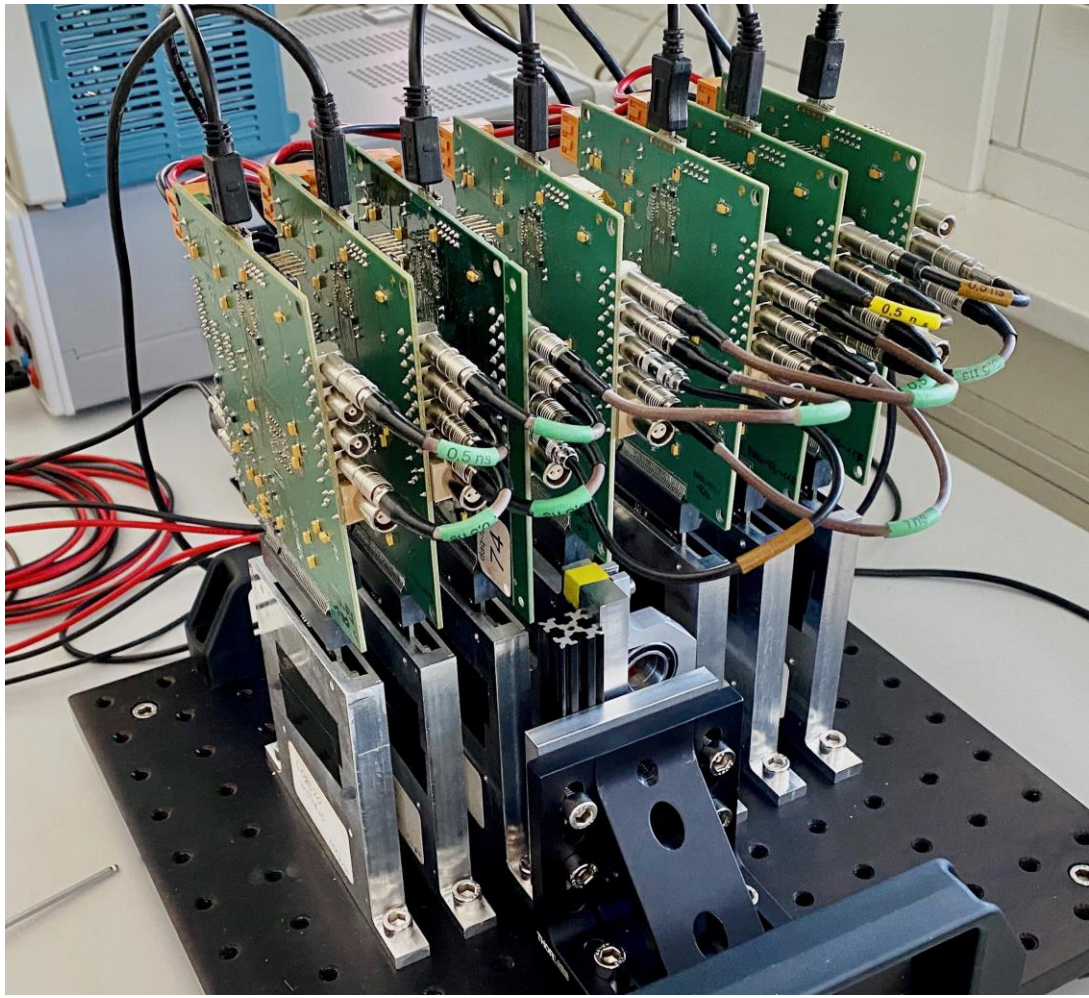
- June 2020 (DESY): first bent chip
- Aug 2020 (DESY): bent chip on cylinder
- Dec 2020 (DESY): bent chip at large radii
- Apr 2021 (DESY): bent chips at all radii, carbon foam
- July 2021 (SPS): µITS3, “₩”
- Sep 2021 (DESY): MLR1, “₩”, carbon foam





Beam test: June 2020 (DESY) one bent ALPIDE





Beam test: June 2020 (DESY) one bent ALPIDE

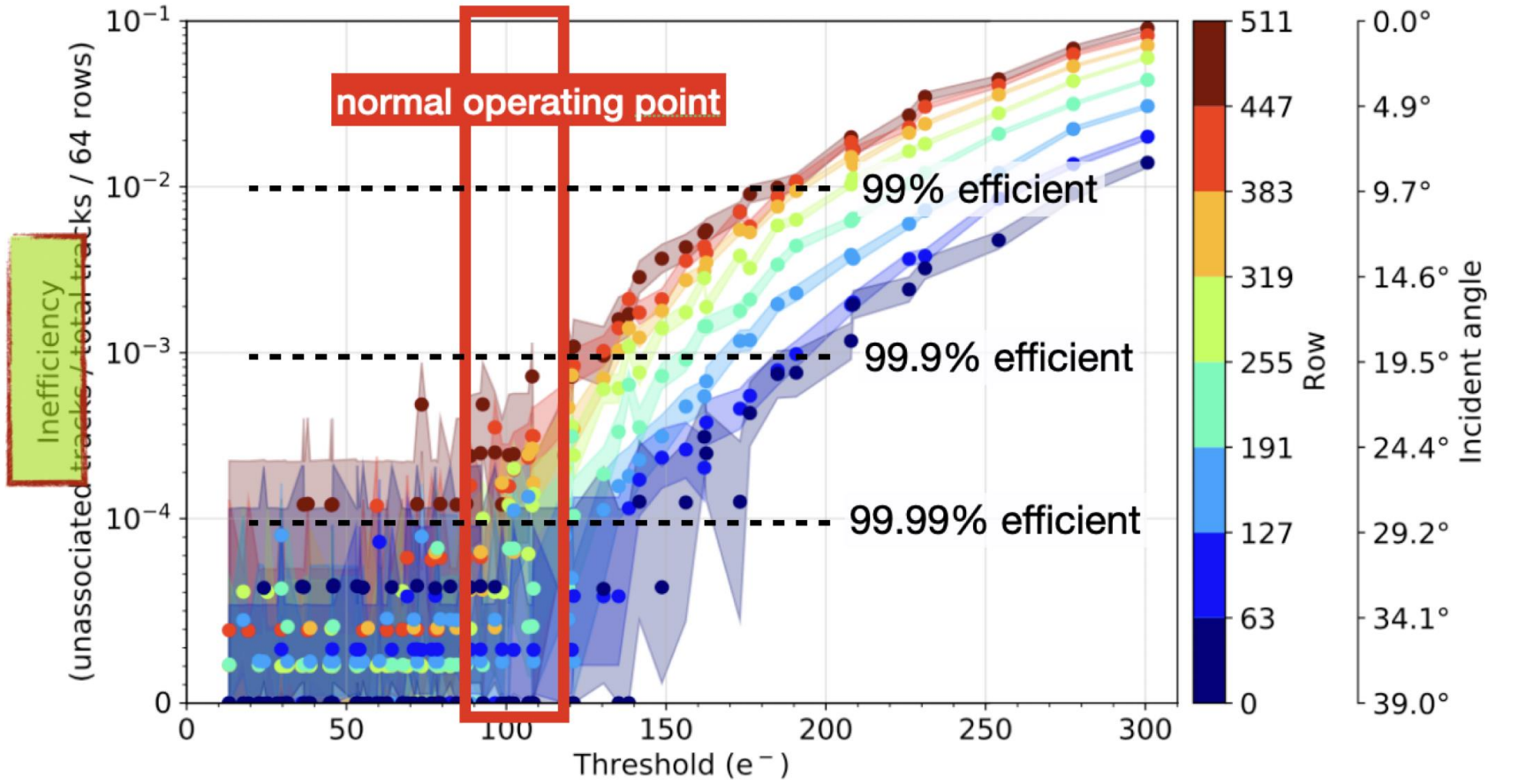
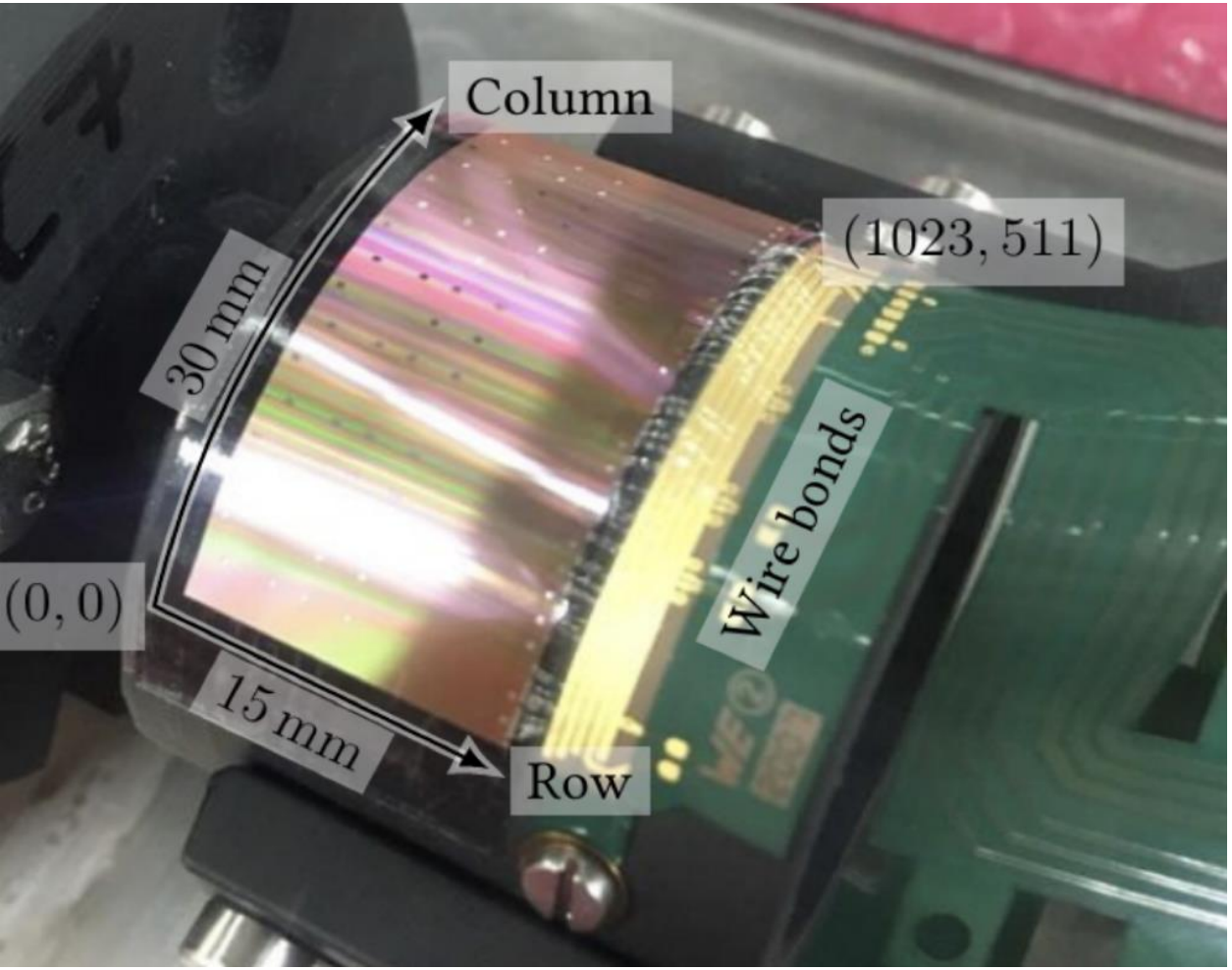


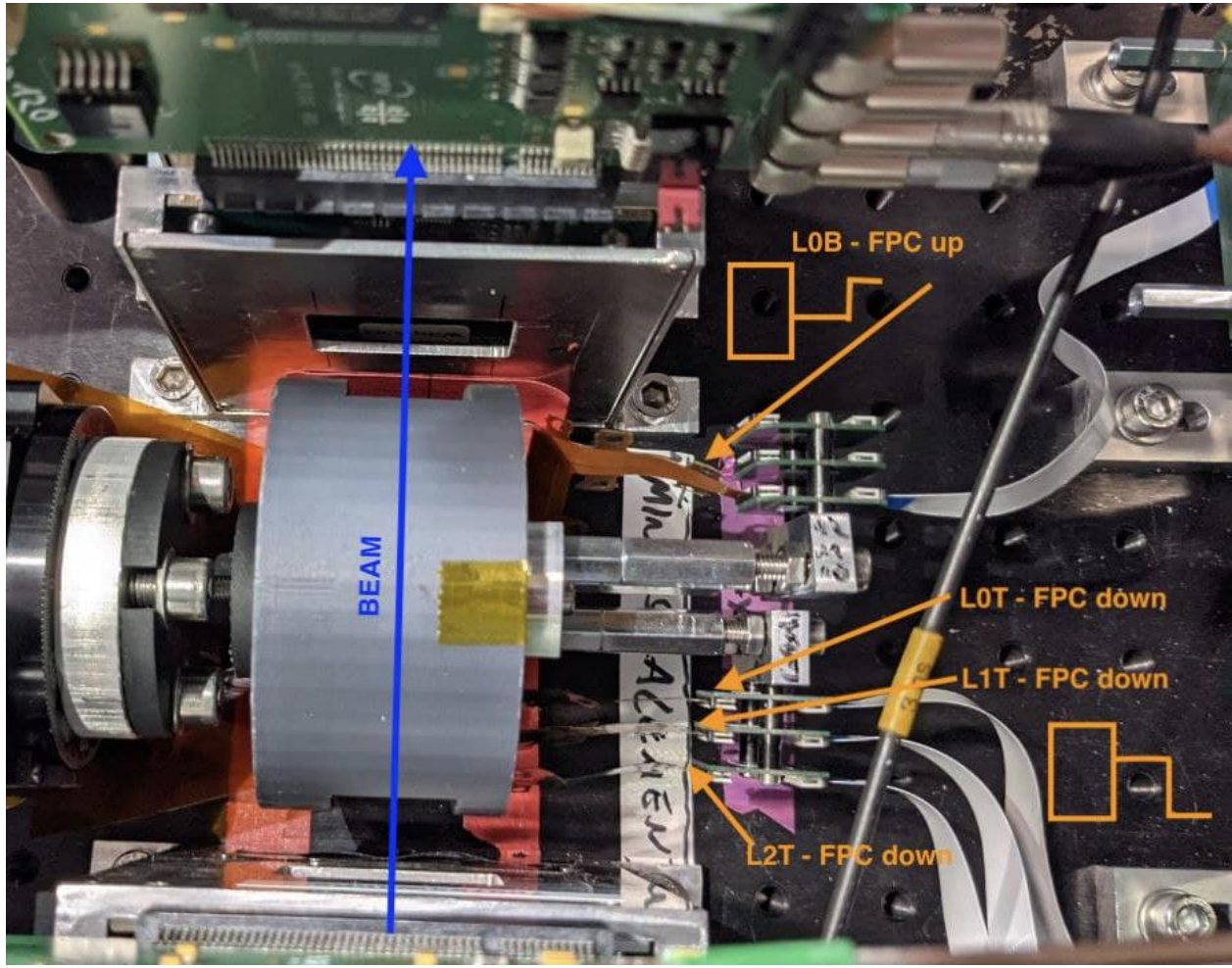
Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

With increasing row number, beam incident angle decreases, thus decreasing particle path in active volume and deposited charge, resulting in smaller clusters

1st paper: https://doi.org/10.1016/j.nima.2021.166280

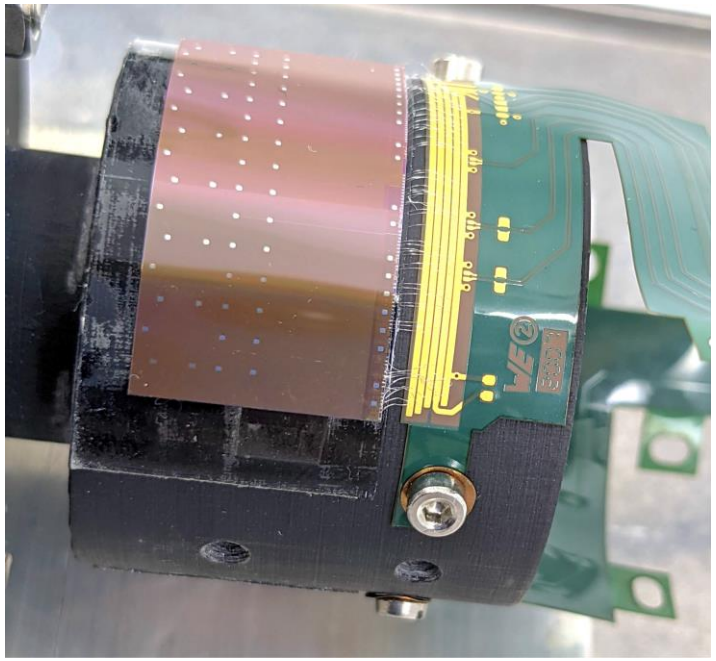
Beam test: Aug 20 - April 21 (DESY) bent ALPIDEs on cylinder

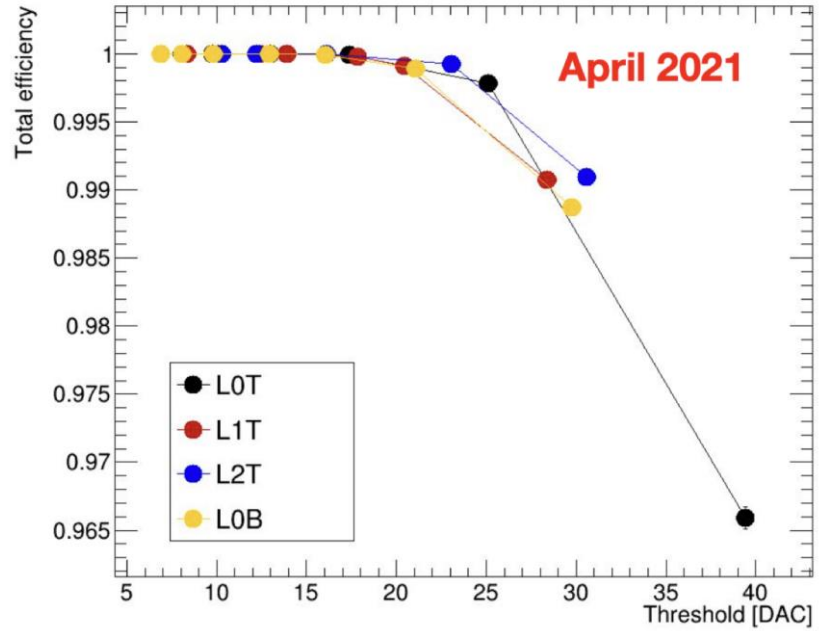


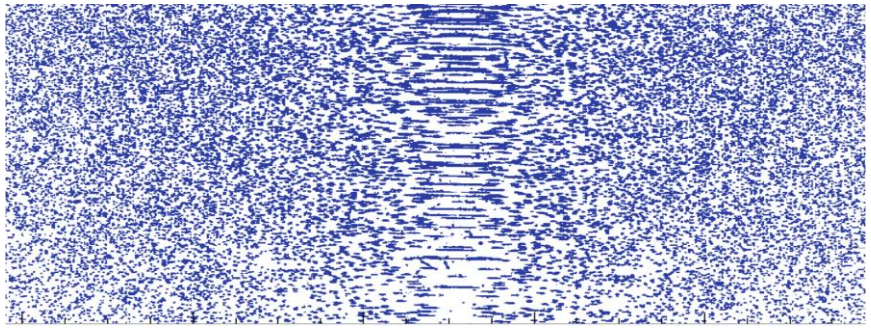


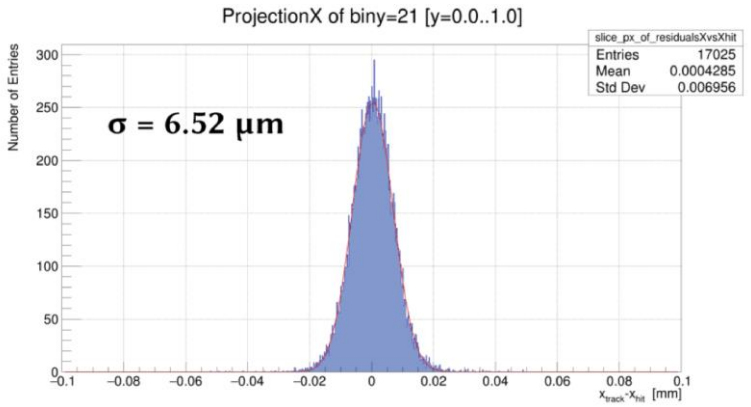
Beam tests: efficiencies and spatial resolutions at different radii

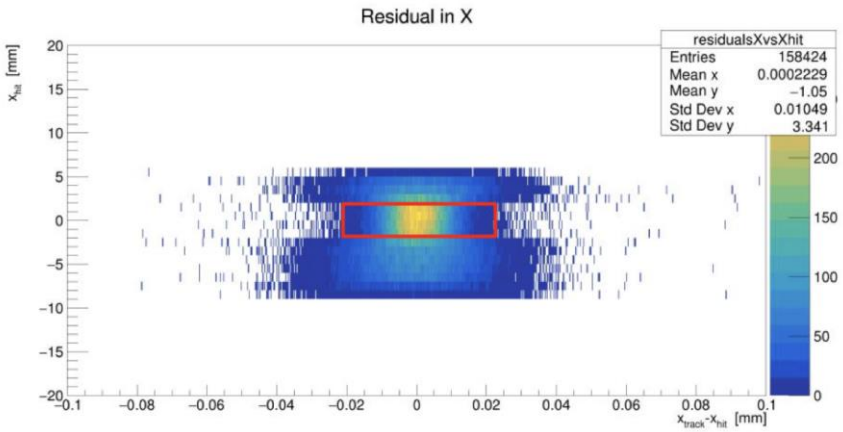
- no effect depending on the radius observed
- Results also match results where the chip was bent along the other direction



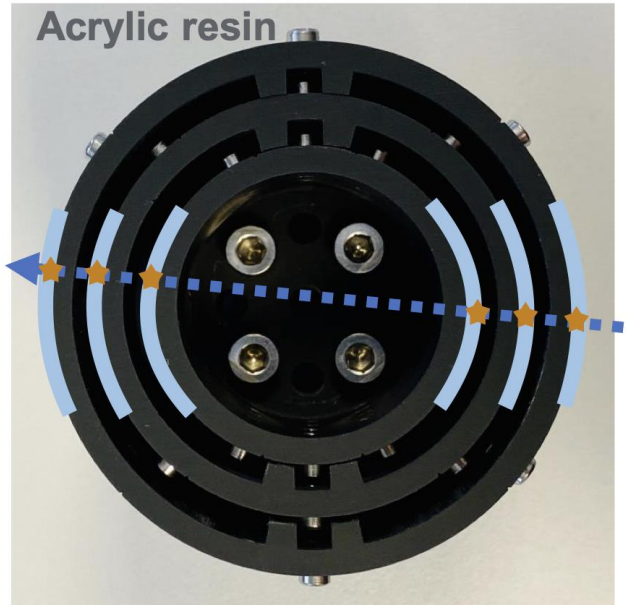


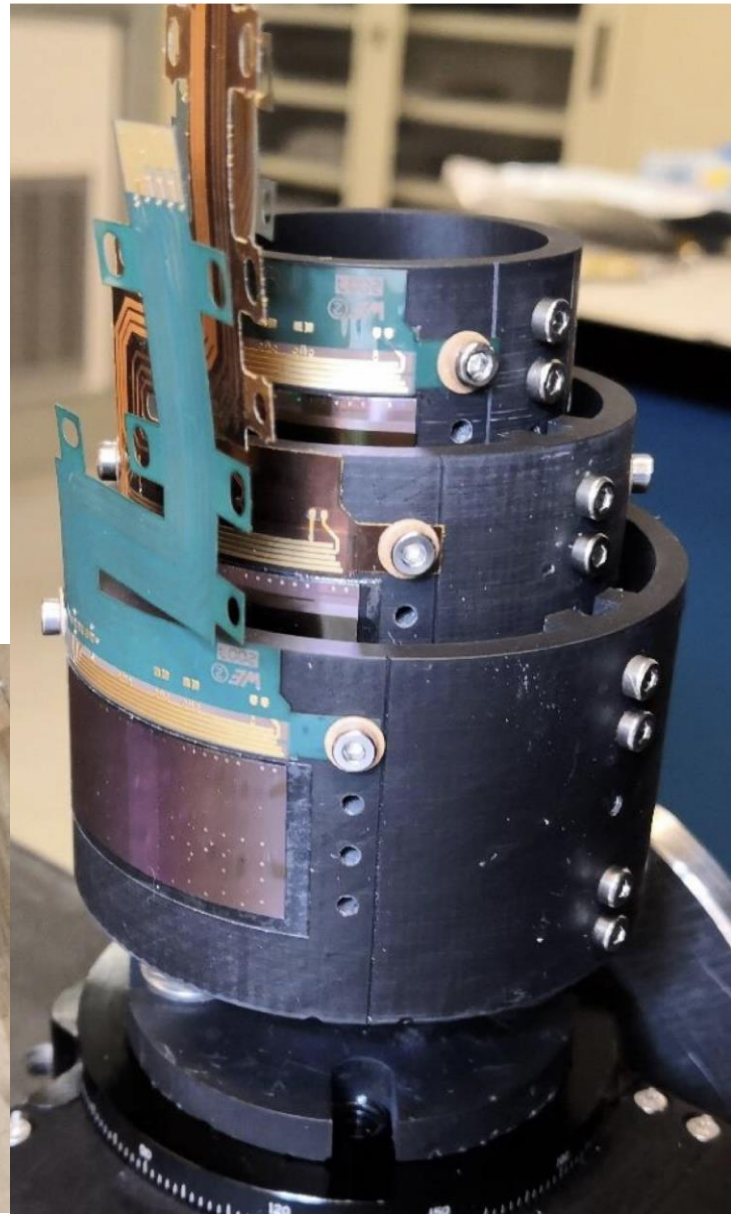






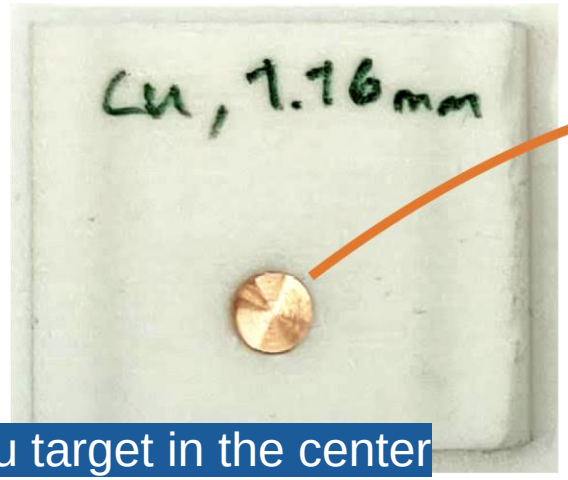
µITS3

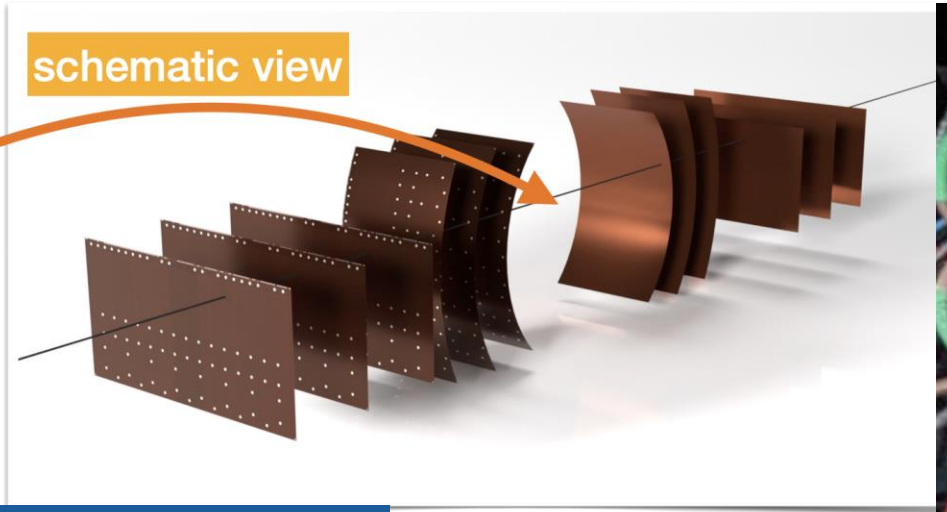




- **µITS3 - mock-up of final ITS3**
  - **6 ALPIDE (ITS2)**
  - bent to ITS3 target radi
  - experience with handling thin silicon was gained
  - **different connection schemes exercised**
  - wire bonding before bending
  - wire bonding after bending (base line)
  - SpTAB bonding

µITS3

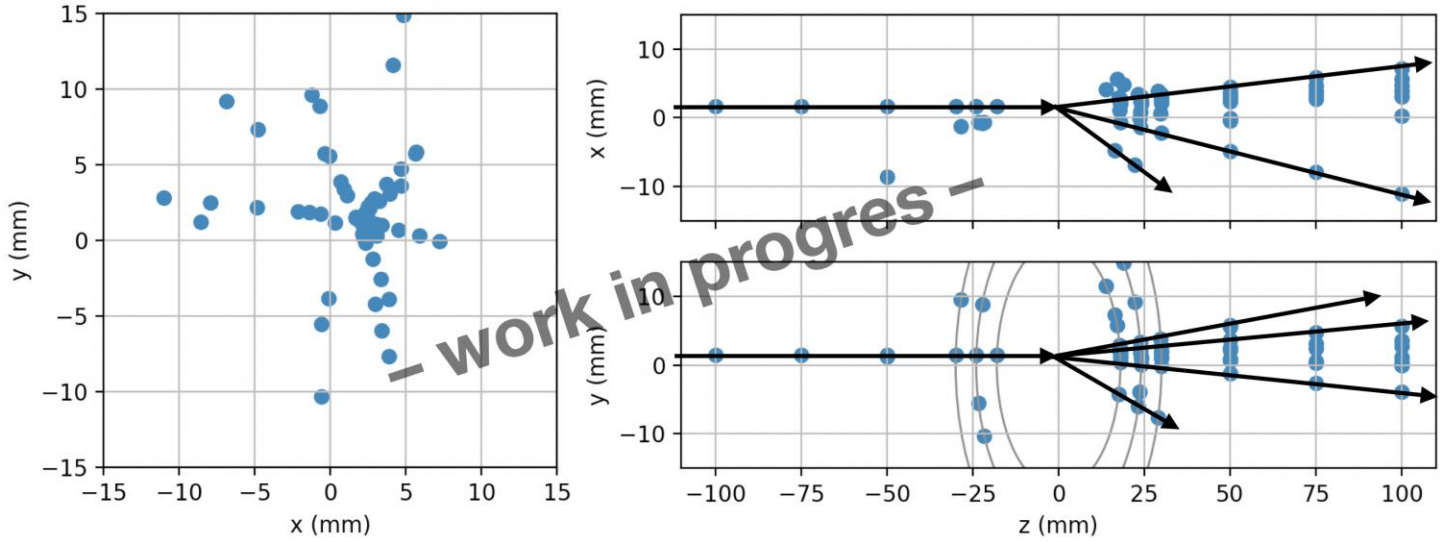




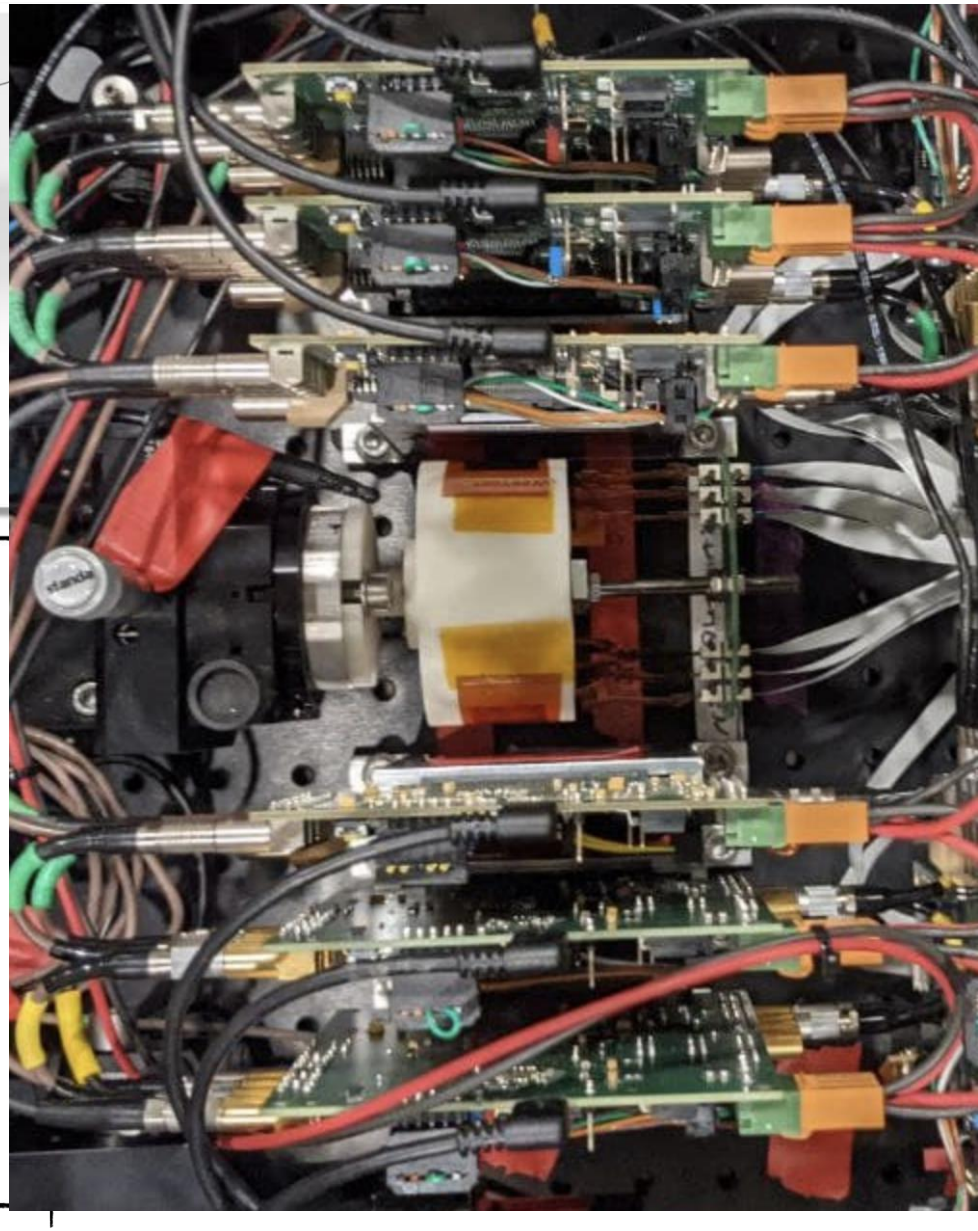
Cu target in the center

expect to see 120 GeV proton/pion–Cu collisions

Example event

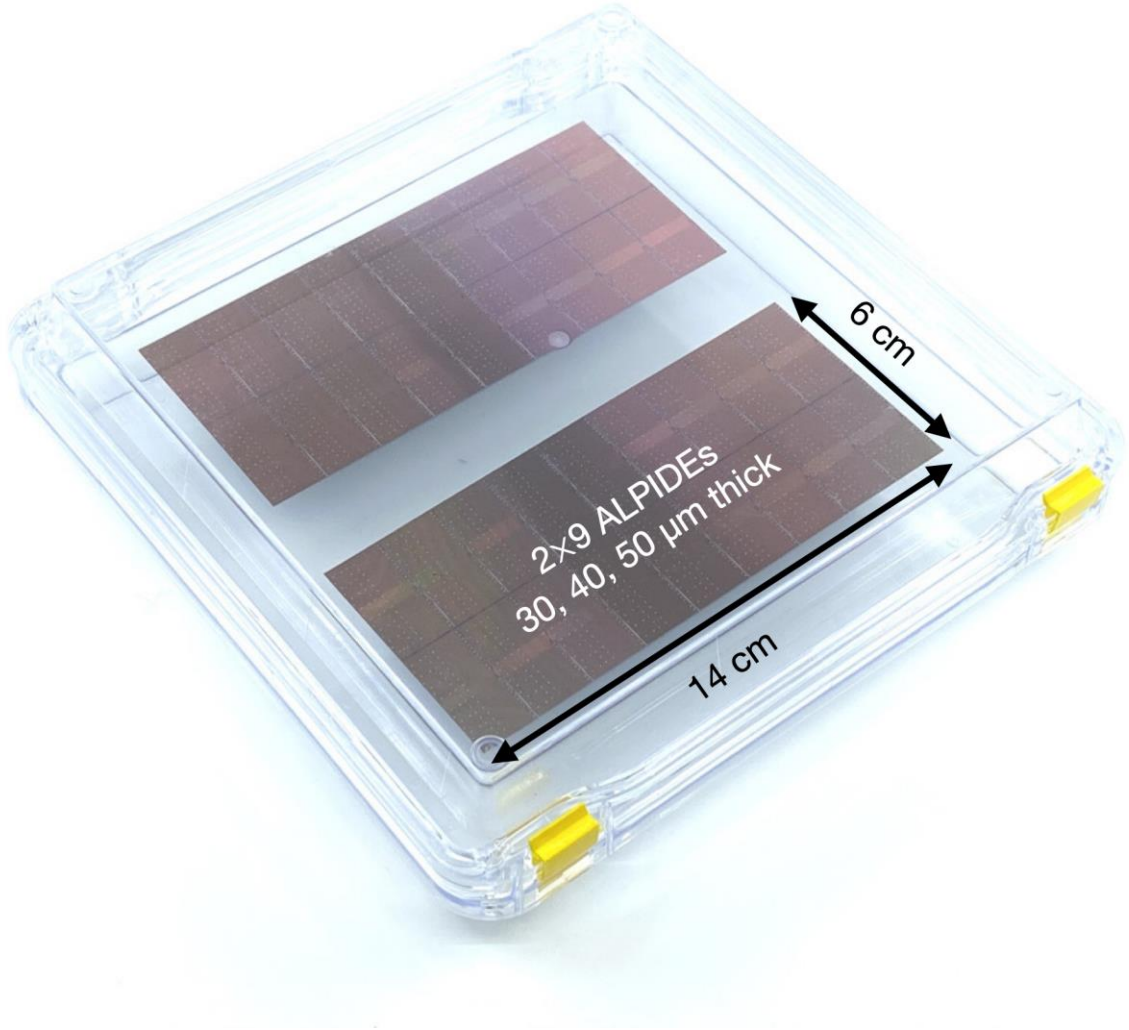


[few hand-drawn track lines to guide the eye]

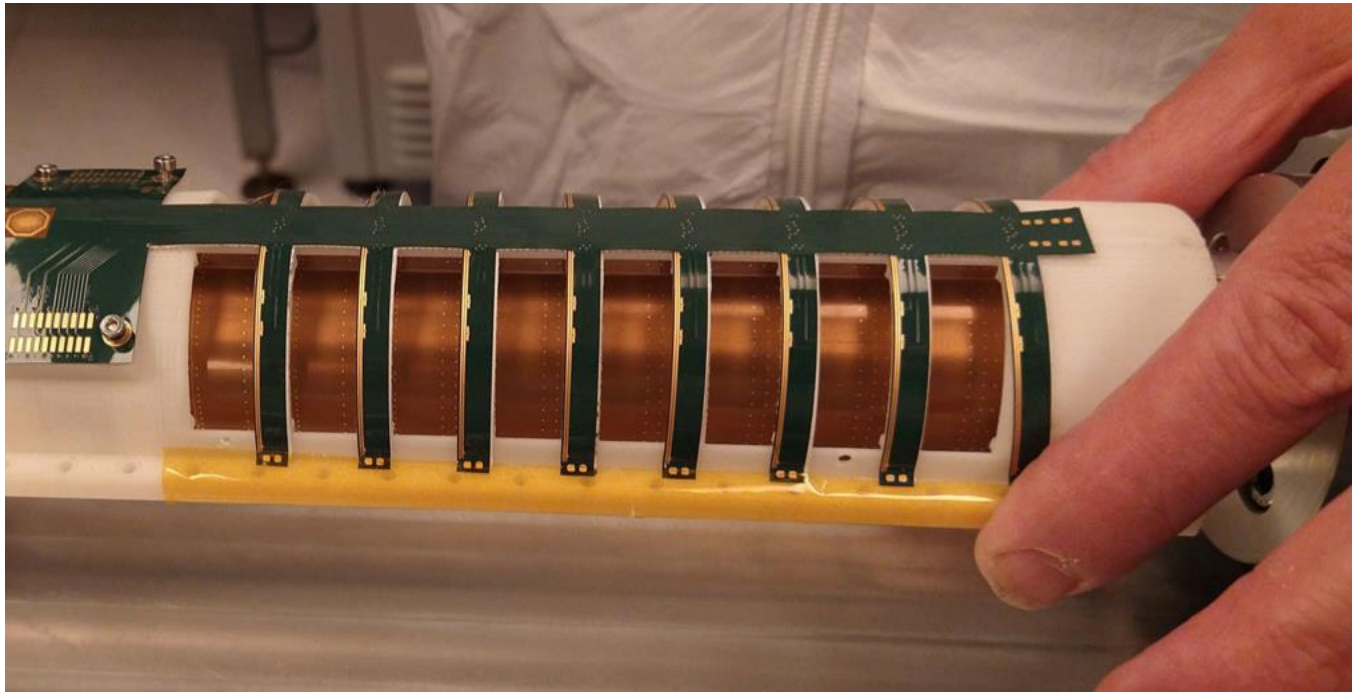


ITS3 bending and interconnection studies

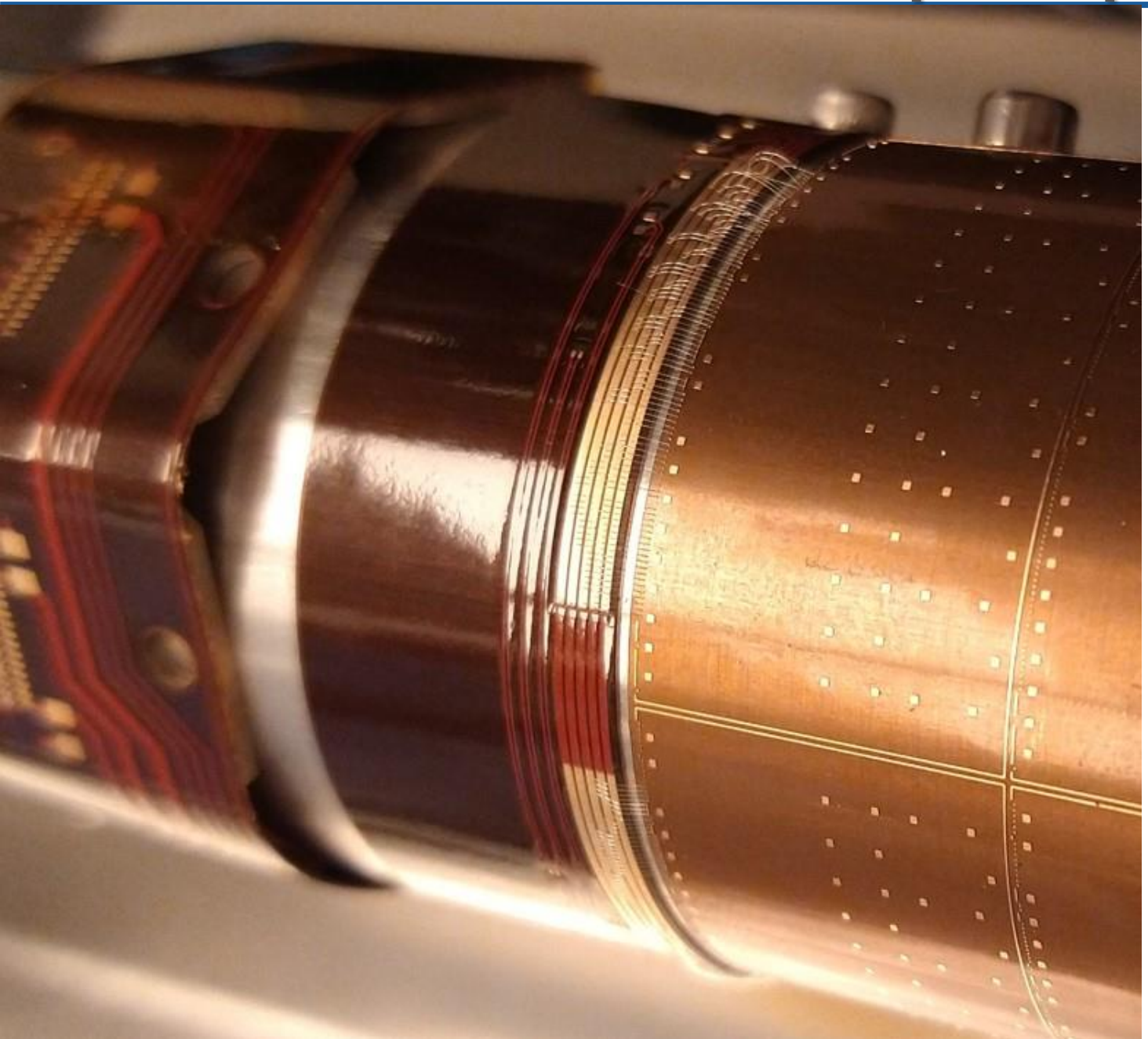
Super-Alpide



- **study bending and interconnection of large pieces of processed chips**
  - **1 silicon piece cut from one ALPIDE wafer (9x2 dies, ~1/2 of layer 0)**



Super-Alpide



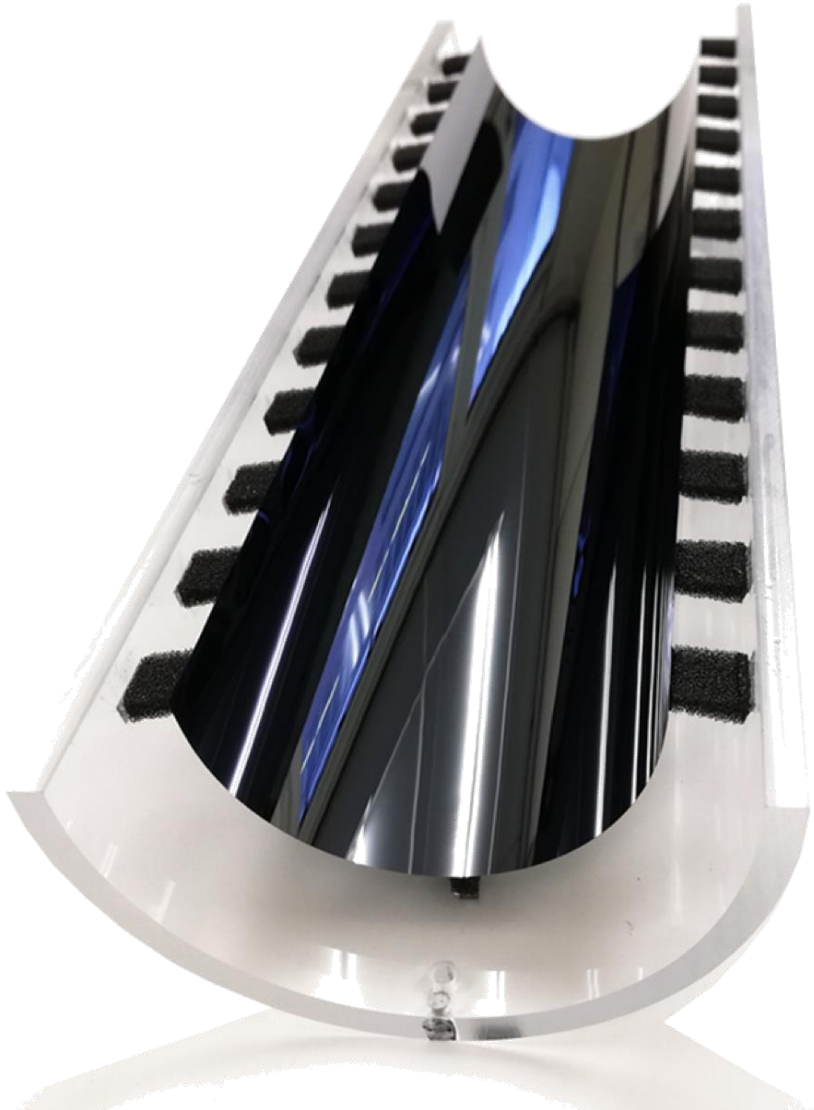
- interconnection prototype on a bent large area (mock-up) sensor

ITS3 integration and cooling studies

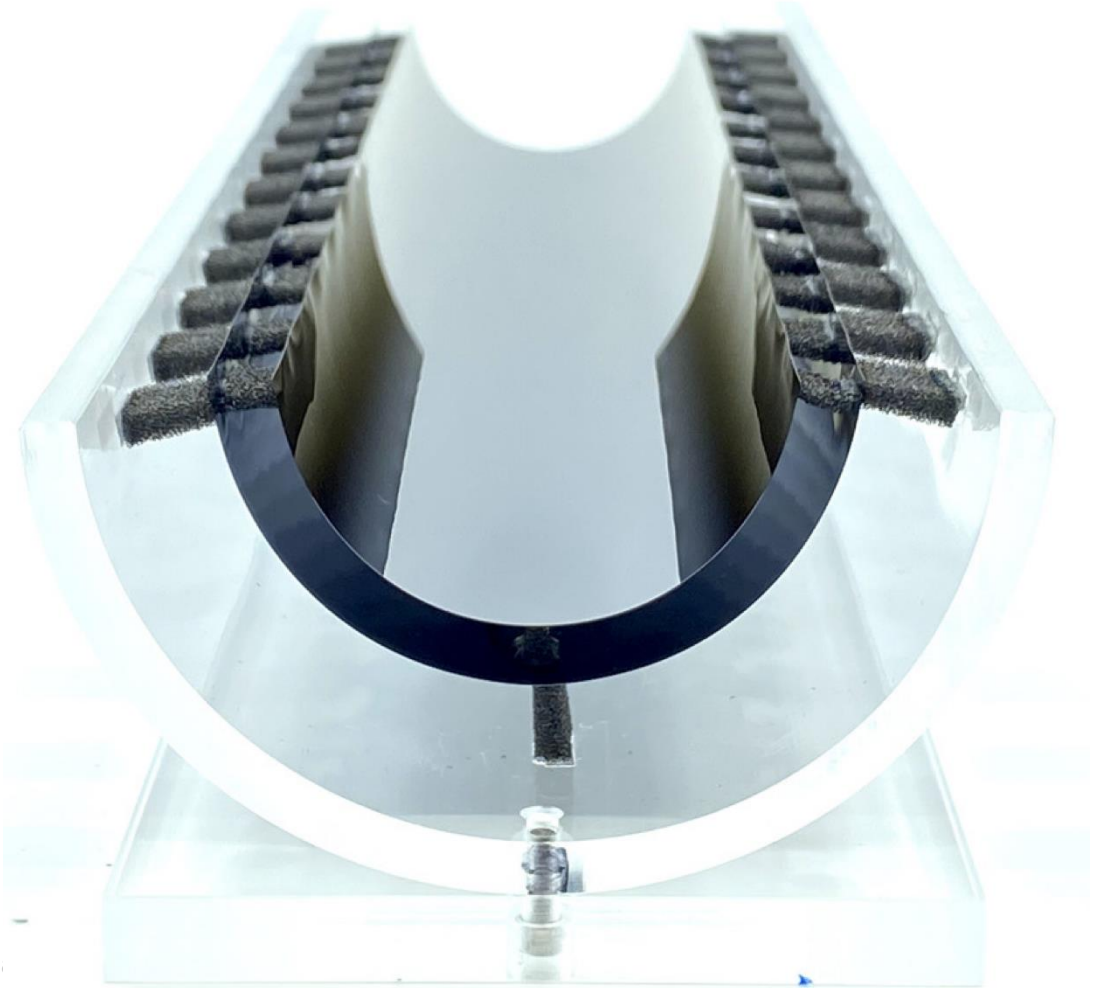
Can long, thinned silicon sensors be integrated without a heavy CF structure?
Can the sensor be cooled with air only efficiently?

Integration

Layer 2

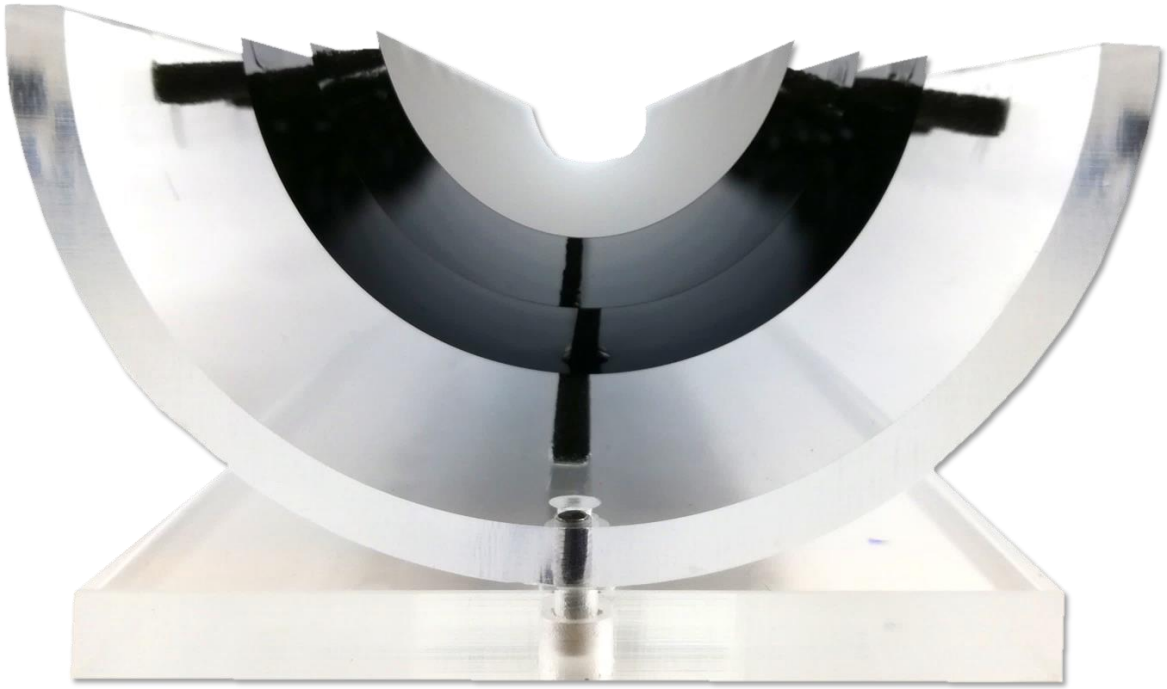


Layers 2+1

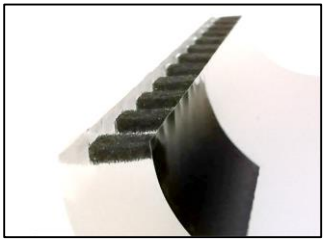


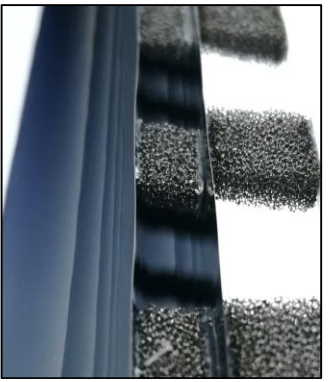
Integration

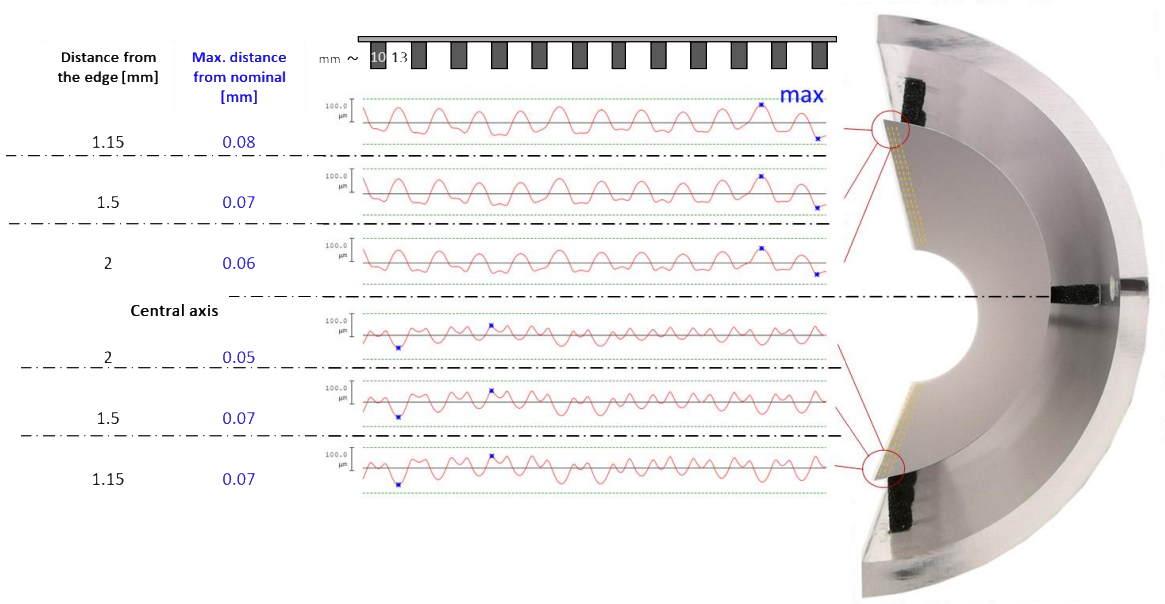
Layers 2+1+0



X-ray tomography



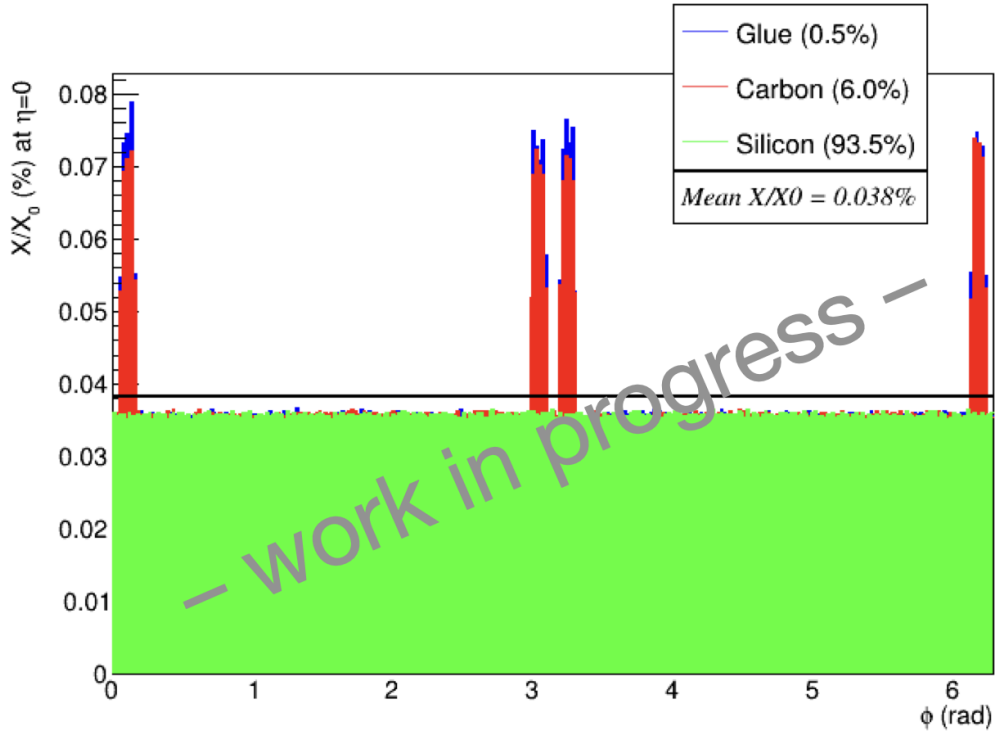




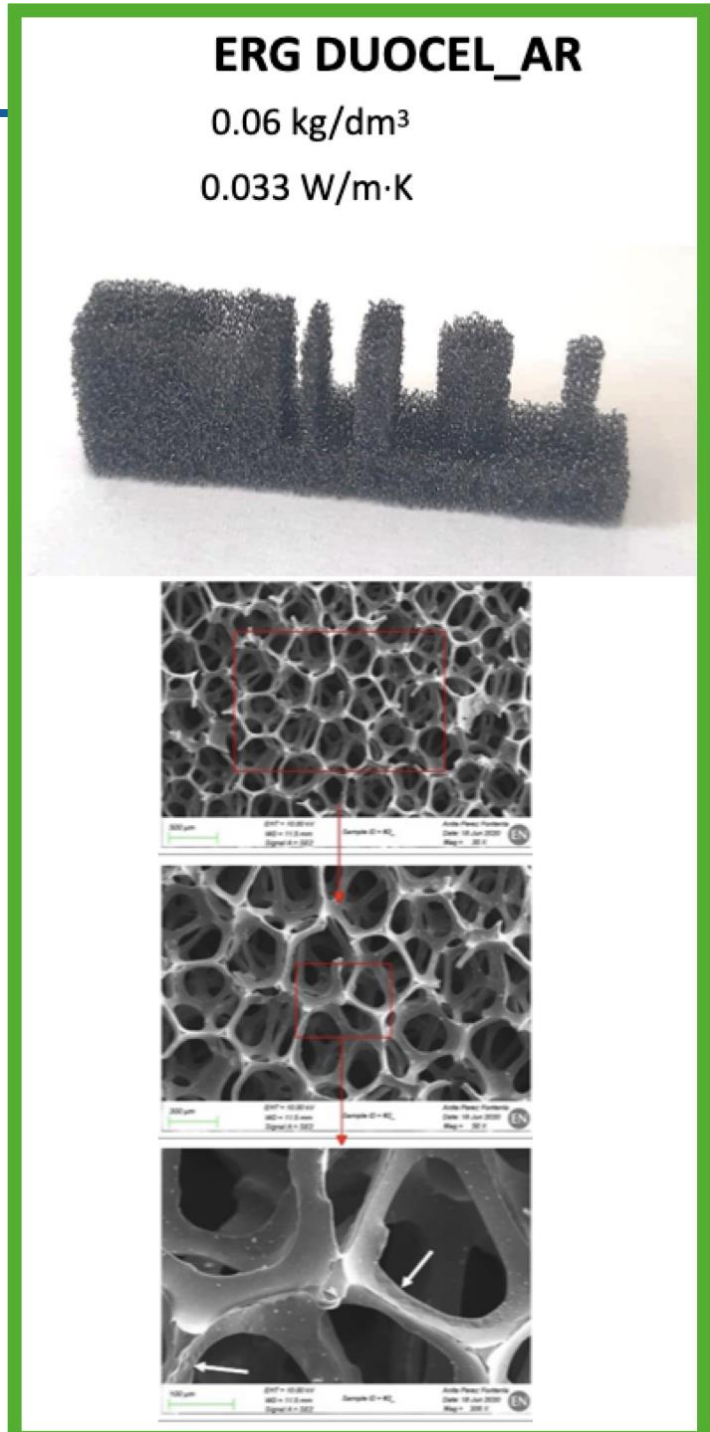
Tomography VS CAD model

- **Detailed analysis of the impact of the carbon foam support wedges**
  - **local deformations of <100 µm**
- **3D X-ray of the full assembly has very good agreement with CAD model**

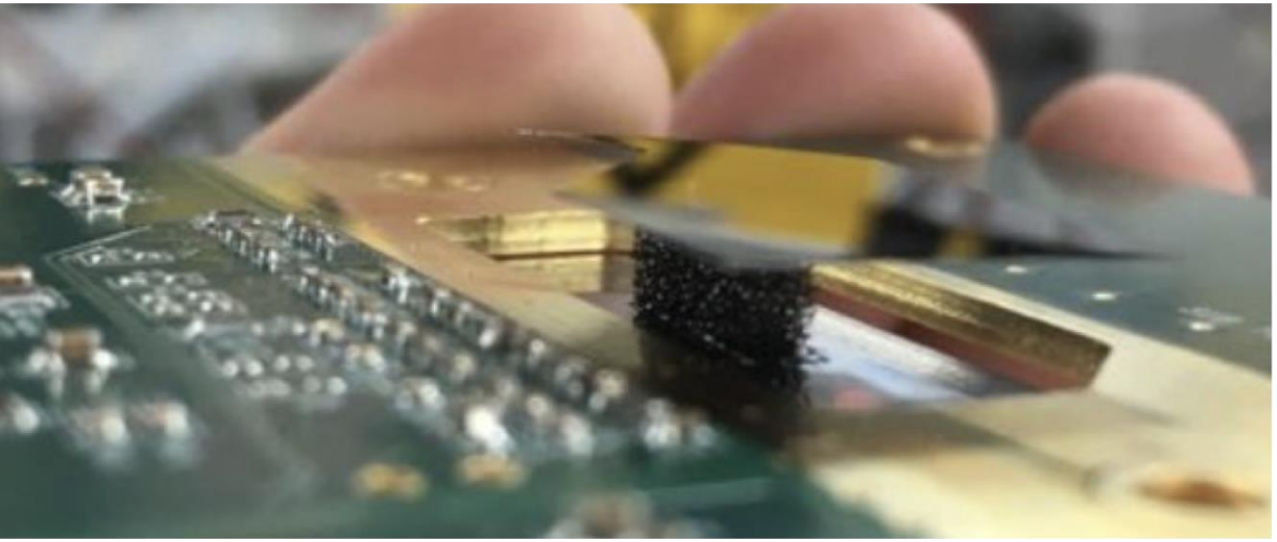
Carbon fiber foam

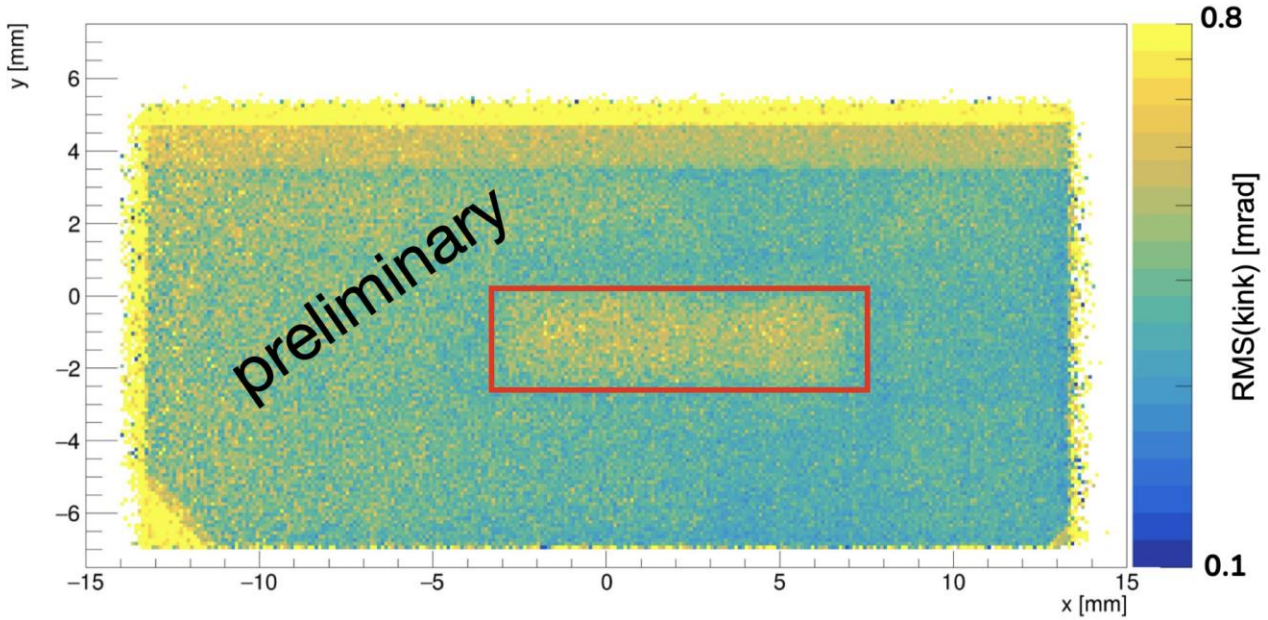


- **Different foams were characterised for machinability and thermal properties**
- **Baseline ERG DUOCEL_AR**
  - features largest radiation length



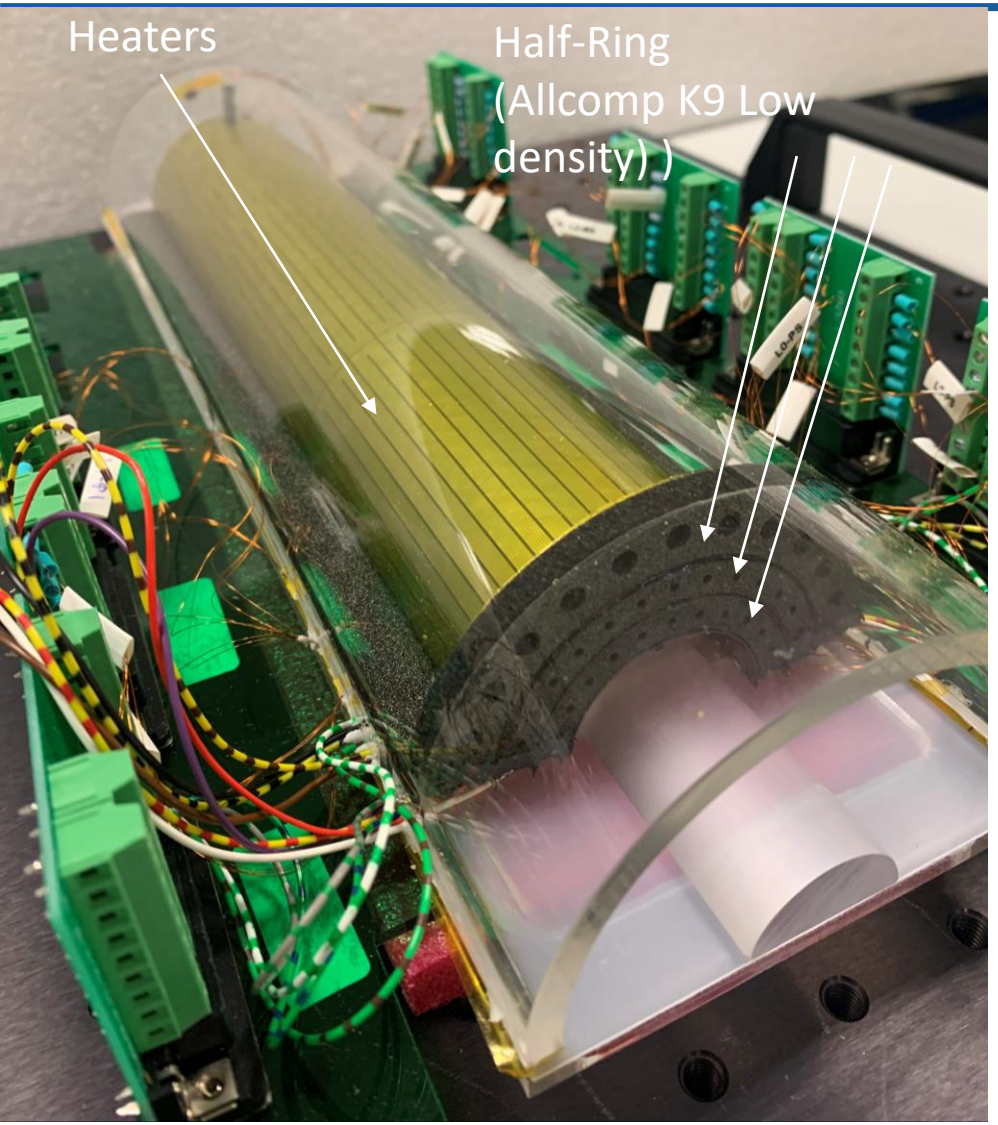
Carbon foam in beam

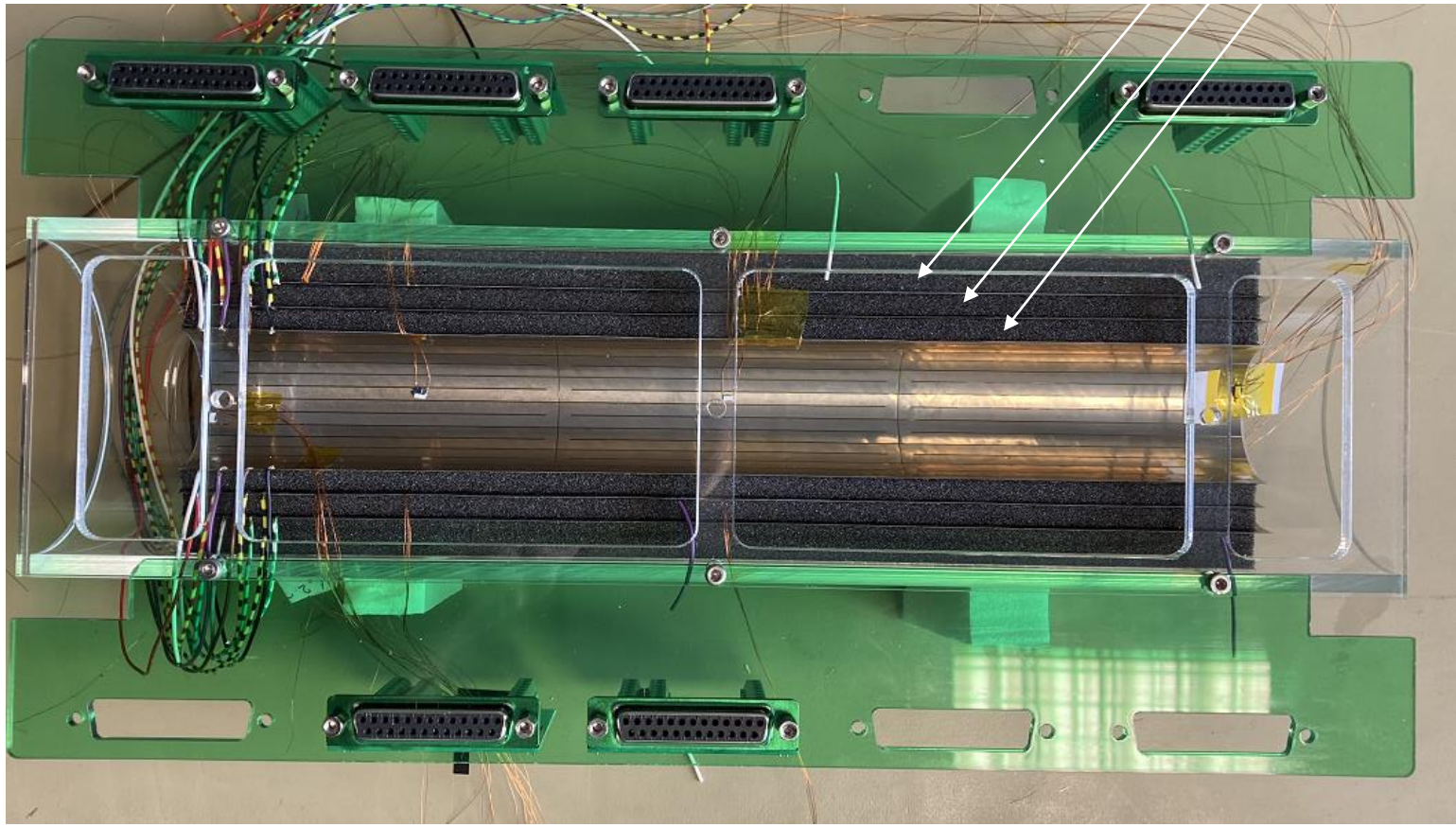




- A sandwich of chip-foam-chip was brought to beam
- Scattering angle due to carbon foam is measured
- Very small (but visible) effect, as expected

Wind tunnel cooling studies





- **Tests have been performed for a Breadboard model equipped with heaters to simulate heat in layer 0, no carbon foam**

Wind tunnel cooling studies

- **Tests with model and heaters**
  - **Different power & air speed**
  - **Carbon foam radiator are key for heat removal at periphery**

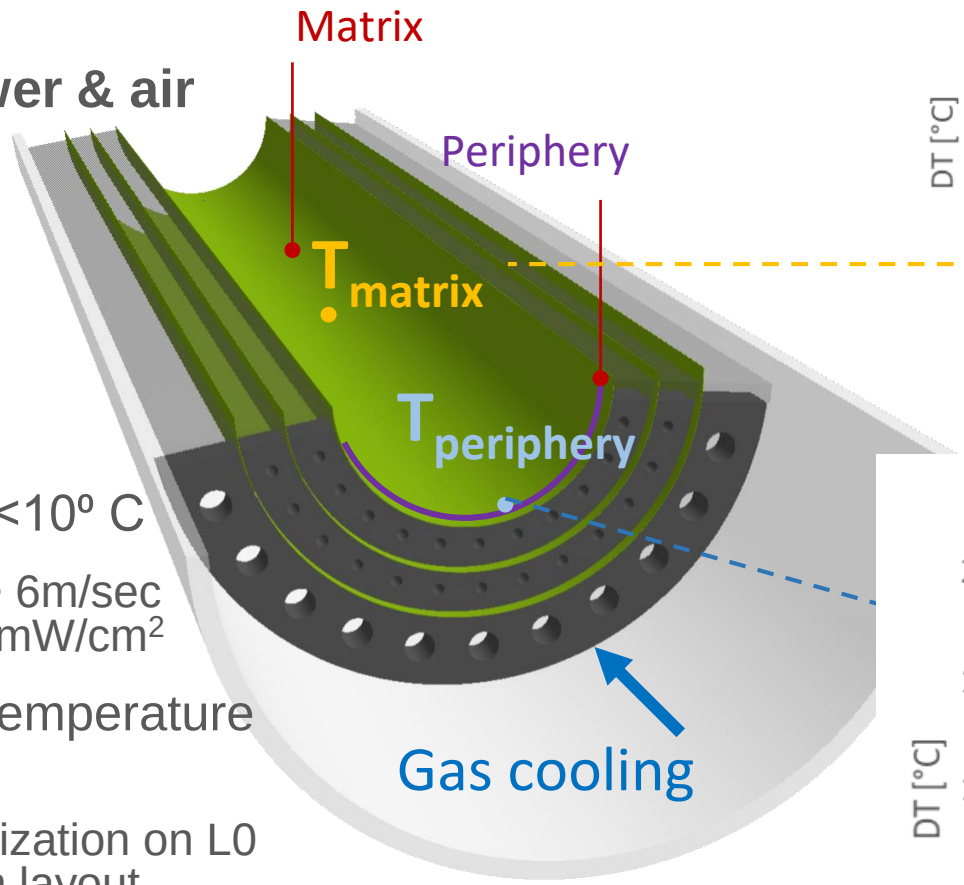
- L1 and L2 DT <10º C

  for gas flow> 6m/sec and PW 900mW/cm^2

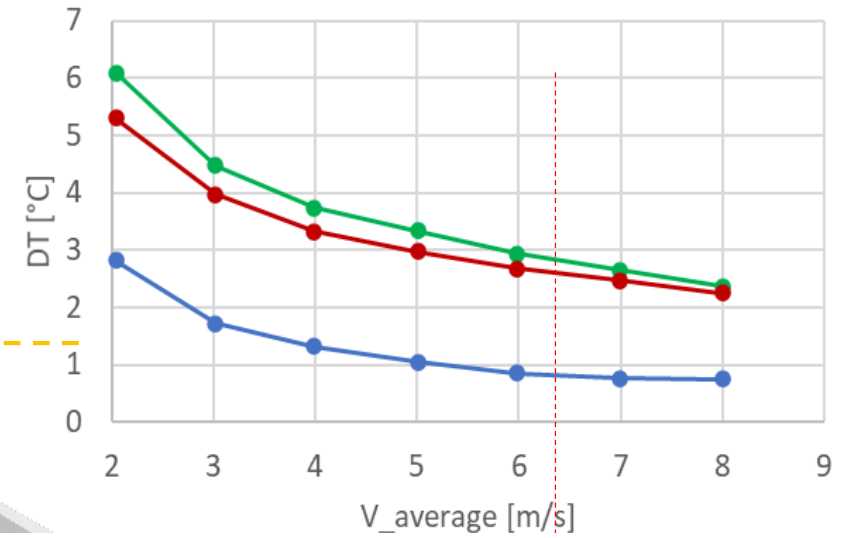
- L0 has larger temperature DT to air

  further optimization on L0 Carbon foam layout

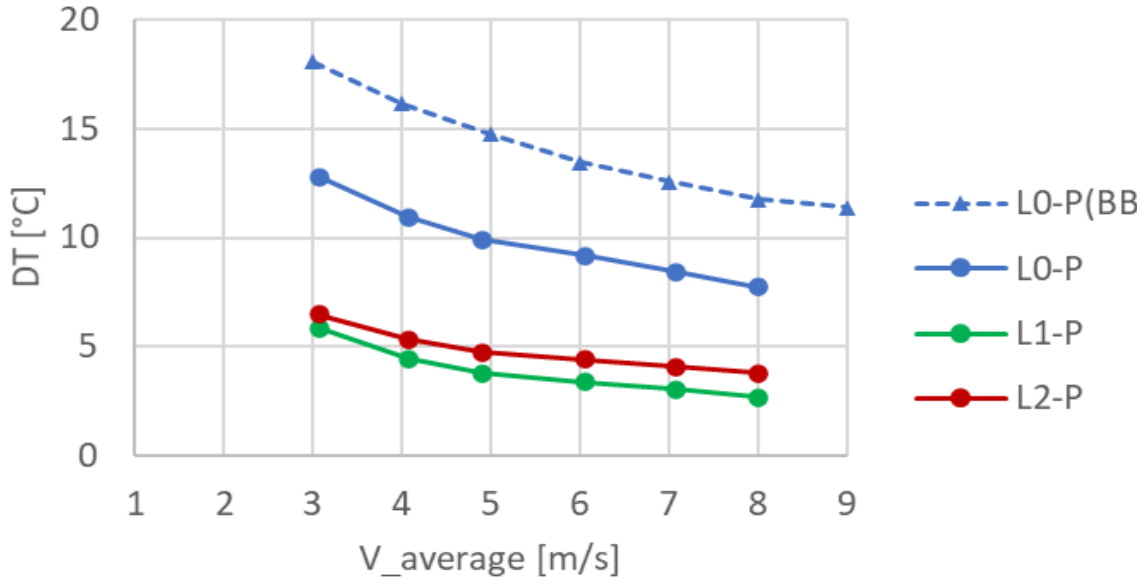
- Power density concentrated on 2.5 mm periphery



DT = $T_{periphery}$ –T_{air_in} Vs Airspeed Matrix 20mW/cm^2



Periphery 900mW/cm^2

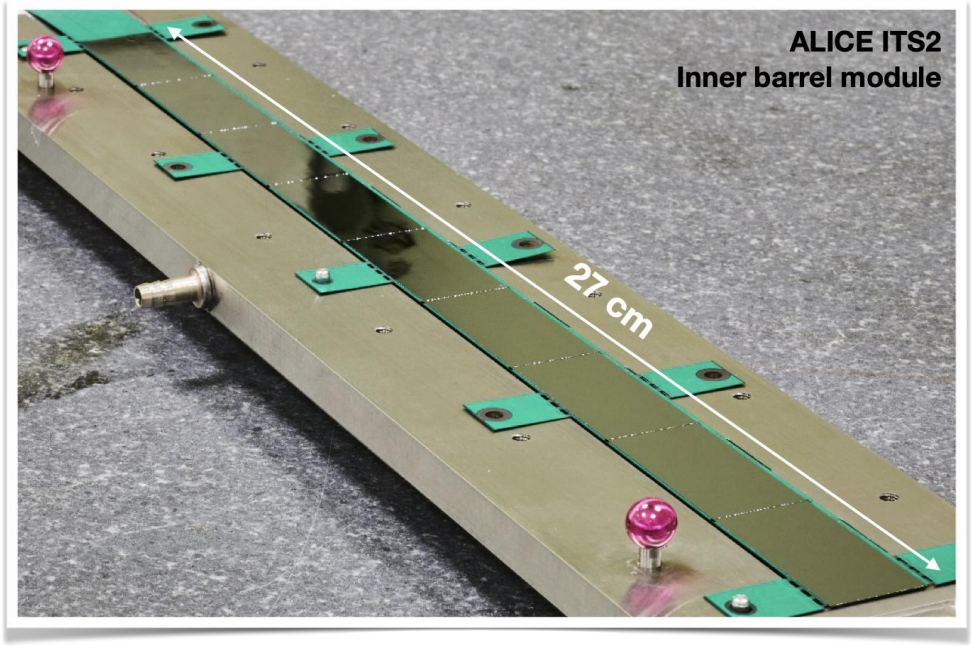


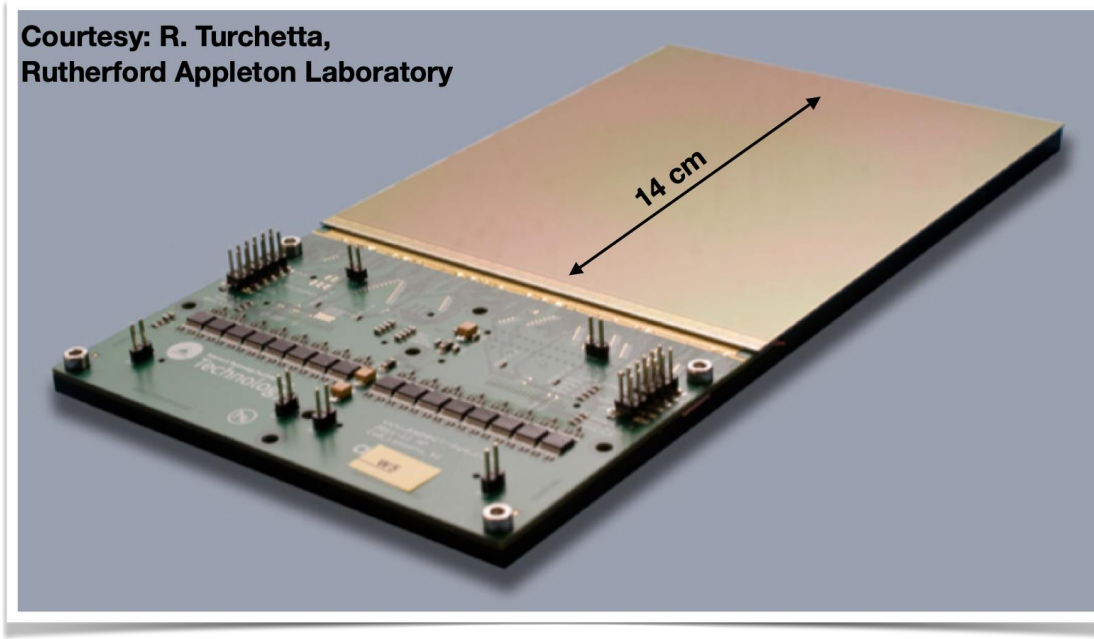
Sensor ASIC development

Can a 280 mm long silicon sensor ASIC be produced?
Can the sensors be connected without additional HDI?

Wafer scale stitching

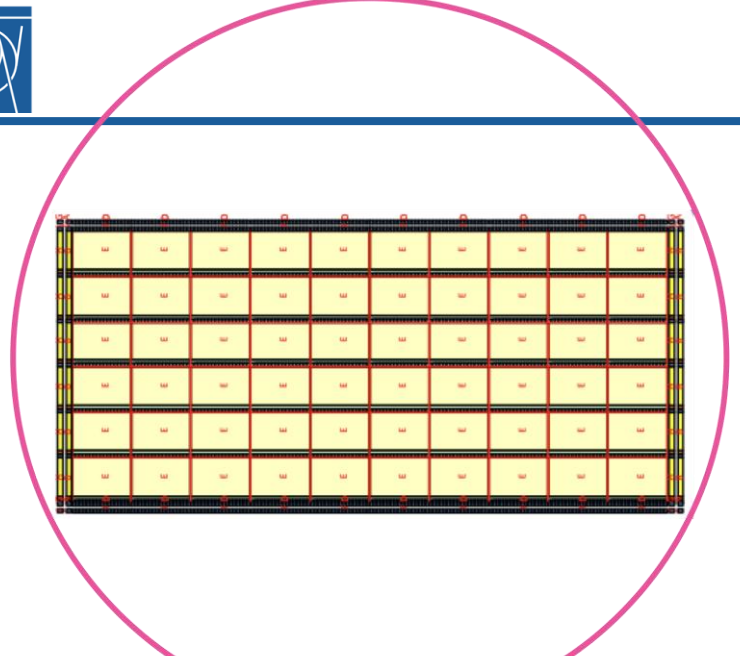
Can one produce 280 mm long silicon sensor ASICs?



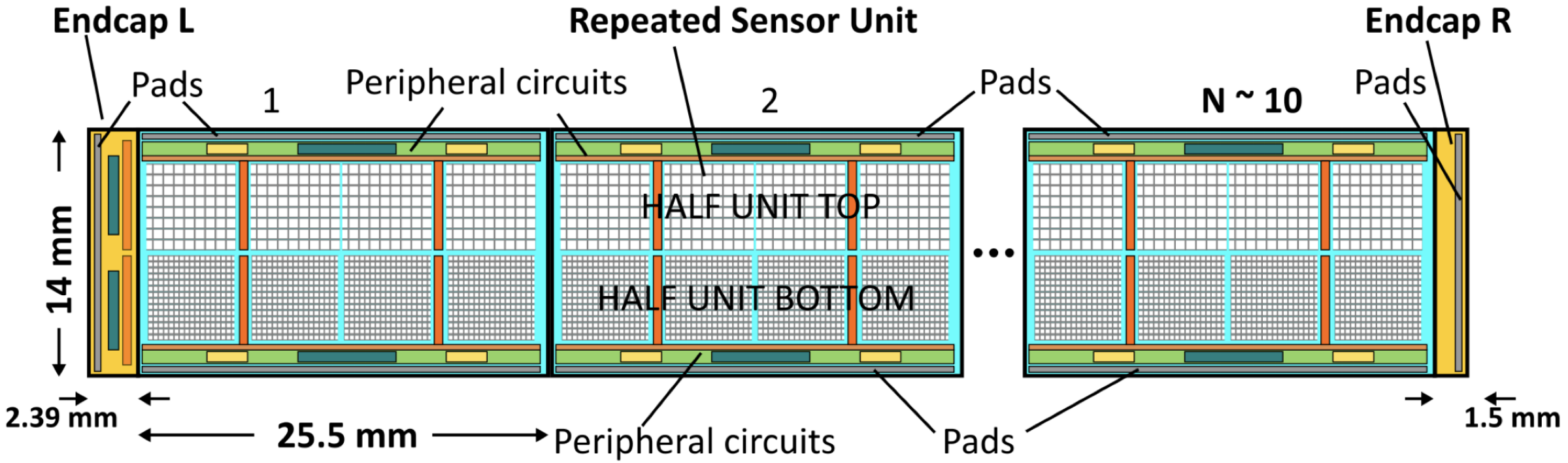


- **ASICs are abutted on a module**
  - **connected with flexible printed circuit**
- **ASICs are stitched to each other**
  - **on wafer scale**
  - **industrial process**

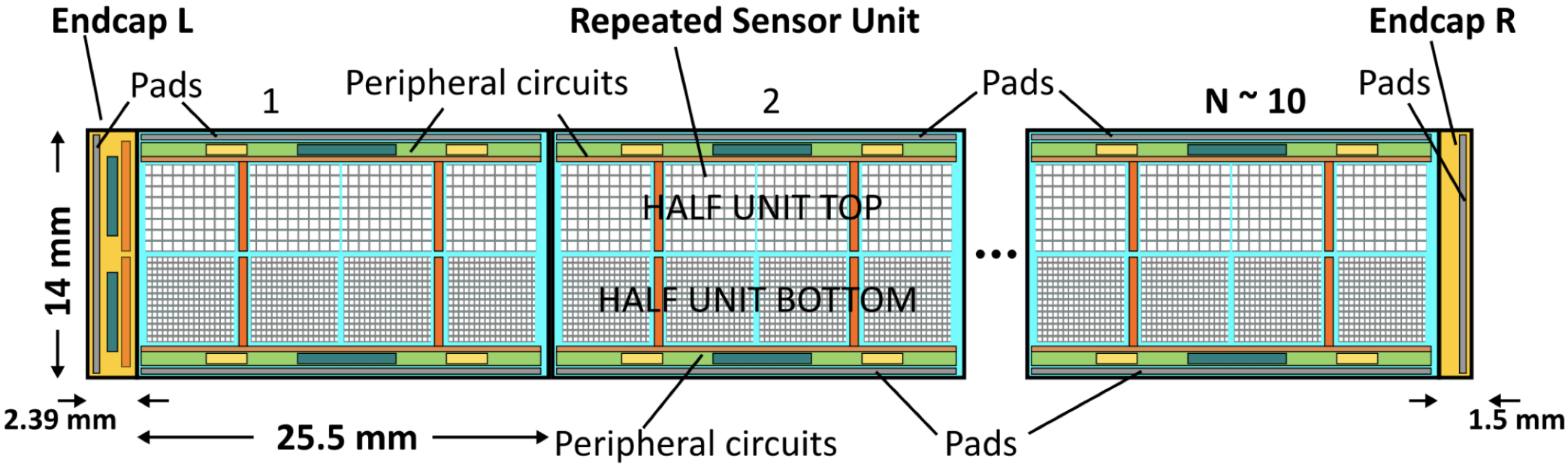
Stitched sensor ASICs



- **Next big milestone in sensor design: stitching**
- **Design activity in full swing**
  - Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

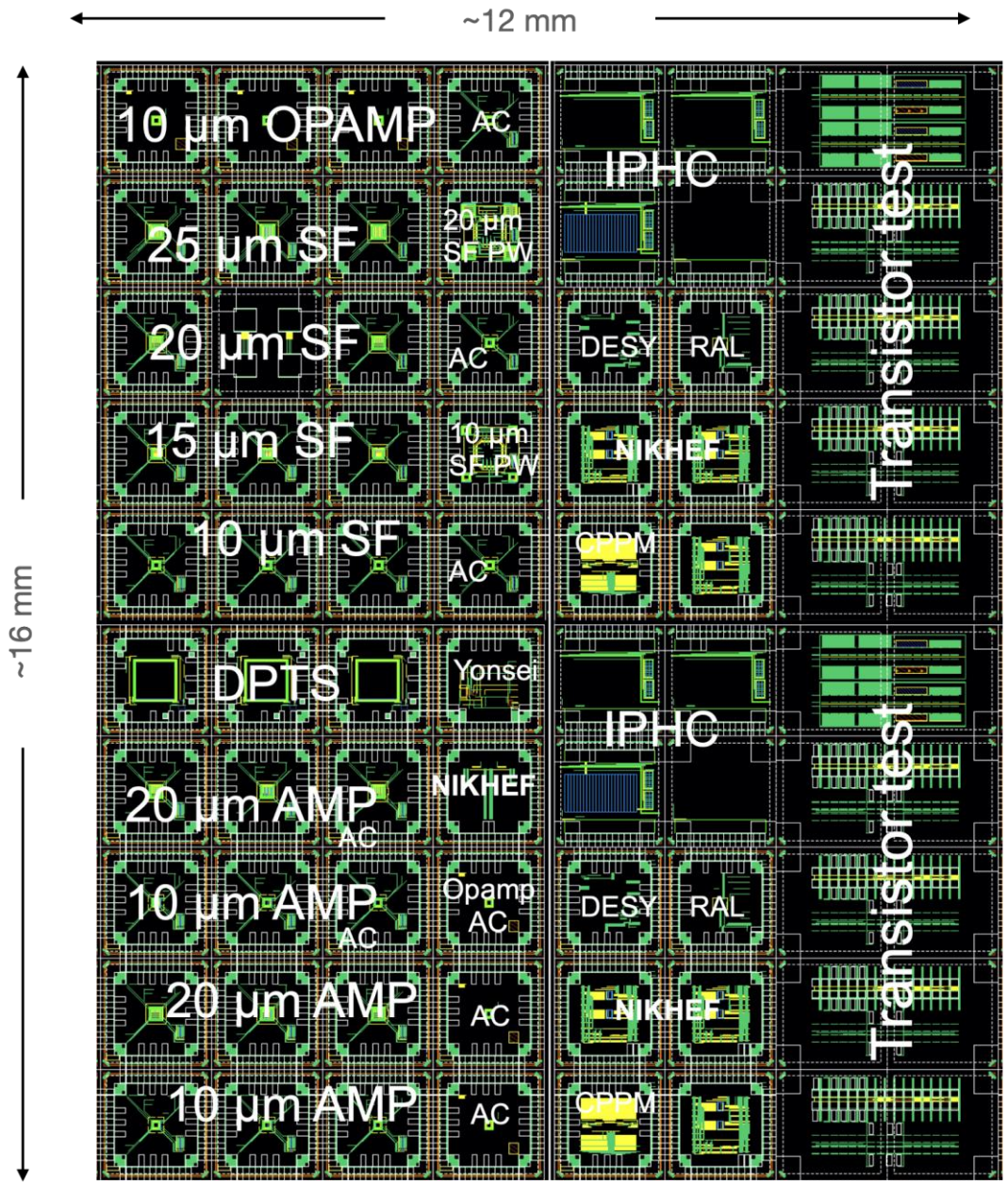


Stitched sensor ASICs



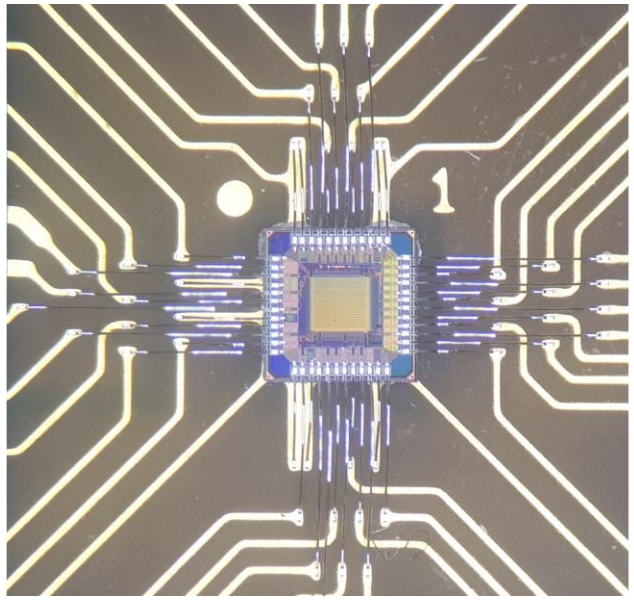
Primary Goals
Learn Stitching to make a charged particle detector
Interconnect power and signals on wafer scale design
Learn about yield and DFM
Study power, leakage, spread, noise, speed

65 nm prototypes, MLR1



- **First submission in TowerJazz 65nm**
  - ALICE ITS3 & non-ALICE groups contributed to CERN EP R&D
- **Contained several test chips**
  - radiation test structures
  - pixel test structures
  - pixel matrices
  - analog building blocks (band gaps, LVDS drivers, etc)

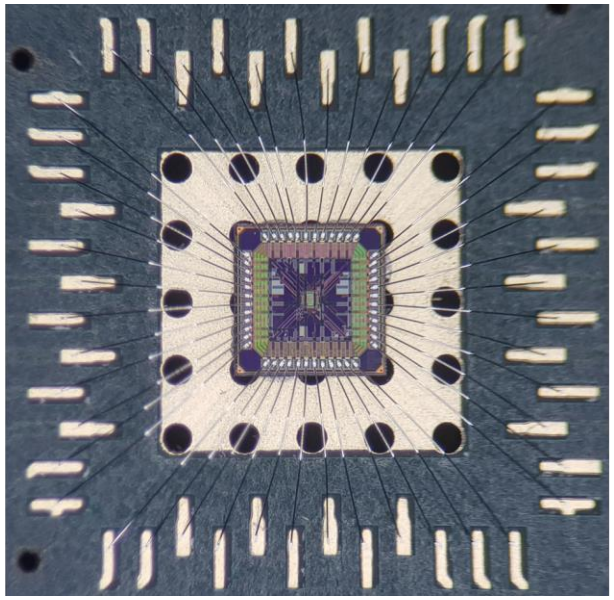
Several flavours of analog and digital test structures



DPTS

32 × 32 pixels, 15 µm pitch

asynchronous digital readout with ToT information



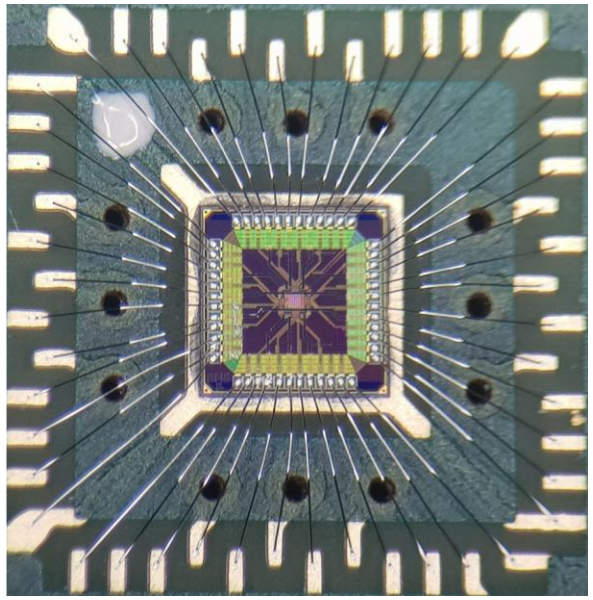
CE65

64x32 pixels, 15 µm pitch

analogue rolling shutter readout

3 pixel architectures

2 currents DACs



APTS

4x4 pixel matrix

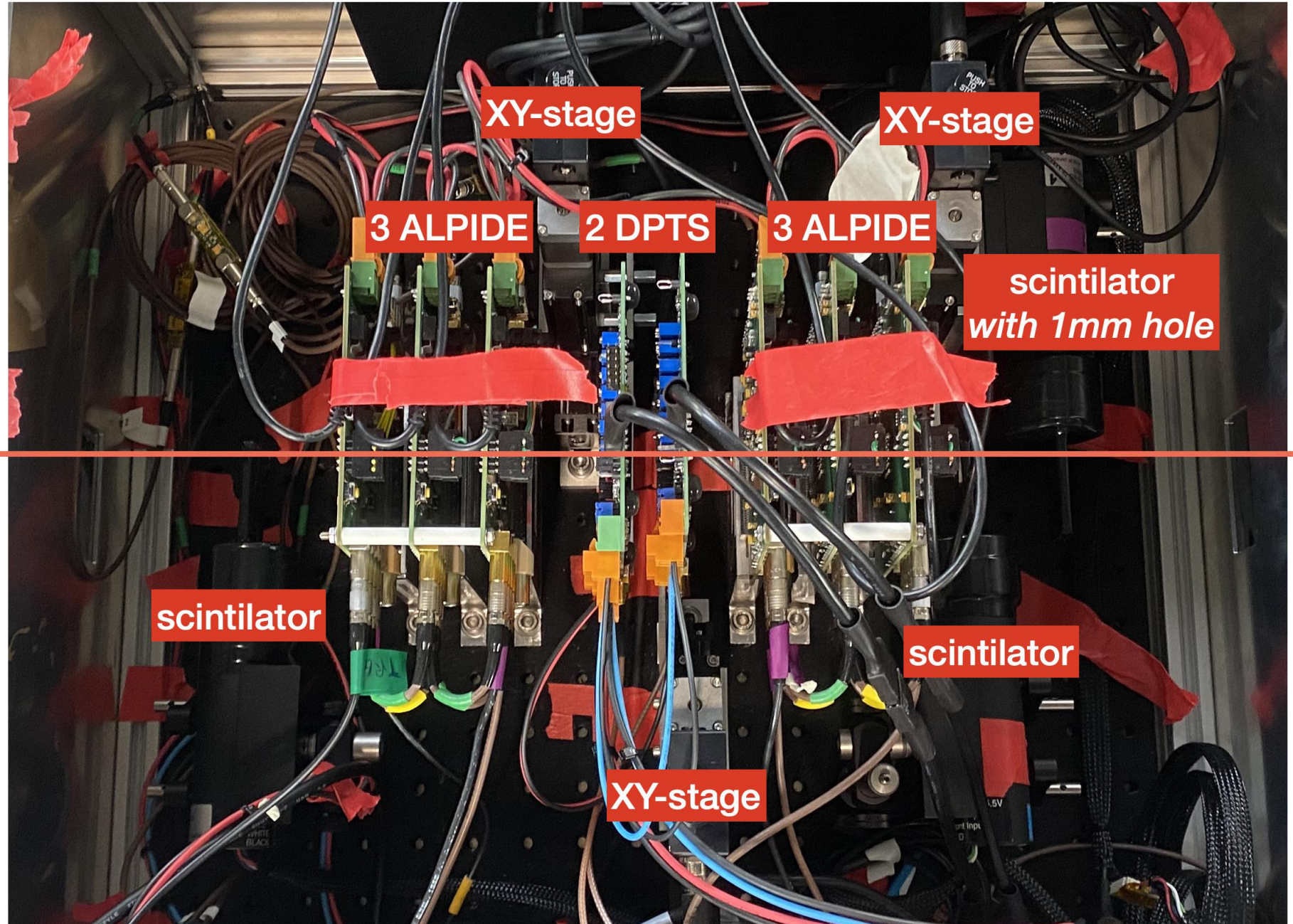
10, 15, 20, 25 µm pitches

Different pixel and amplifier architectures

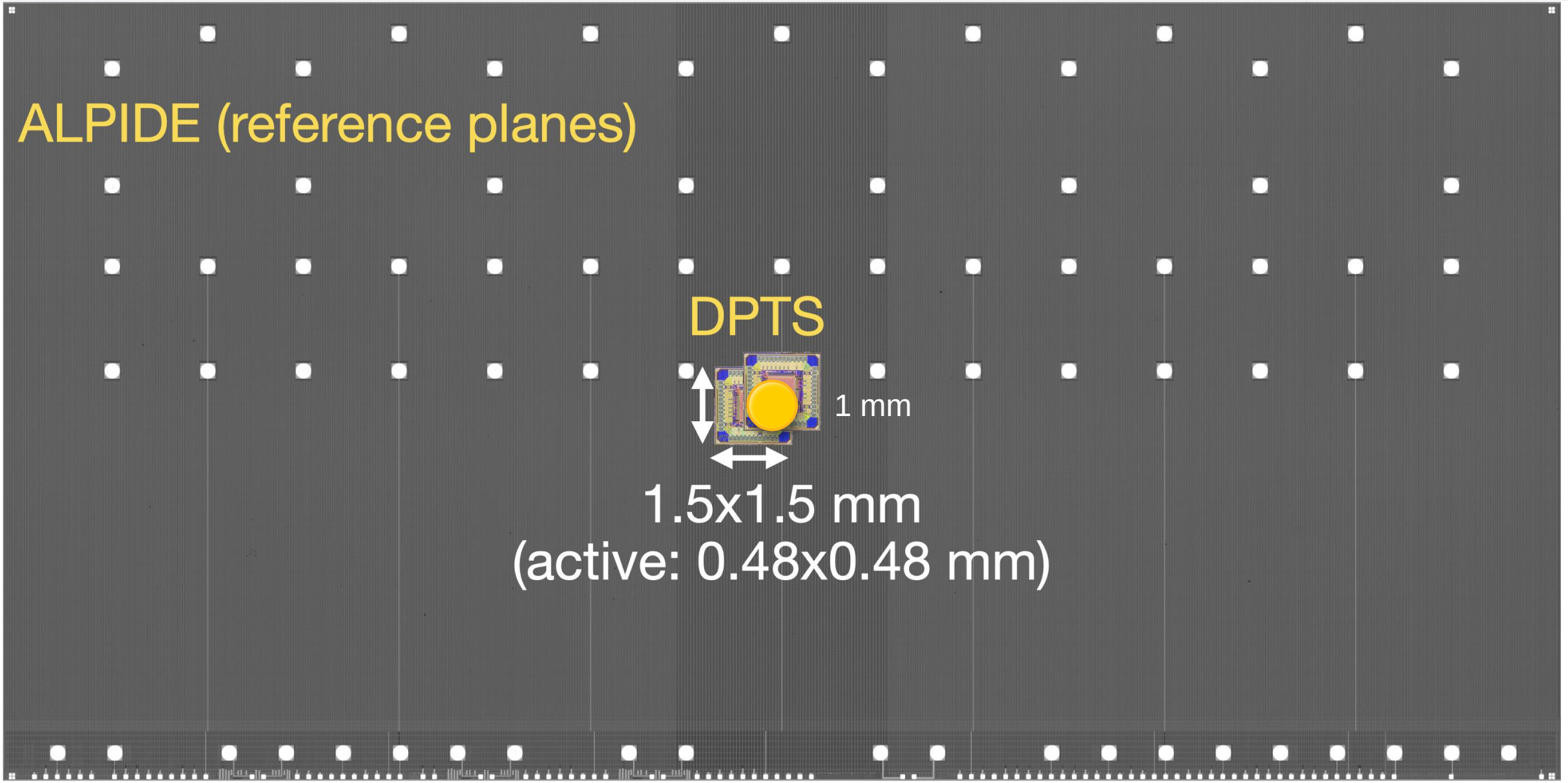
Direct analogue readout of all 16 pixels

Beam test with Telescope with DPTS

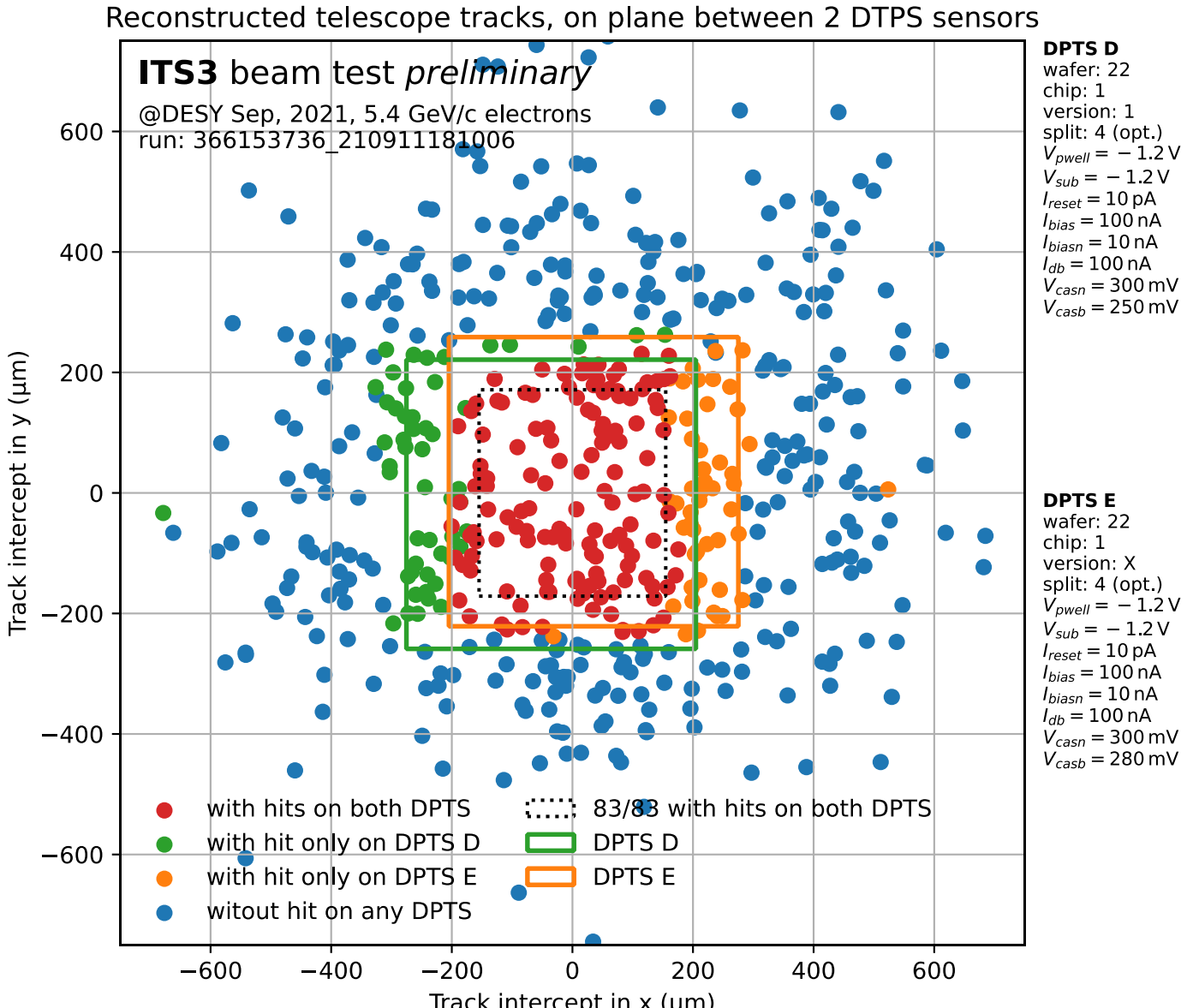
- **Scintillator with 1mm hole**
  - used to trigger on narrow beam spot
- **6 precision linear stages**
  - to align 2 DTPS and scintillators



Beam test with Telescope with DPTS



Beam test with Telescope with DPTS



- **Tracks without hit in the DPTS**
  - **have 100% shadow over DPTS**
- **166/166 tracks in DPTS1**
- **162/162 tracks in DPTS2**
- **and even for both in coincidence 83/83 tracks**
- **100% efficiency**
- **Excellent sensor/front-end performance already from first 65 nm prototype**

Summary

- ITS3 replaces first 3 inner ALICE ITS2 layers with
  - a bent, wafer scale MAPS detector
  - reduces drastically material budget
- major milestones have been passed such as
  - full size mechanical integration prototypes exist
  - air cooling concept verified by full size mockup
  - bending of thinned sensors verified
  - Tower Jazz 65 nm technology qualified
  - building blocks and basic pixel matrices efficient
  - successful beam characterisation of pixel sensor
- next step to prove stitching and power/signal distribution
  - on large structures underway