Charge sensing properties of monolithic CMOS pixel sensors fabricated in 65 nm technology

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on behalf of the IPHC, ALICE & CERN EP-R&D-WP1.2 teams.

24.02.2022

TPSCo. 65 nm Development

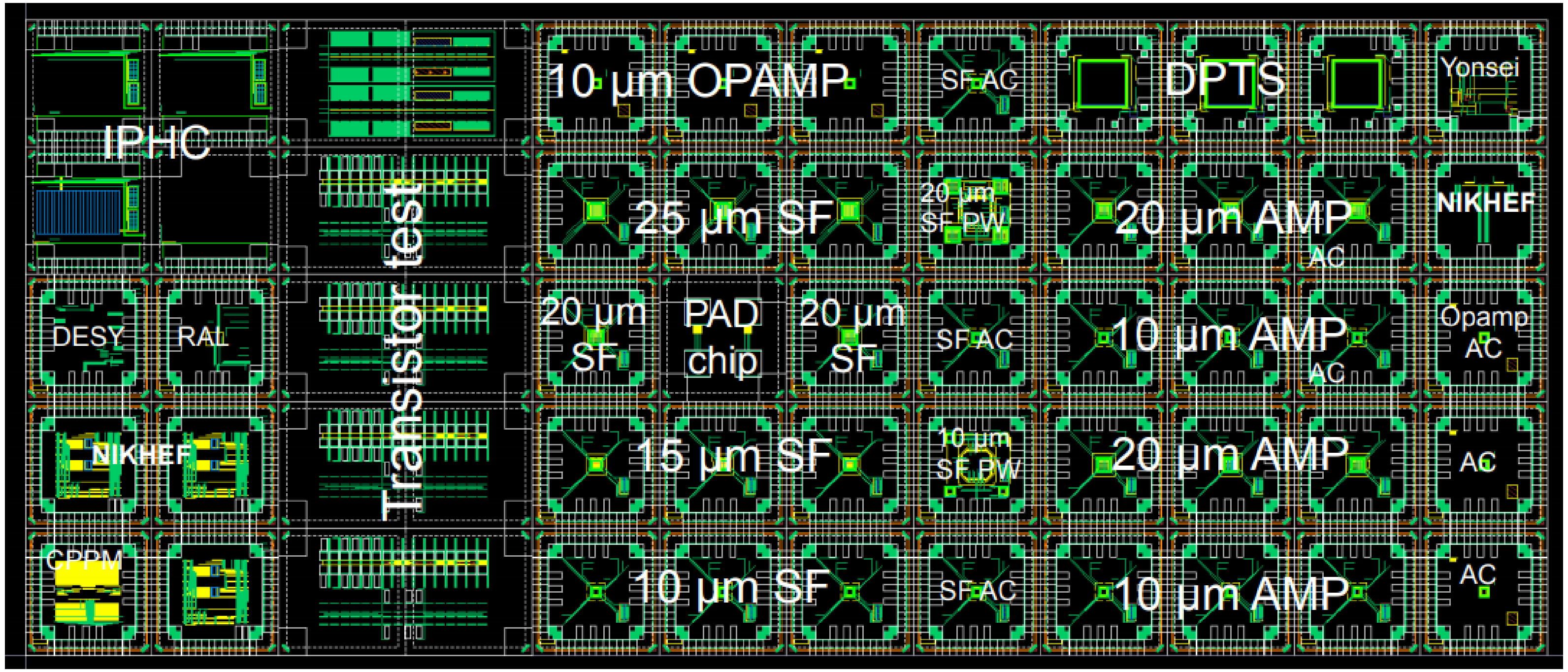
Objectives for first submission (MLR1):

- **Technology validation**
  - detection performance
  - radiation hardness
- **Design know-how**
  - understanding the design kit limitation/features
  - getting familiarity with IO structure
  - understanding possibilities for sensing node optimization
- **Delivering first batch of common functional blocks**
  - Temperature sensor
  - Bandgap
  - DAC
  - LVDS/CML
  - ....
- **Development done in the framework of WP1.2 EP R&D and the ALICE ITS3**
- **Collaborative effort undertaken by many institutes**
  - CERN / CPPM / DESY / IPHC / NIKHEF / RAL / Yonsei / ...
  - Very well coordinated by CERN in the spirit of joint development

- **Final approval/masks ordering early January 2021**
  - unified reticle size 1.5 x 1.5 mm^2
  - 55 different chips submitted!
- **Chip delivered in July 2021**
  - extensive test program started straight away
- **Currently the second submission is being prepared**
  - prototypes of large stitched sensors (MOSS/MOST)
  - revized versions of small test chips

Why to explore smaller CMOS nodes:

- smaller pitch, with other features preserved → required by future experiment (Higgs factory)
- decreasing the power dissipation
- unlock new read-out schemes
- get to very large size devices → stitched 12 inch wafers

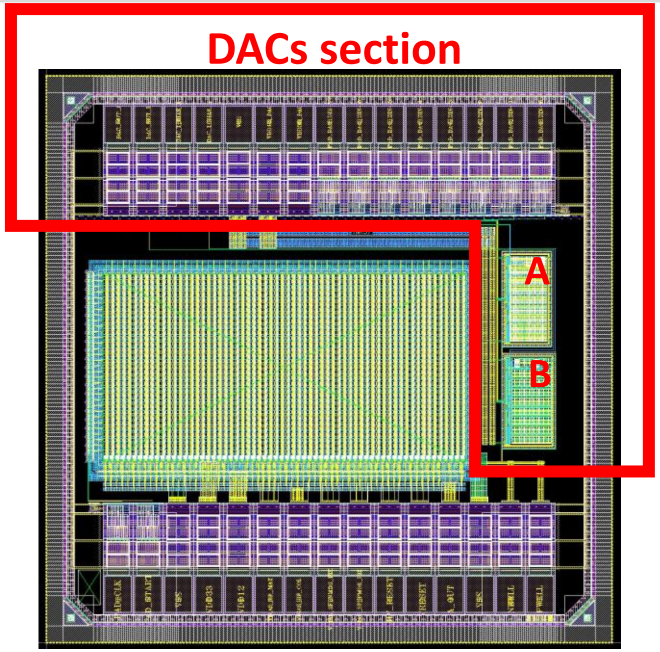


From: „Ongoing activities and status of the 65 nm MLR1 submission" by W. Snoeys

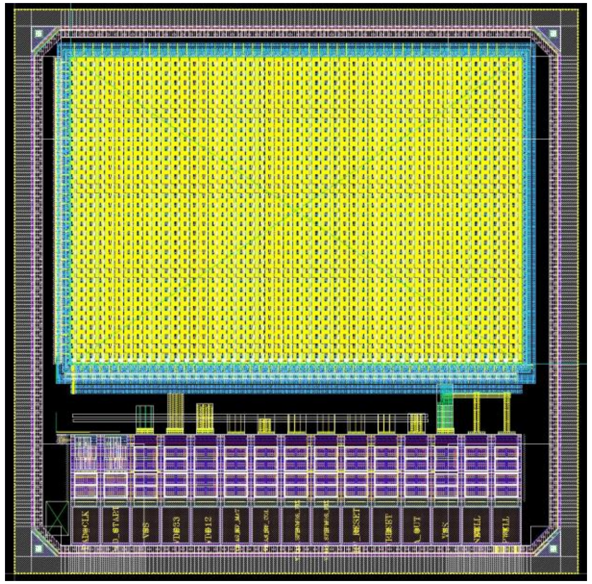
IPHC CONTRIBUTION

FOUR `CE65` CHIPS SUBMITTED:

- Each with a relatively small matrix (~0.5 and 1 mm^2), but large enough to be suitable for beam tests
- **Aimed to study:**
  - charge collection properties
  - different front-end options



Variants A/B/C



Variant D

➢ Variant A/B/C

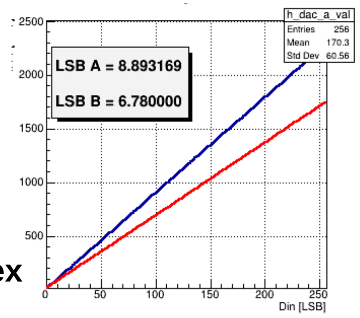
- pixel pitch: 15um
- matrix size: 64x32
- Different sensing node geometries:
  A → basic collection electrode
  B → collection electrode optimized to enhance lateral depletion
  C → further optimized collection electrode
- Hosts also 8`b DAC`s prototypes

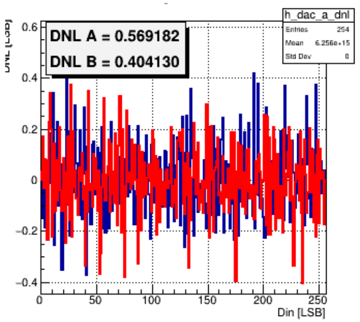
➢ Variant D

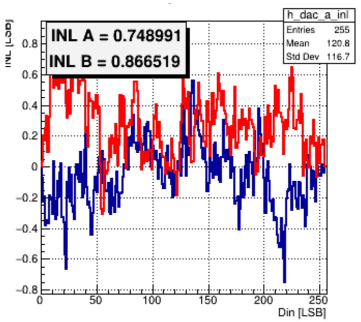
- pixel pitch: 25um
- matrix size: 48x32
- basic collection electrode geometry

DAC`s

- Measured and validated
- Monotonic in full range
- DNL < ~0.6 LSB
- INL < ~1 LSB
- **Already in use in the upcoming, more complex designs**

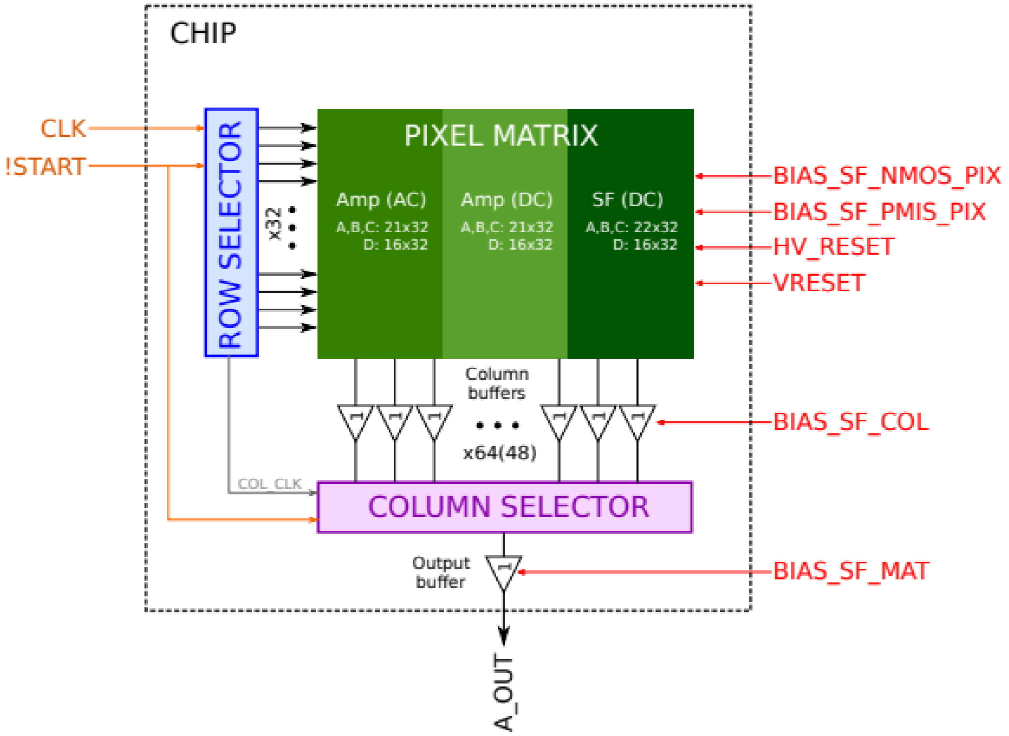






CE65 MATRIX DESIGN OVERVIEW

- **Rolling shutter readout**
- **Integration time down to 50 us (@40MHz clk)**
- **External digitization**
- **Three sub-matrices:**
  - AC coupled pre-amplifier [Amp (AC)]
  - DC coupled pre-amplifier [Amp (DC)]
  - DC coupled source-follower [SF (DC)]

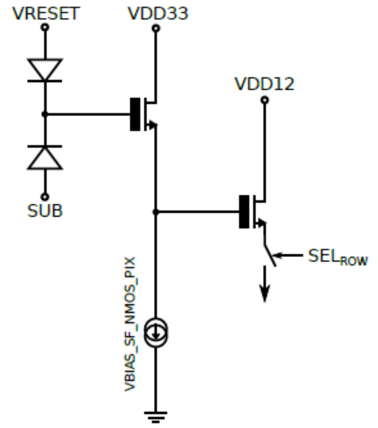


SF pixel:
- The simplest approach
- Allows for a direct estimation of input capacitance

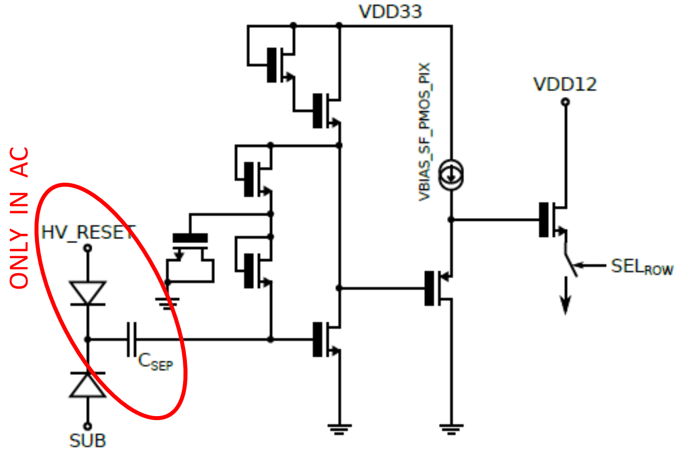
DC AMP:
- Self-biased
- Input node voltage determined by the pre-amp operating point
- In-pixel gain →potencially improved SNR

AC AMP:
- Sensing node depletion voltage can be applied independently and go over the supply voltage
- Slightly reduced gain in comparision with DC Amp due to parasitic capacitances

DC SF pixel



AC/DC pre-amp pixel



CE65 Readout System

Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

DAQ BOARDS:

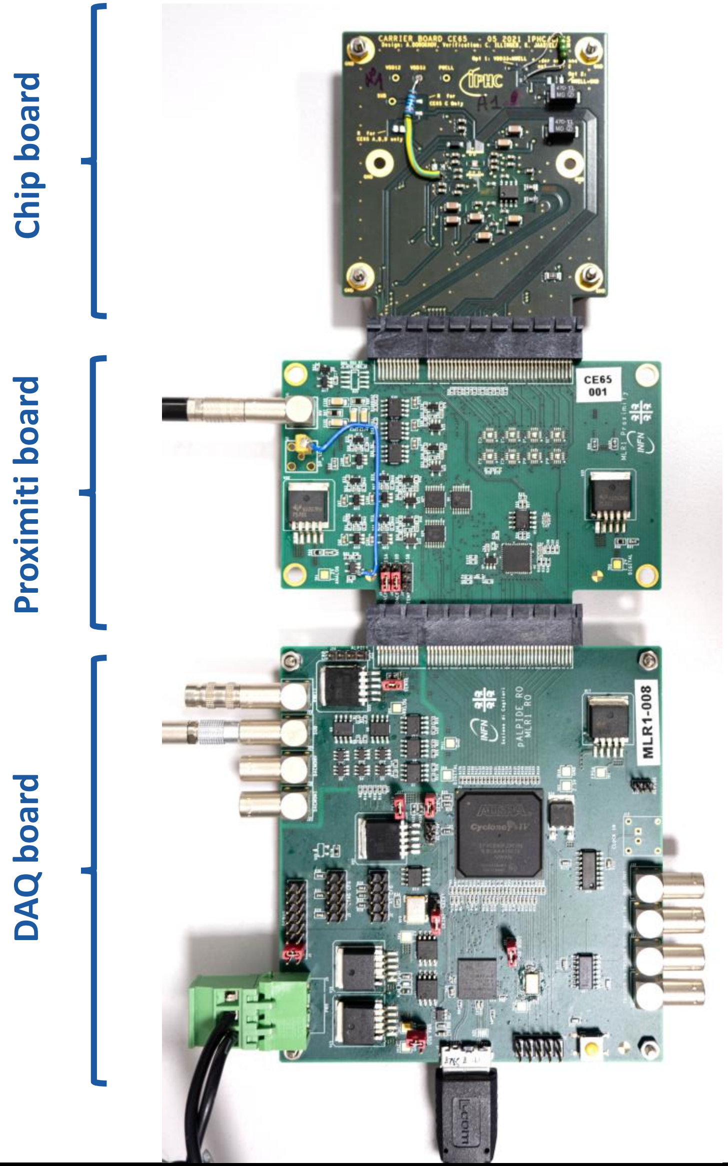
- PCB and firmware developed by the team from Cagliari University & INFN
- Common readout system for multiple MLR1 devices (CE65, APTS, DPTS)
- Based on Altera Cyclone IV FPGA
- Readout speed up to 40 MHz
- USB protocol used for the communication with the PC
- Readout software integrated into the EUDAQ framework (compatibility with the beam test infrastructure)

PROXIMITI BOARD:

- PCB developed by the team from Cagliari University & INFN
- Specific for a given device
- Provides all chip biasing
- CE65 proximity equipped with fast 16-bit ADC

CHIP BOARD:

- PCB developed at IPHC
- Analog output buffering
- Decoupling



CE65 Lab Characterization

- **Lab characterization done with the ^{55}Fe source**
  - All measurements done at the room temperature
  - No back bias applied ($V_{substrate}$ = 0V)
  - Readout frequency: 10MHz
- **Numerous chip flavours available:**

		CE65 VARIANT			
		A	B	C	D
SPLIT	1	(green)	(red)	(white)	(white)
	4	(green)	(green)	(green)	(green)

- green: - operational
- red: - not responding
- white: - not yet tested

Covered in details during talk

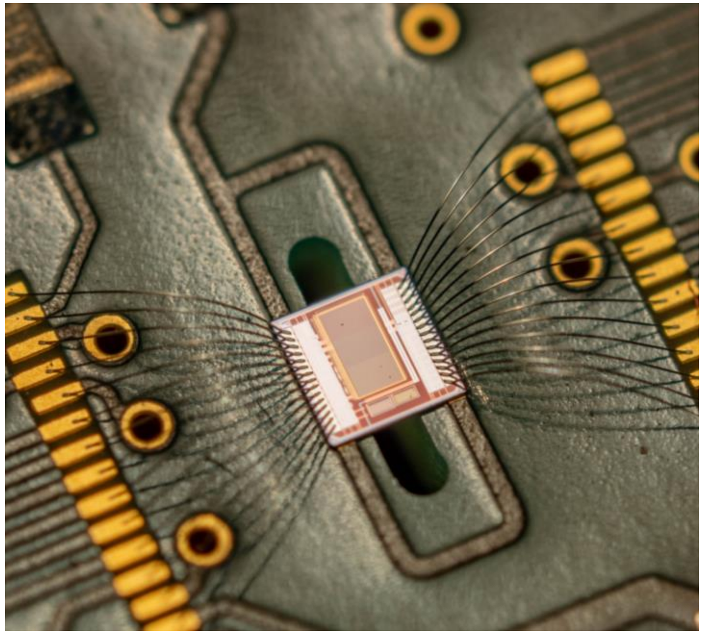
- **Sensor optimisation similar to modifications that have been used in TowerJazz 180nm**
  - Aimed to increase the lateral electric field near the pixel border

CE65 Variants:

- **A:** pitch = 15 um
  sensor – basic diode
- **B:** pitch = 15 um
  sensor – optimized diode
- **C:** pitch = 15 um
  sensor – further optimized diode
- **D:** pitch = 25 um
  sensor – basic n-well

Splits – process optimizations:

- Split 1 – default
- Split 4 – target process



Baseline and Noise

Baseline:

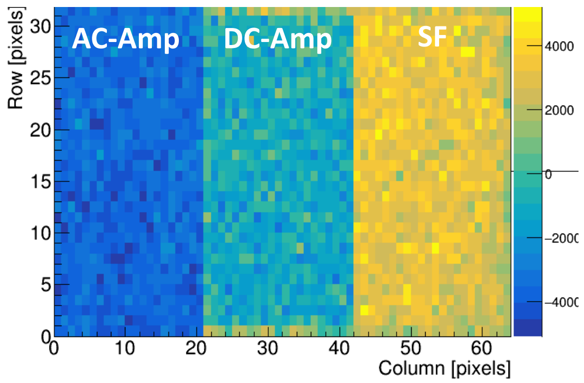
- Clearly visible sub-structure on the baseline map
  → as expected from the design
- No significant differences in the baselines for different diode flavours
- Edge pixels degradation slightly more pronounced for a standard structure

Noise:

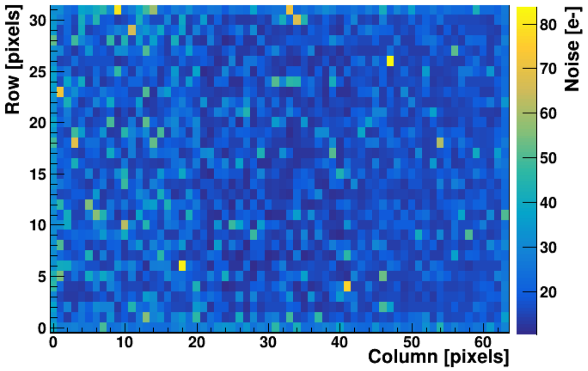
- ENC calibrated based on the ^{55}Fe peak position
- No significant differences between the sub-matrices
- ENC measured to be in range **15 e$^-$: 25 e$^-$** (depends on the settings optimization, biasing conditions)

Basic diode [A4]:

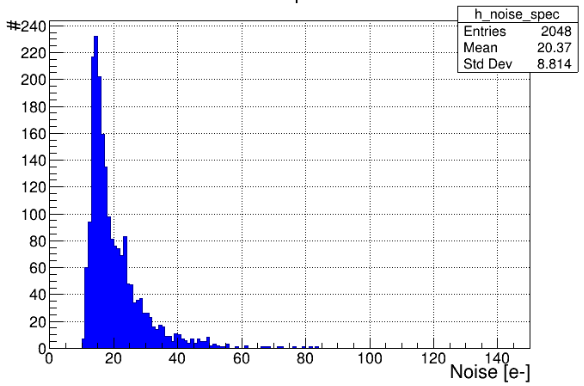
Baseline Map



ENC Map

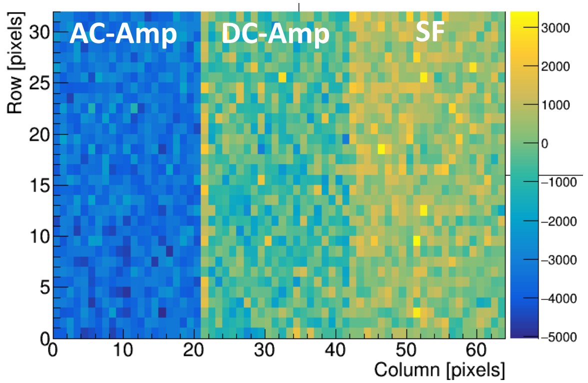


ENC Spectra

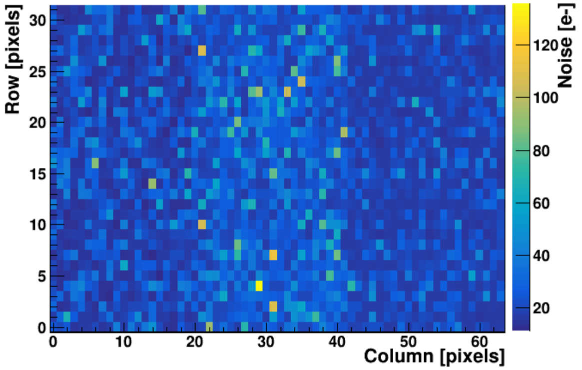


Optimized diode [B4]:

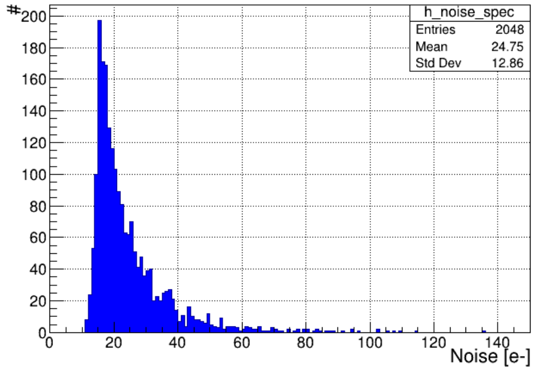
Baseline Map



ENC Map



ENC Spectra



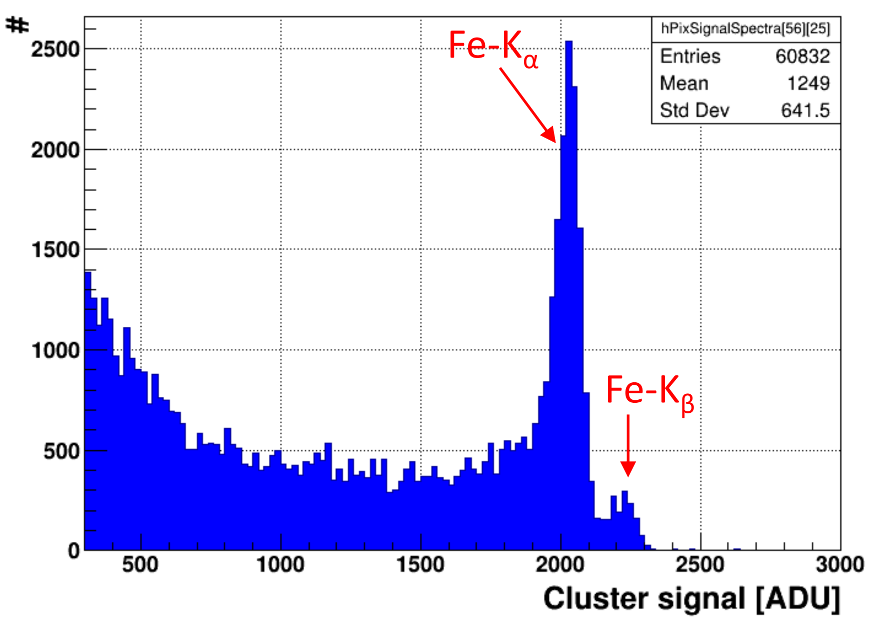
EXEMPLES OF ^{55}FE SPECTRA

- **Exemplary plots shown for Source-Followers sub-matrix with optimized sensor**
  - similar behaviour observed on others structures with this sensor geometry

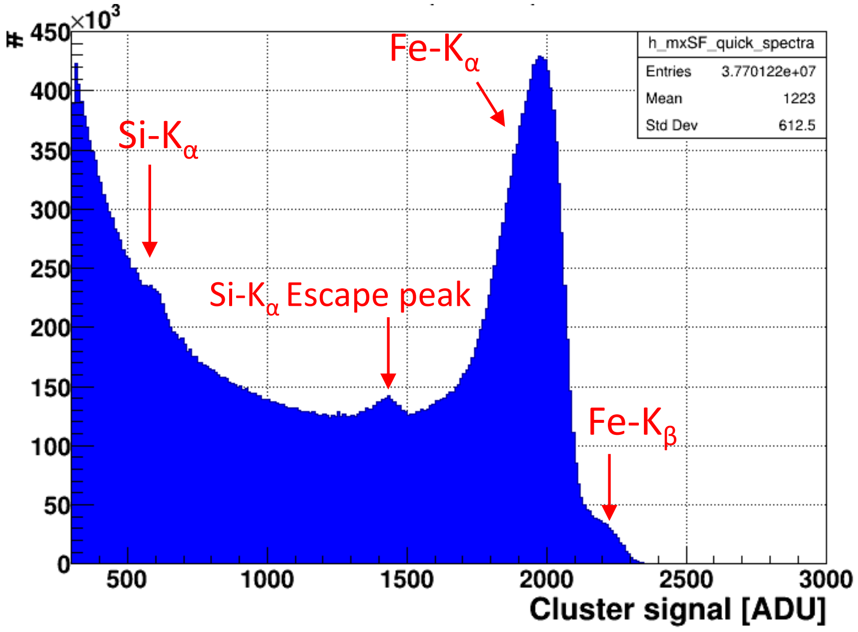
- **Energy resolution for single-pixel clusters high enough to clearly distinguish K-alpha (5.90 keV) and K-beta (6.49 keV) lines**

- **Pixel-to-pixel gain variations slightly smears the spectum for the whole matrix**
  - K-beta line still visible but without clear separation
  - Increased statistics allows to distinguish also the Si-escape peak ($FeK_\alpha - SiK_\alpha$=4.16 keV) and SiK_α peak (1.74 keV)
  - All peak positions well alligned with respect to theirs energy

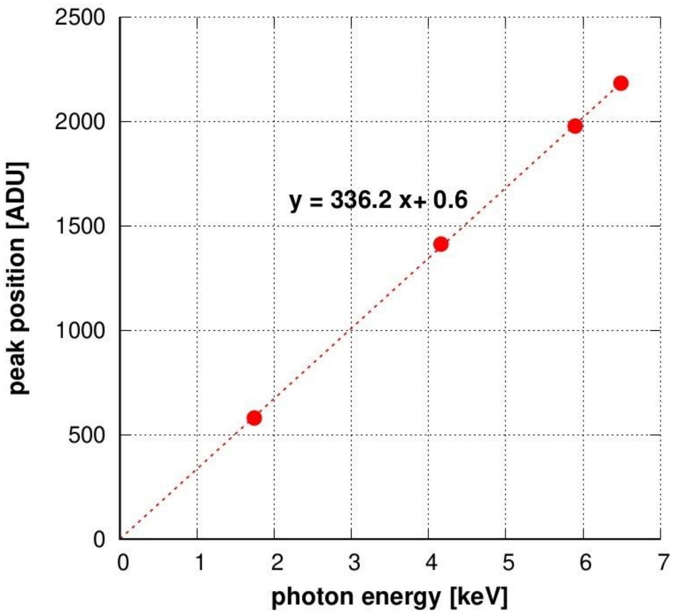
SINGLE PIXEL CLUSTERS SPECTRUM FROM ONE PIXEL



SINGLE PIXEL CLUSTERS SPECTRUM FOR WHOLE SF SUB-MATRIX



CALIBRATION FIT

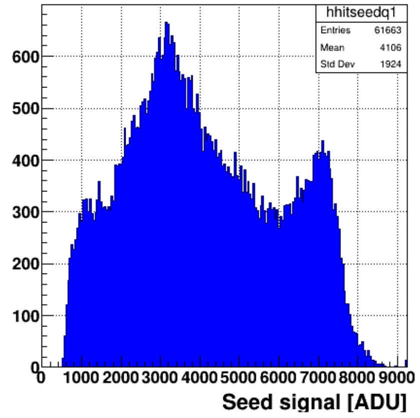


^{55}Fe Results: AC amplifier

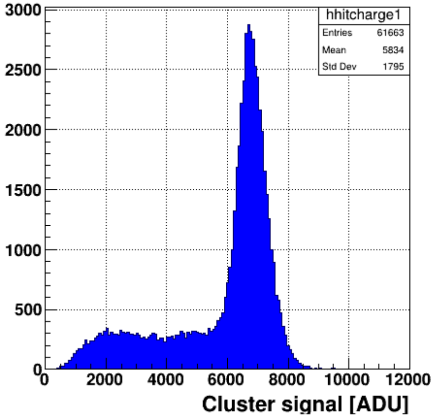
- **Reverse bias:**
  - **10V** (HV_RESET = 10V - applied to the sensing node [see slide4])
  - maximal depletion reached at this point
- **Total cluster energy independent from the diode geometry**
  - Similar input node capacitance after the depletion
- **Significant difference in the charge sharing**
  - Optimized diode:
    - vast majority of the events are single pixel depositions
    - seed energy spectrum similar to cluster energy spectrum
  - Basic diode:
    - significant charge sharing
    - seed carries only about half of the total energy

Basic diode [A4]:

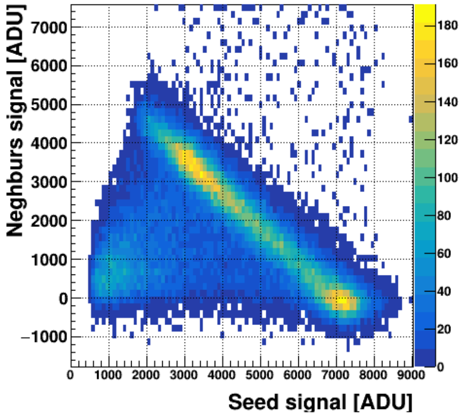
SEED ENERGY



CLUSTER ENERGY

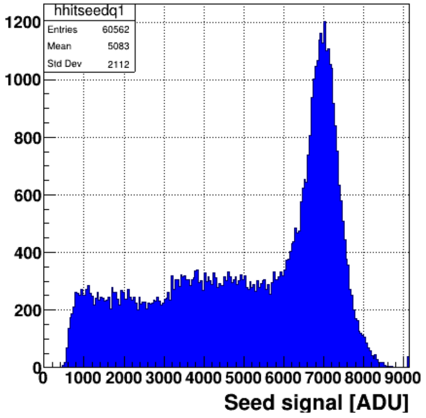


SEED VS NEIGHBOURS

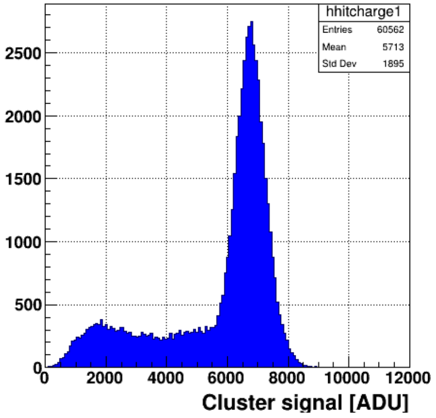


Optimized diode [B4]:

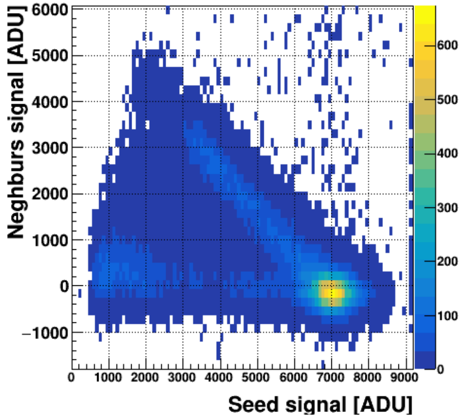
SEED ENERGY



CLUSTER ENERGY



SEED VS NEIGHBOURS



^{55}Fe Results: DC amplifier

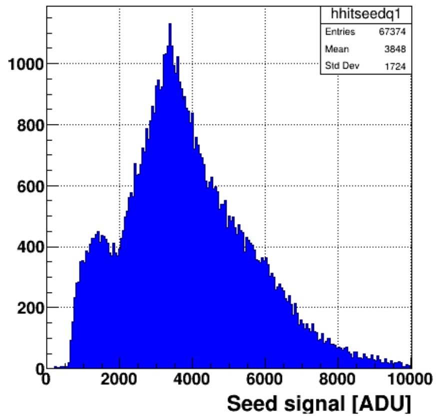
- **Reverse bias:**
  - **1V** (self biased [see slide4])
  - far from maximal depletion

- **Total cluster energy depends on the diode geometry**
  - ~40% larger gain of a basic structure
  - optimized diode has larger capacitance when not depleted

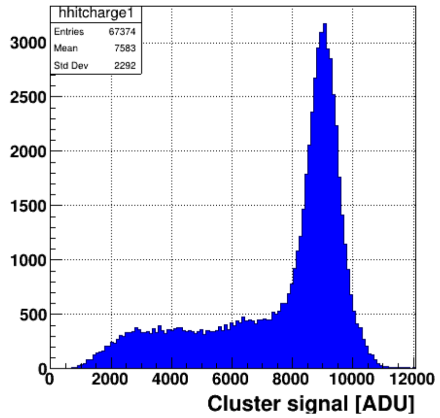
- **Significant difference in the charge sharing**
  - Optimized diode:
    - vast majority of the events are single pixel depositions
    - seed energy spectrum similar to cluster energy spectrum
  - Basic diode:
    - significant charge sharing
    - almost no single pixel depositions
  - Even more pronaunced than for the AC Amp
    (attributed to difference in depletion)

Basic diode [A4]:

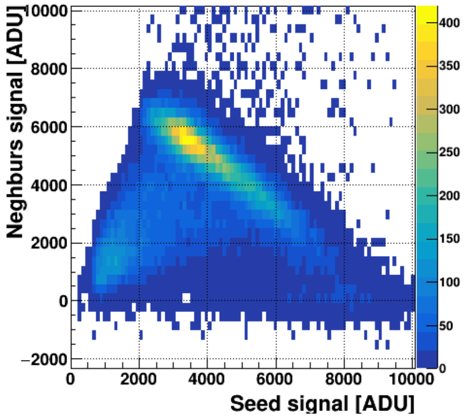
SEED ENERGY



CLUSTER ENERGY

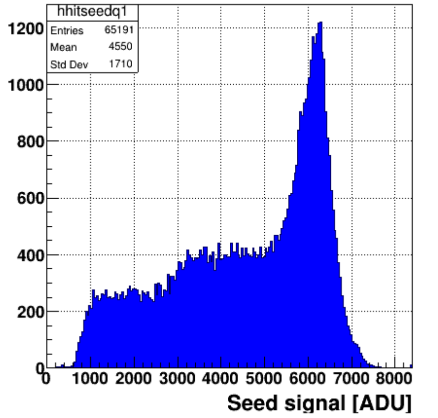


SEED VS NEIGHBOURS

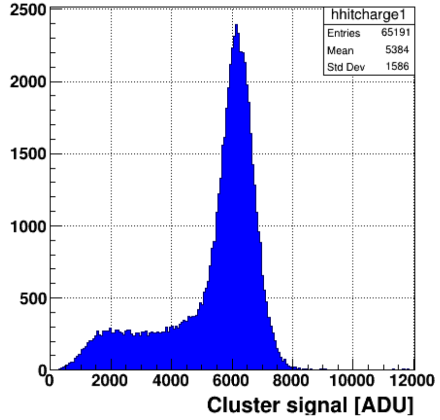


Optimized diode [B4]:

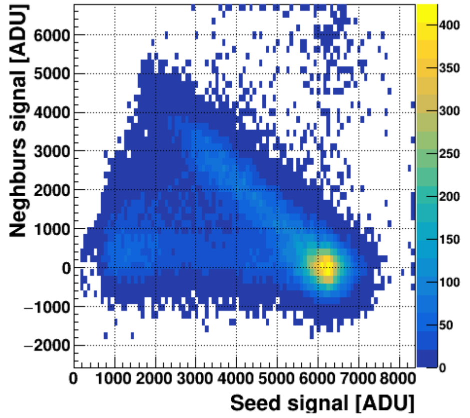
SEED ENERGY



CLUSTER ENERGY



SEED VS NEIGHBOURS



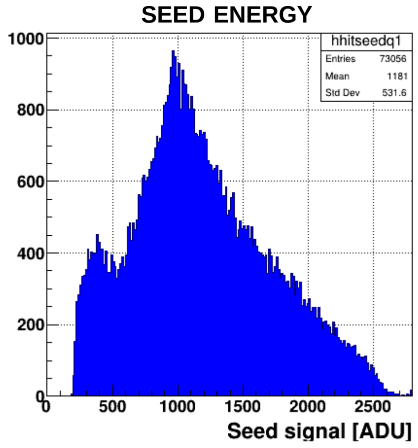
^{55}Fe Results: Source-Follower

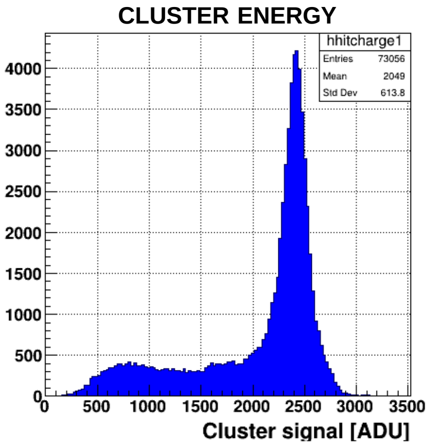
- **Reverse bias:**
  - **3.3V** (VRESET = 3.3V- applied to the sensing node [see slide4])
  - relatively close to maximal depletion

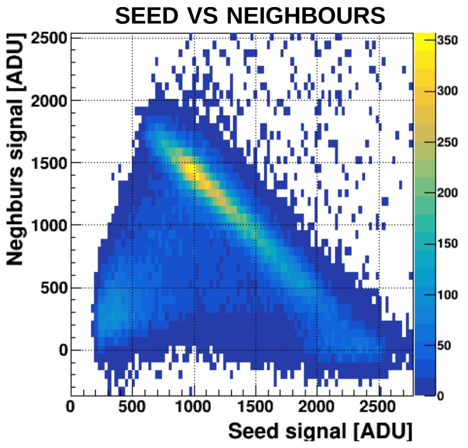
- **Total cluster energy depends on the diode geometry**
  - ~20% larger gain of a basic structure
    → less pronounced than for the DC Amp because more depleted
  - optimized diode has larger capacitance when not depleted
  - gain difference less pronounced than for the DC Amp because of larger depletion

- **Significant difference in the charge sharing**
  - Optimized diode:
    - vast majority of the events are single pixel depositions
    - seed energy spectrum similar to cluster energy spectrum
  - Basic diode:
    - significant charge sharing
    - almost no single pixel depositions

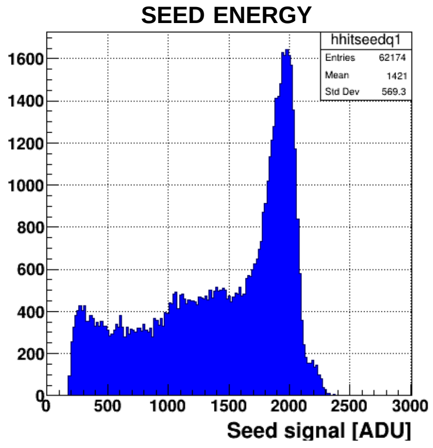
Basic diode [A4]:

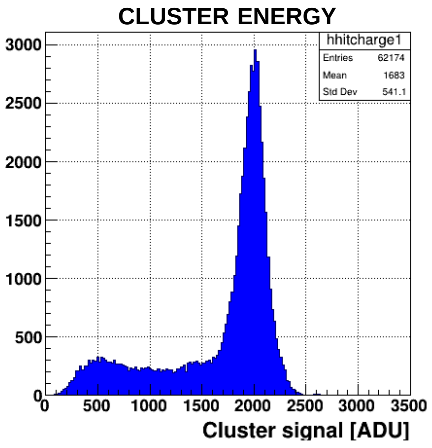


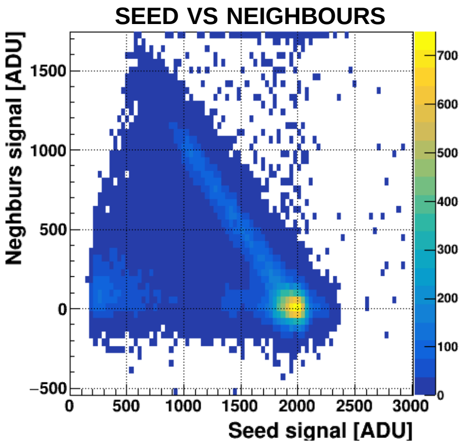




Optimized diode [B4]:







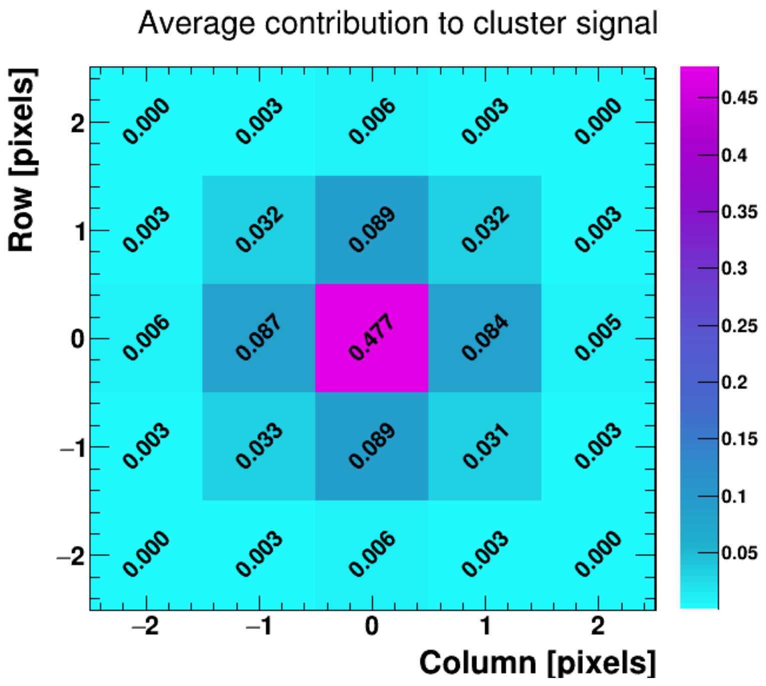
Charge sharing between neighbouring pixels

- **Exemplary plots shown for DC-Amplifier submatrix**
  - Very similar behaviour observed on others structures

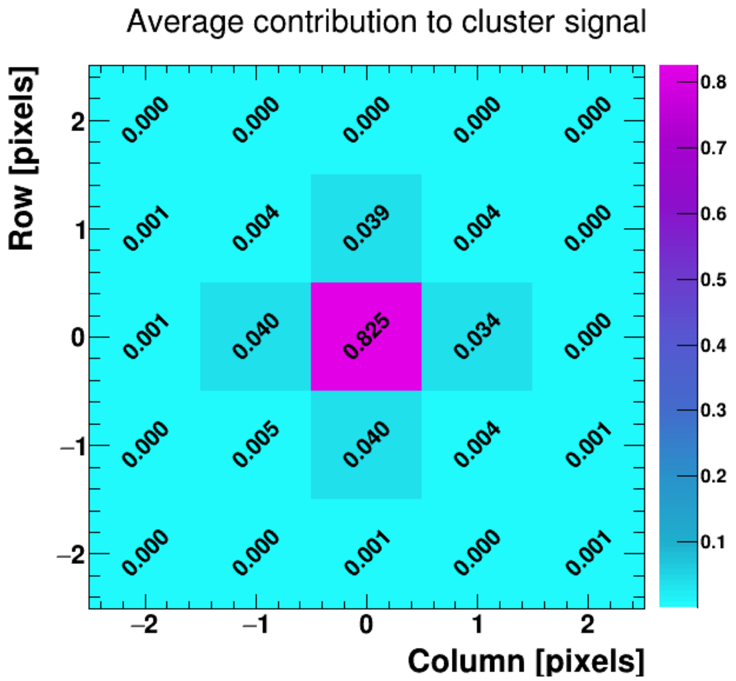
- **Results inlined with previous observations:**
  - Basic diode:
    - significant charge sharing
    - seed carries less than half of the total charge
  - Optimized diode:
    - charge sharing highly suppressed
    - charge concentrated on single pixel
      → more operating margin

- **Consequences:**
  - Basic diode:
    - one may expect outstanding spatial resolution
    - harder to maintain high efficiency
  - Optimized diode:
    - charges „guided" directly to the closest collection electrode
      that indicates:
      → higher electric field
      → faster collection (higher ToA resolution)
      → more resistant to displacement damages
  - Indirect hints → to be verified in direct measurements!

Basic diode [A4]:



Optimized diode [B4]:



SENSOR DEPLETION DEVELOPMENT

➢ **Sensor depletion can be developed by:**

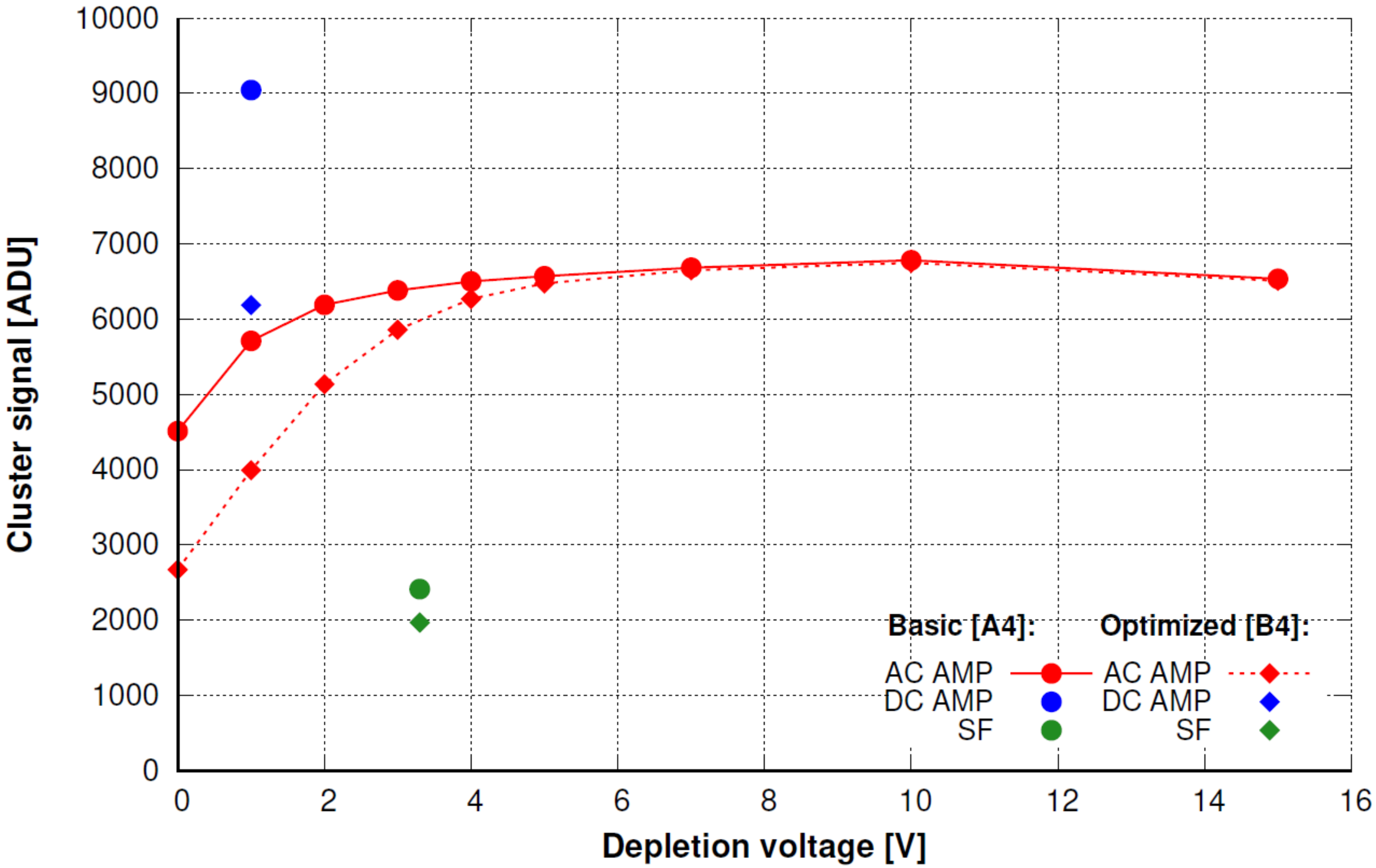
- Applying negative voltage to the substrate (back-bias) → not possible for this chip because of accompaning operating point shifts
- Utilizing AC coupling and directly biasing the collection electrode (HV_RESET)

➢ **For both sensor geometries depletion develops up to 5V**

- Above 5V, amplitudes staurates at the same level → for depleted device the detector capacitance does not depend on the sensing node geometry
- Optimized diode geometry has noticeably larger capacitance when not depleted

➢ **For DC sub-matrixes only single points available**

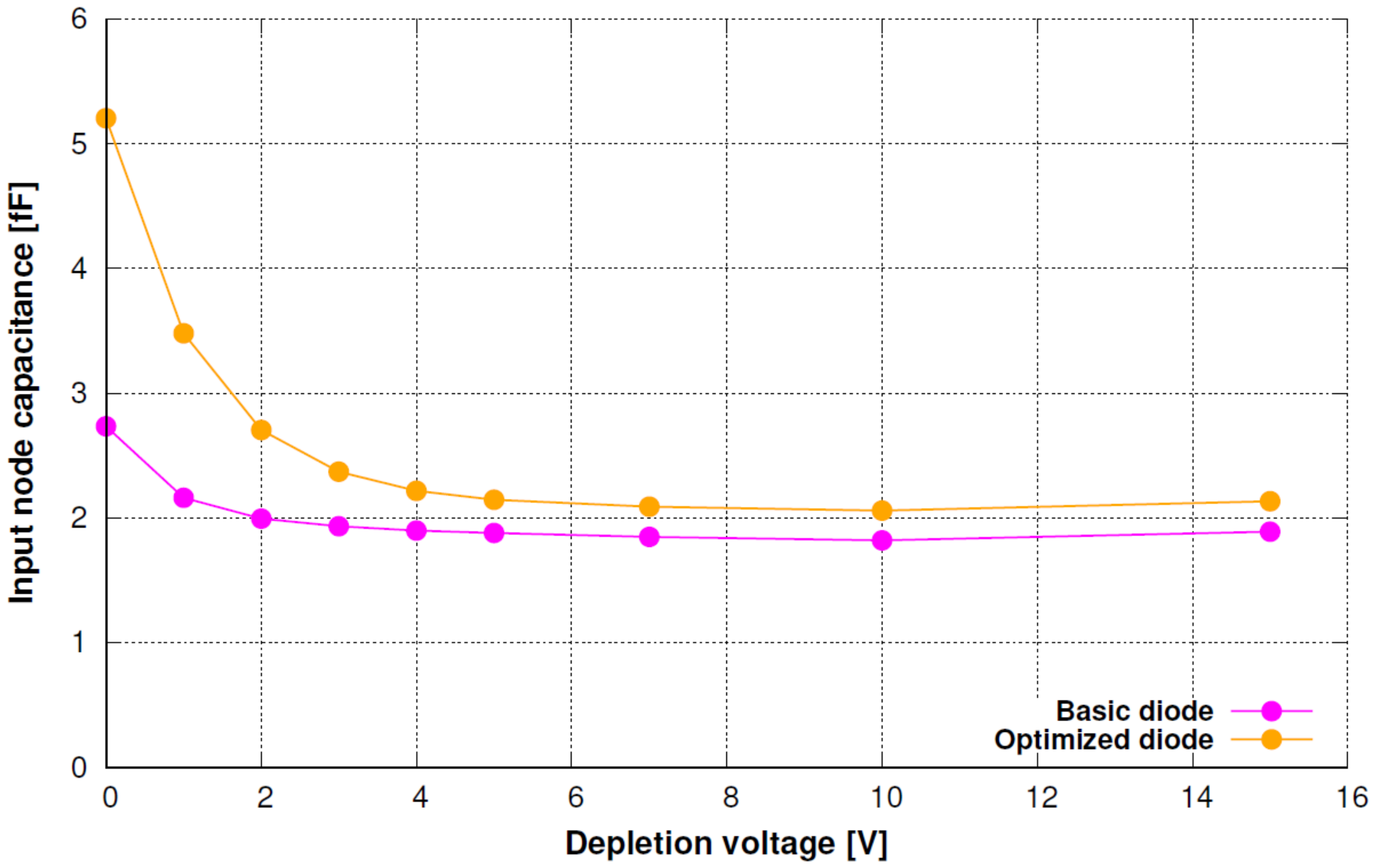
- AC-Amplifier: ~3 times higher gain than SF
- DC-Amplifier: ~5 times higher gain than SF



INPUT NODE CAPACITANCE ESTIMATION

- **Input node capacitance for the SF-structre:**
  - Indirectly obtained from the measurements by:
    - taking into account gain calibration curve
    - assuming 3.6 eV for e-h pair generation
    - using the ^{55}Fe calibration peak
- **Values obtained for the 3.3V of the depletion voltage:**
  - $C_{IN}^{A4} \approx 1.9$ fF
  - $C_{IN}^{B4} \approx 2.4$ fF

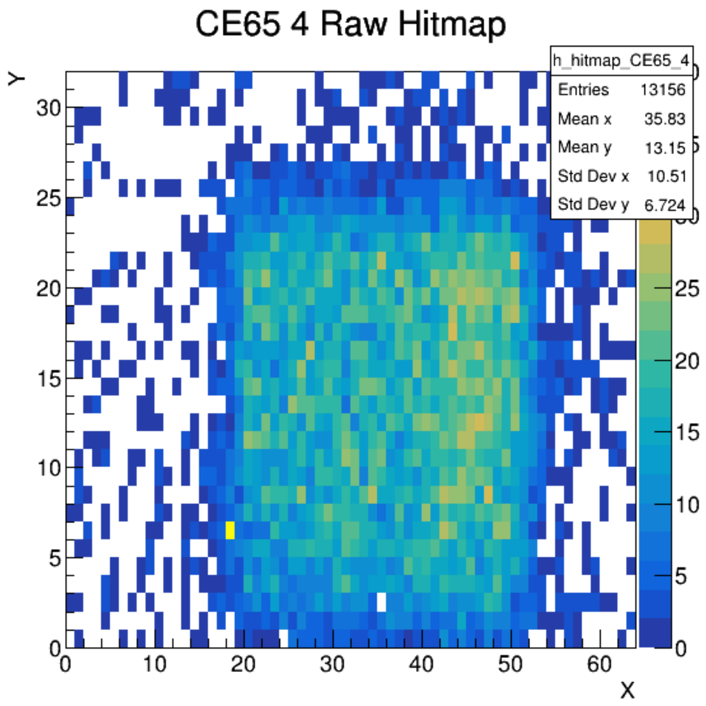
- **Assuming that input node capacitance is similar for all devices at given depletion voltage, one can exprapolate this over the whole range based on the results obtained for the AC-amplifier**

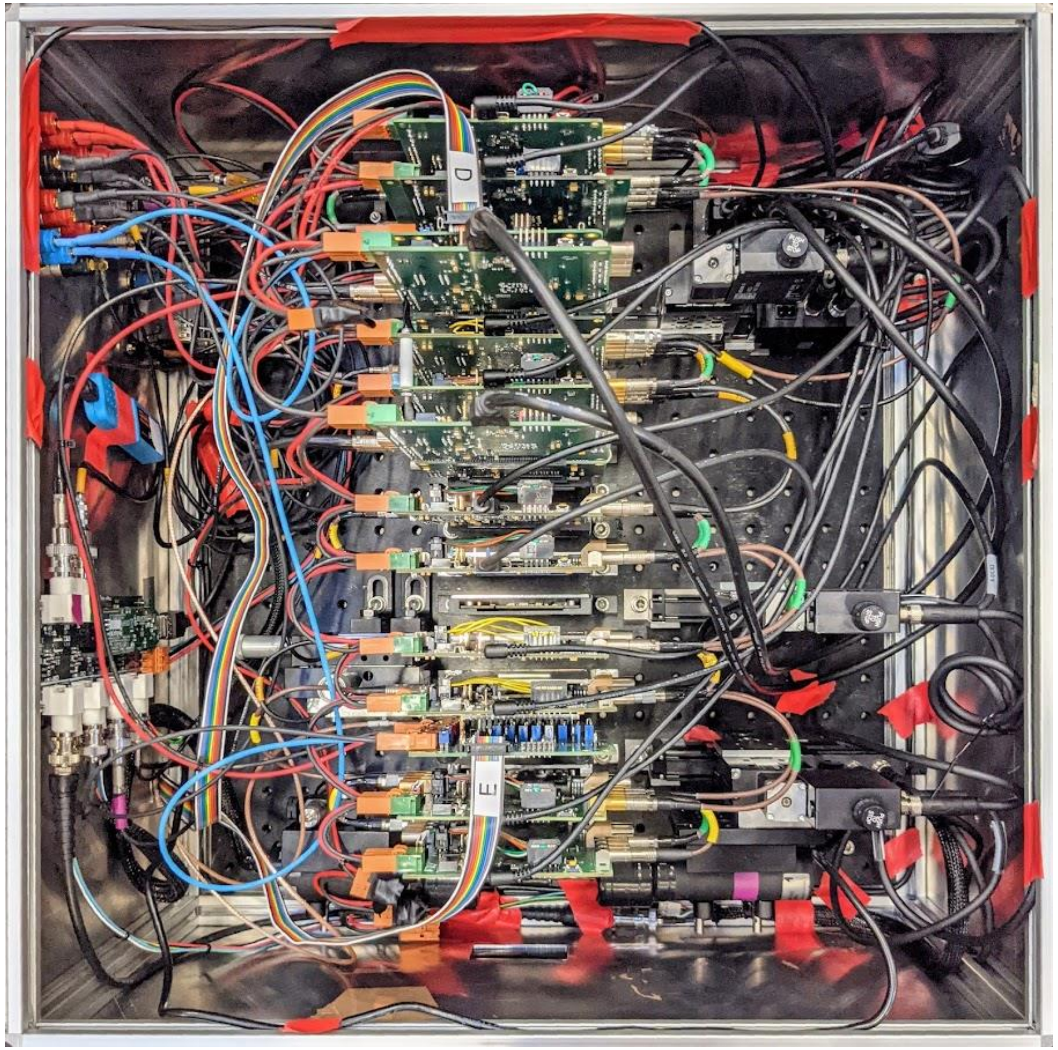


CE65 Beam Test

- **Already several test beams took place:**
  - Tracking made with Alpide telescope
  - aimed to measure different MLR1 devices (including CE65)
  - CE65 readout integrated with the telescope infrastructure and validated

- **Data analysis ongoing:**
  - Basic checks show the correlation with the telescope
  - Detailed studies of the efficiency / resolution estimations not yet finalized





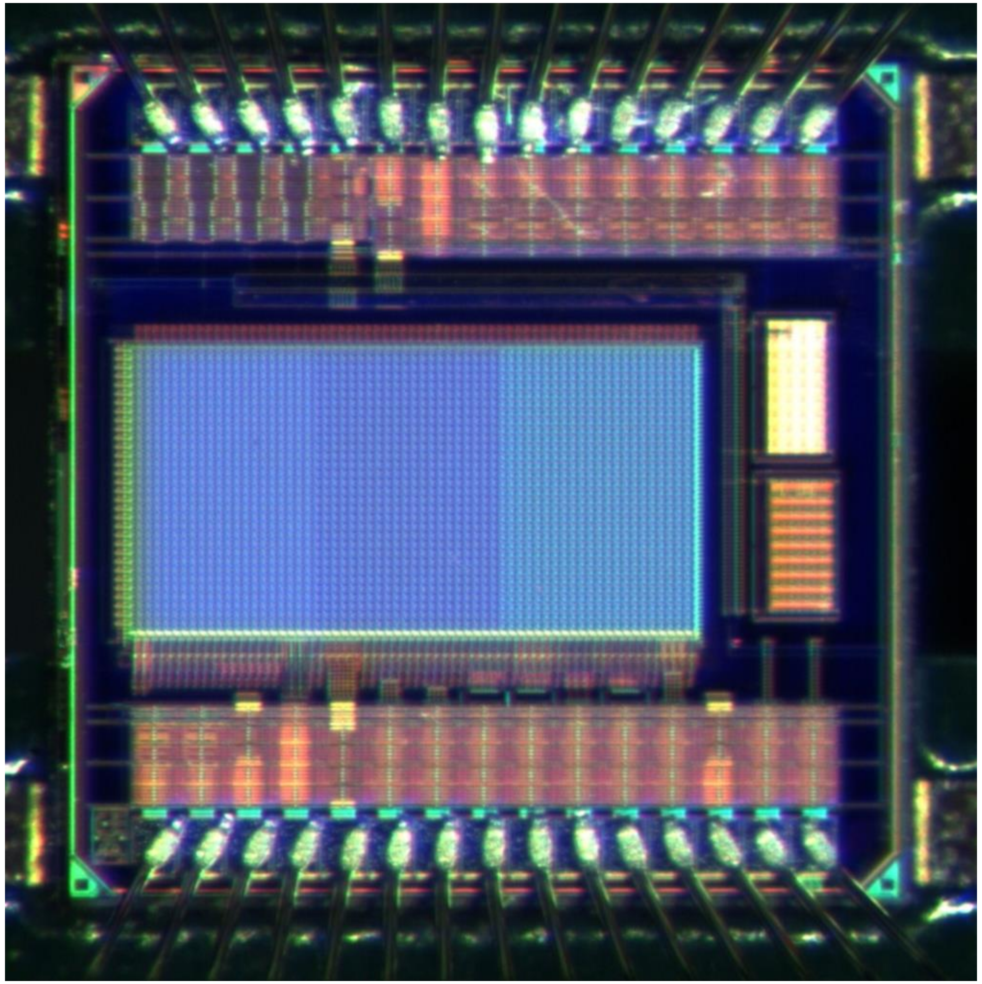
SUMMARY

- **SIGNIFICANT EFFORT MADE TO VALIDATE THE TECHNOLOGY:**
  - First prototypes received in July 2021
  - Work ongoing on many different fronts

- **MEASUREMENT RESULTS KEEPS COMING IN:**
  - Overall technology understanding is constantly growing
  - Investigating this technology in different directions (radiation tolerance, signal timing, digital pixel output)

- **CE65 OUTCOMES:**
  - **Low noise** operation, proved with the **high quality ^{55}Fe spectra**
  - Very first measurements give a clear indication that the **sensor geometry optimization has a significant impact on the charge collection properties**
    → inline with the expectations
  - Detailed level studies will be continued to build up a in-depth understanding
  - Test beam results upcoming

- **INTENSE WORK ONGOING TO FINALIZE CHIPS FOR THE SECOND SUBMISSION**
  - Revised small test prototypes (including CE65.v2)
  - Build up the variety of common functional blocks
  - Submitting a first prototypes of **a large (wafer scale) stitched sensor**

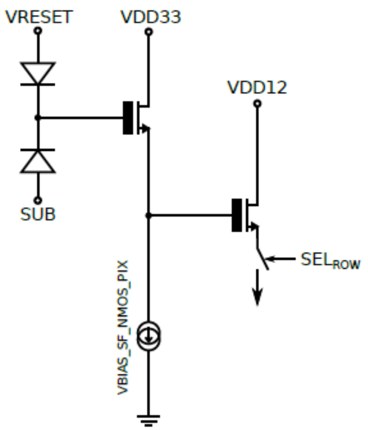


BACK-UP

CE65 CALIBRATION

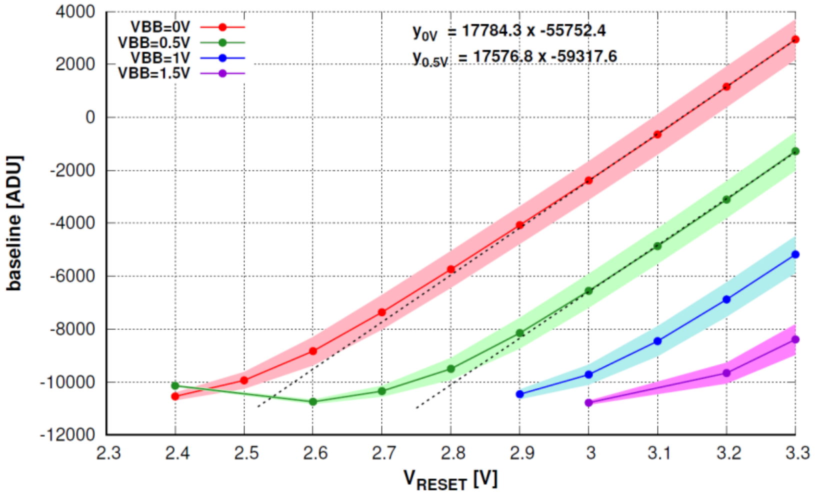
READOUT CHAIN CALIBRATION:

- Precise determinatin of conversion factor between the ADC units and input voltage level made using SF submatrix
- Monitoring baseline shift while scanning over the V_{RESET}



- Very small influnce of the back bias on the readout gain
- Significant shift of the DC levels after applying back bias
  → source followers out of dynamic range at VBB>1V
  → probably even faster for the amplifier based pixels
- Almost impossible to use back bias to enhance the depletion
- All results presented for VBB = 0V

BASIC DIODE [A4]:



OPTIMIZED DIODE [B4]: