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Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology

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Decreasing the process feature size of monolithic CMOS pixel sensors is expected to enhance their overall performance, in terms of time and spatial resolutions, power dissipation and hit handling capabilities. CERN has organized the access to the Tower 65 nm CMOS sensor process, which is currently investigated by a large consortium as a potential technological candidate for the design of sensors to be used in a wide range of future detectors, the closest in time being the ALICE-ITS3 project.

Among other exploratory chips, small pixel matrices, dubbed CE-65, with analogue outputs have been fabricated in 2021. They feature pitches of 15 and 25 μm , various amplification schemes as well as sensing layer modifications allowing for depletion under proper biasing. These prototype sensors are being tested both in labs and in beam to study their charge collection properties, which drive the main performance as detection efficiency and spatial resolution. This contribution will report on the test results contributing to the first evaluation of the detection performance of the Tower 65 nm process.

Primary experiment

ALICE

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