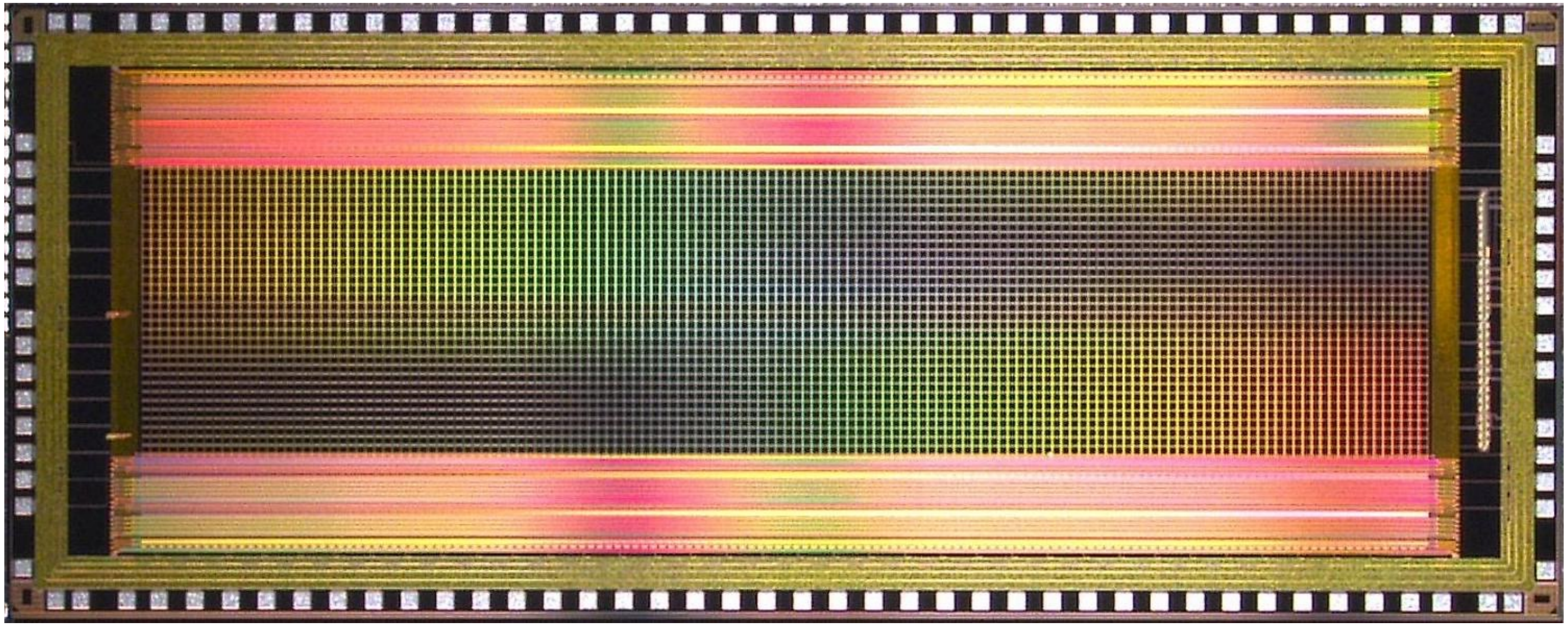
CMOS SPAD Sensor Chip for the Readout of Scintillating Fibers



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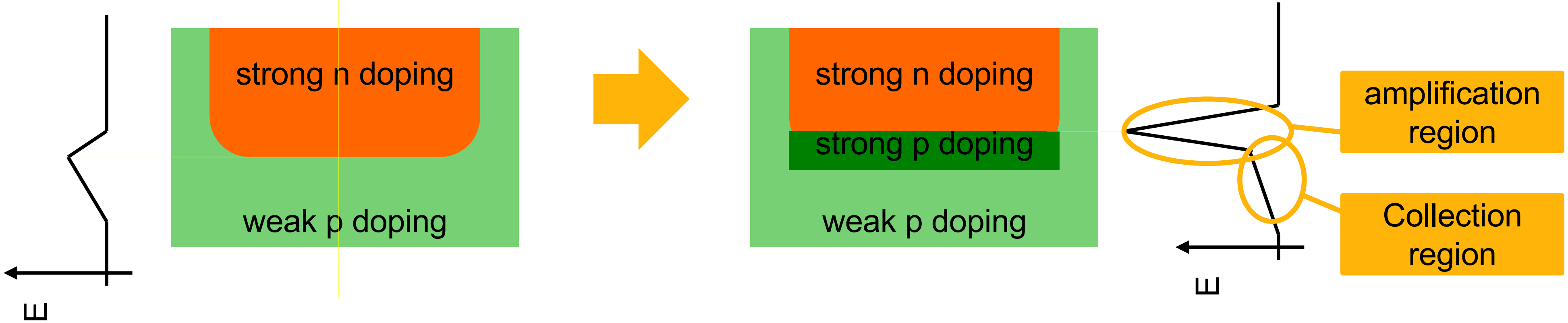
Content

- Reminder: SiPMs & Digital SiPMs
- Motivation for Fiber Readout
- Chip Architecture
- Characterisation
- Outlook and Summary

Single Photon Avalanche Photo Diode (SPAD)

- ***Goal***: Detect a single photon
- ***Problem***:
  - This photon creates only ***one*** electron-hole pair when absorbed
  - This charge is ***very*** small and ***very hard to see directly*** (electronics noise!)
- ***Solution***: Amplify the signal *in the device*
  - Create a diode with a ***very high field*** in the depletion region.
    This needs strong doping & a ‘high’ external voltage (30-300 V)



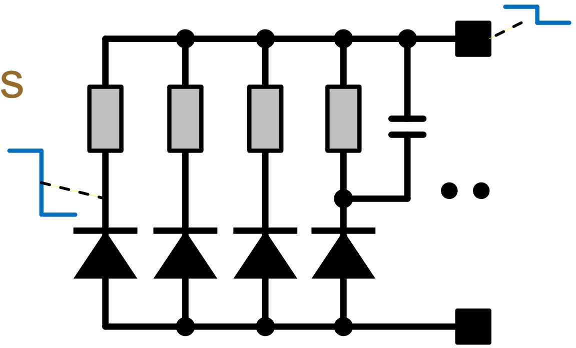
amplification region

Collection region

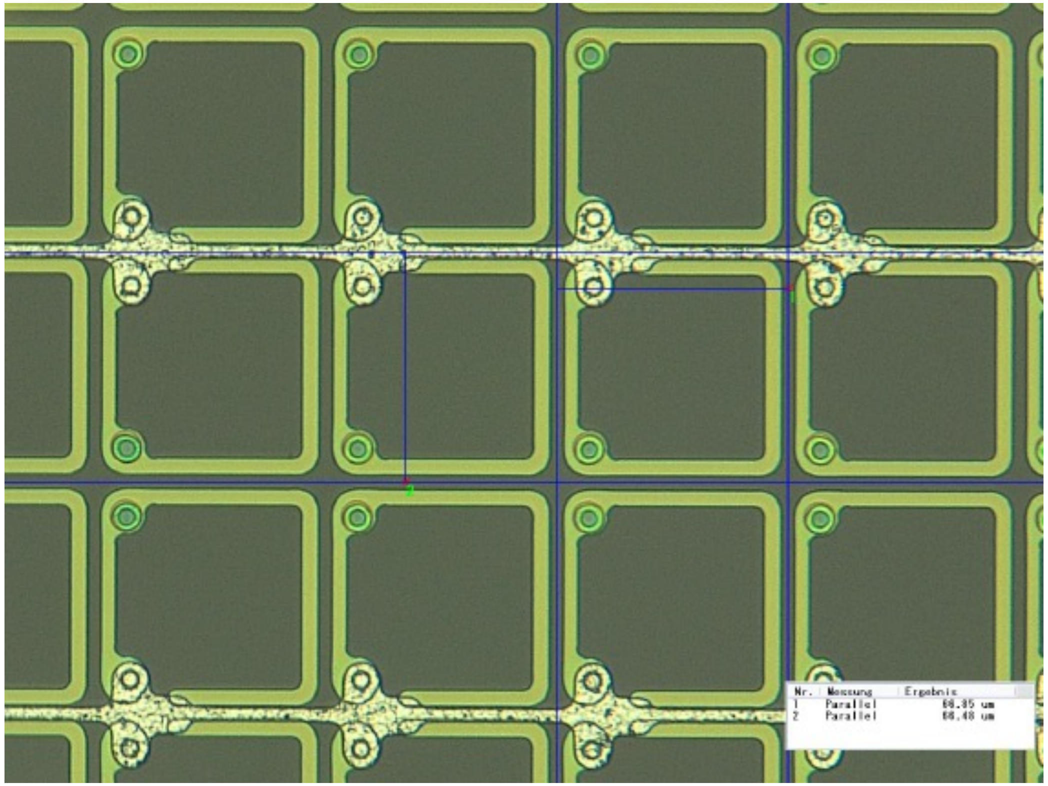
- Carriers drift from the depletion=collection region to the amplification region
- They are accelerated and create secondary ionization
  → an ***avalanche*** is created, leading to a ***large charge*** (10^5-10^6 eh pairs)
- This normally discharges the device so that the fields drop and avalanche stops

‘Silicon Photomultiplier’ (SiPM, MPPC)

- How to get a signal proportional to # photons?
  - Add many SPADs in parallel with separate quench resistors
  - Each SPAD (Single Photon APD) works in ‘Geiger’ mode
  - The total signal is proportional to the number of fired cells, i.e. to the number of detected photons



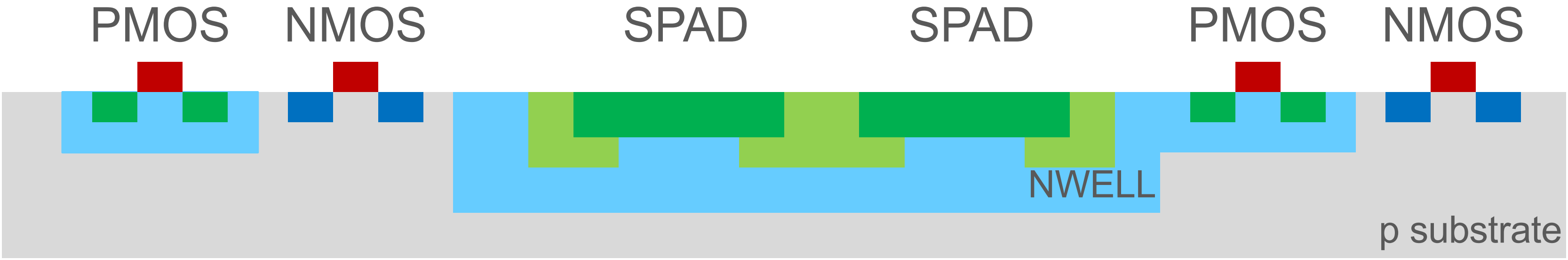
- Drawbacks:
  - Breakdown of a single SPAD creates a large (voltage) signal ‘internally’ but only a only a small (voltage) fast signal ‘outside’
  - Readout ASIC needed
    - Power!
    - Complex mechanics
  - One ‘noisy’ cell degrades device



CMOS SPADs

- An obvious extension is to add NMOS and PMOS transistors:

"CMOS SPADs" or "Digital SiPMs"



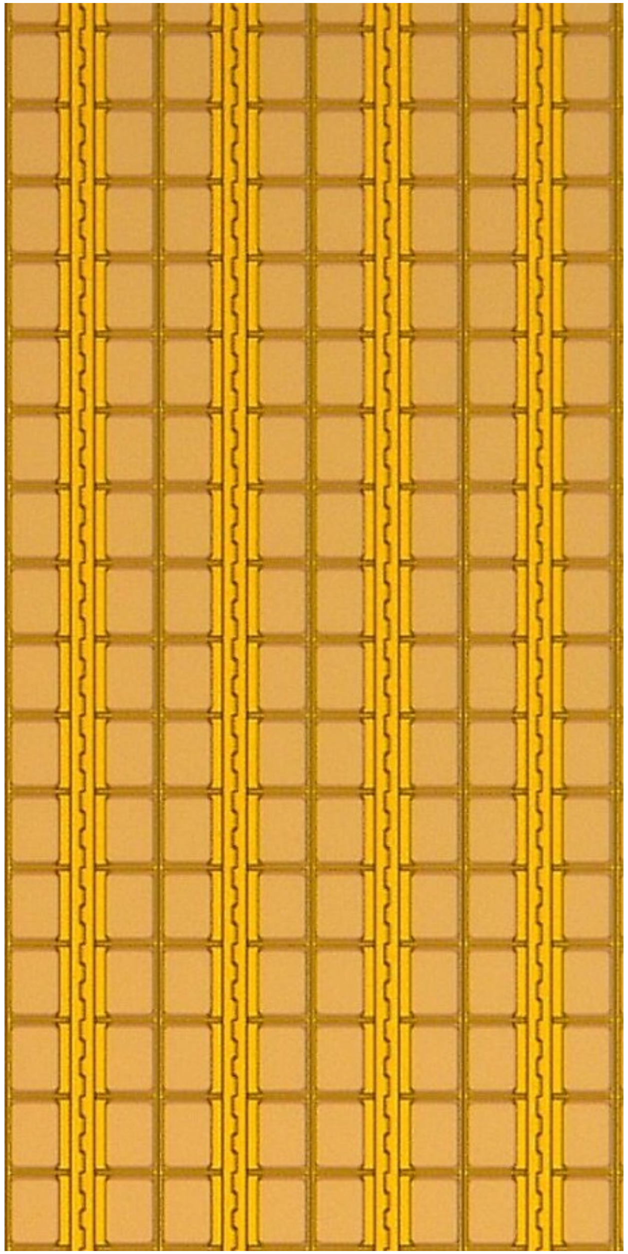
- Problem:
  - SiPMs manufacturers cannot make transistors (many process steps & know-how)
  - CMOS vendors produce SPADs of poor quality

- Solution:
  - Some CMOS vendors introduce extra processing steps and use suited wafer material to improve SPAD quality
  - This is steered by the market: High demand → more vendors…

Why CMOS SPADs?

- Advantages (compared to ‘SiPM + ASIC’)
  - Very high signal per SPAD (‘3V’)
  - Can disable ‘broken’ (noisy) SPADs
  - Specialized readout architectures possible (gating, summing, TDC, …)
  - Lower power (to be shown…)
  - Fine granular 2 D position information available
  - Simple mechanics (only one component)
  - Lower cost (to be shown…)

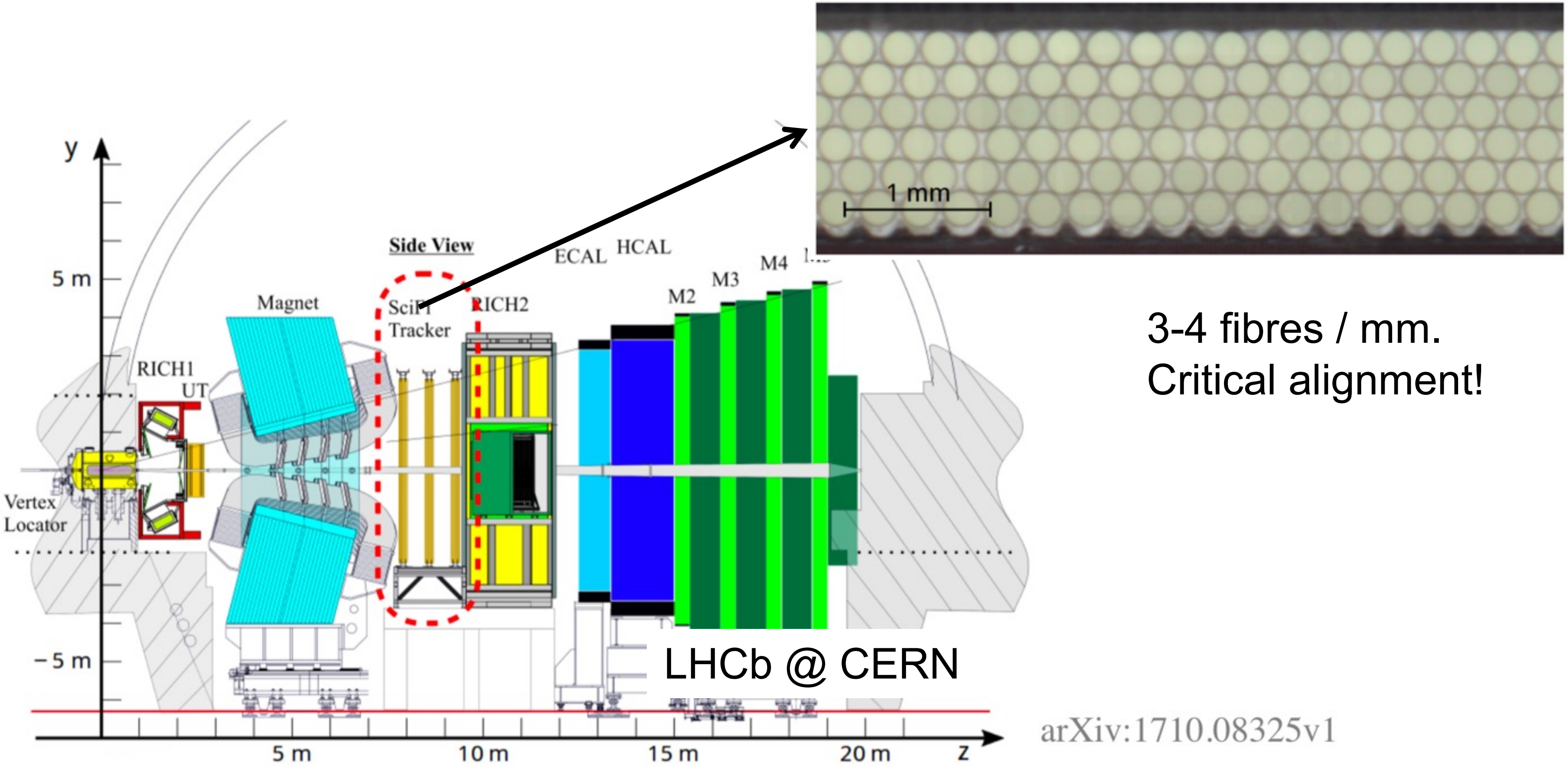
- Drawbacks
  - Often higher dark noise (but: switch off bad SPADs!)
  - Reduced fill factor (from pixel circuitry)
  - Quantum efficiency harder to optimize
  - CMOS technology often ‘simple’ (we use 350nm, 4M)
    - Limited Density → must reduce # MOS
    - ‘Slow’



Readout of Optical Fibers: Motivation

Optical Fiber Readout

- Some detectors place scintillating fibres in the sensitive volume and detect the light ‘outside’
- Example: ‘Scintillating Fibre Tracker’ of LHCb



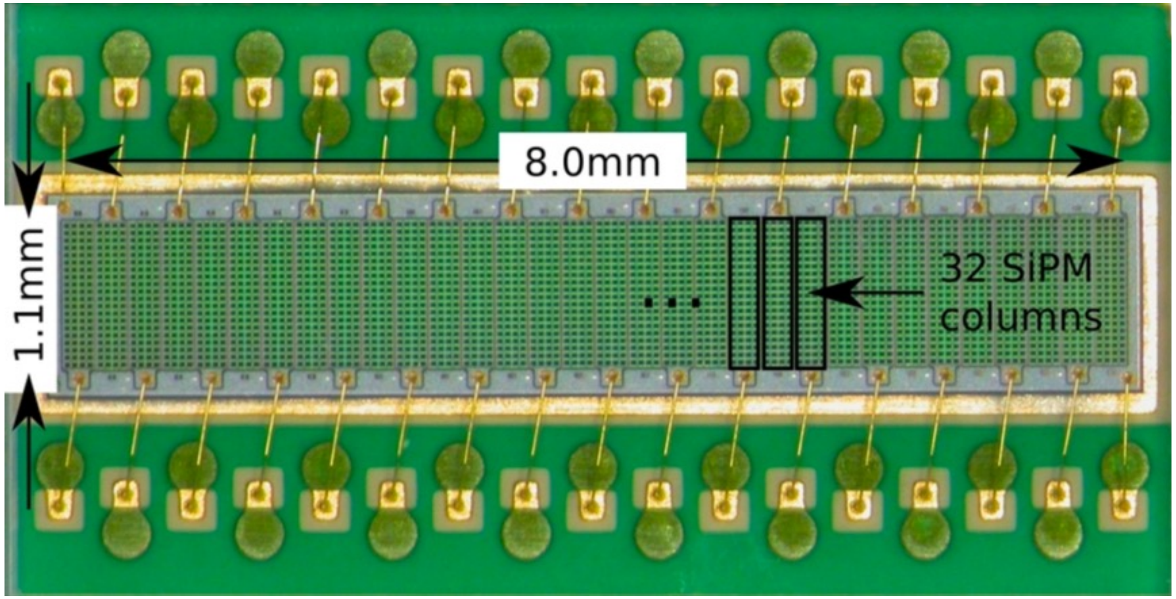
3-4 fibres / mm.
Critical alignment!

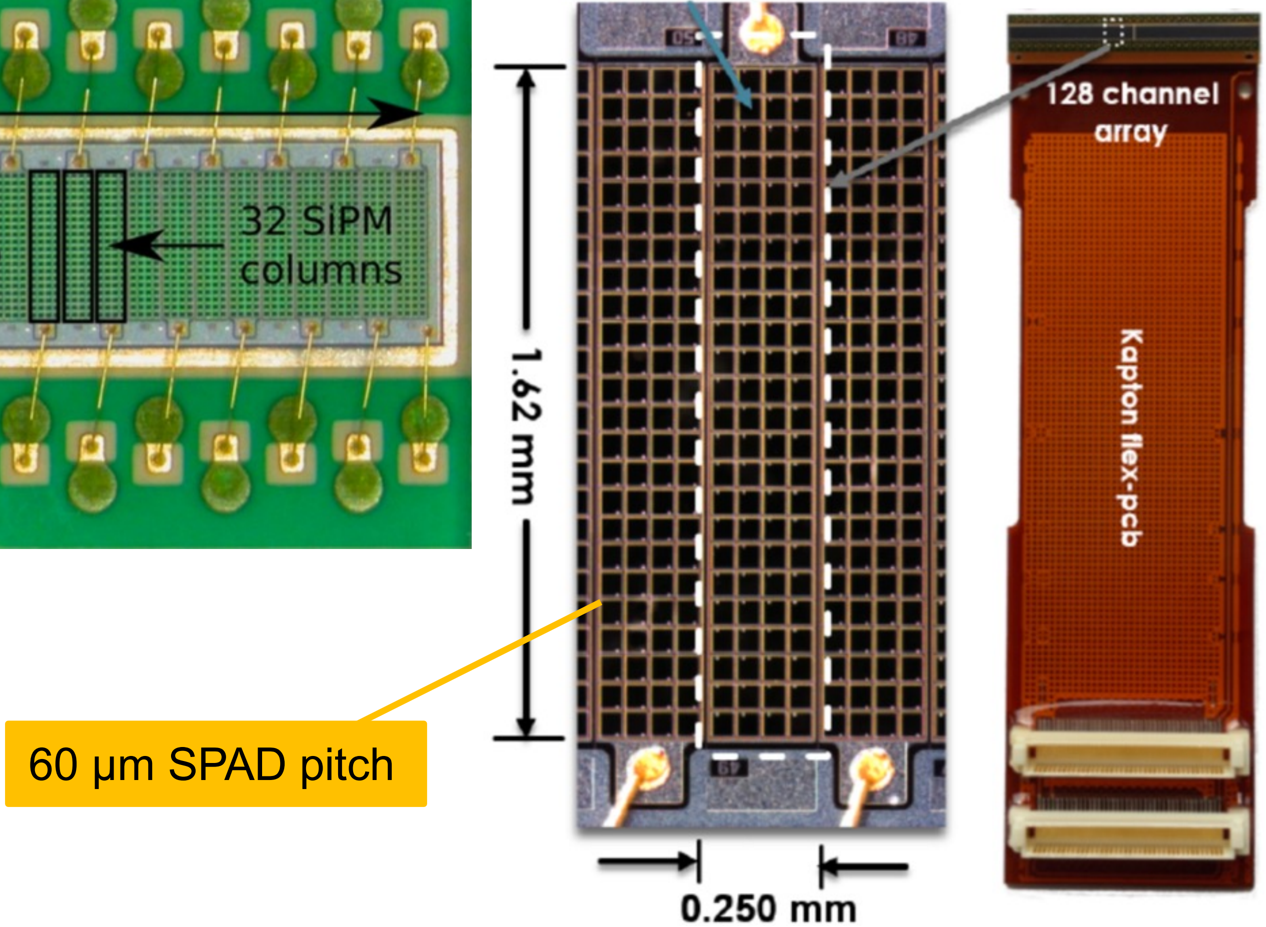
LHCb @ CERN

arXiv:1710.08325v1

State of The Art

- SiPM Arrays + Boards + Cables + dedicated ASICs (e.g. PACIFIC in LHCb)





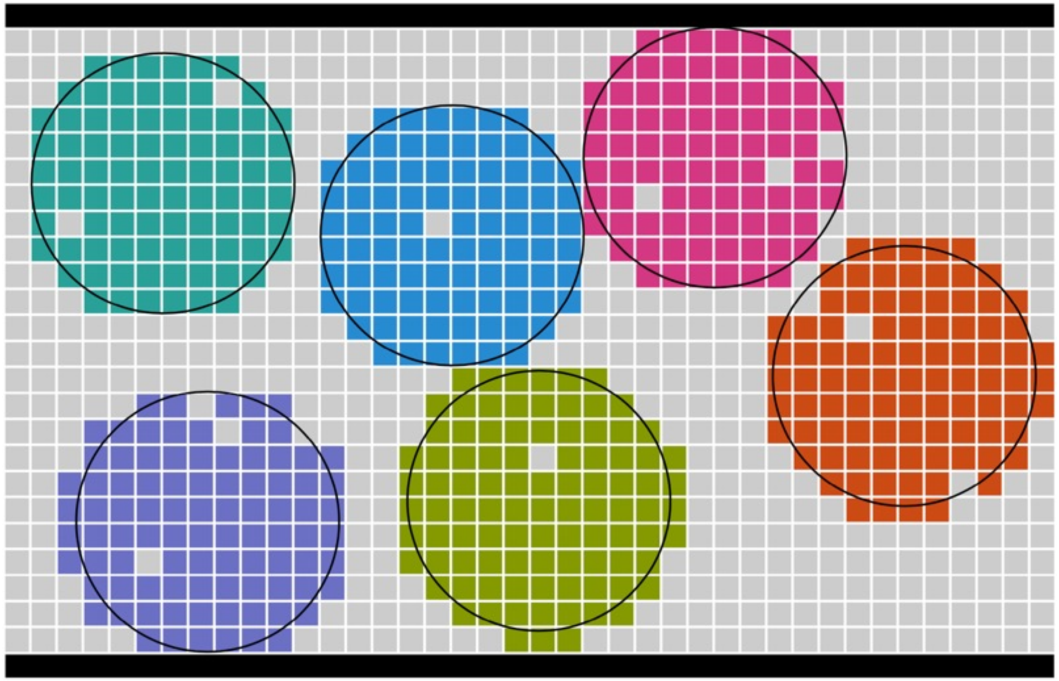
- Many parts !
- Critical Alignment !
- Expensive !
- Modest timing !

arXiv:1011.0226v1
arXiv:1710.08325v1

Using CMOS SPADs:
Concept and Implementation Details

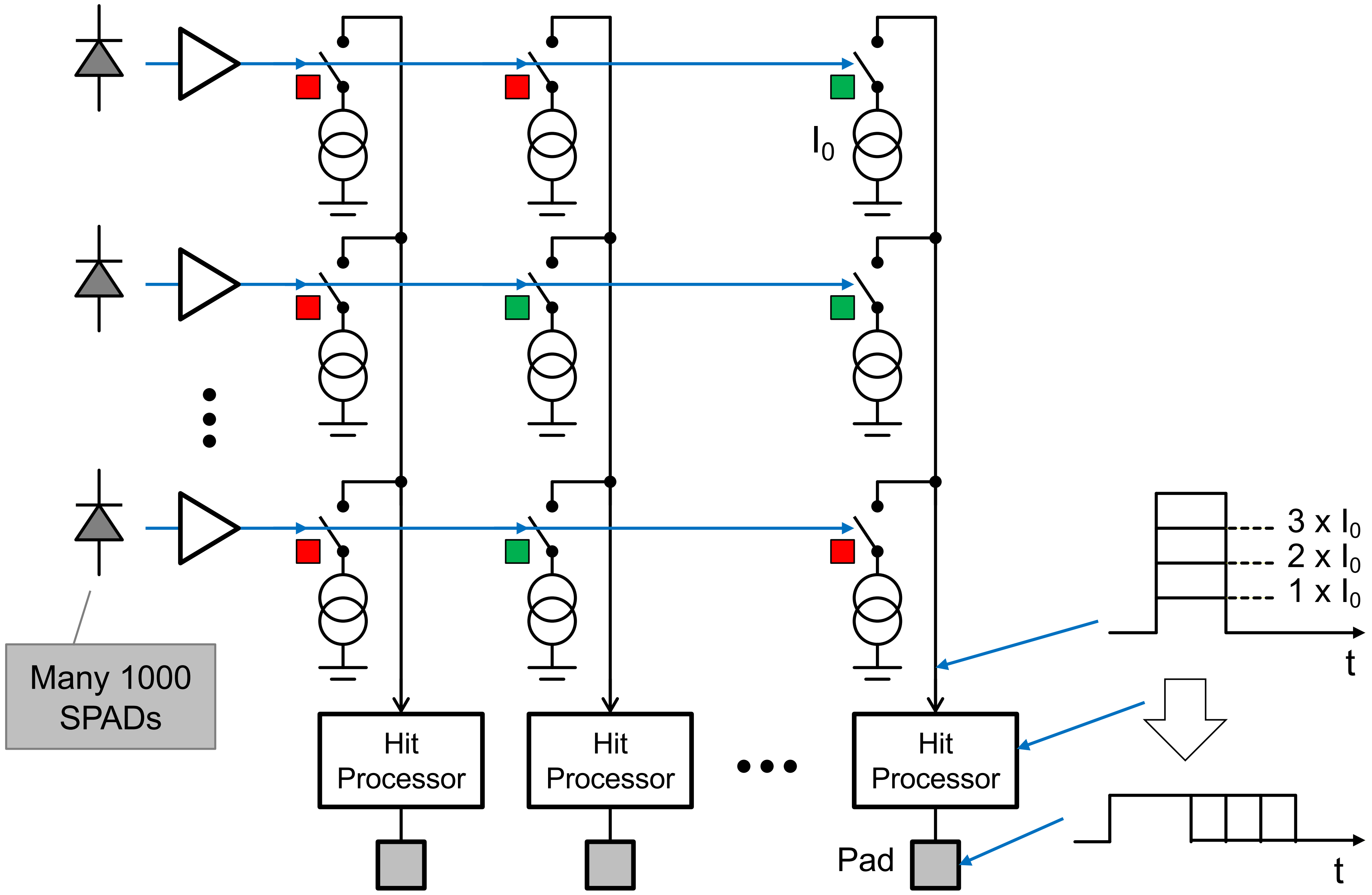
SPAD Group Readout Architecture

- Each SPAD can be freely assigned to a ‘group’ (by programming the chip)
- # of hits in a group is ‘counted’ and sent to a (single) output pin per group



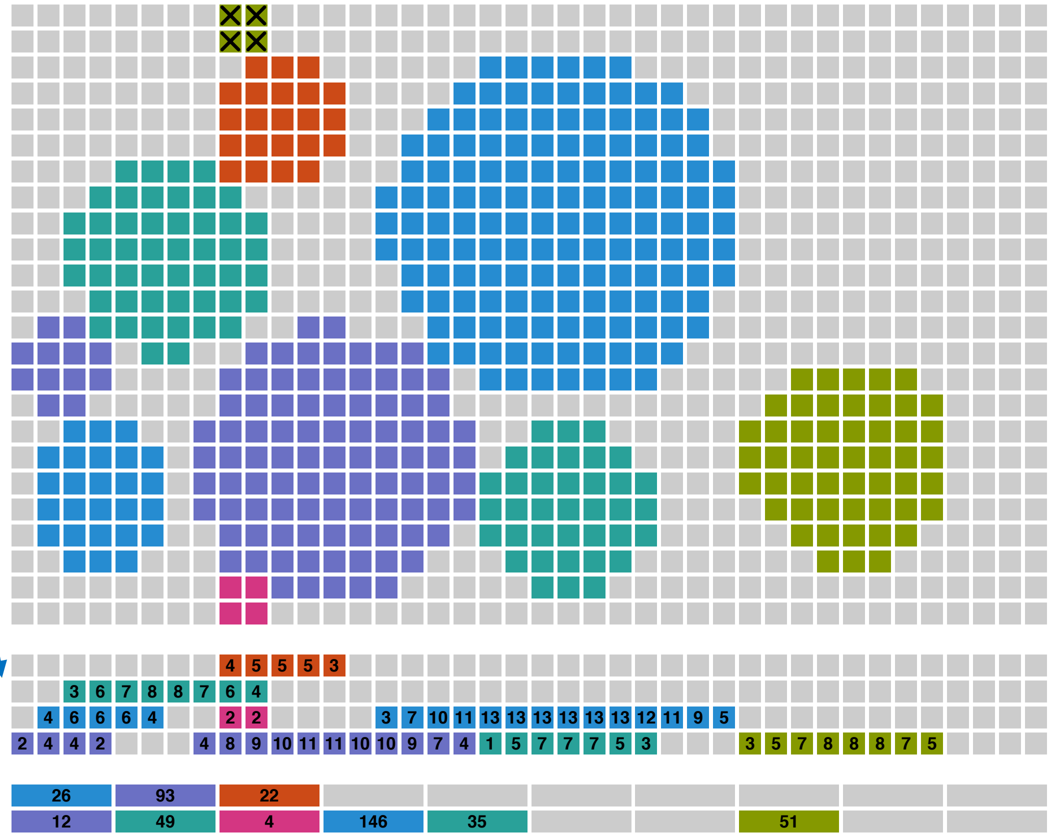
- Alignment (of fibres) fully uncritical
- No dark noise from ‘unused’ SPADs
- Simple system with only **one element (**sensor + readout)
- Fair timing (~ 500ps so far)

Concept of Group Assignment



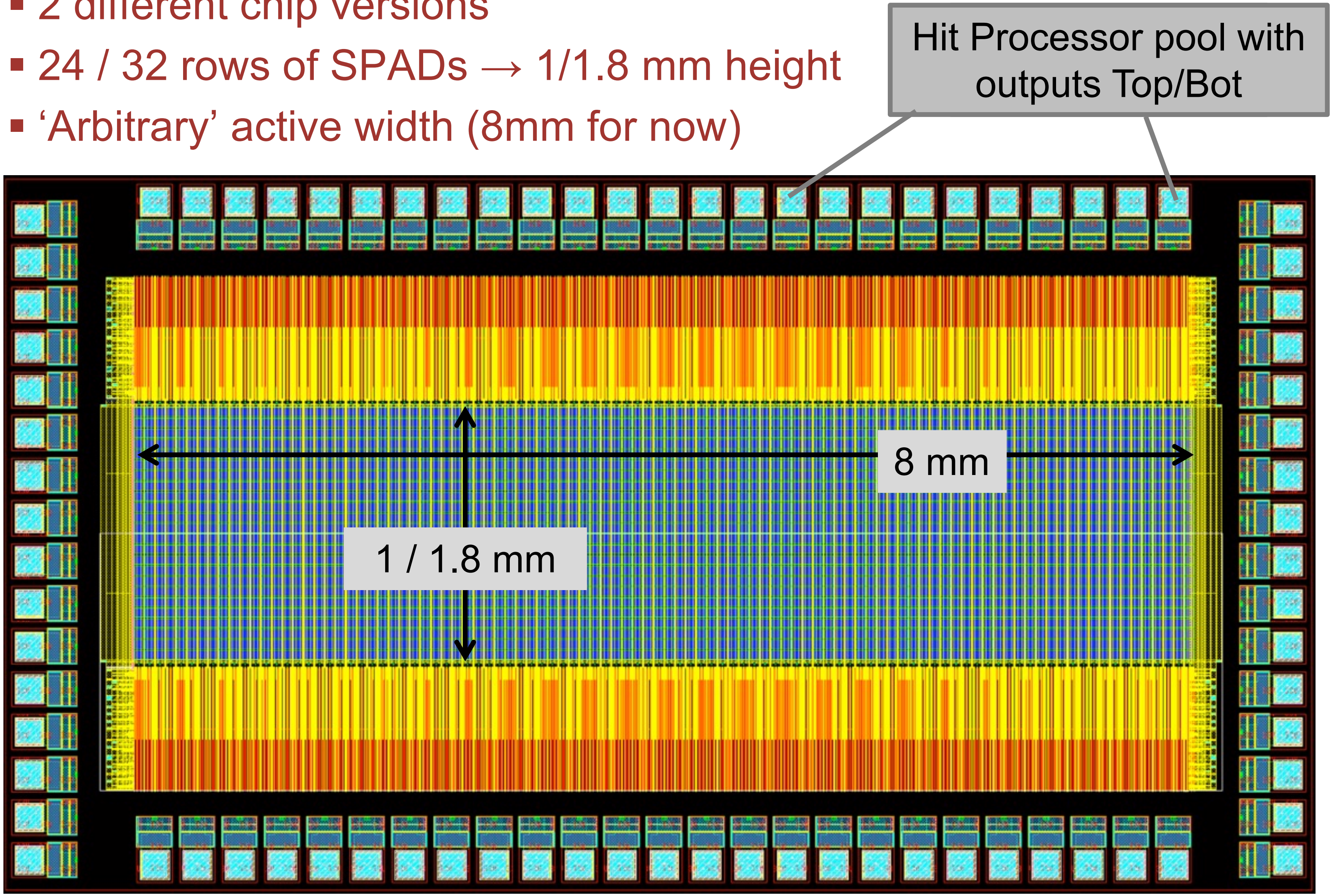
Architectural Challenge

- Assigning EACH SPAD on the chip to EACH group would require too many configuration bits.
- Solution: Exploit that groups contain ‘only’ *neighboring* SPADs
  - Work at column level
  - Each column has 4 ‘*local*’ groups
  - A SPAD can contribute to each such group (→ 4 bits/SPAD)
  - 4 ‘group repeaters’ buffer the local group signals
  - Local groups are then merged in the periphery to ‘final’ groups
  - Each merged group is assigned to a hit processors (from a pool)



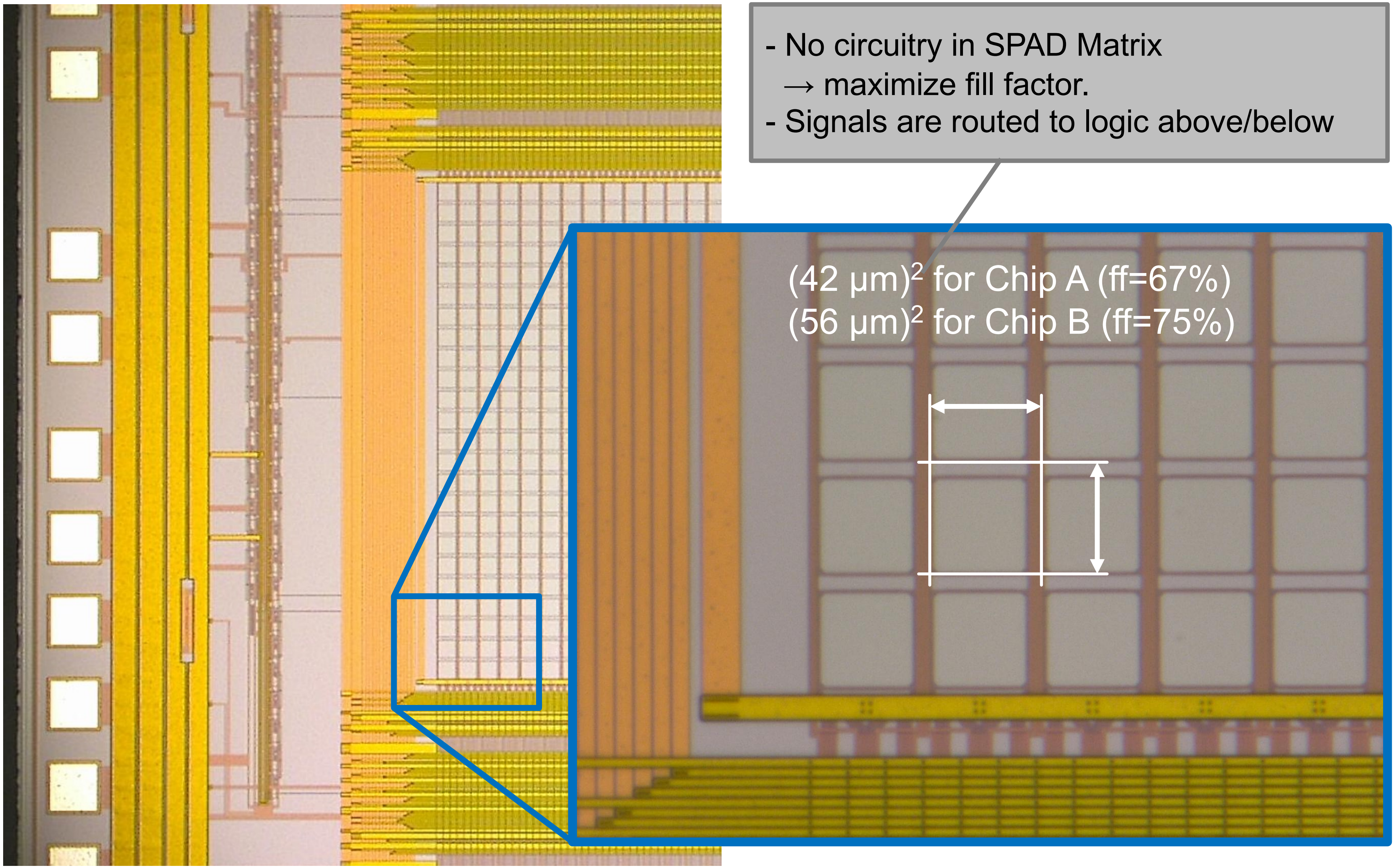
Demonstrator Chips

- 2 different chip versions
- 24 / 32 rows of SPADs → 1/1.8 mm height
- ‘Arbitrary’ active width (8mm for now)


Hit Processor pool with outputs Top/Bot

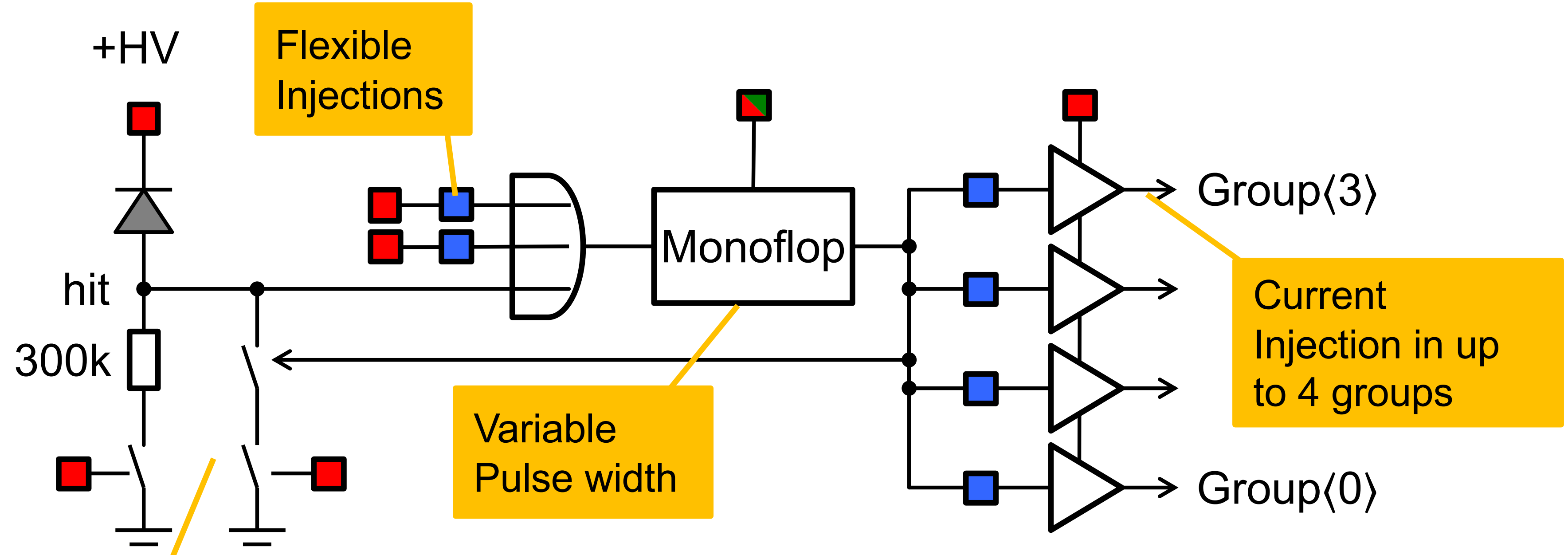
Chip Detail

- No circuitry in SPAD Matrix
  → maximize fill factor.
- Signals are routed to logic above/below



(42 μm)^2 for Chip A (ff=67%)
(56 μm)^2 for Chip B (ff=75%)

Circuit Detail 1: Circuit per SPAD



Flexible Injections

Variable Pulse width

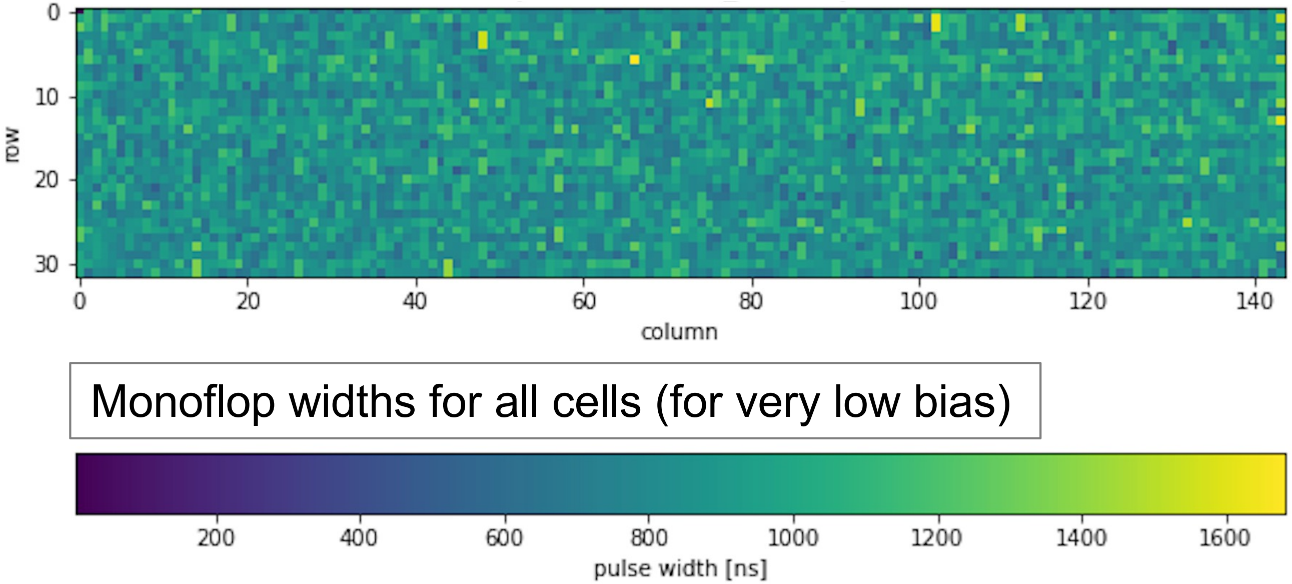
Current Injection in up to 4 groups

SPAD recharge via resistor or active

🟦 : Local configuration bit

🟩 : Global signal

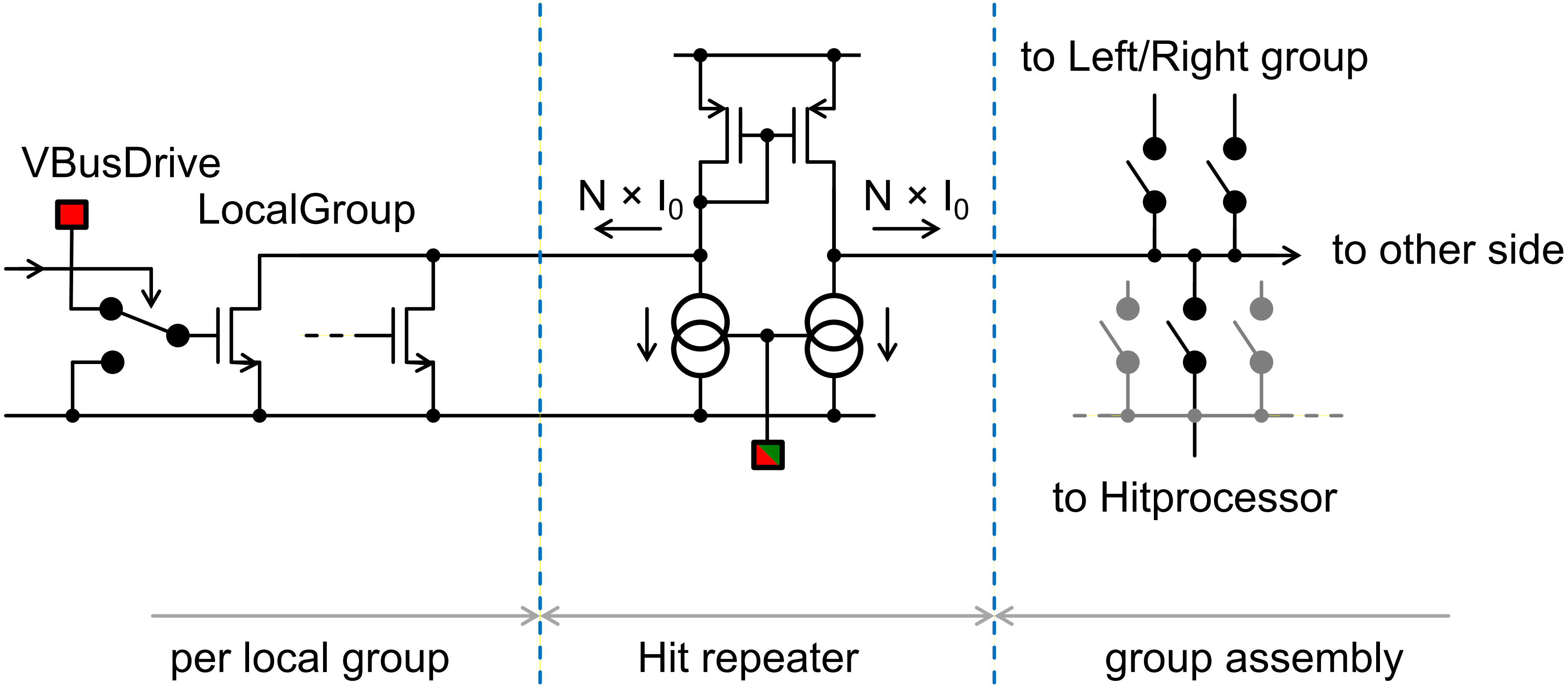
🟥 : Chip pin



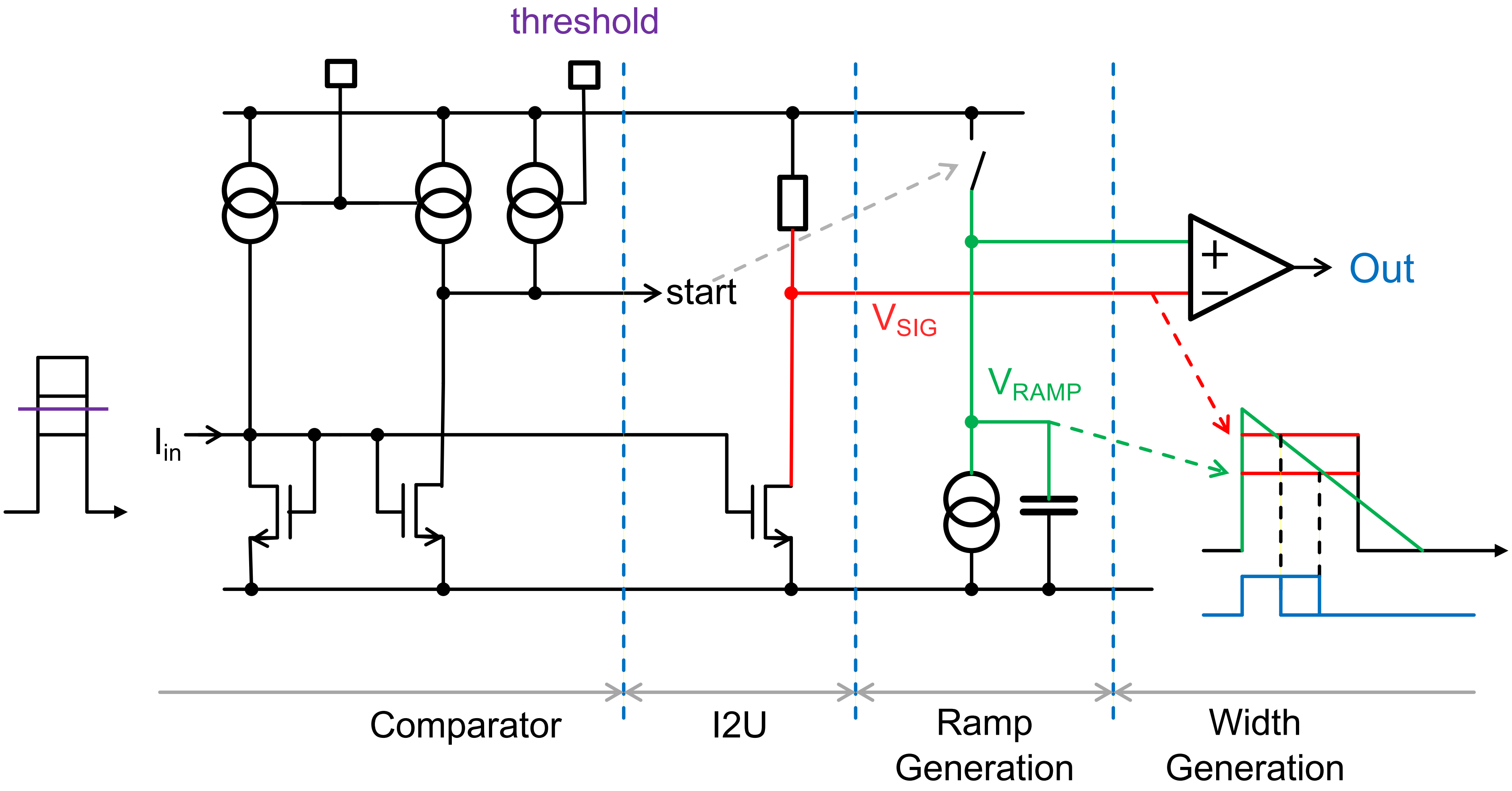
Monoflop widths for all cells (for very low bias)

Circuit Detail 2: Hit Repeater

- Low bus impedance by diode-connected PMOS
  - Many such groups – must watch power dissipation!

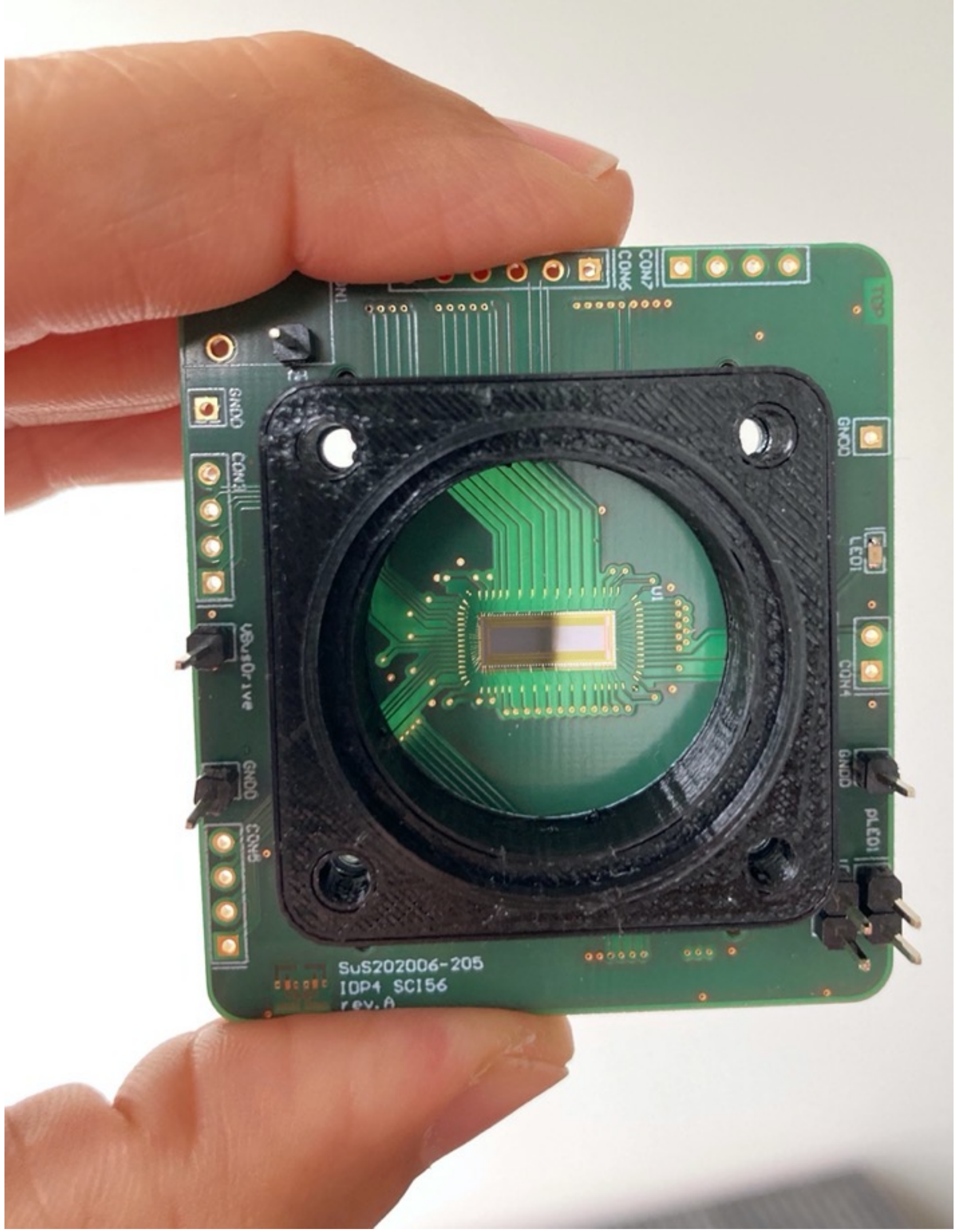


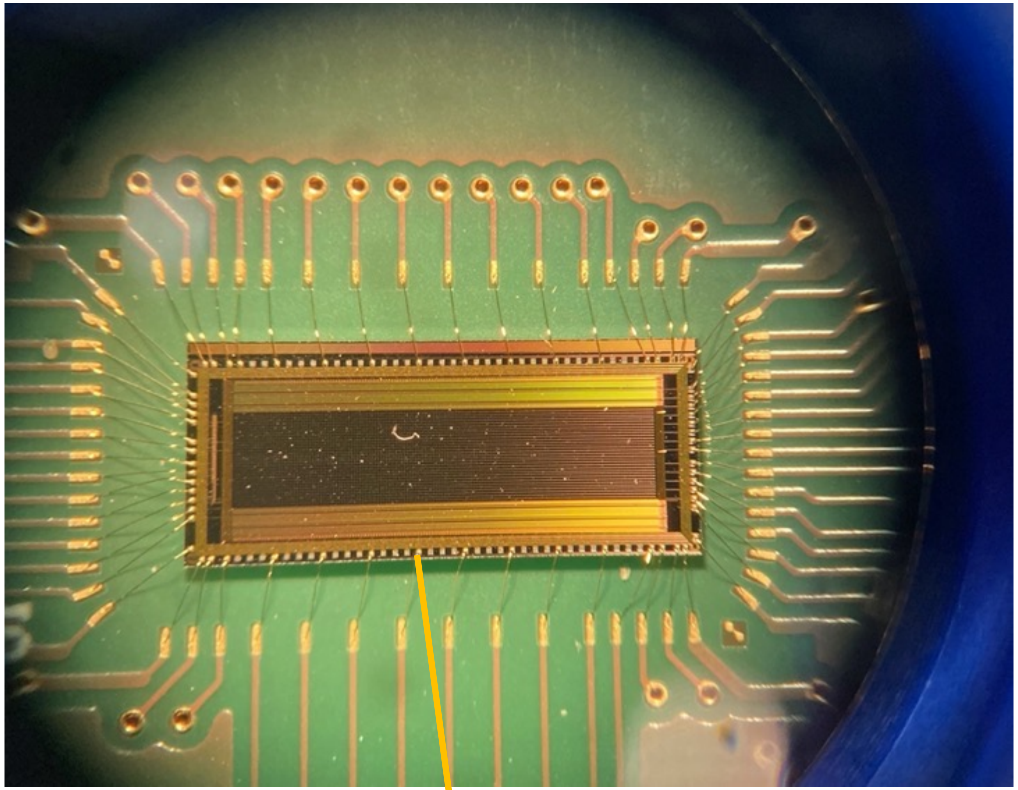
Circuit Detail 3: Hit Processor (simplified)



- Unused processors can be disabled (~150 uW / processor)

Chip on Test Board



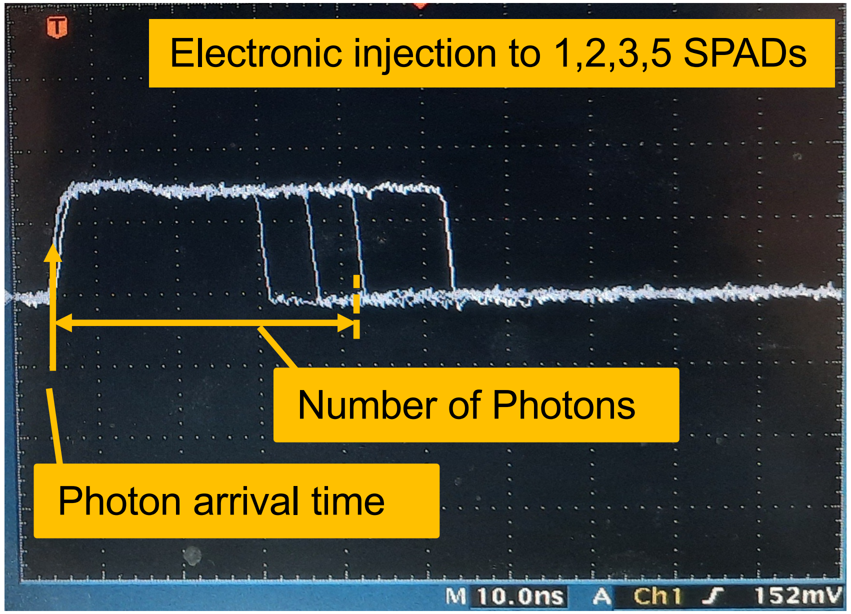


Only a fraction of the hit processors are bonded

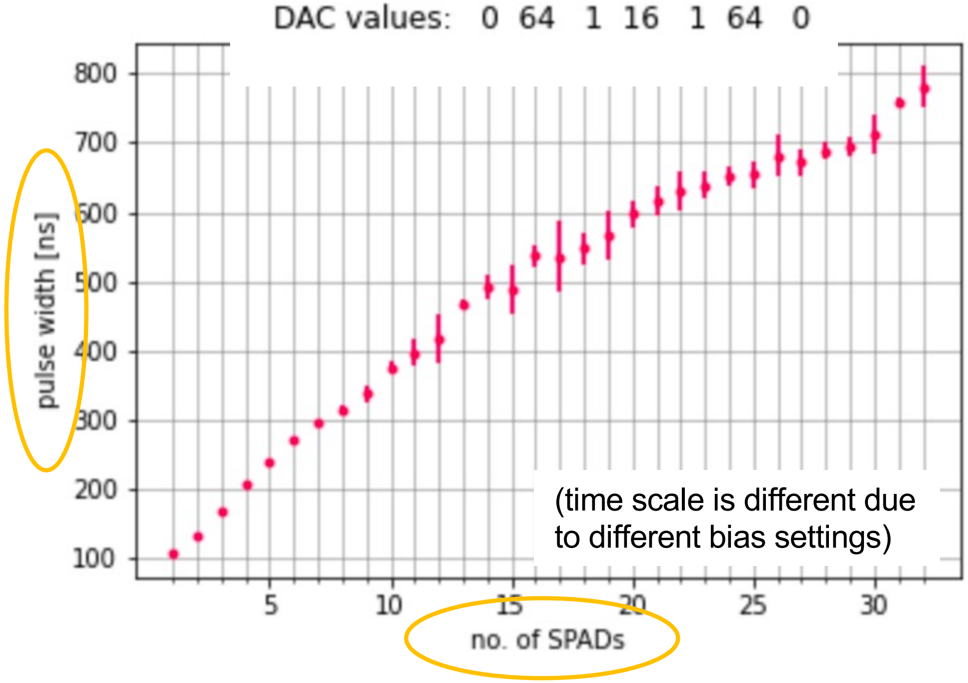
Chip Operation: Multiplicity Output

- *Hit 'arrival' time* given by rising edge
- Group *Multiplicity* is encoded as pulse width
- Low # of photons expected in application. Multiplicities up to 30 tested
  - Resolution degrades for many hits due to mismatch of current sources
  - Still need to optimize settings…

Hit Processor Output:



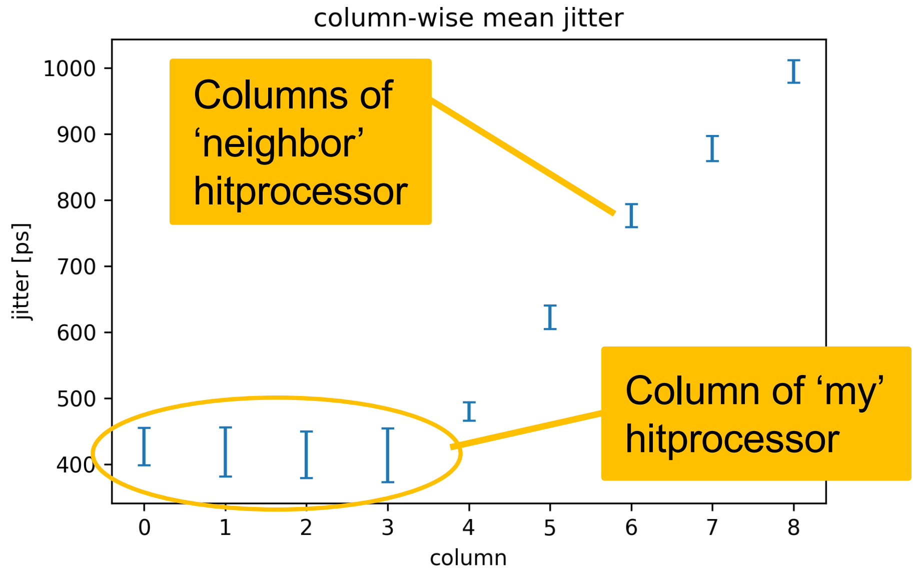
(BSc thesis R. Zimmermann)



(time scale is different due to different bias settings)

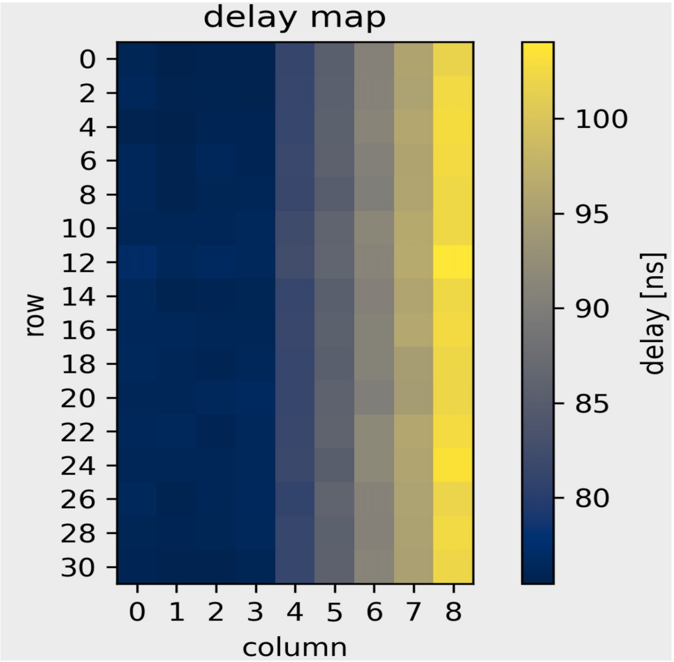
Chip Operation: Jitter

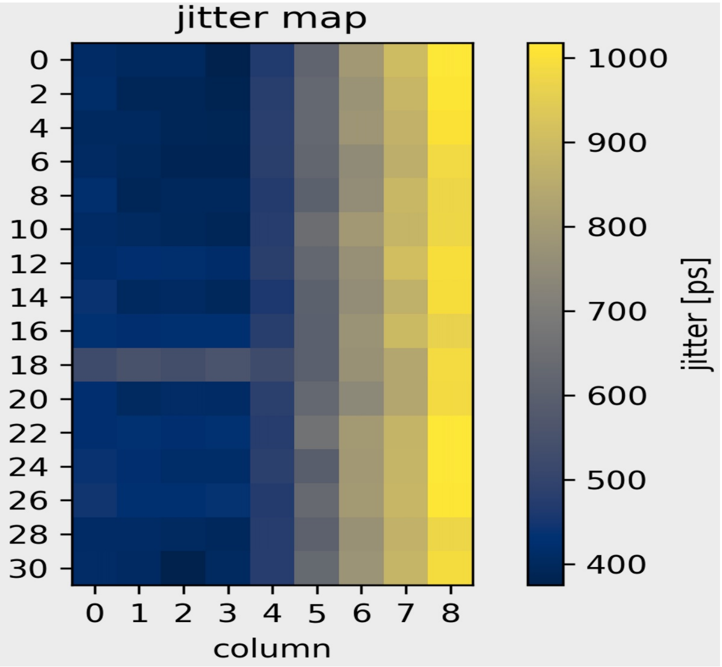
- Larger groups slow down signals (large capacitance)
- Jitter for groups ’close’ to hit processor is < 500ps
- Depends very much on power allowed

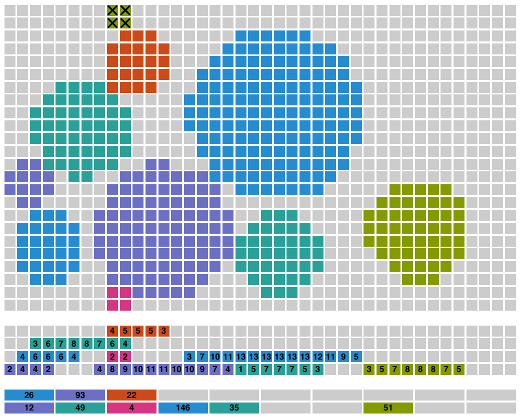


Columns of ‘neighbor’ hitprocessor

Column of ‘my’ hitprocessor



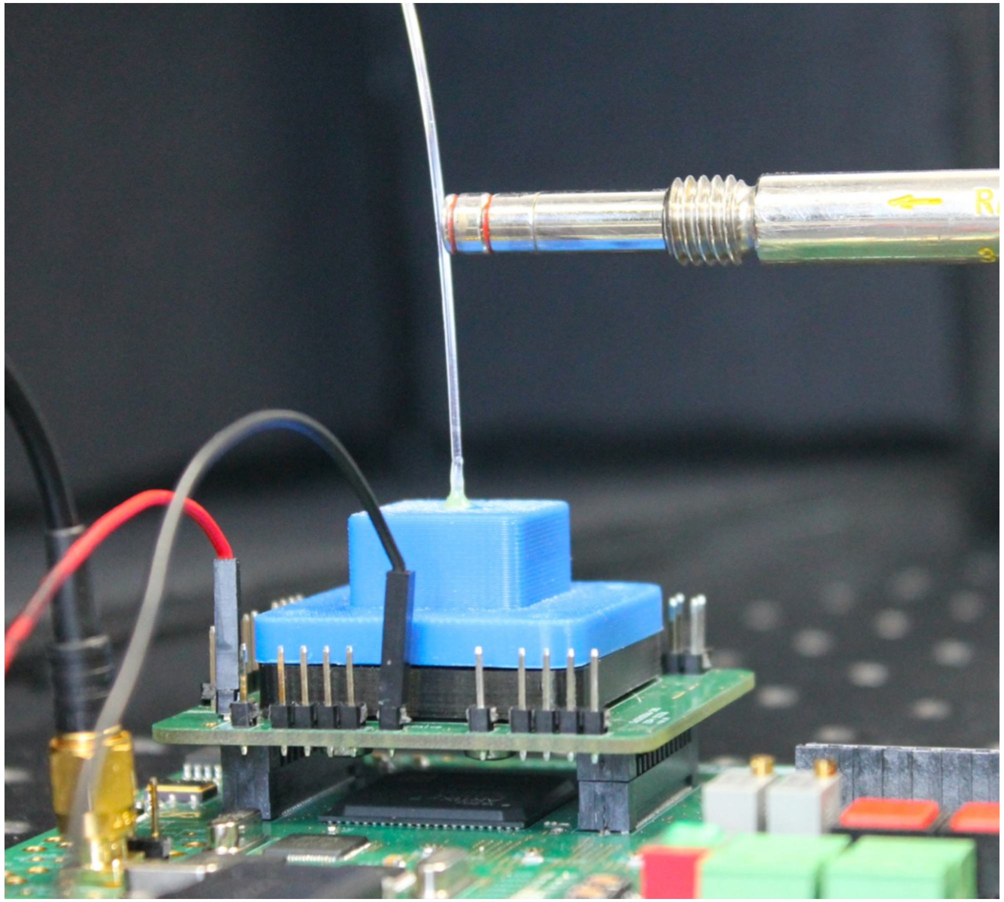


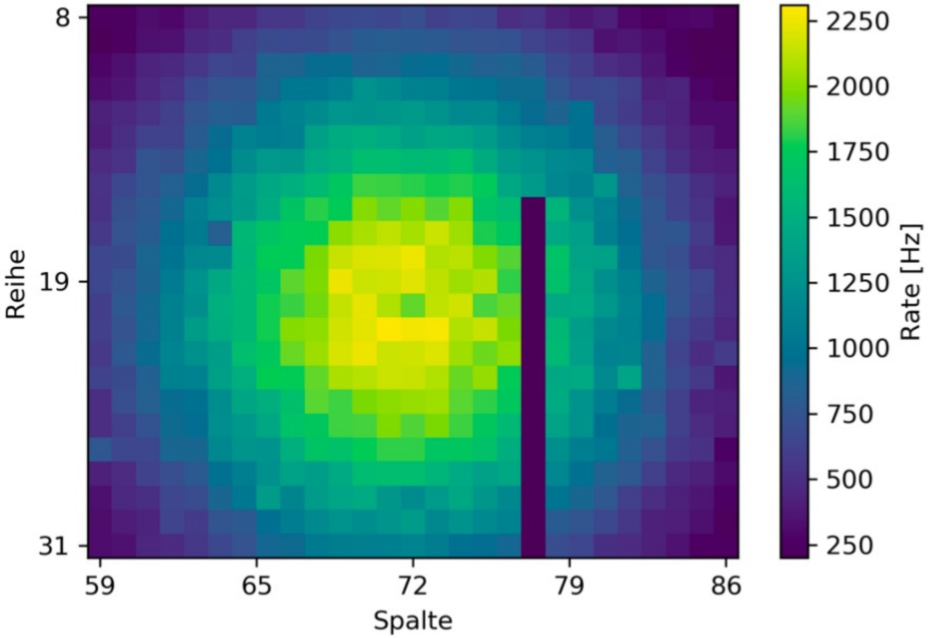


(R. Zimmermann)

Readout of Single Fiber

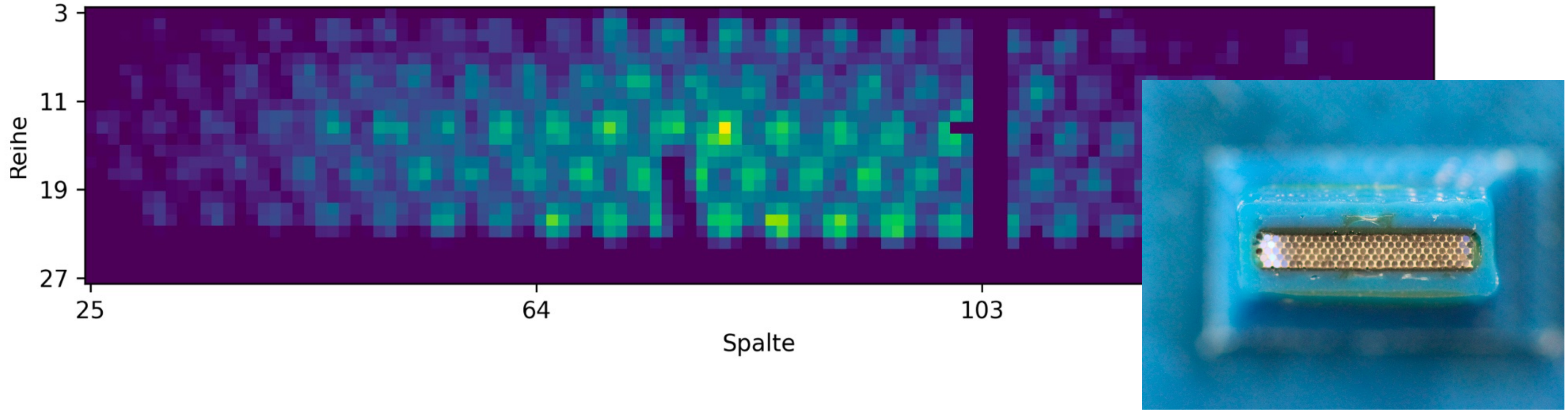
- Single scintillating fiber illuminated with radioactive source
  - (Fiber not touching chip -> wide light spread)



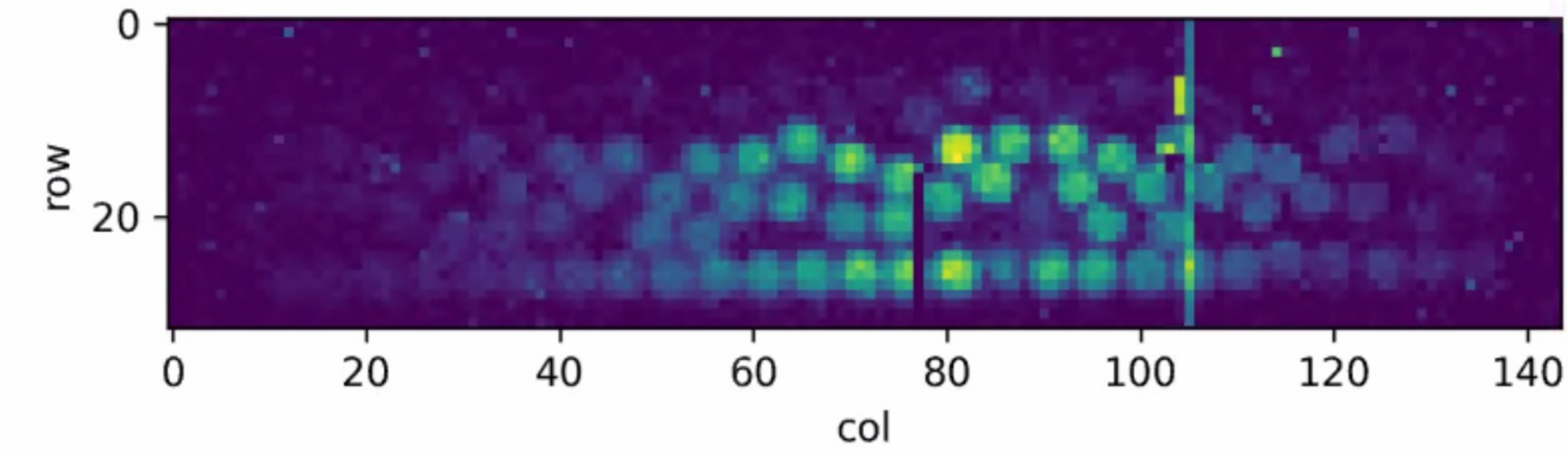


Imaging of Fiber Bundles

(BSc thesis B. Maisano, PI)



- This bundle nicely shows that fiber alignment is not critical:

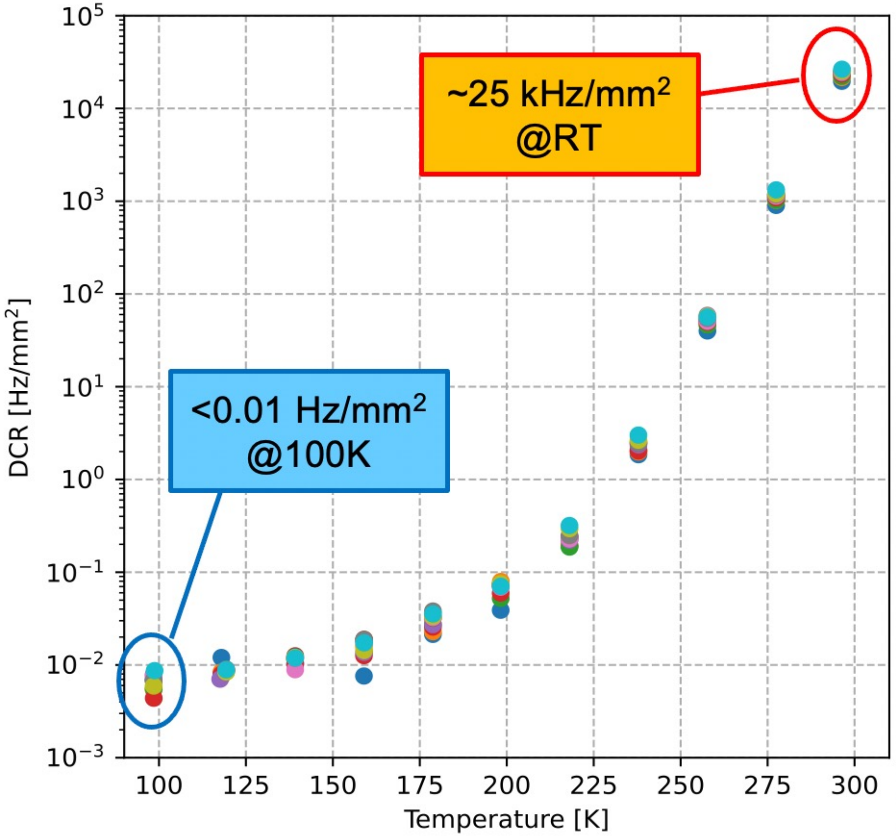


Next Steps

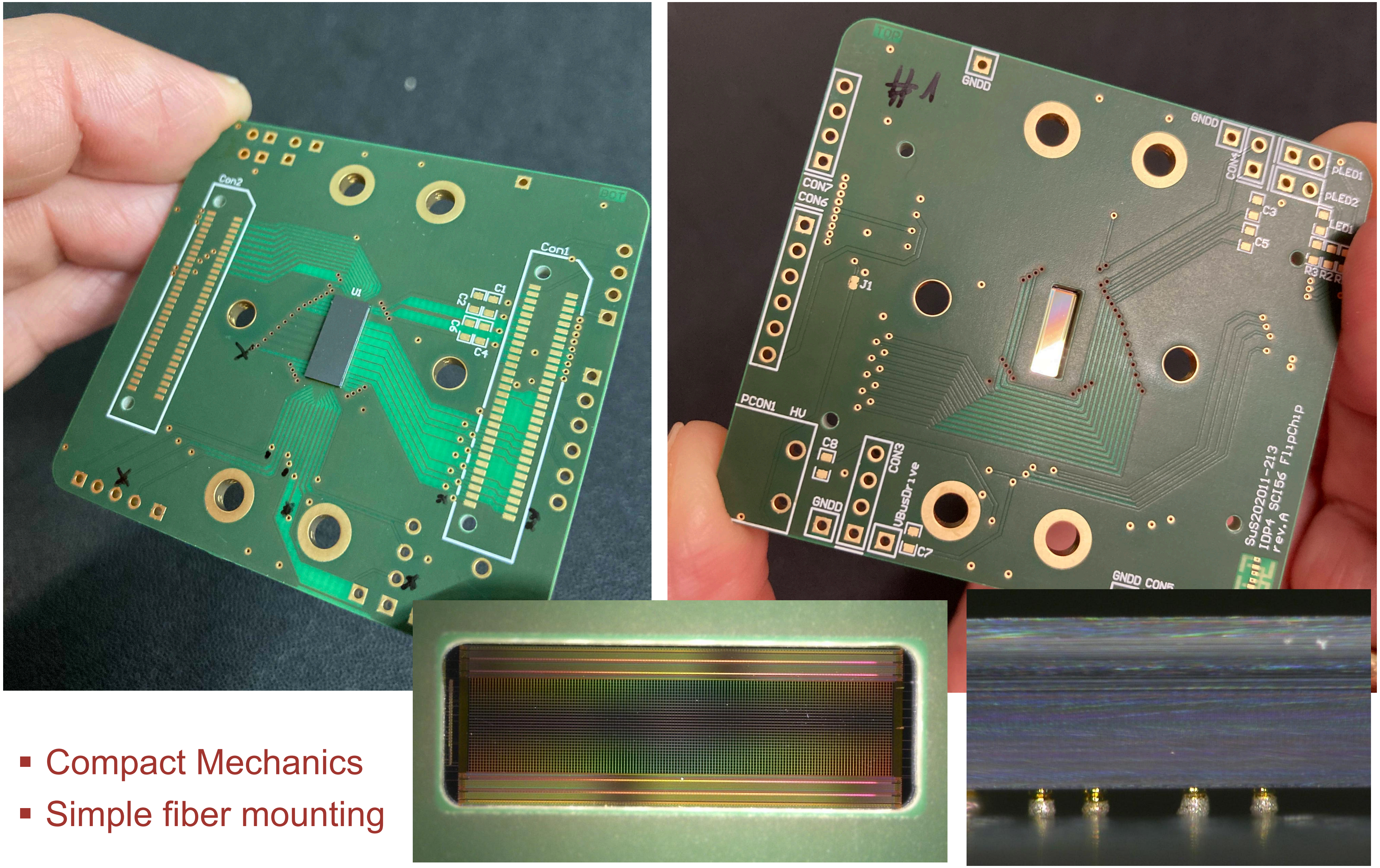
Next Steps

- Establish FPGA code to precisely measure Hit Processor signal edges
  - So far oscilloscope is used -> very slow
- Construct setup to cool SPADs
  - Reduce Dark Count Rate
- Improve coupling of fiber to Chip
  - Use flip chip mounting (see next slide)
- Measure many groups simultaneously
- Prepare new chip submission with
  - Some bug fixes
  - faster bus signals

Dark Count Rate
(measured on different chip)



Flip Chip Assembly



- Compact Mechanics
- Simple fiber mounting

Summary

- A chip for the detection of photons in optical fibers has been designed

- SPAD groups at arbitrary positions can be defined in software

- Chip has purely digital outputs (pulse – width coded):
  - Event Time has a jitter of < 500 ps for small groups
  - Few photons can be clearly distinguished
  - Photon number of up to 30 are possible

- First coupling to fiber bundles has been successful

- The proposed concept could provide compact, low power, cost efficient readout for large fiber systems

Thanks for your attention!

Questions?