

Status of GE2/1, the 2nd CMS muon Triple-GEM system

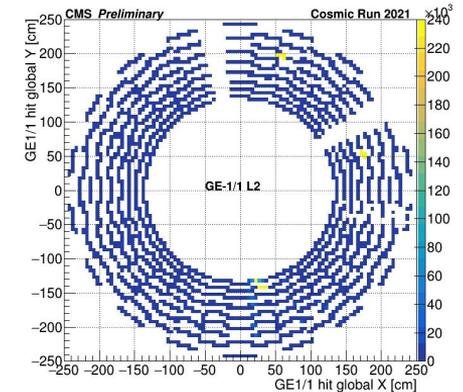
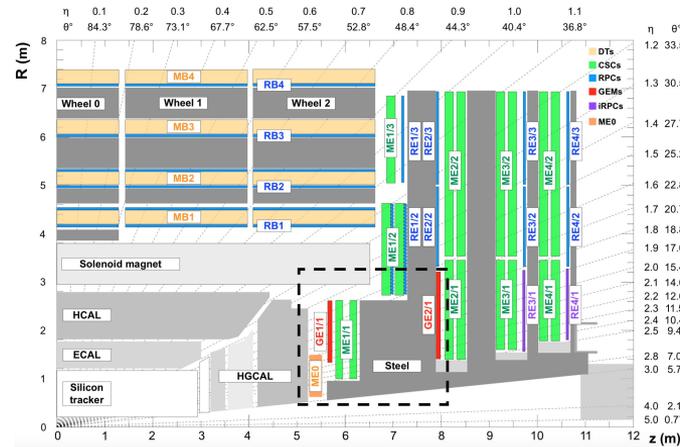
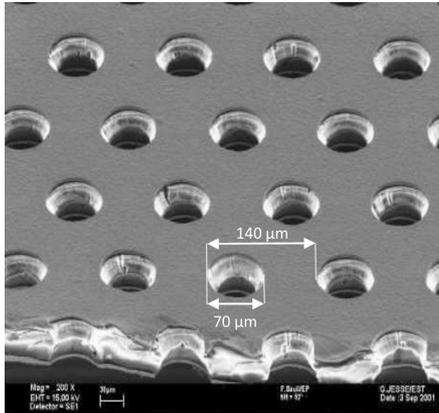
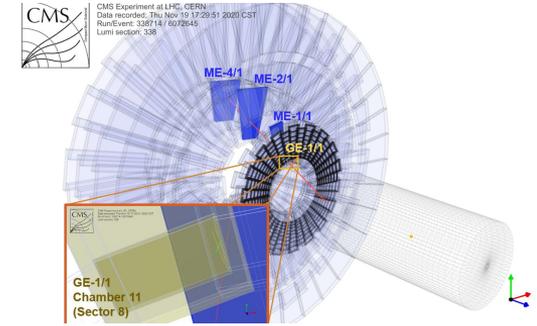
Laurent Pétré, on behalf of the CMS Muon Group

The CMS GEM project

The CMS GEM project is part of the CMS upgrades preparing for the high-luminosity LHC phase. New detectors based on the Triple-GEM technology are being installed in CMS to cope with the increase in background rates and trigger requirements.

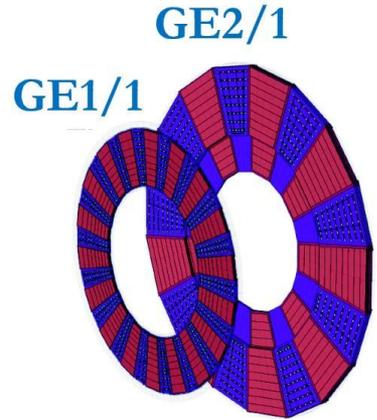
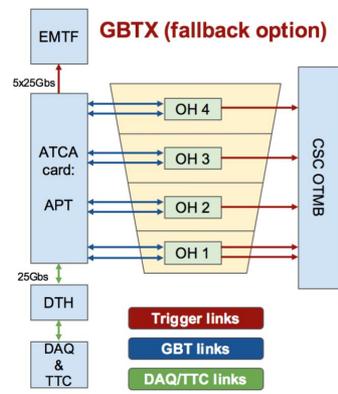
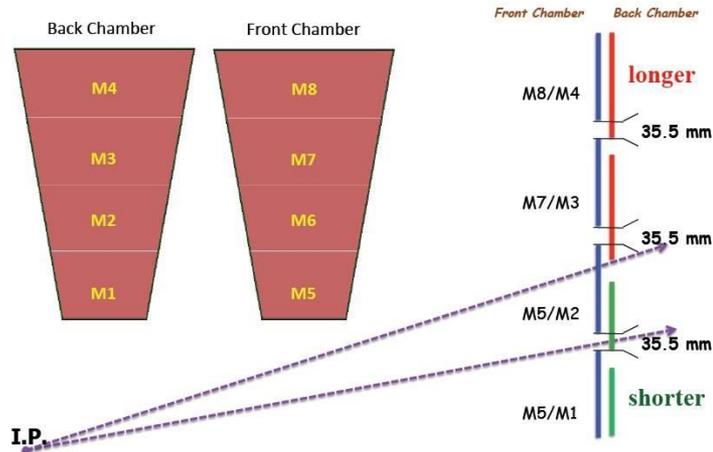
Triple-GEM detectors, gaseous micro-pattern detectors, meet the environmental and physics requirement in terms of time and spatial resolution, efficiency, and rate capability as well as robustness against aging. The GEM upgrade consists of 3 stations, ME0, GE1/1, and GE2/1 of which GE1/1 has already been installed in CMS in September 2020. GE2/1 is scheduled to be installed in 2023 and 2024, while ME0 is scheduled to be installed in 2027.

GE1/1's 144 chambers are now routinely used in CMS data-taking during cosmics acquisition and are still under active commissioning activities.



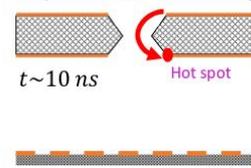
The GE2/1 upgrade

- Same Triple-GEM technology as GE1/1
 - Pseudorapidity $|\eta|$ coverage: 1.62-2.43
- 18 super-chambers per endcap
 - 2 layers of different types to avoid overlapping dead areas
 - 4 modules per chamber
 - M1, M2, M3, M4 or M5, M6, M7, M8
- 288 modules (300 with spares)
 - Module angular opening: 20°
 - Size similar to GE1/1
- 442,368 readout channels
- Similar readout electronics as GE1/1
 - Each module equipped with one OptoHybrid (OH) board
 - 2 GBT links per OH
 - One embedded FPGA for triggering purposes
 - Front-end trigger and readout ASIC (VFAT3)

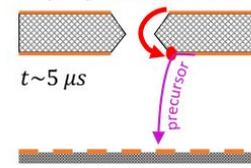


Discharges mitigation

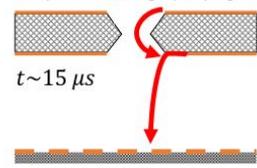
Step 1: initial GEM discharge



Step 2: precursor current



Step 3: discharge propagation



Front-end channel loss was experienced during the GE1/1 slice test (demonstrator chambers installed in 2017 up to the end of the LHC Run-2)

- The process was understood and attributed to discharges propagating to the anode and front-end ASIC

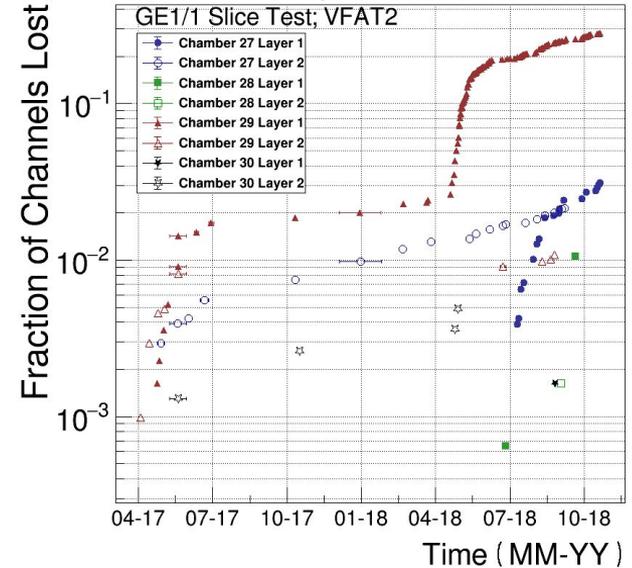
The process of discharge propagation is mainly driven by the large capacitance of the foils. Possible mitigations strategies are

- Usage of drain resistors GE2/1
- Reduction of the foil capacitance GE2/1
- Increase of the HV filter resistance GE1/1 GE2/1

The process of damage is mainly due to the re-ignitions of the propagating discharge. Possible mitigations strategies are

- Improvement of the electronics input protection GE1/1 GE2/1
- Increase of the de-coupling with the HV filter capacitance GE2/1

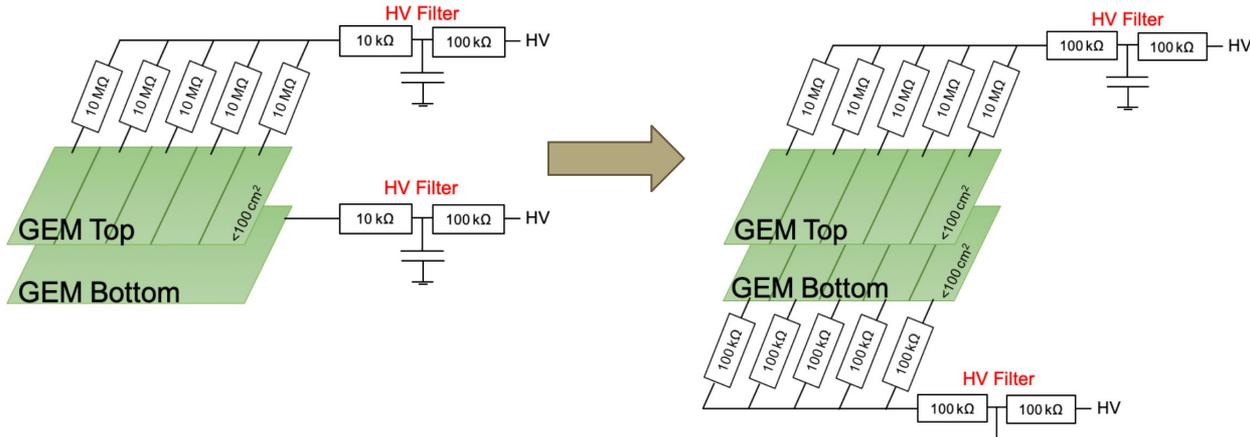
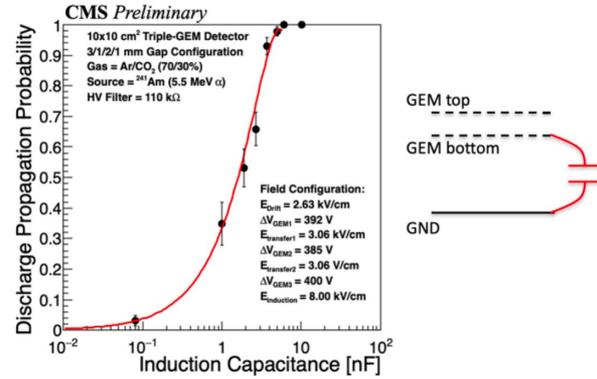
CMS Preliminary



$$\text{channel loss rate} = \text{background rate} * \text{discharge prob.} * \text{propagation prob.} * \text{damage prob.}$$

Double-segmented GEM foils

- In GE1/1, single-segmented (top segmented) foils used
 - Protect the detector in case of discharges
 - Allow to operate the chamber in case of shorts
 - Large “induction” capacitance
 - Enough energy to trigger a propagating discharge
 - Enough energy to damage the readout electronics
- In GE2/1, double-segmented foils (top and bottom segmented) have been designed
 - Limited energy to trigger discharges and damage the electronics

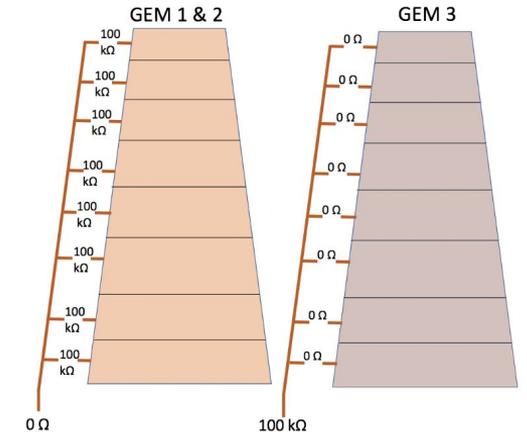
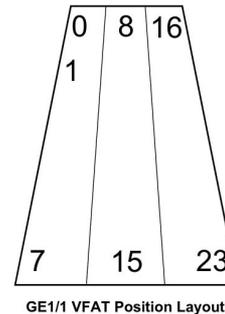
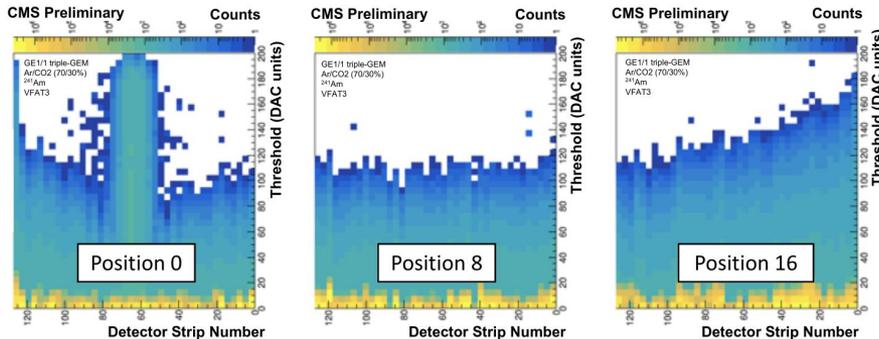
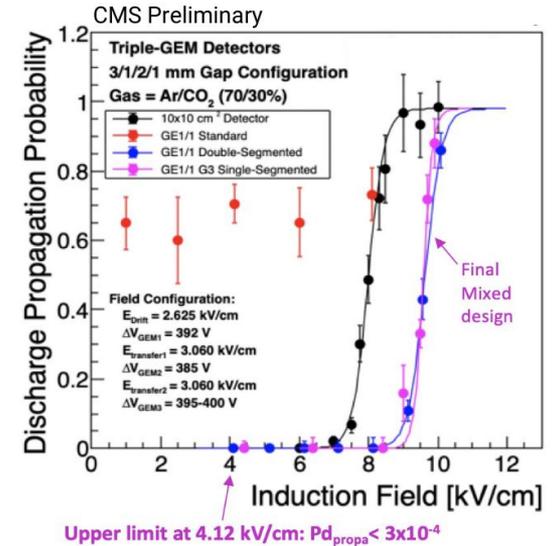


Cross-talk mitigation

Reducing the “induction” capacitance creates a cross-talk effect

- A parasitic signal of opposite polarity is induced on the electronics front-end channels facing the same HV sector as the one with the real particle hit
- The undershoot of large-amplitude signals of opposite polarity can cross the threshold and be recorded as a fake hit
- Highly-ionizing particles create deadtime

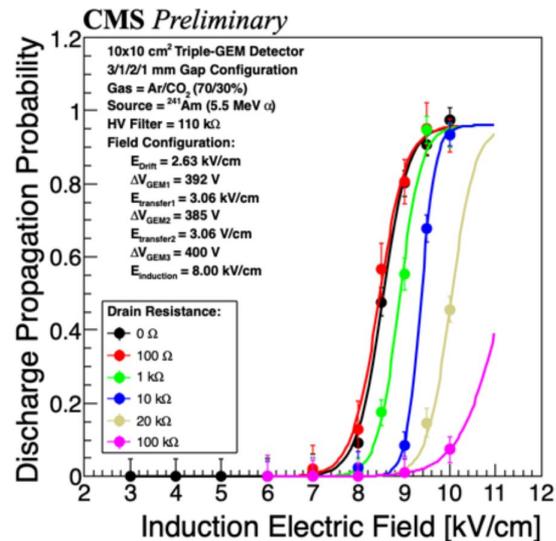
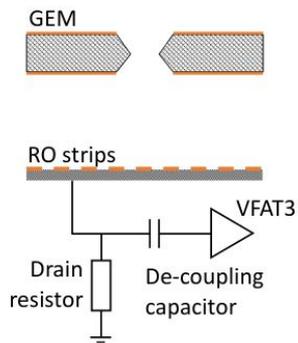
A mixed design was implemented where the first two GEM foils use a double-segmentation while the last one uses a single-segmentation. This solution effectively reduces the discharge propagation probability while keeping the cross-talk under control.



Electronics input protection

GE2/1 allowed the re-design of the front-end electronics PCB with the implementation of a protection circuit targeting two purposes

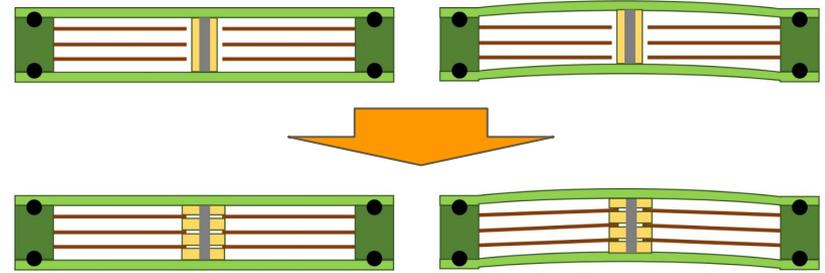
1. Reducing the damage probability via a decoupling capacitor
 - Avoid the ASIC input channel to absorb the full energy of the discharge
2. Reducing the discharge propagation to the anode via a drain resistor
 - Quenches the precursor current by increasing the readout strip potential and suppressing the induction field



Production challenges

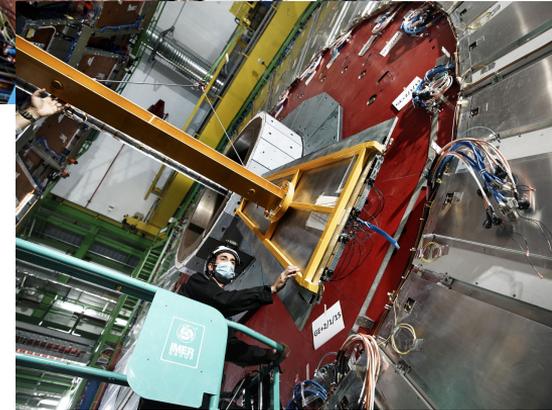
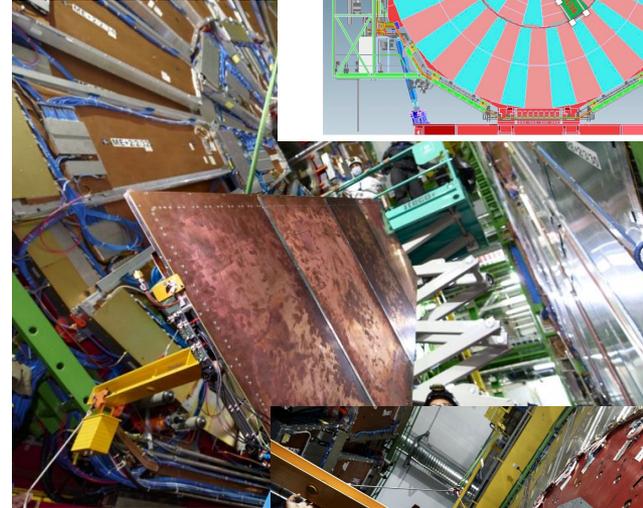
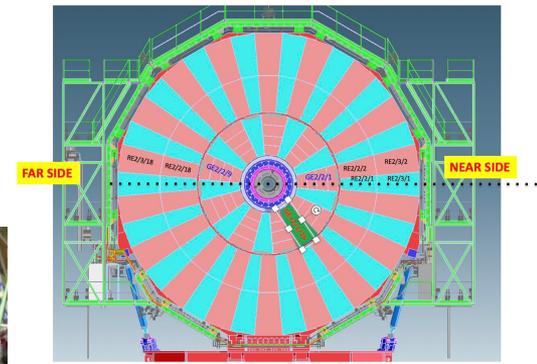
Large PCBs such as the ones used for the GE2/1 Triple-GEM drift and readout boards tend to bend when subject to stretching forces.

- Causes of a variation of gain across the detector
- A set of pillars were introduced in the GE2/1 design as an enhancement with respect to GE1/1
- Help to keep constant the gap between drift and readout PCB
 - Increase minorly in the dead area
 - Work well only if the PCBs are produced flat
- Replace the pillars to maintain the distance not only between the drift and readout PCBs but between all electrodes
- Maintain the gap distances even for significant bending of the PCB



GE2/1 demonstrator

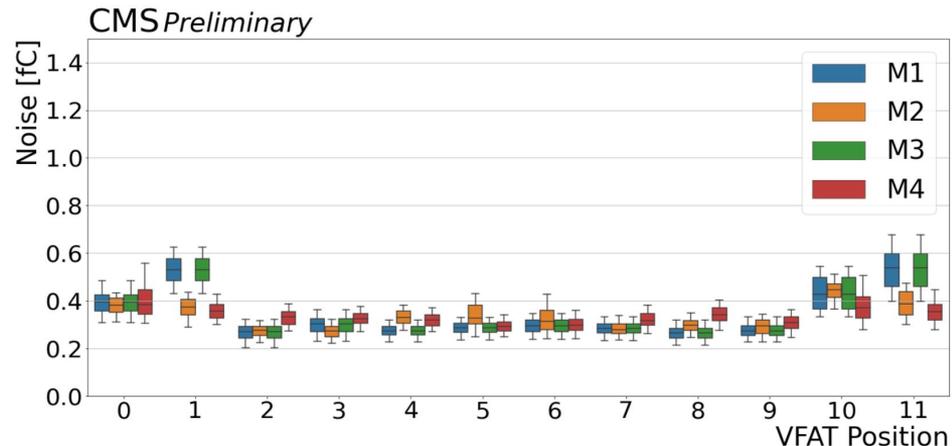
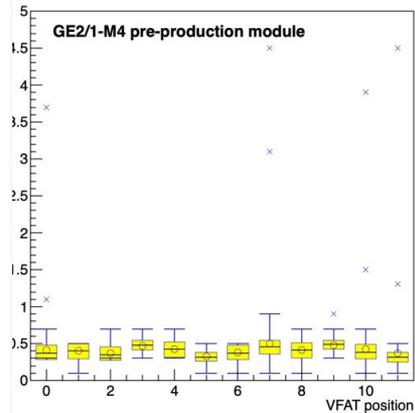
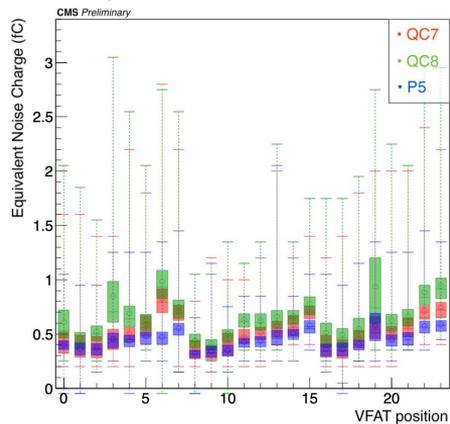
- The GE2/1 demonstrator is a complete GE2/1 prototype layer 2 chamber that was installed in CMS (sector 16, layer 2, positive end-cap) in November 2022 as preparation for the installation and operation of the full GE2/1 system
- Exercise the installation steps
 - Mechanical installation tools
 - Services (gas, low-voltage, high-voltage) connection
- Gain operational experience
 - Test the readout electronics
 - Develop and test the DAQ system
 - Develop and test the DCS system
- Perform various confirmatory measurements:
 - Test the updated foil design and the discharges protection schemes in a real environment
 - Evaluate the channel loss rate
 - Assess the noise levels and ensure the effectiveness of grounding solutions
 - Estimate the noise rates and the cross-talk in a realistic environment



Noise levels

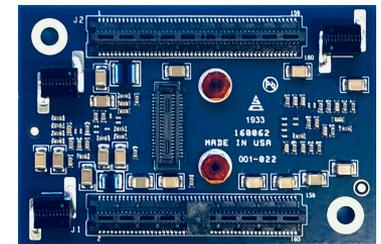
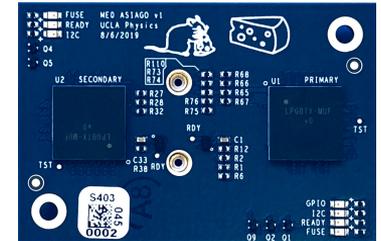
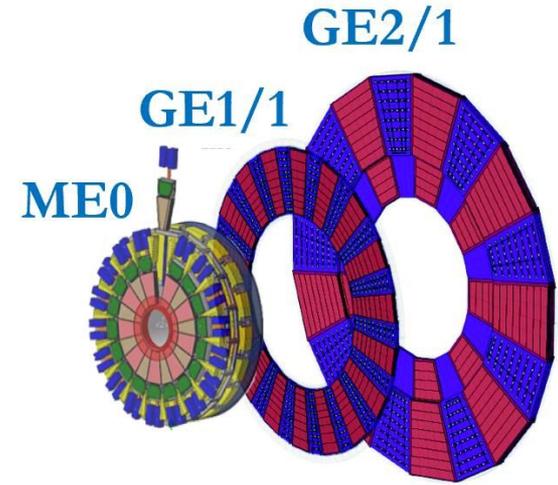
- Significant work invested into grounding and electronics noise optimization
 - Based on the noise optimization campaign of GE1/1
- Reached ENC levels similar or better than GE1/1
 - In single GE2/1 modules, as well as the complete demonstrator during its quality control
 - More measurements to come from within the CMS environment
- Thresholds around 3 fC (after VFAT trimming)

ENC comparison QC7-QC8-P5 – GE1/1-X-S-INDIA-0006



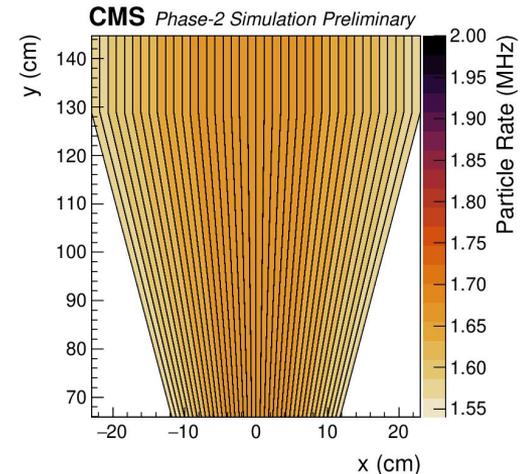
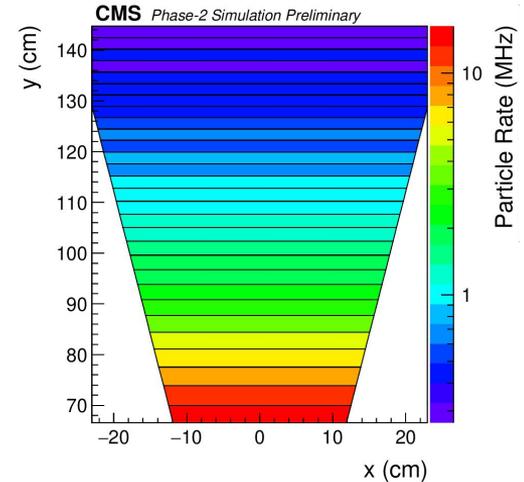
The ME0 station

- Last part of the Triple-GEM upgrade of CMS
 - Pseudorapidity $|\eta|$ coverage: 2.03–2.8
 - Closer to the beamline, closer to the interaction point
 - Higher background rate (up to 150 kHz/cm²)
- 18 stacks per endcap
- 6 modules per stack
- 216 modules
 - Module angular opening: 20°
 - Module active area: 0.296 m²
- 331,776 readout channels
- New readout electronics design with respect to GE1/1 and GE2/1
 - GBTx links -> IpGBT (4.8 Gbps -> 10.24 Gbps)
 - No embedded FPGA
 - Stub building for the L1 trigger
 - Same readout ASIC (VFAT3)



The ME0 station

- The GE1/1 and GE2/1 HV segmentation (i.e. horizontal segmentation) is not suited to ME0
 - The high non-uniform background rate in the ME0 region would lead to gain drops of up to 40%
- The solution is to change the orientation of the HV segmentation, i.e. use vertical segmentation
 - All HV sectors will see the same particle rate without dependency on the background shape
 - Current and thus voltage drop uniform across sectors that can be compensated
- Finalization of the R&D studies to find the best balance between discharges protection and rate capability
 - HV sector size \leftrightarrow foils capacitance
 - HV filter resistors
 - Protection resistors



Conclusion

- The GE1/1 station is the first Triple-GEM detector installed as part of the CMS upgrades for high-luminosity LHC
- The GE2/1 station is starting mass production
 - VFAT3 front-end ASIC, OptoHybrid boards, GEM foils, and modules
 - Final quality control and integration steps at CERN are being reviewed and implemented
 - First end-cap (144 modules) to be installed end of 2023; second end-cap to be installed end of 2024
- The ME0 is mostly under the developing stage
 - Prototypes designed and under test for all components
 - Integration of a complete stack planned in the upcoming weeks and months
 - Chamber installation scheduled for the end of 2027 during the Long Shutdown 3



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