ALDO2
A multi-function rad-hard linear regulator for SiPM-based detectors

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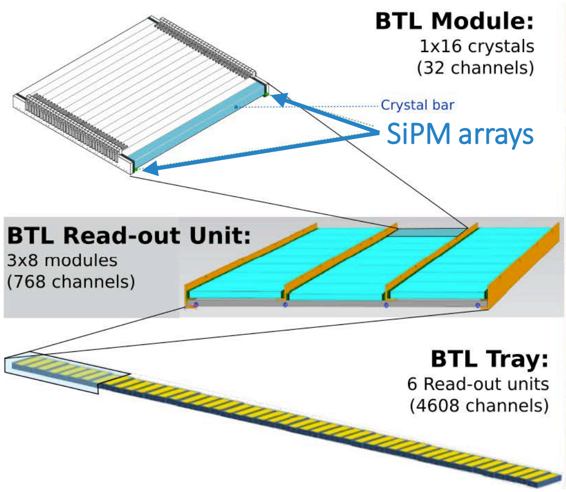
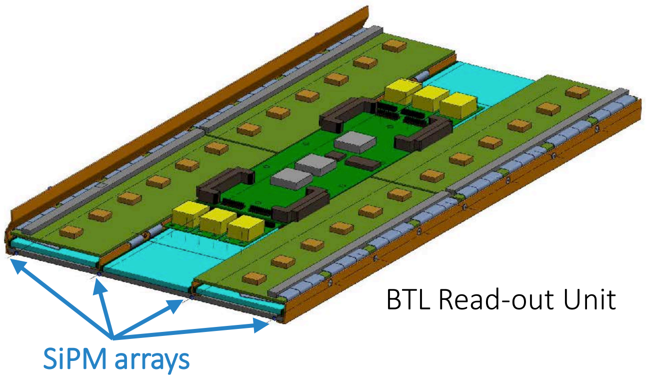
Content

Introduction: SiPM-based detectors for HEP

- SiPMs/MPPCs are gaining more and more popularity in the HEP community, as they offer many substantial advantages over other classes of photodetectors like vacuum devices
  - Compactness, robustness, small pixel size, low voltage bias, excellent linearity and dynamic range, high photon detection efficiency, immunity to magnetic fields
- On the other side they also have a few, but very crucial, drawbacks
  - High dark current, poor radiation hardness, optical cross-talk, after-pulses, precise bias
- At HL-LHC, several detectors are planning to adopt them as the baseline photodetectors
  - In CMS: Barrel Timing Layer (BTL, see below) and High-Granularity Calorimeter (HGCAL)



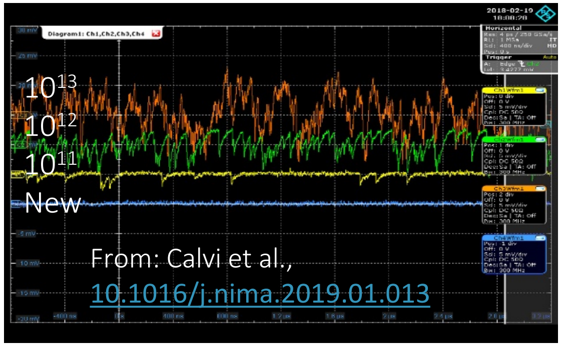
For more info on CMS BTL, see CMS-TDR-020



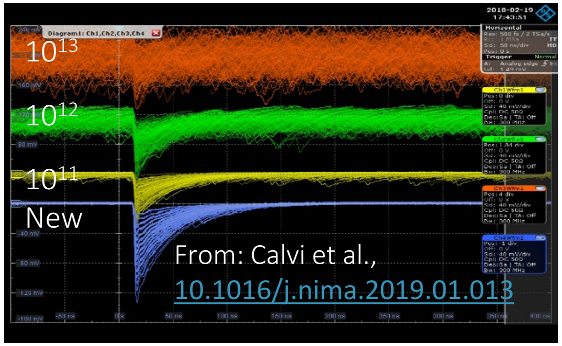
Introduction: Challenges of SiPMs at HL-LHC

- The main challenge of using SiPMs at HL-LHC comes from their poor radiation hardness
  - Dark count increases up to tens of GHz at 10^{14} n_{eq}/cm^2
    - Power consumption up to about 50 mW/SiPM
  - Breakdown voltage shifts with radiation damage
    - On-detector I-V curves are required to set optimal working point (gain and dark current have a strong dependence on SiPM overvoltage)
- Possible mitigations only marginally improve the situation
  - Cooling (typically limited to liquid CO_2 in LHC detectors)
  - Annealing (also limited in tight detectors)
- These challenges also affects the power supplies of SiPMs
  - O(1000) SiPMs are connected in parallel → ~50 W load
  - Bias voltage stability and noise are crucial for the precise setting of the working point (but usually bias supplies are very far from the detectors)
  - Bias voltage trimming in front-end chips adds complexity due to AC coupling and added parasitics on the read-out node

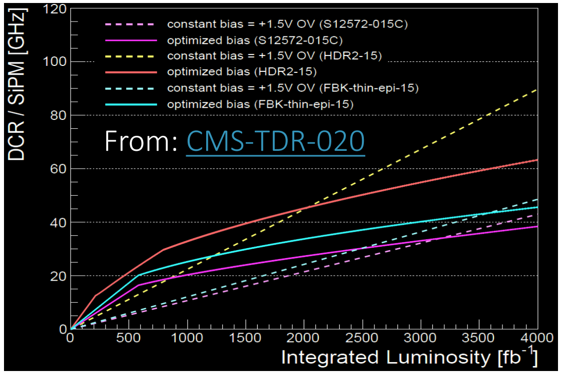
Dark counts at -30°C with irradiated SiPMs



Laser pulses at -30°C with irradiated SiPMs

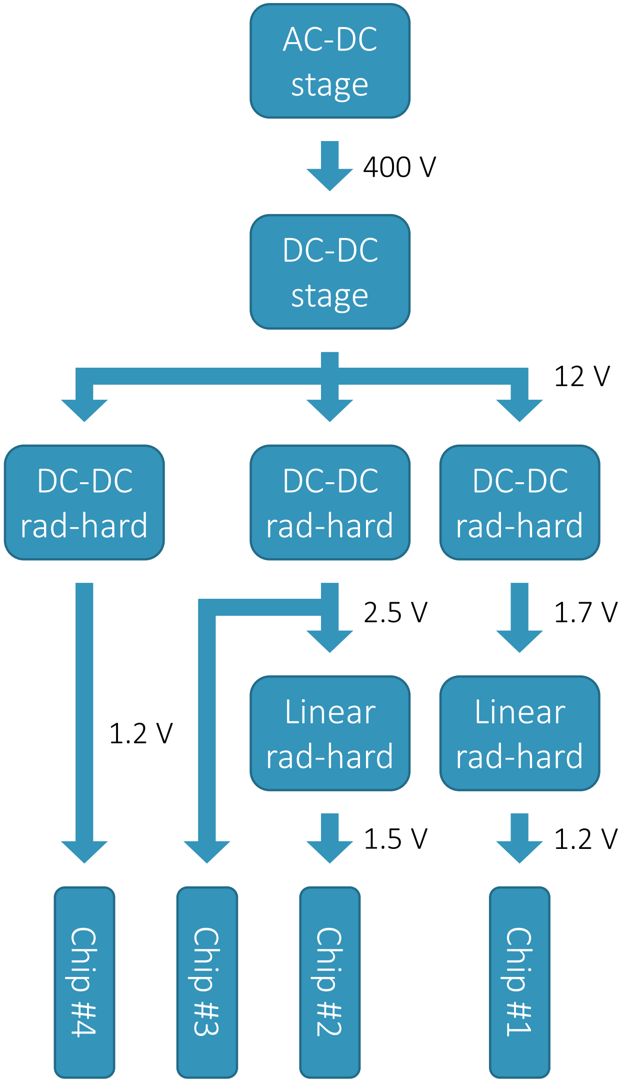


Dark count rate vs Luminosity in BTL



Introduction: Power supplies for LHC detectors

- Power distribution at LHC is usually based on a multi-stage approach
  - AC-DC(HV) stage outside experimental area (>100 m from detector)
  - First DC(HV)-DC(LV) stage in experimental area (30 m from detector)
  - Point-of-load (PoL) rad-hard DC-DC stage on the front-end boards
- But…
  - …modern front-end chips may require multiple supplies
  - …with tighter noise and stability specifications
  - …and chips from different technologies may coexist on the front-end
- Furthermore, as highlighted before, photodetectors like SiPMs also require precise PoL power supply for their bias voltage
- There is the need to design a further stage
  - More modularity → One ASIC per regulator, less current per channel
  - More thermal stability and less noise → Linear regulator
  - Suitable for several uses → Adjustable voltage
  - Able to provide SiPM bias voltage → "HV" technology
  - With additional features → Output current measurement, shutdown, overtemperature and overcurrent protections, etc.
  - Able to work inside detectors → Rad-hard
- We designed an ASIC for all these functions, ALDO2



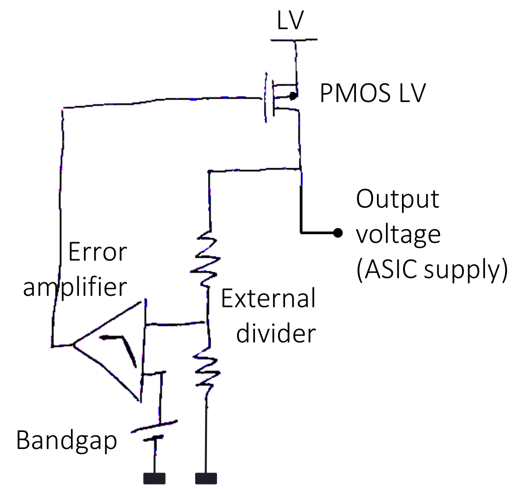
ALDO2: General scheme

ALDO2 features 4 independent and fully adjustable linear regulators

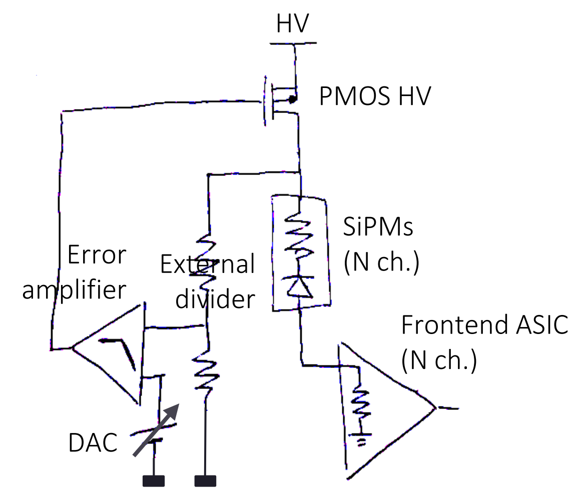
The regulator scheme is the classic low dropout scheme, with an error amplifier and PMOS pass element

- LV regulators
  - Voltage reference is provided with an internal bandgap
  - Output voltage can be adjusted with an external divider
- HV regulators
  - Both inputs of the error amplifier are available externally
  - The fixed range can be adjusted with an external divider
  - Output value can be changed during operation by applying an analog voltage from a DAC on the other input of the error amplifier
    - In BTL the DAC is embedded in the front-end chip, while HGCAL will use the DAC in the CERN slow control chip (GBT-SCA)

Basic scheme of the LV regulator

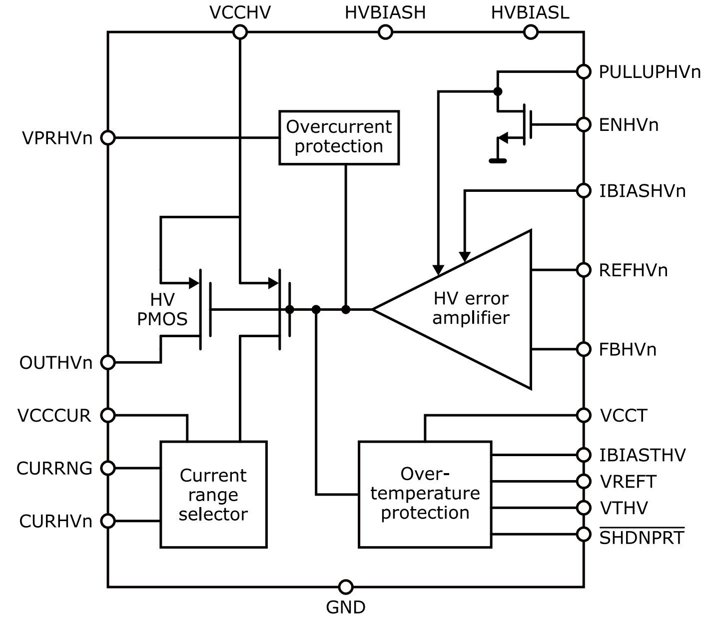


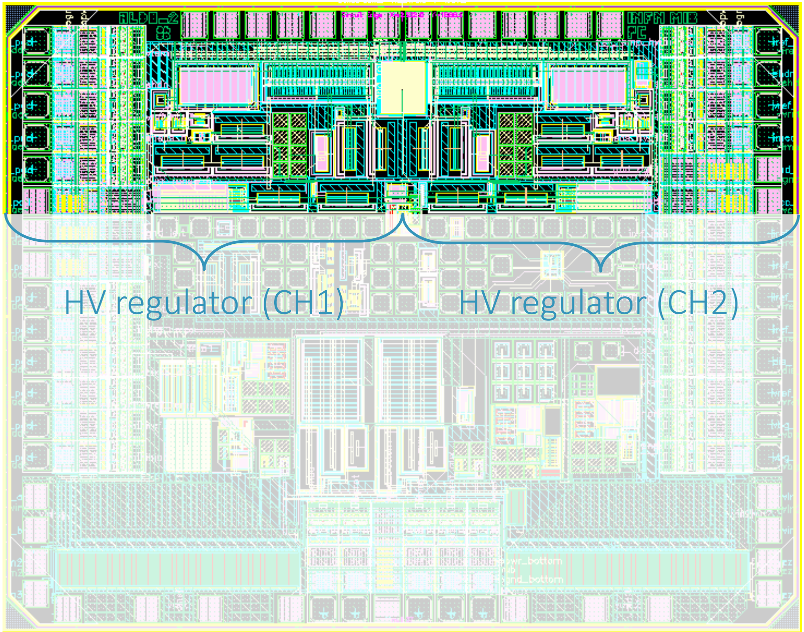
Basic scheme of the HV regulator



ALDO2: HV regulator

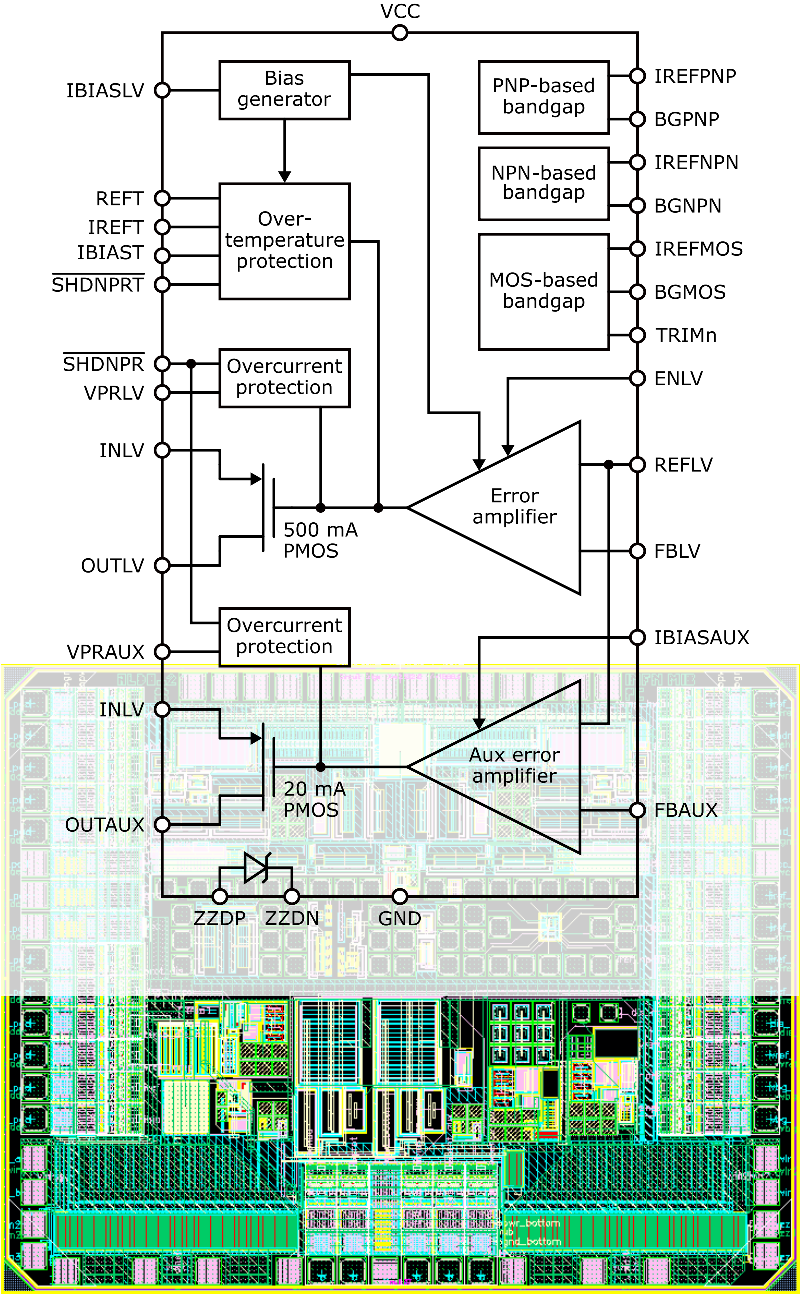
- Bias voltage generation for groups of 16 SiPMs
  → 2 channels per chip
- Input voltage: 25 V – 70 V
- The DAC used in BTL has 8 bits with two ranges:
  - Range 1: 100% – 74% of output voltage with 0.1% LSB (8 bit)
    - E.g., 44 V – 32.7 V, with 44 mV LSB (SiPM specs still floating)
  - Range 2: 95% – 82% of output voltage with 0.05% LSB (8 bit)
    - E.g., 41.8 V – 36.3 V, with 22 mV LSB (SiPM specs still floating)
- Maximum output current: 45 mA (current limit 55 mA)
- Minimum dropout:
  - <1 V on not irradiated chips (> 97% efficiency @ 38 V)
  - 3 V with EOL irradiation (92% efficiency @ 38 V)
- External low ESR capacitor for stability
- Channels can be individually disabled
  - If a SiPM fails with a short, only its group of 16 SiPMs is affected
- Protected against overcurrent and overtemperature
- Allows output current measurement by mirroring output current (2 ranges available, factor x20 between the two)
  - Voltage conversion using an external resistor, range can be tuned





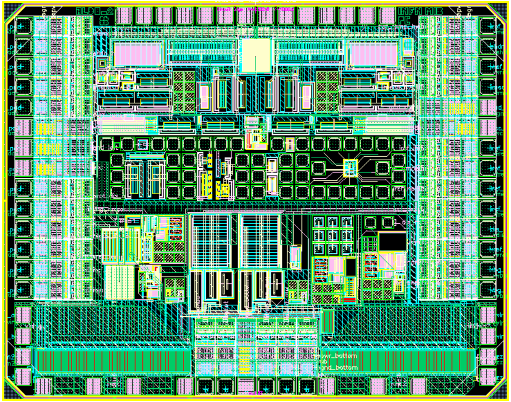
ALDO2: LV regulator

- Power supply filtering and stabilization
- Input voltage: 1.7 V – 3.3 V (at maximum load and EOL radiation levels)
- 2 channels:
  - Main regulator, 500 mA current output
  - Aux regulator, 20 mA current output, used for internal references but can be used by other components as a precise buffered reference
- Power efficiency: 71% (output 1.2 V, input 1.7 V, load 0.5 A)
- 3 bandgap voltage references:
  - 2 based on BJTs, better stability and precision, worse radiation hardness, nominal value about 1.2 V
  - 1 based on MOSFETs, better radiation hardness, trimmable, nominal value about 630 mV
- External low ESR capacitor for stability
- Output enable, allowing the shutdown of individual ASICs
- Protected against overcurrent (typical limit 900 mA) and overtemperature

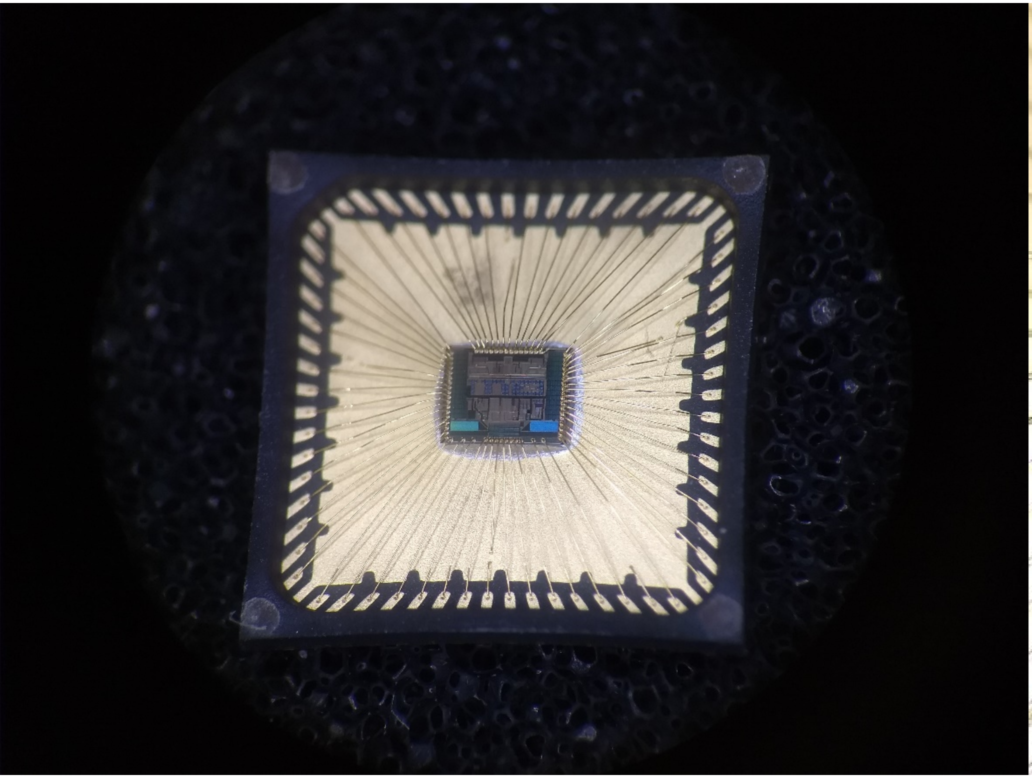


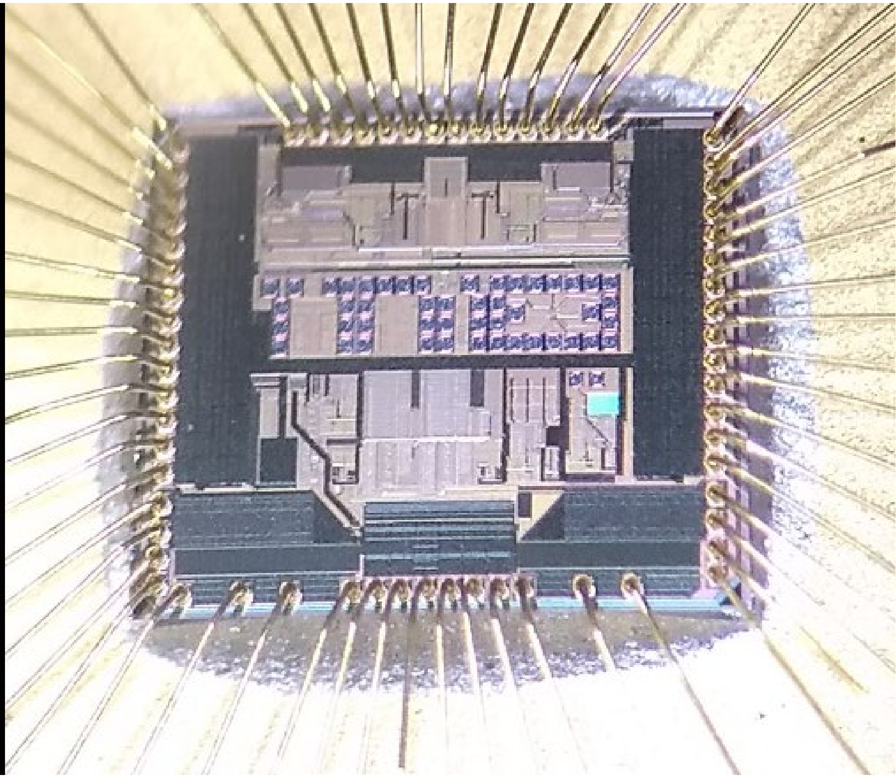
ALDO2: Technology and prototyping

- The chip is designed in onsemi I3T80 HV CMOS technology (350 nm), which proved to be sufficiently radiation tolerant in other CERN designs (FEAST DC-DC) and publications (see Faccio et al., 10.1109/TNS.2010.2049584)
- ALDO2 was produced in 3 prototypes (ALDO2v0 in 2019, ALDO2v1 in 2020, and ALDO2v2 for production run in 2022)
- The package is QFN64 (9x9 mm^2)



Die area 2.47 x 1.95 mm^2





ALDO2: Radiation hardening techniques

BTL maximum expected radiation levels at **3000 fb^{-1}**

TID	Neutron fluence (1 MeV eq.)	Charged hadron fluence
3.2 Mrad	1.9e14 cm^{-2}	1.5e13 cm^{-2}

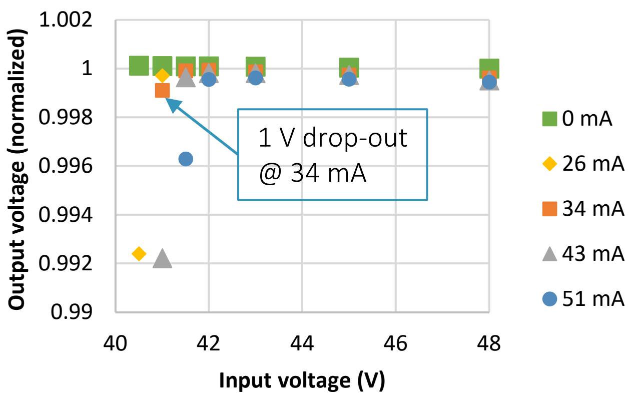
- Target radiation levels in hottest areas of BTL is within reach of I3T80 technology (HGCAL has lower radiation levels)
- Several radiation hardening techniques adopted
  - Enclosed layout for all LV NMOS transistors
  - The HV NDMOS implements a special “enclosed/guarded” layout to reduce leakage above 100 krad (extended P+ diffusion around the source contact to avoid parasitic gate formation in the lateral oxide)
  - On resistance of HV MOSFETs increases with displacement damage
    - Not super critical for our application, effect minimized by using larger transistors
  - Wide use of guard rings
  - Increased spacing between devices and cells
  - High density of substrate contacts
  - Strict adoption of anti-latchup rules provided by the technology

Measurements: HV regulator

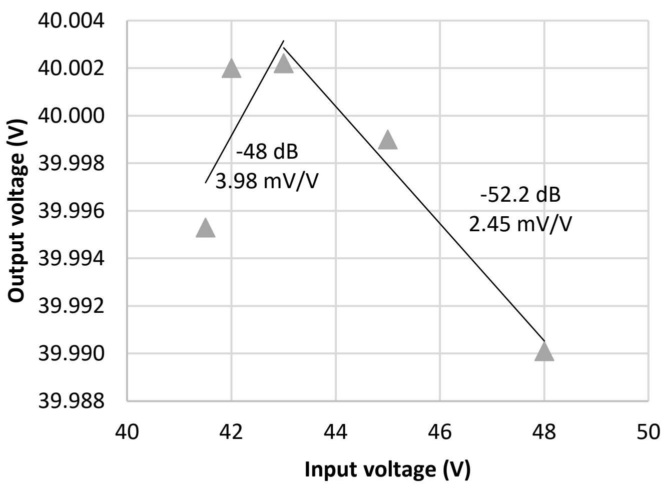
Selected measurements…

Line regulation

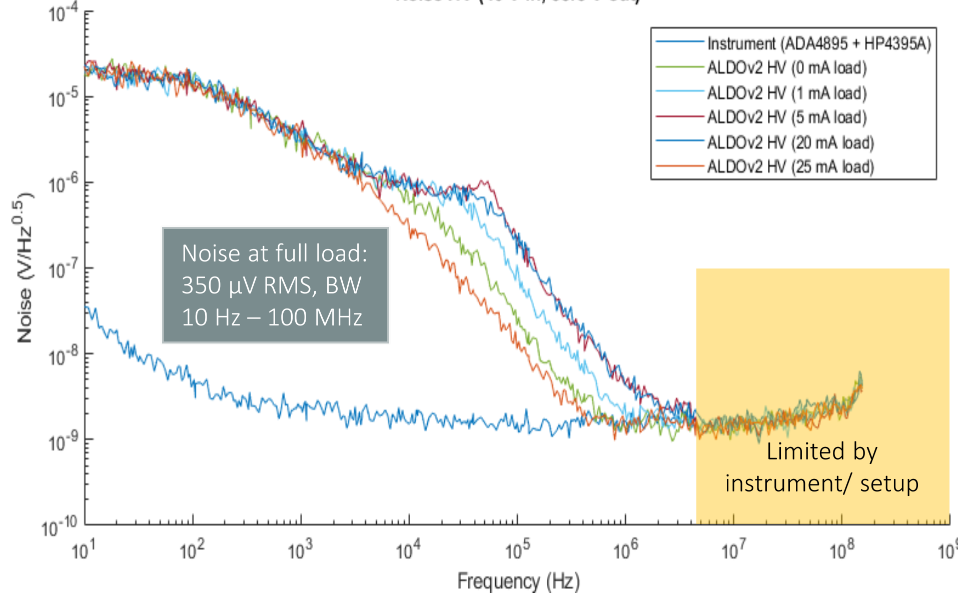
Line regulation (40 V)



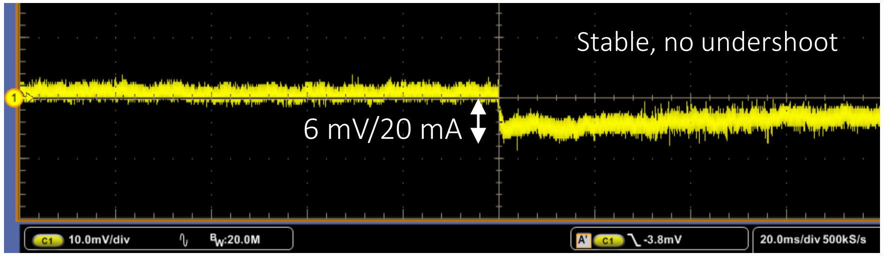
Line reg. (40 V, 43 mA)



Noise



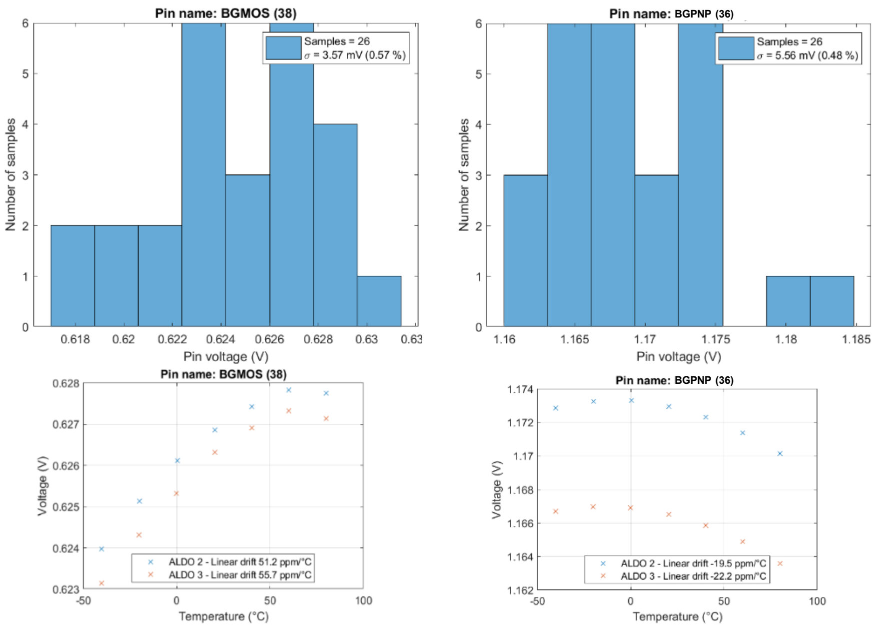
20 mA current step



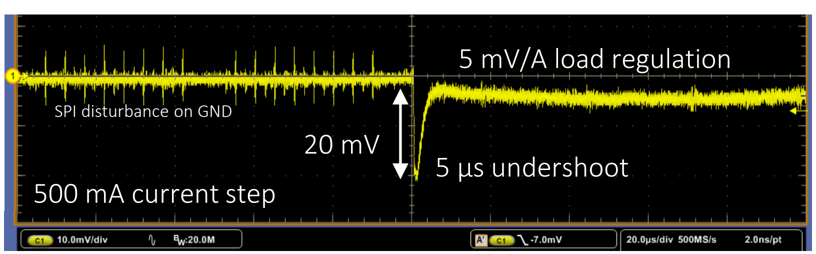
Measurements: LV regulator

Selected measurements…

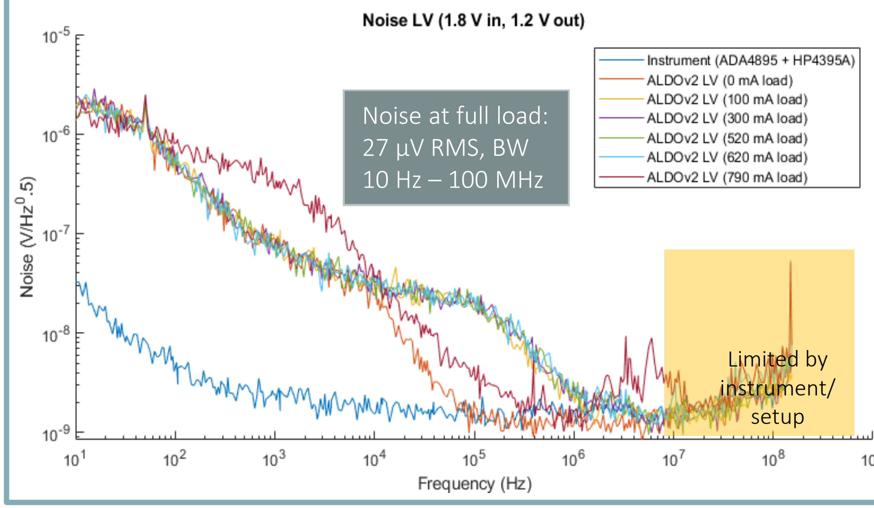
Bandgap spread and thermal stability



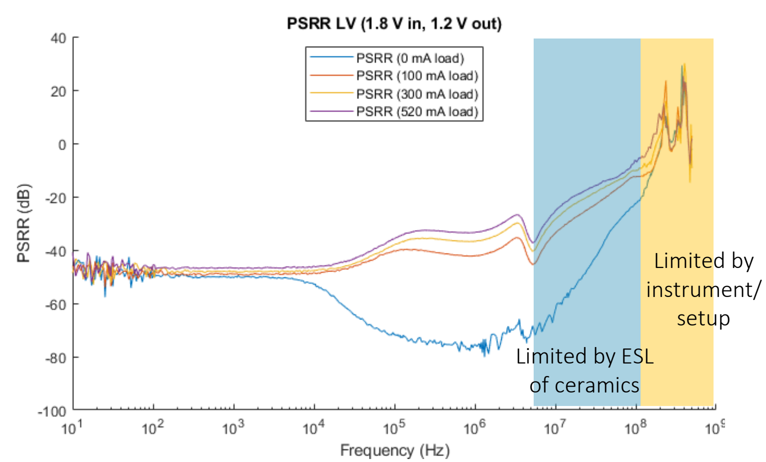
500 mA current step



Noise



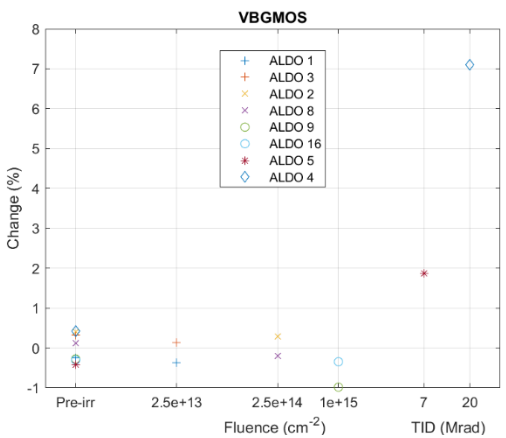
Power supply rejection ratio



Measurements: Radiation hardness

- The chip was successfully tested with TID (X-rays), displacement damage (neutrons in nuclear reactor) and single-event effects (heavy ions), beyond the expected radiation levels. A few selected results…

Bandgap drift with radiation

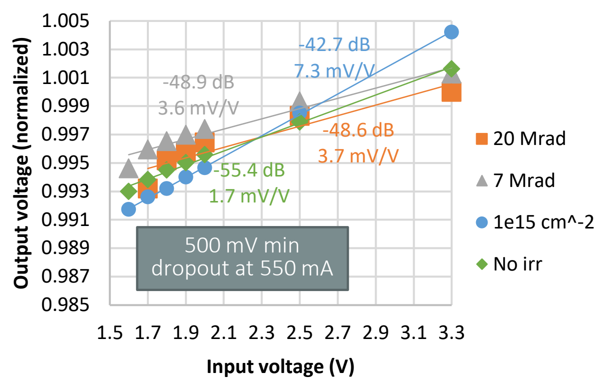


MOS	Value	Var	T Drift
Pre-irrad	625 mV	-	70 ppm/°C
2.5e14 cm^{-2}	625 mV	0%	-
1e15 cm^{-2}	621 mV	<1%	120 ppm/°C
7 Mrad	637 mV	2%	70 ppm/°C
20 Mrad	669 mV	7%	100 ppm/°C

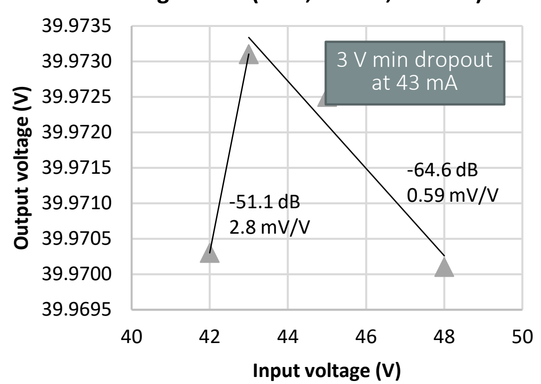
Line regulation degradation

Minimum dropout has to be increased after radiation damage, both on LV and HV regulator

LV line regulation (520-550 mA)

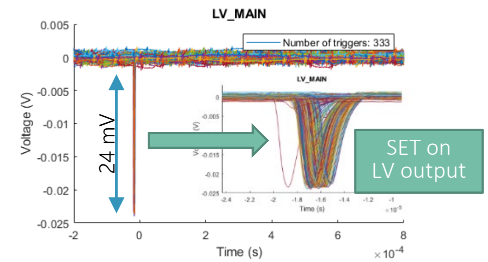


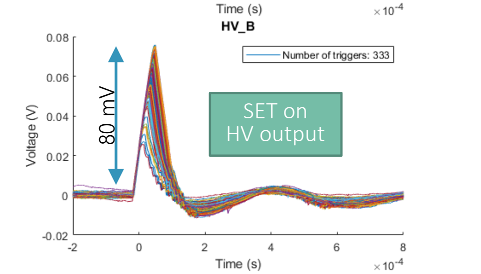
HV line regulation (40 V, 43 mA, 7 Mrad)



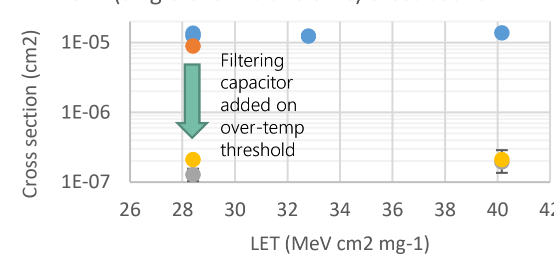
Single event transients (SET)

Single event transients observed at high LET, cause was identified, rate in final detector is negligible (mHz) and amplitude low (few %)



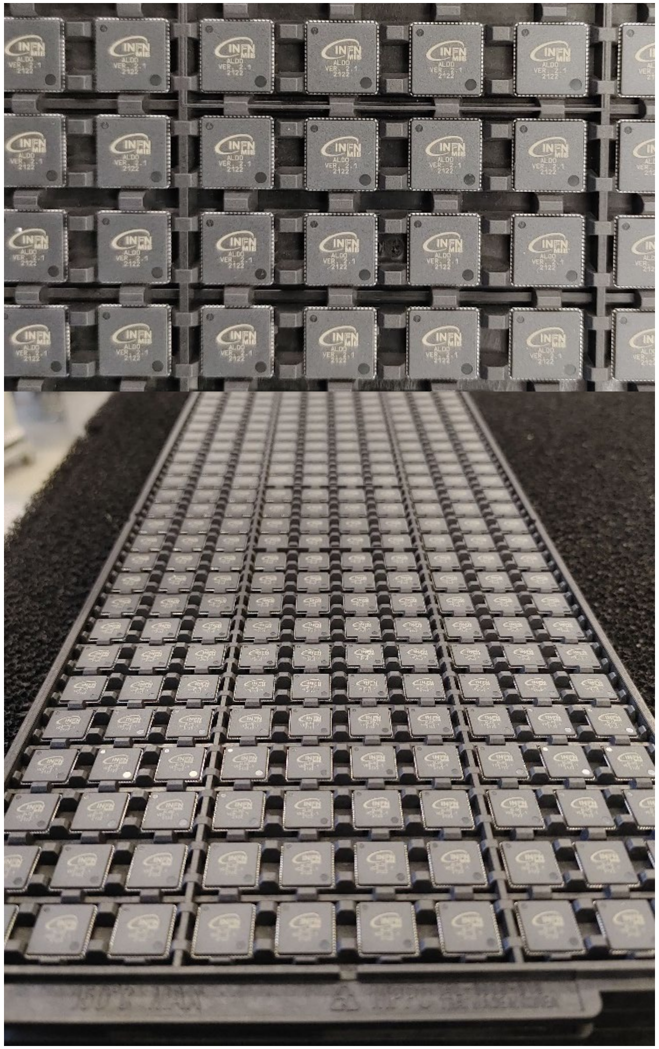


SET (single event transients) cross section



Conclusions: Chip production

- The chip has completed its development phase
  - Some measurements are still ongoing, like the stress tests to determine reliable operating parameters over long periods of time
  - Few minor changes proposed during PRR (production readiness review) will be implemented directly in production run (fail-safe)
- Production has started, chips expected in Q3 2022
  - Chip production had to be anticipated wrt HL-LHC schedule because onsemi I3T80 fab in Oudenaarde (Belgium) will be sold and has stopped MPW services in 2022
  - 45k chips produced, more than double the needs of BTL and HGCAL (19.2k), just to be covered in case of issues in production phases
  - An alternative I3T80 fab in Gresham (USA) is available, but was not qualified for radiation hardness
    - Can be studied if ALDO2 project will continue for other detectors
  - ALDO2v1 demonstrated very high yield (103 out of 103) and small spread between wafers (< 1%) → No individual chip testing is planned



Thanks for reading till here