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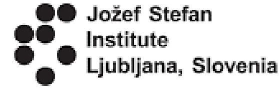

UNIVERSITY OF BIRMINGHAM

Radiation damage investigation of epitaxial p-type silicon using Schottky and pn-junction diodes

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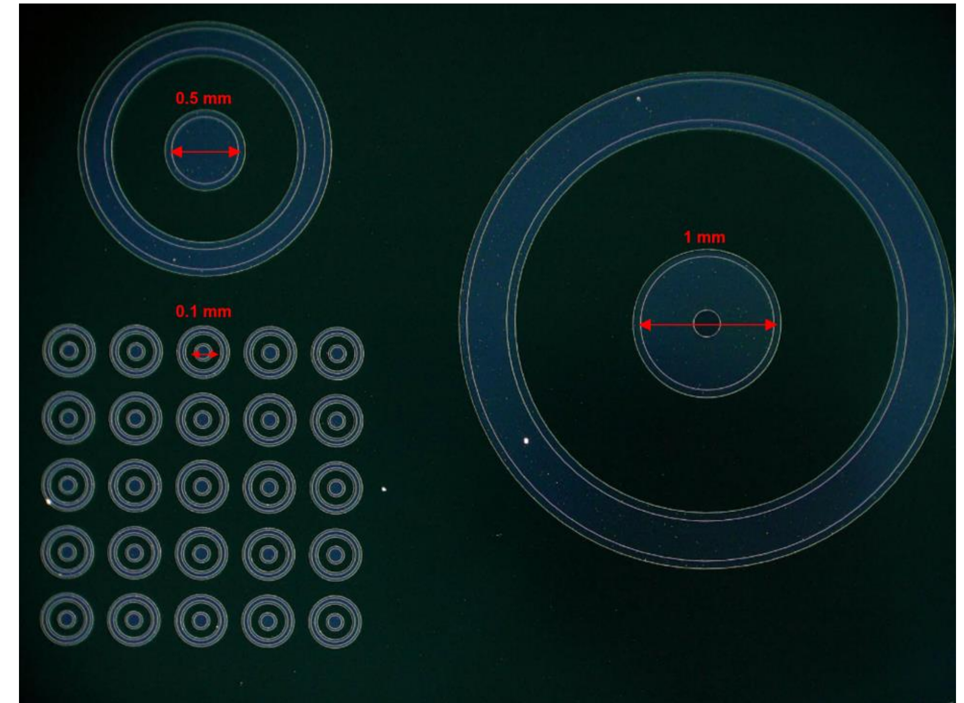
Schottky Project description and goals

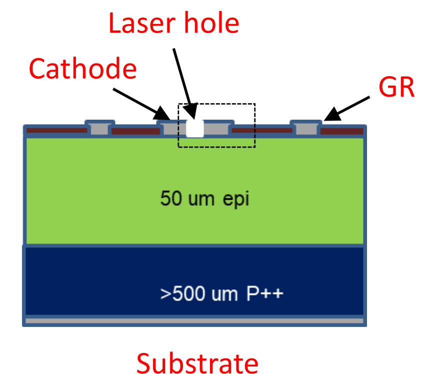
- **What:**
  - fabricate Schottky and n^+p diodes on p-type epitaxial (50µm thick) silicon wafers
  - doping concentrations as they are normally found in CMOS MAPS devices
- **Why:**
  - investigate and gain a deeper understanding of radiation bulk damage in CMOS sensors.
  - develop reliable damage models that can be implemented in TCAD device simulators (Synopsys or Silvaco)
- **How:**
  - purchase of 6-inch wafers at five B-doped epitaxial levels (10^{13}, 10^{14}, 10^{15}, 10^{16} and 10^{17} cm^{-3}) 25x each, total **125 wafers**
  - fabrication process has started both at ITAC (RAL) and Carleton University Microfabrication Facility (CUMFF).
  - tests will be carried out at RAL, Carleton, Birmingham, JSI, IHEP

Design and layout of devices

5 type of devices proposed:

- #1: 2 mm Ø cathode with 0.4 mm Ø central hole, 10 x 10 mm^2 area
- #2: 1 mm Ø cathode, 0.2 mm Ø central hole, 5 x 5 mm^2
- #3: 0.5 mm Ø cathode, no central hole, 2.5 x 2.5 mm^2
- #4: 0.1 mm Ø cathode, no central hole, 0.5 x 0.5 mm^2
- 'cell' with the previous 3 flavors (2,3,4) grouped together, to exploit wafer uniformity on small area
- #5: 6 TLM points for contact and epi resistance
- 2 masks only (metal and oxide)
- detailed description during the 35th RD50 workshop





Fabrication details & comparison

RAL-ITAC

- Schottky fabrication process only, optimised on test wafers
- oxide deposition @150°C
- Al sputtering immediately after etching (no thin SiO2 layer)
- Al lift-off in Acetone ultrasonic tank

CUMFF

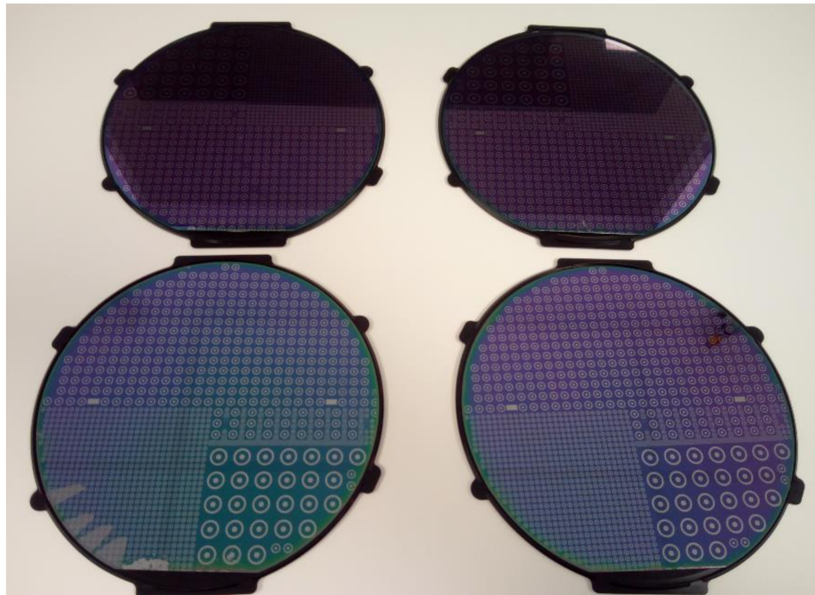
- pn-junction and Schottky processes, optimised on test wafers
- 6” substrate wafers laser cut into 4” or 6” wafer pieces
- high temperature thermal oxidation
- Al front metal thermal deposition, back Al via e-beam evaporation
- front metal patterning + etching

full details of fabrication processes in E.G. Villani’s talk from the 36th RD50 Workshop

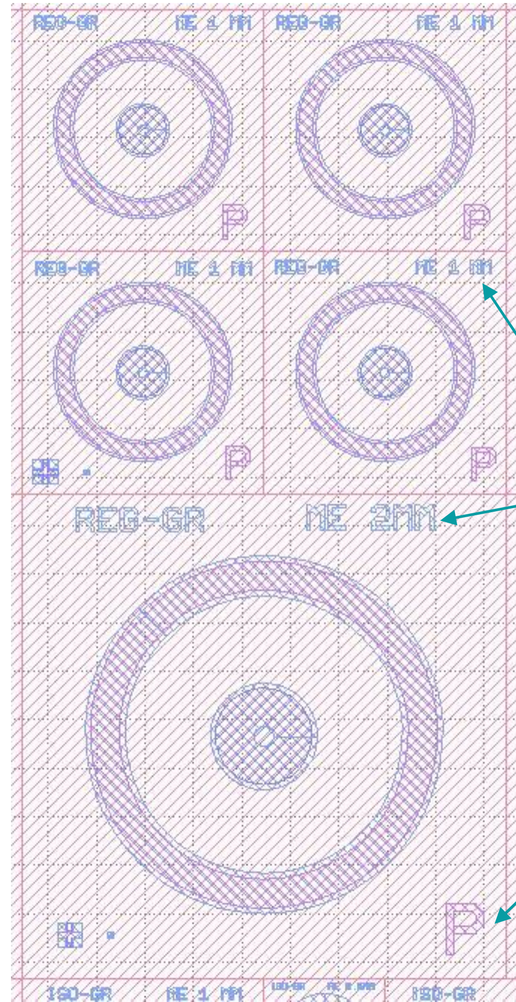
Fabrication details

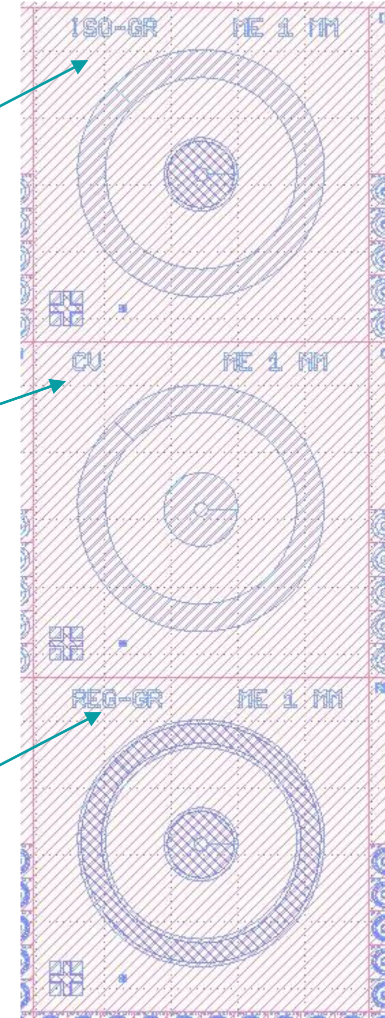
CUMFF

- new masks made, including isolated MOS gate GR variation for all device types + optional p-stop



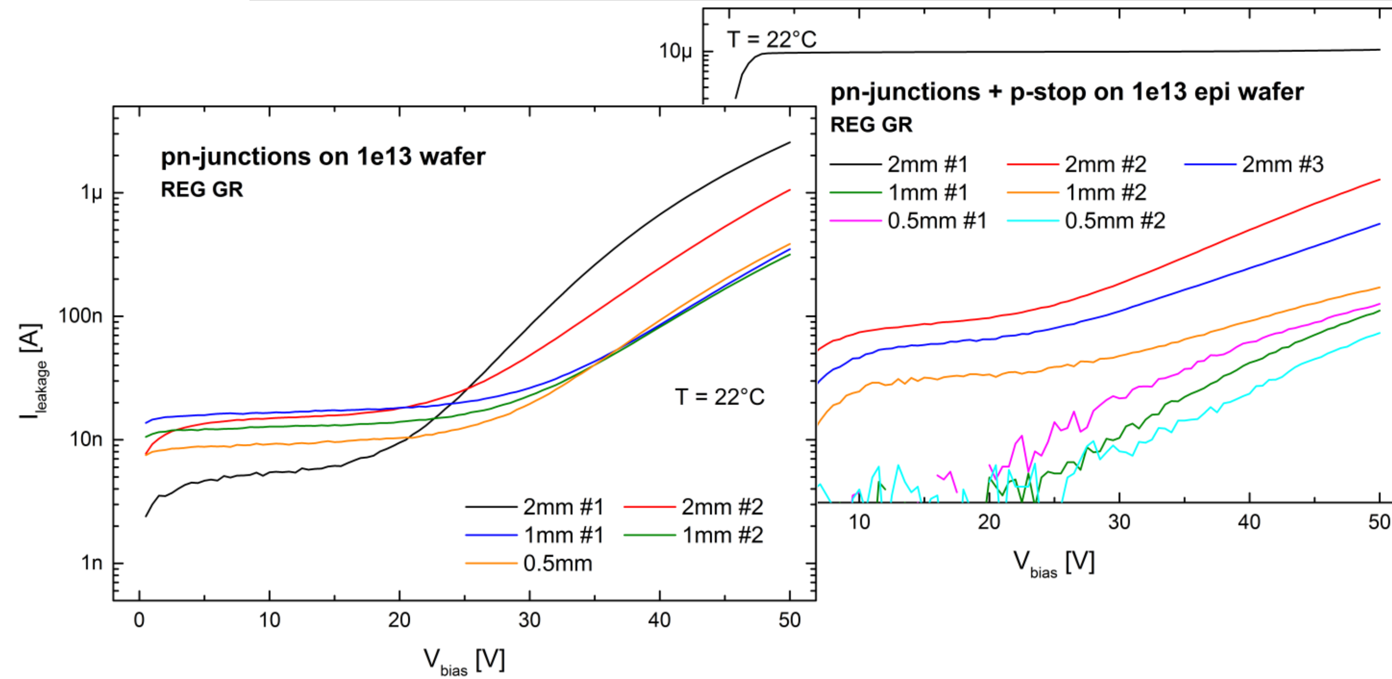
full 6” Schottky wafers @RAL

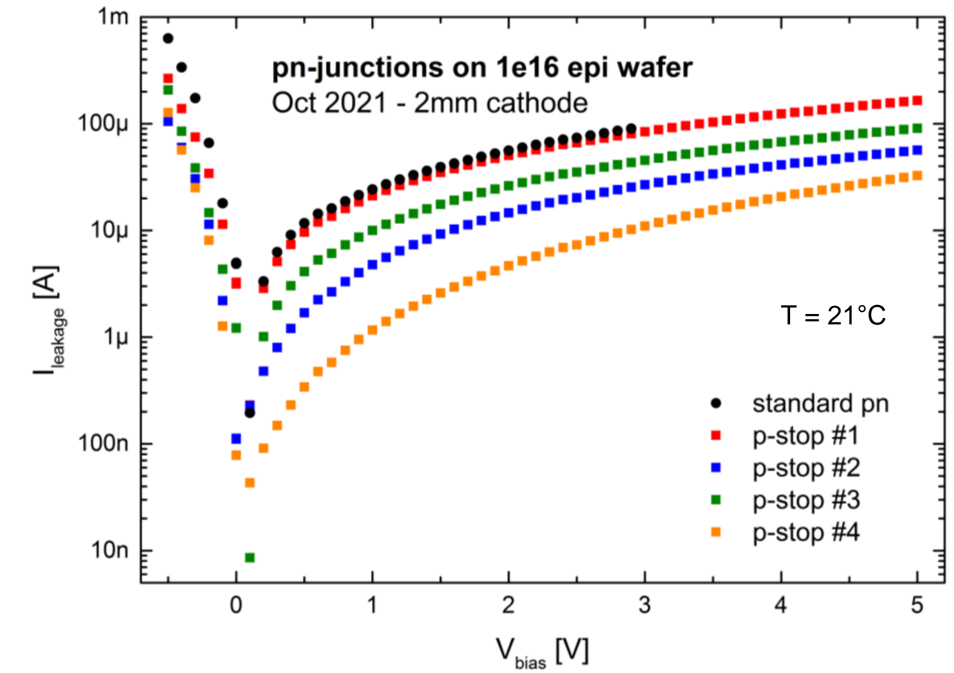




new masks with different structure flavours @CUMFF

IV measurements: CUMFF pn-junctions (1e13 vs. 1e16)





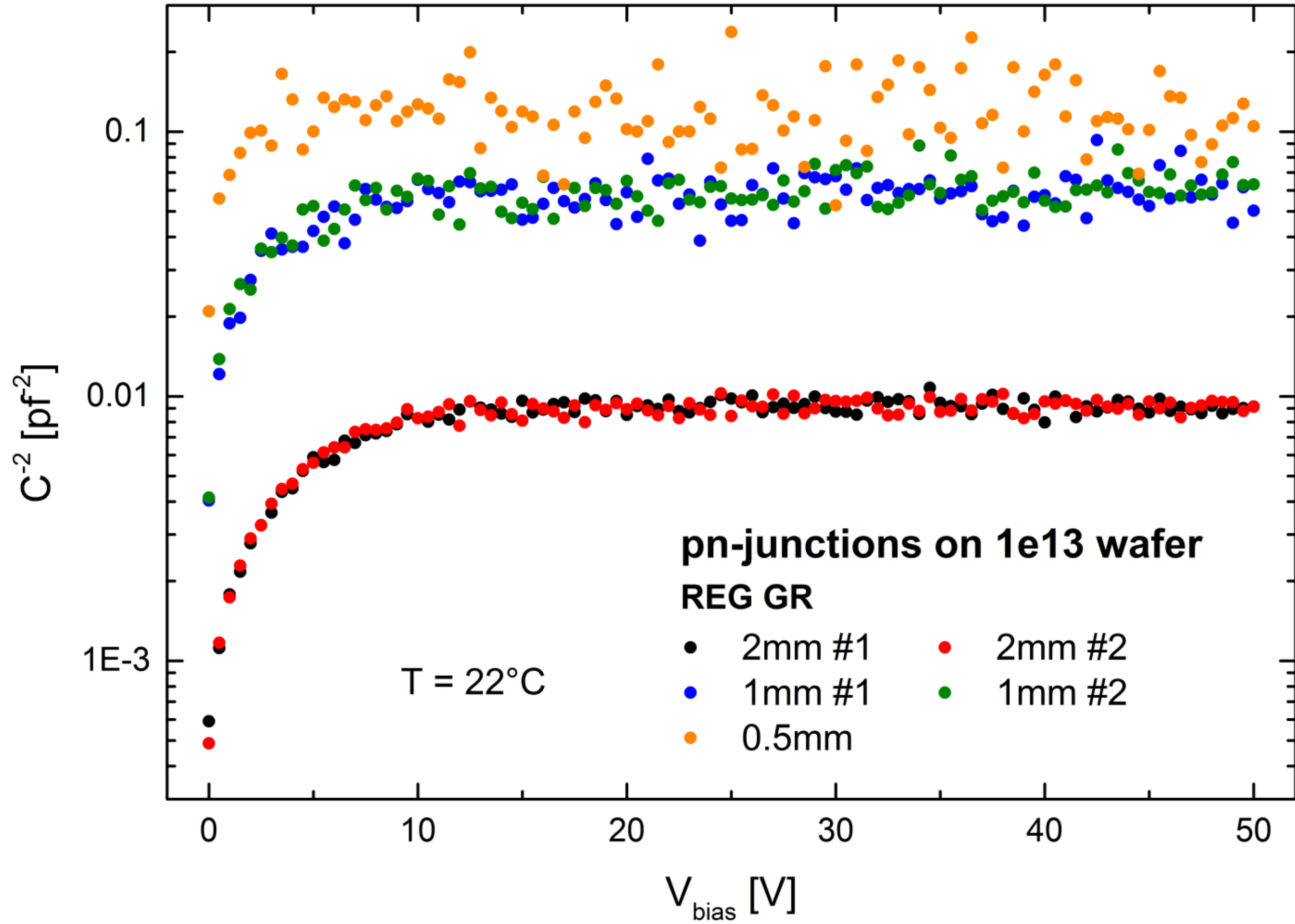
- current can vary by large margin on same wafer
- very low initial current often seen
- no hard breakdowns observed; gradual increase in current
- ➢ leakage current at much lower levels compared to first iterations

- high leakage current even at low bias voltages
  - no ‘plateau’, current keeps increasing
- smaller structures often have inconsistent IV curves
- ➢ first fabrication on low-resistivity wafer, improvements in future iterations expected

CV measurements: CUMFF 1e13 pn-junctions

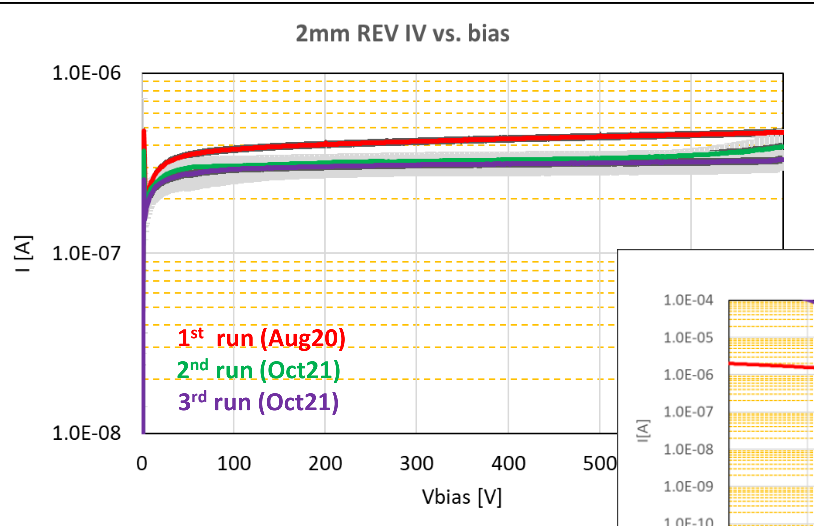
T = 22°C
f = 100kHz
V_{AC} = 100mV

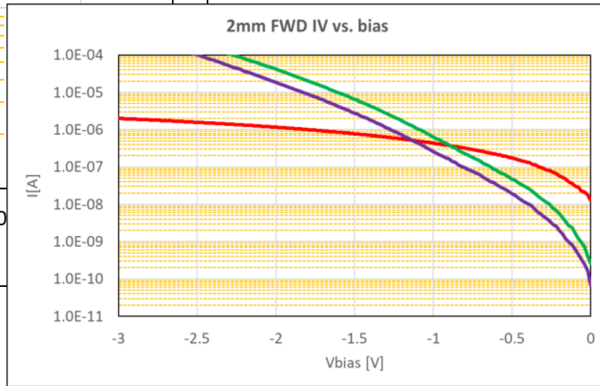
- depletion of epi layer at low voltages
  - small differences for different structure flavours
  - agrees with back-of-the-envelope calculation for high-resistivity 50um epi layer
- capacitance scales nicely with structure size



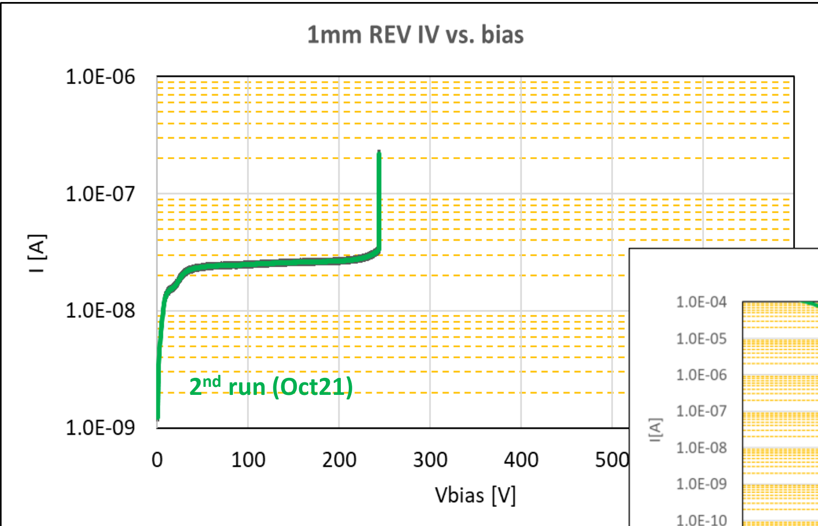
T = 21°C

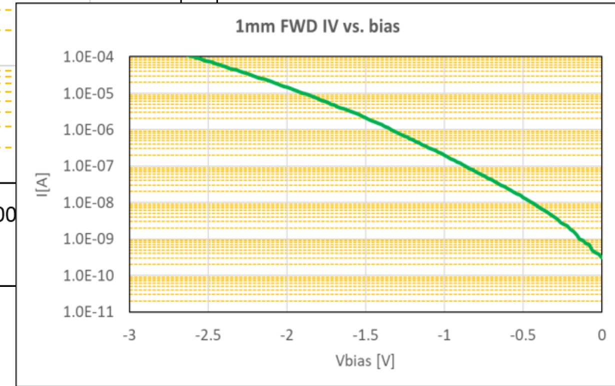
IV measurements: RAL Schottky (1e13 vs. 1e15)





1e13 wafer





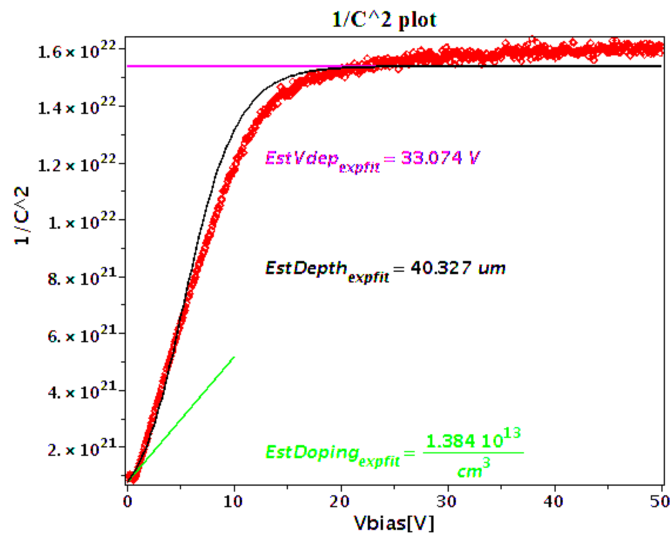
1e15 wafer

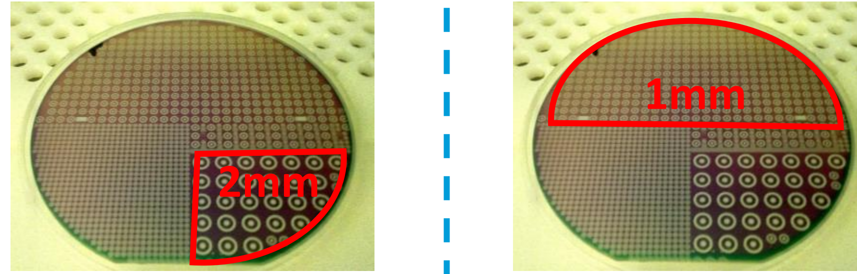
- reverse bias IV similar in all runs, slightly lower leakage in the two latest runs
  - breakdown voltage > 700V
- forward bias shows very different characteristics

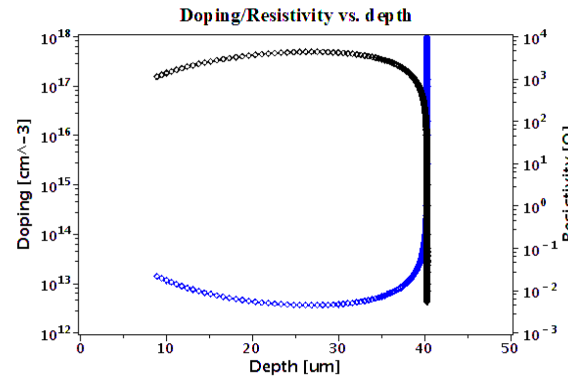
- expected lower leakage in reverse bias, with lower BV
- measured BV is high for this doping
- forward bias ~linear

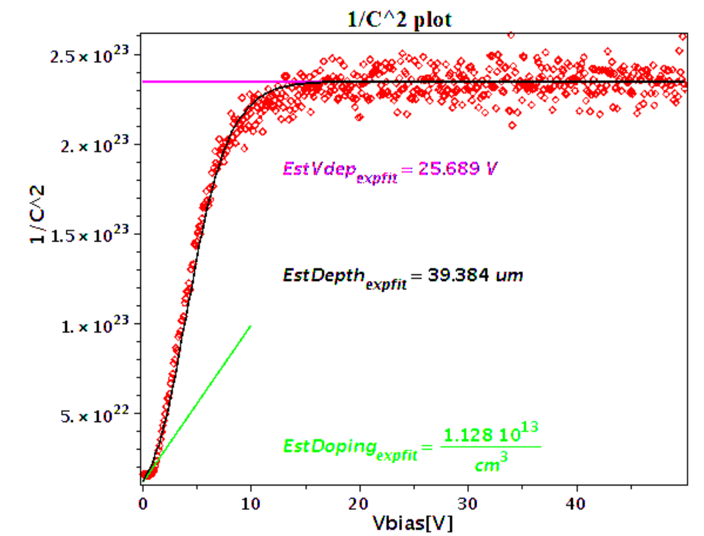
CV measurements: RAL 1e13 Schottky

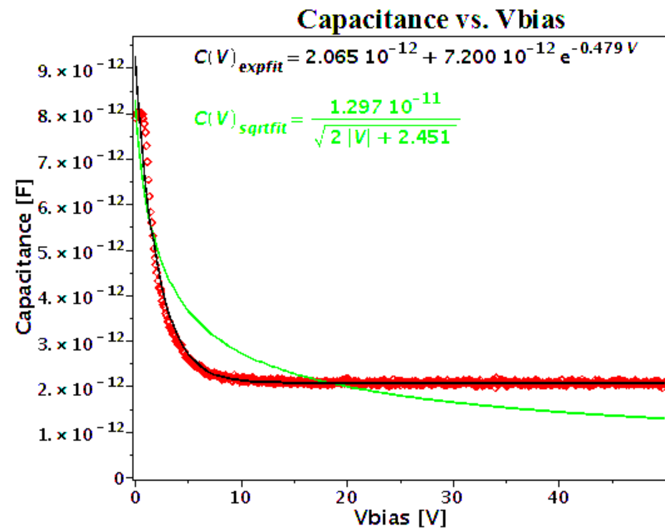
T = 21°C
f = 100kHz
V_{AC} = 30mV

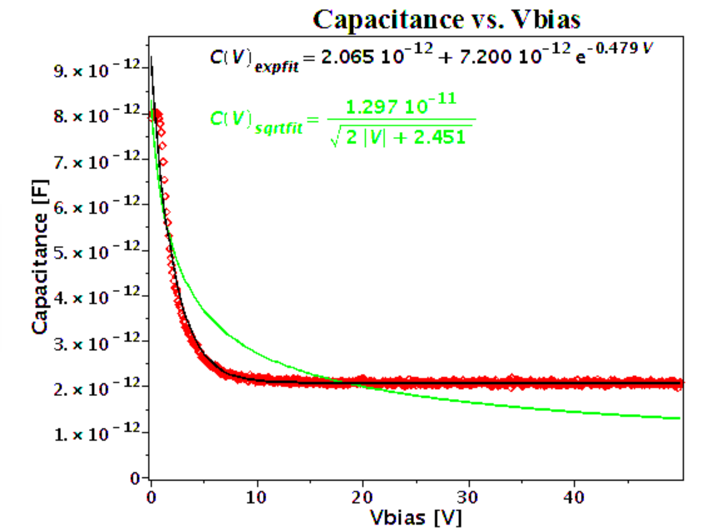












V_d	1.716
φ_b	2.134

V_d	1.343
φ_b	1.739

Φ(Al) = 4.1 [eV]
χ(Si) = 4.05 [eV]

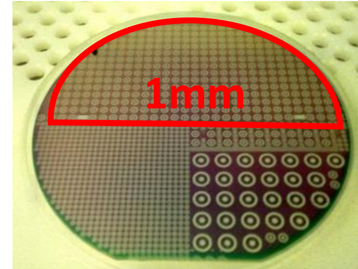
φ_b = 1.16 - (4.1 - 4.05)
= 1.11 (ideal case)

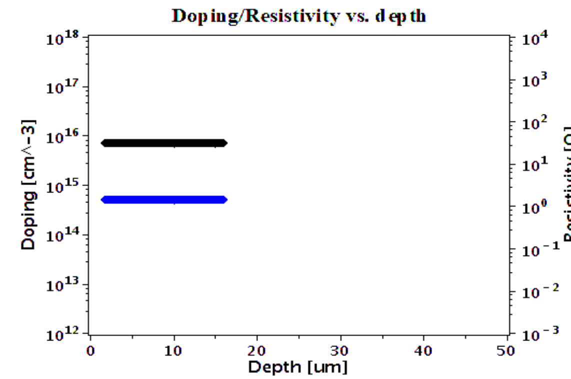
φ_b from CV too high – needs further investigation (TCAD)

CV measurements: RAL 1e15 Schottky

T = 21°C
f = 100kHz
V_{AC} = 30mV

- 2 HR wafers show doping as expected
  - CV plot not really well described by 1/√V fit
  - barrier height estimate from CV too high
  - estimate from IV in progress
- devices on 1e15 wafer so far show very good 1/√V Cap dependence
  - doping as expected
  - barrier height clearly too high

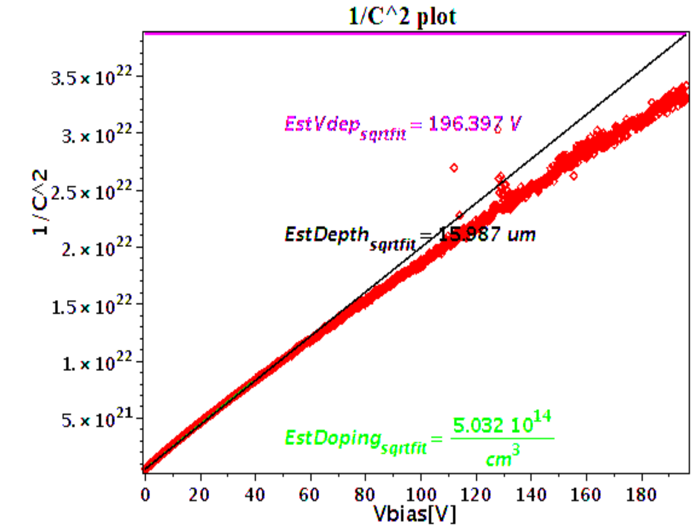


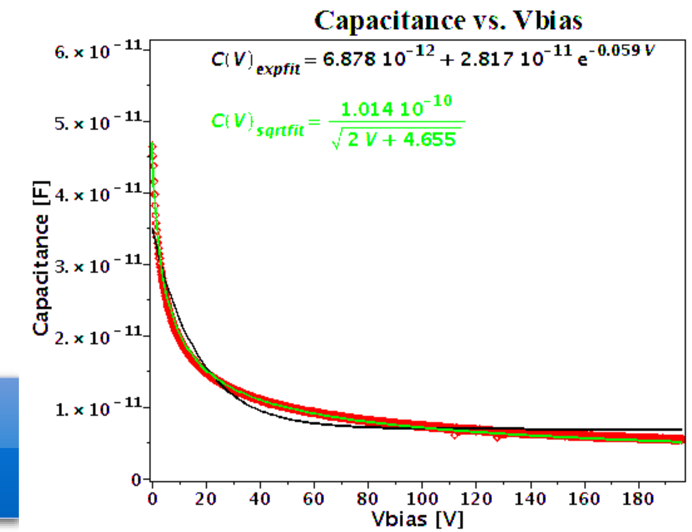


Φ(Al) = 4.1 [eV]
χ(Si) = 4.05 [eV]

φ_b = 1.16 - (4.1 - 4.05)
= 1.11 (ideal case)
φ_b from CV too high – needs further investigation (TCAD)

V_d	2.328
φ_b	2.646

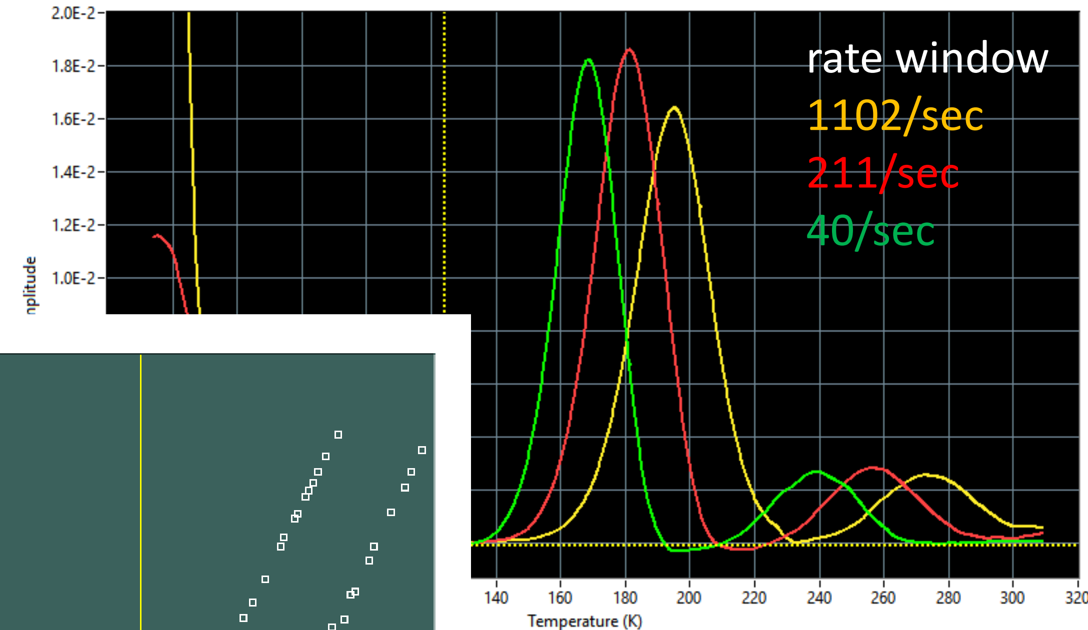


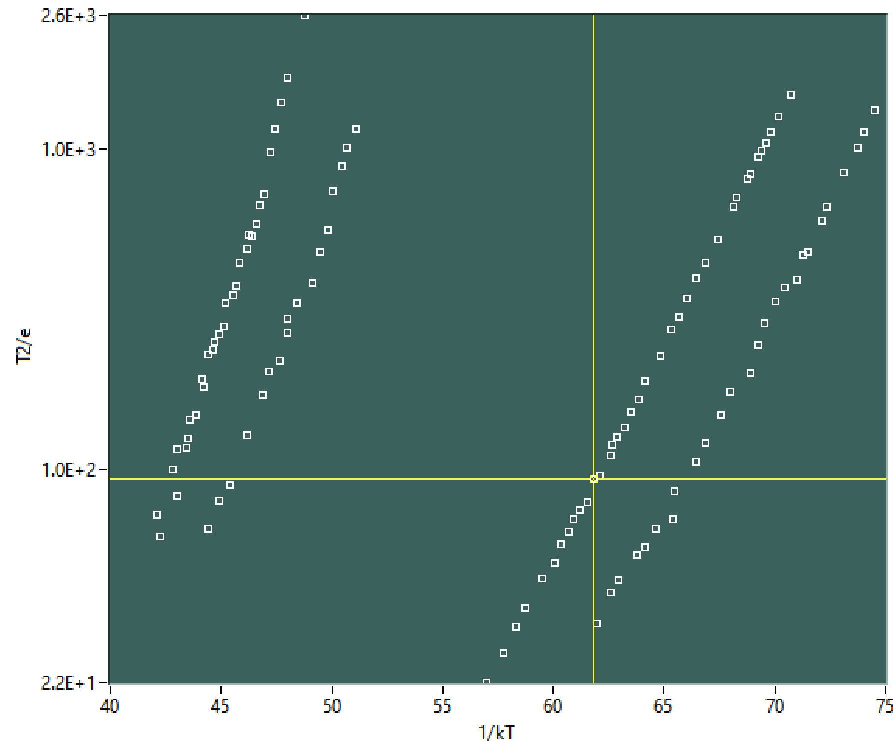


DLTS measurements: pn-junction diode

DLTS spectrum:

- 2 maxima
- analysis with Gaussian deconvolution
  ⇒ peaks contain 2 traps each





Vf=0V
tf=10ms
Vbias=-1V

trap params from Arrhenius plot:

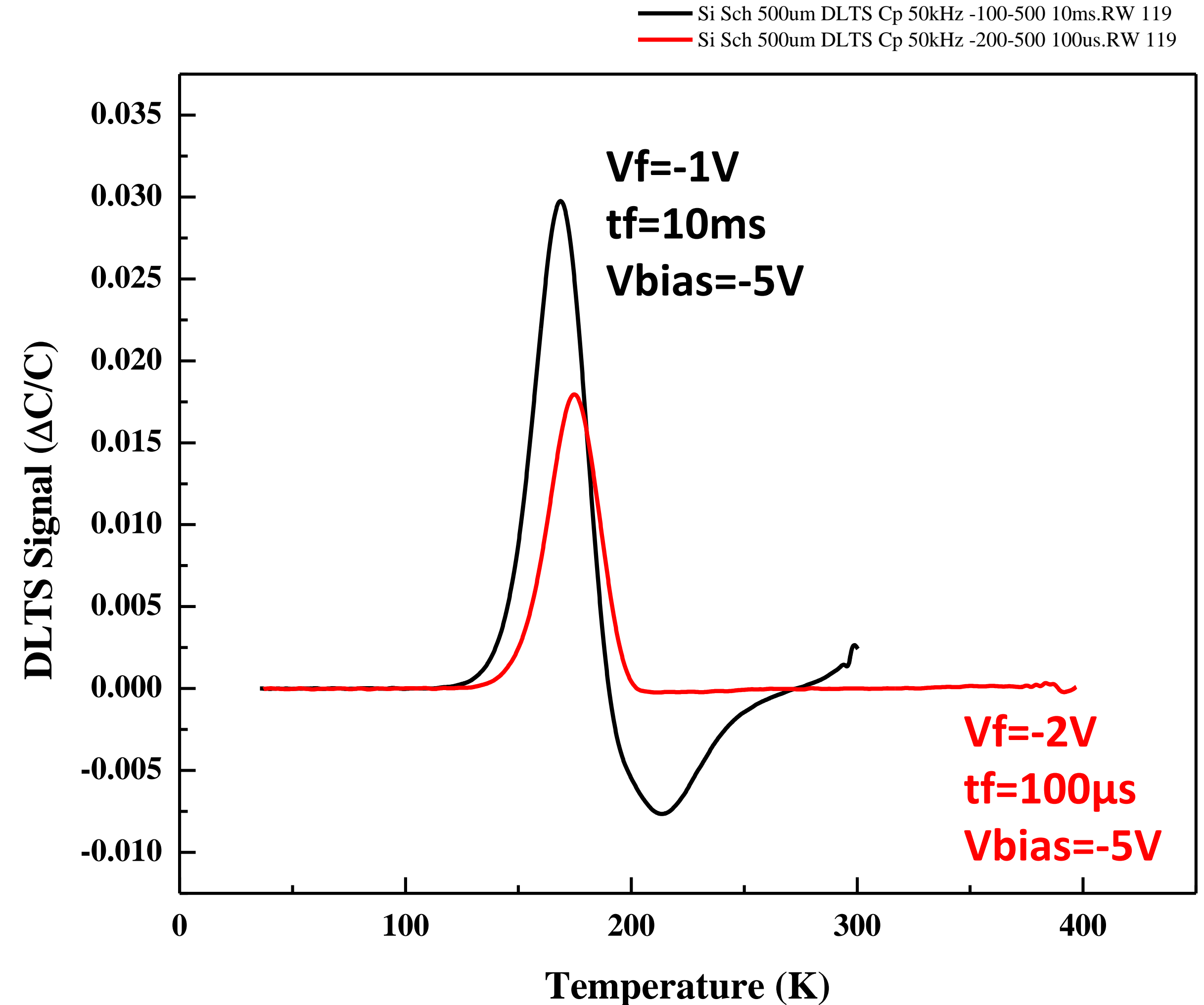
Midpoint temp (K)	E_t (eV)	Sigma (cm^2)	N_t/N_s
170.6	0.293	7.6E-16	9.7E-3
182.8	0.310	7.0E-16	2.1E-2
241.8	0.430	1.0E-15	7.6E-4
258.5	0.536	3.2E-14	3.5E-3

DLTS measurements: Schottky diode

DLTS spectrum:

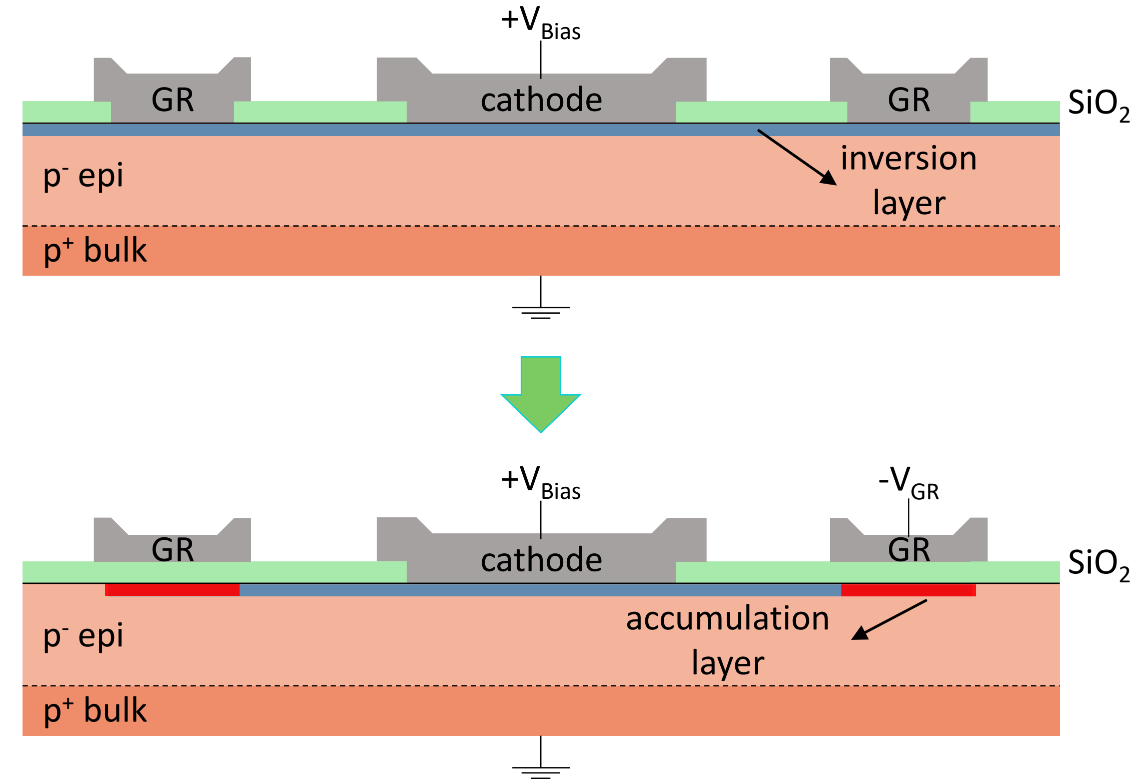
- 1 peak with 2 majority carrier traps
- ‘minority’ carrier trap
  ⇒ vanishes for reduced + shorter filling pulse
  ⇒ surface/interface states likely
- large majority carrier trap for larger filling pulses at room temperature

Midpoint temp (K)	E_t (eV)	Sigma (cm^2)	N_t/N_s
170	0.312	5.5E-15	7.8E-3
180	0.294	3.3E-16	2.2E-2



Reducing leakage current: MOS gate guard ring structure

- some Schottky diodes on 1e13 cm^{-3} wafer had high leakage currents
- tests showed that cause was formation of electron inversion layer
- expected typical behaviour after radiation damage in oxide
  - outlook to actual behaviour after irradiation
- mitigate by modifying the masks to isolate GR on oxide
- apply low negative V to gated GR
  - accumulation layer formation in interface
  - limit inversion layer



solve this issue now

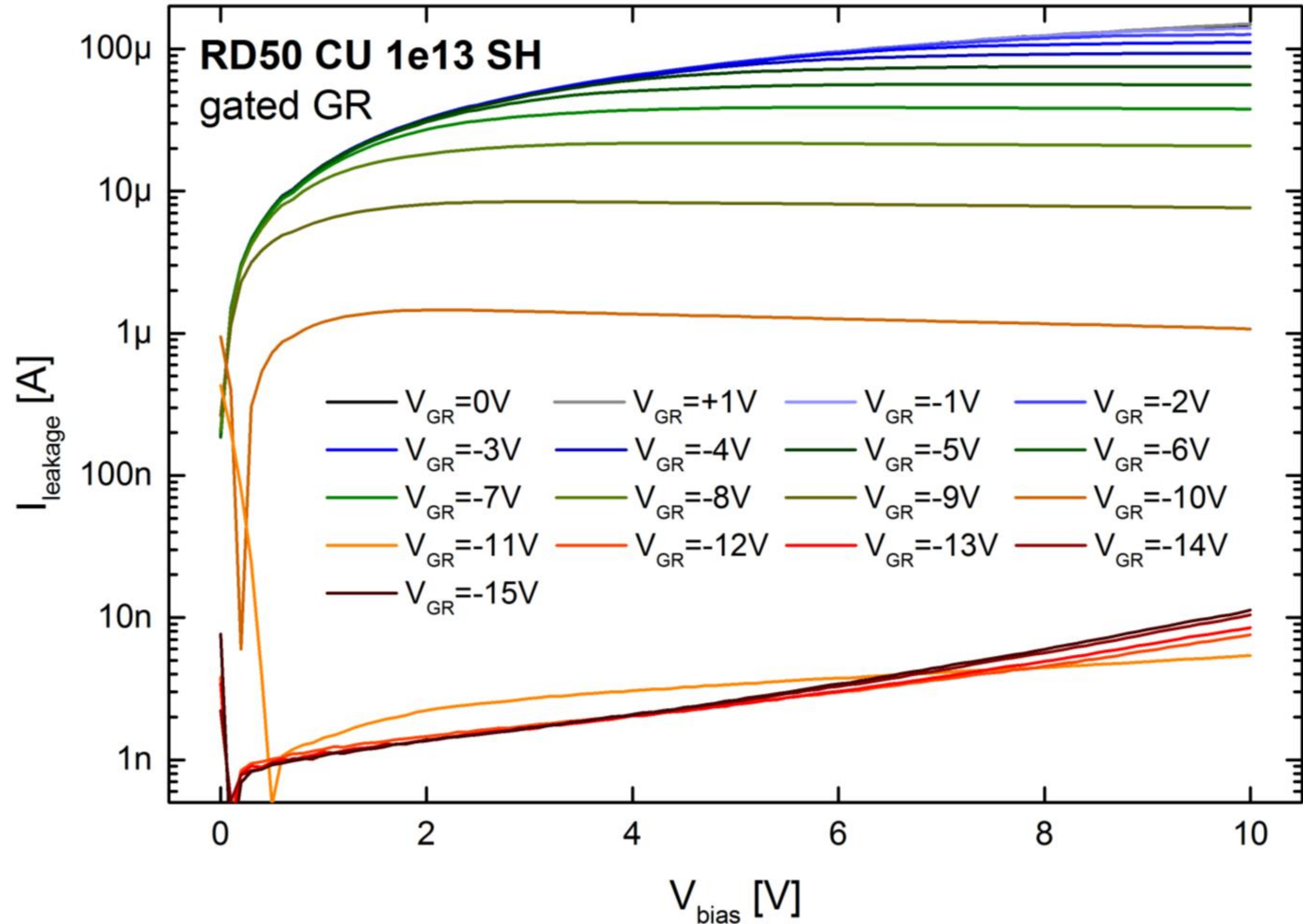
⇒ improve performance of irradiated devices later

Reducing leakage current: MOS gate guard ring structure

- gated GR yielded expected results
- high leakage fully mitigated for V_{GR} <-10V
  - depending on oxide thickness
- devices even showed ‘memory effect’
  - stable-ish charge traps in interface
  - further improvements during repeated scans

➢ use p-stop for comparison and more consistent performance
  ➢ better definition of active volume

➢ looking forward to effects on irradiated devices



Summary & outlook

- fabrication and testing has proceeded successfully after shutdown periods due to Covid
- TCAD simulations of Schottky diodes ongoing
  - need to improve breakdown voltage simulation
- fabrication efforts at RAL and CUMFF has ramped up
  - new mask design at CUMFF proves adaptability of fabrication process to findings

<u>Outlook:</u>

- ➢ charge collection measurements at RAL
- ➢ DLTS + TAS measurements at Carleton
- ➢ RAL Schottky diodes underwent neutron irradiation at Ljubljana
  - ➢ post-irradiation results coming soon (including DLTS)
  - ➢ CUMFF pn-junction diodes will be irradiated in coming months