MALTA3: concepts for a new radiation tolerant sensor in the TowerJazz 180nm technology

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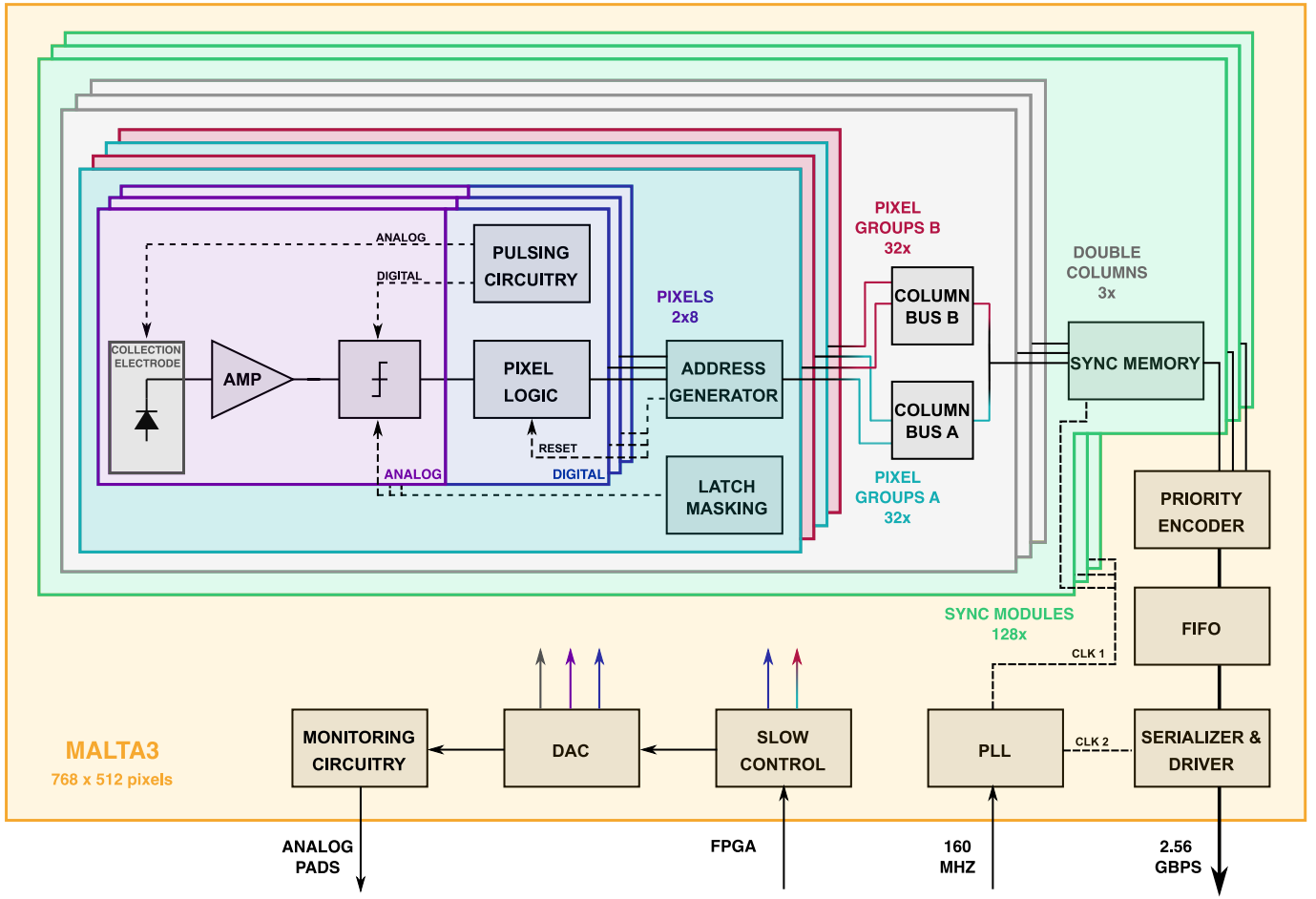
VCI 2022

MALTA3 concept

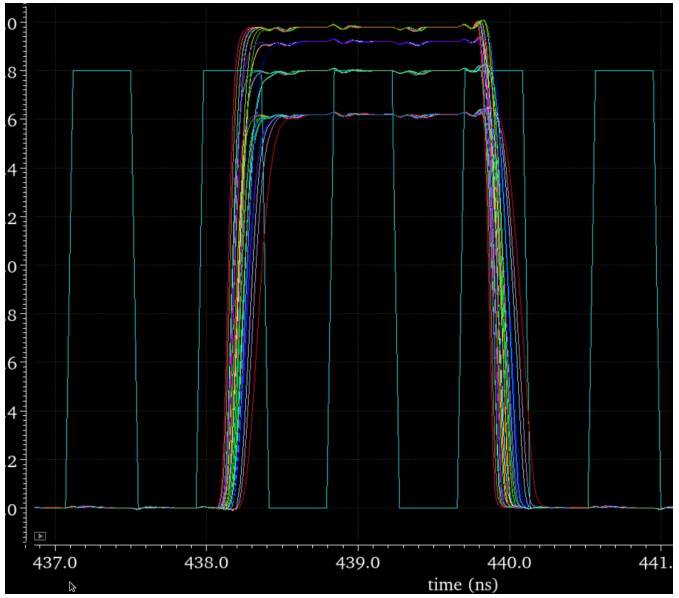
- The MALTA3 will expand the on-chip synchronization concept explored with the miniMALTA
- The MALTA merging structure will be replaced by multiple stages of FIFO memories with corresponding priority encoders
- A new 1.28 GHz PLL will be implemented to drive the output serializers and the snychronization memory
- Output data will be encoded using the standad 64b/66b Aurora protocol
- The slow control will be based on the I2C protocol



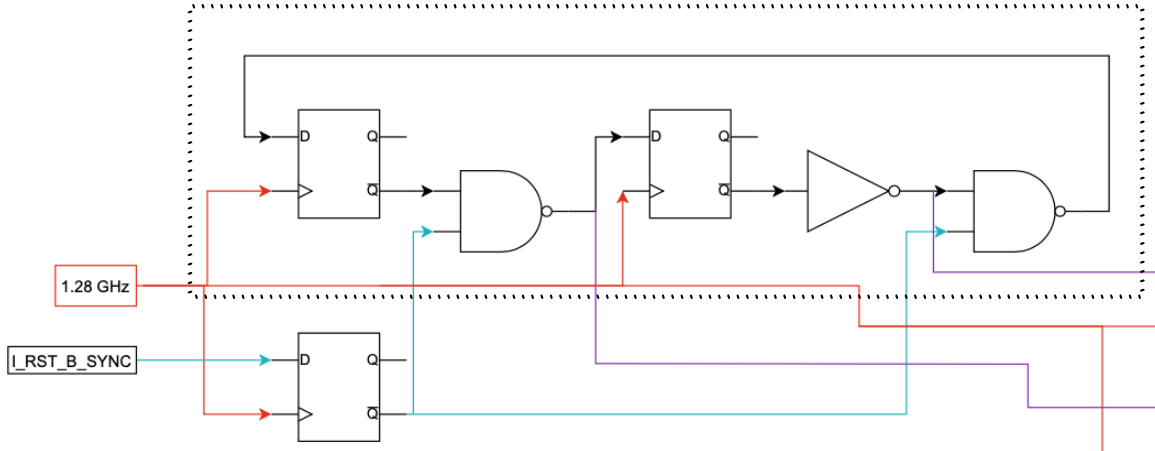
MALTA3 upgrades

- The synchronization memory will be upgraded with a 1.28 GHz Gray encoded twisted ring counter
  - A sub-nanosecond timing resolution is the primary motivator
- The module is demonstrated to work in extracted simulations
- Synthesized module made completely out of standard cells (180nm)

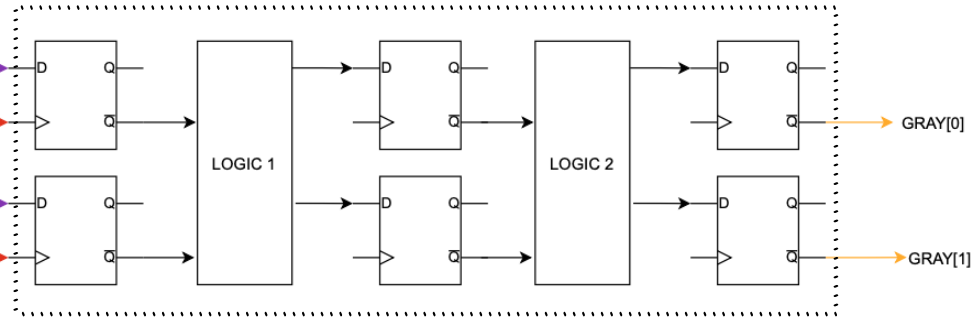
Least significant bit of the Gray encoded timestamp



Twisted ring counter



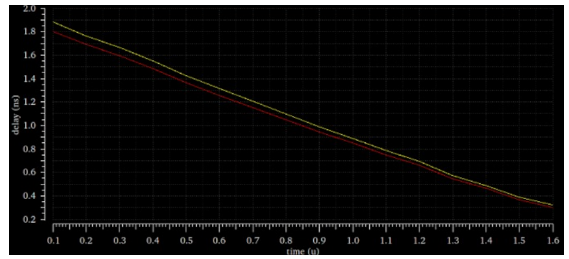
Multi stage gray encoder



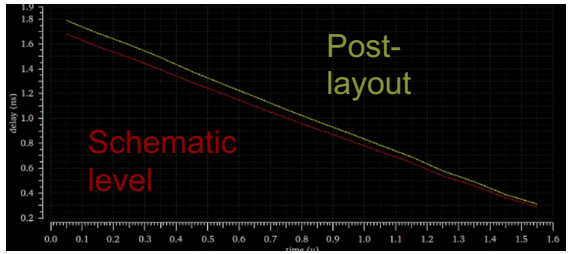
MALTA3 upgrades

- Previous MALTA sensors implemented a pulse generator circuit based on an inverter chain delay cell
  - Although made to work at 4 operating points between 0.5 – 2ns, measurements shown less consistent results (2 - 5ns)
- Long pulses occupy the column bus for longer, reducing the theoretical max throughput
  - Fine control of this pulse is needed to find the limits of the synchronization memory at the end of the columns, as well as making corrections throughout the service life of the sensor
- The new circuit implements a feedback path, allowing the use of a single delay cell to generate the two subsequent pulses (reference and reset)
  - Reduces the footprint of the circuit, allowing other features to be implemented in the already spatially constrained pixel group

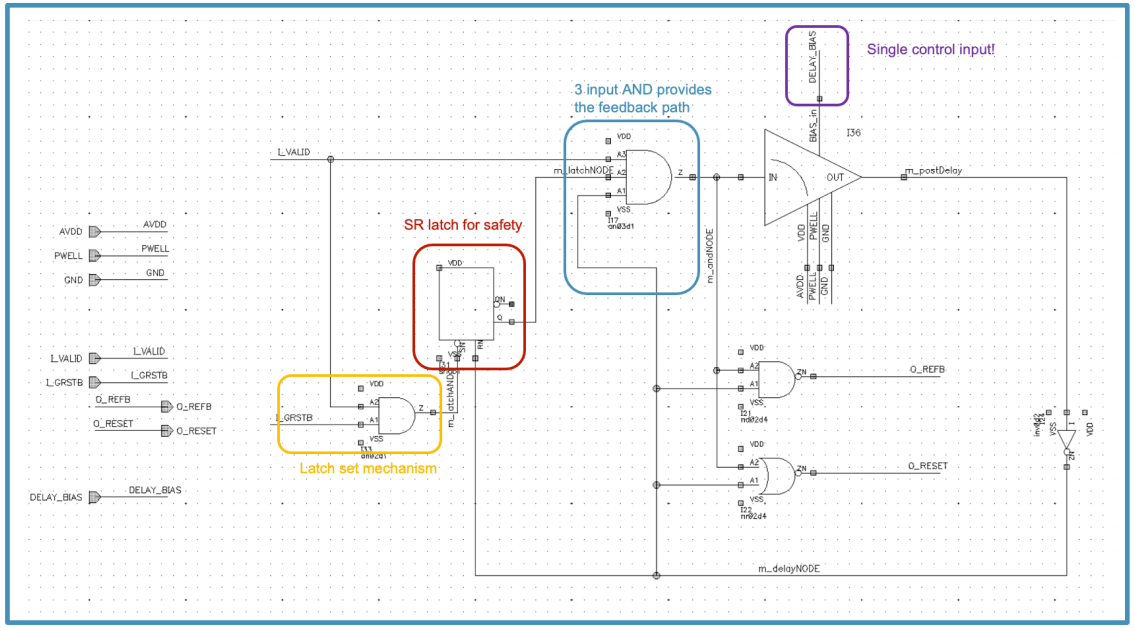
Falling edge delay



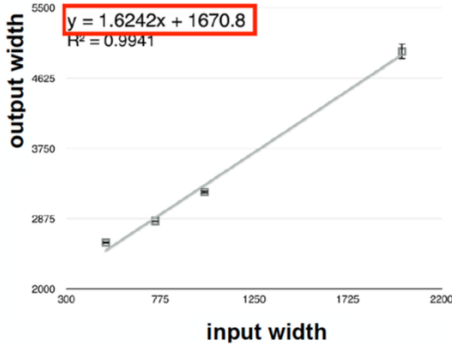
Rising edge delay



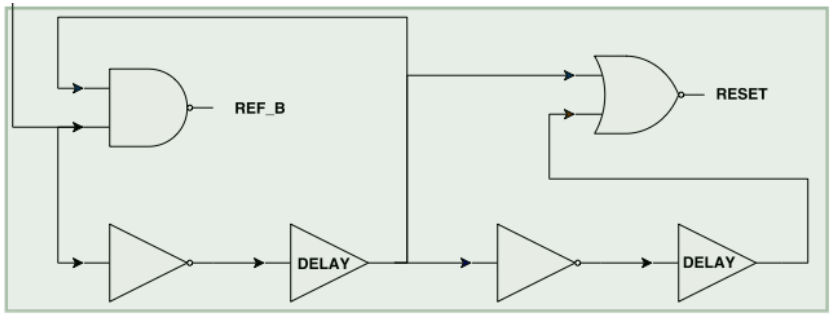
MALTA3 design



Original pulse width measurement

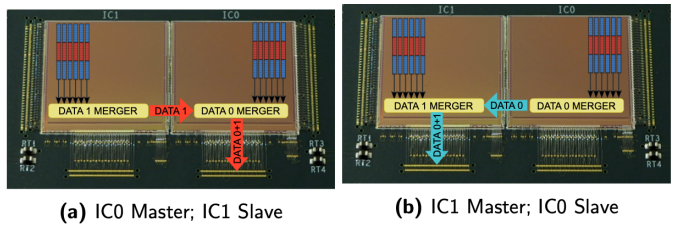


Original design



MALTA3 upgrades

- An important feature of the original MALTA chip is the ability to merge registered hits between multiple chips
  - Done asynchronously as an extension of the merging structure
  - This approach is not applicable in the synchronized periphery
- Multiple serial links between chips are proposed – these links would be independent and would serve a predetermined part of the sensor
  - Inspired by the RD53B channel bonding solution, but in this case the additional encoding/decoding step would be skipped
- 1st stage FIFO memories would be used as temporary buffers before transmisison is able to occur



(a) IC0 Master; IC1 Slave **(b)** IC1 Master; IC0 Slave

MALTA3 concept →

← MALTA solution