A Highly Programmable SiPM Readout ASIC for Neutron Imaging Applications

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Overall Project Goals

- Develop an application specific integrated circuit (ASIC), to use in conjunction with existing photosensor technologies (SiPMs) and plastic/organic scintillator materials to demonstrate a portable and compact pixelated neutron camera
    - This technology can also be used for neutron tagging in nuclear recoil calibration systems for high energy physics experiments (dark matter, neutrino)
- Set up a SiPM+Scintillator characterization testbed for in-depth fast neutron/gamma PSD studies with various scintillators and radioactive sources

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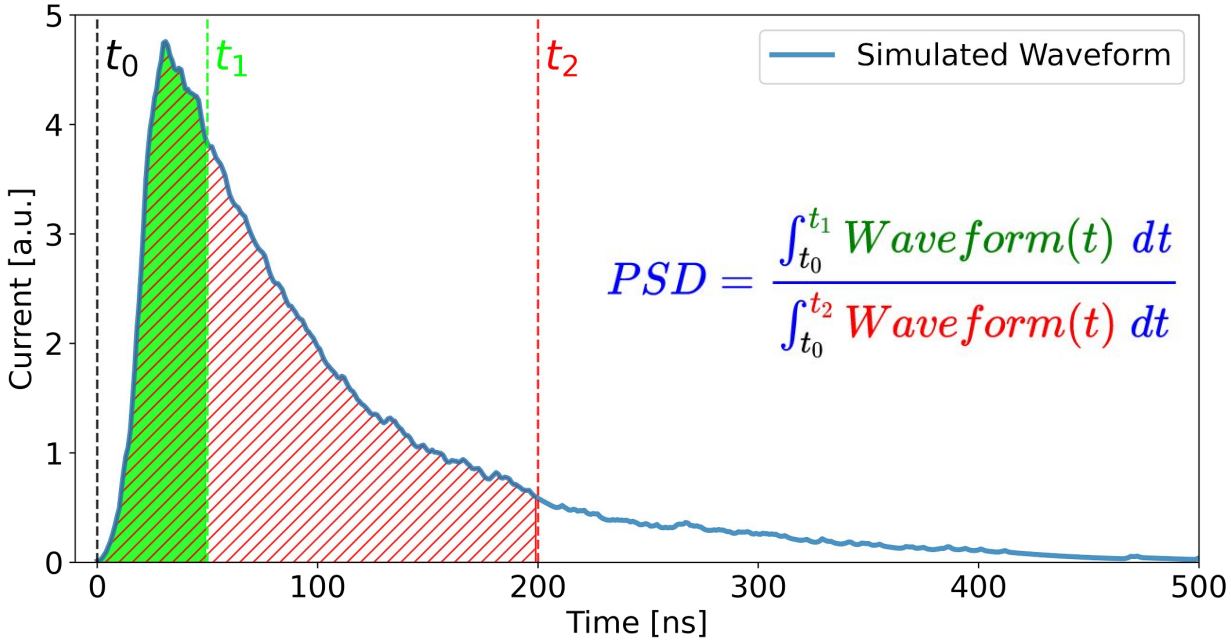
If interested in more details, please email jyjohnson@ucdavis.edu.

What is Pulse Shape Discrimination? (PSD)

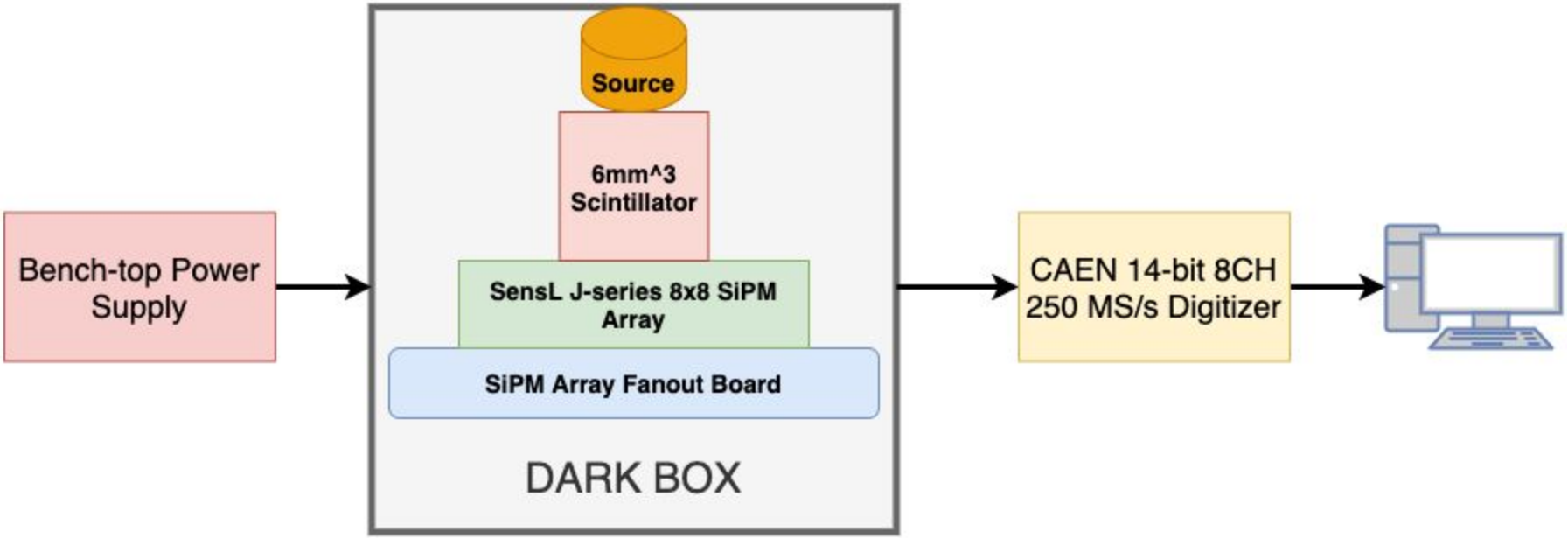
The **emission spectra** from a scintillator can be **dependant on the type of interacting particle**. Therefore, the **resultant electronic pulse** output by an optical sensor has characteristics (timing and intensity) **dependant on the particle type**. This allows for the **discrimination of particles by their induced pulse shape**.



SiPM-Scintillator Testbed Single Pixel Studies

- **Overall goal is to characterize the (energy dependent) PSD capabilities of both EJ-276 and Stilbene scintillators coupled to SiPMs using sealed sources**
  - This will then later be expanded to include other scintillators
- **First, characterize baseline noise of the testbed and optimize appropriate triggering threshold for data collection (to account for dark count pileup effects)**
- **Obtain observed energy response of the scintillators (i.e. get number of photons detected [phd] to keV conversion factor)**
  - Fold in SiPM bias-dependent gain
  - Use several known peaks from sealed gamma sources (^{57}Co, ^{109}Cd and ^{137}Cs)
- **Evaluate PSD, using AmBe neutron source (also emits low and high energy gammas)**

SiPM+Scintillator Testbed Setup



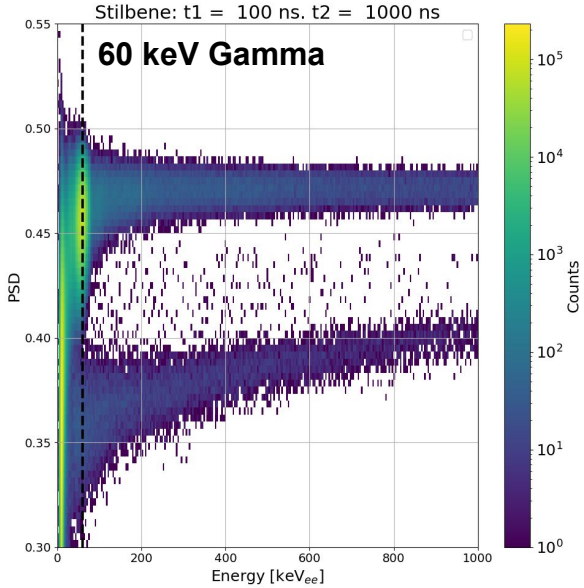
PSD as a Function of Energy Using AmBe

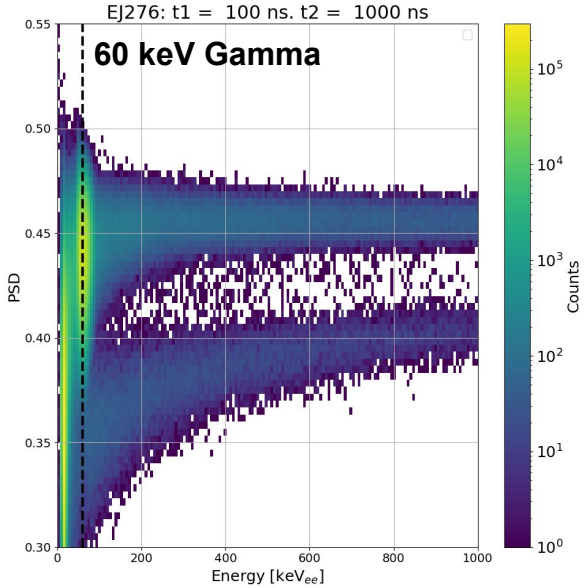
Data collected using CAEN thresholds of -0.24mV and -12.45 mV

Low energy population attributed to dark count pile up effects

Population at ~60 keV in gamma band is from the 60 keV gamma of Am-241 decay

Higher population in gamma distribution attributed to the 4.4 MeV gamma





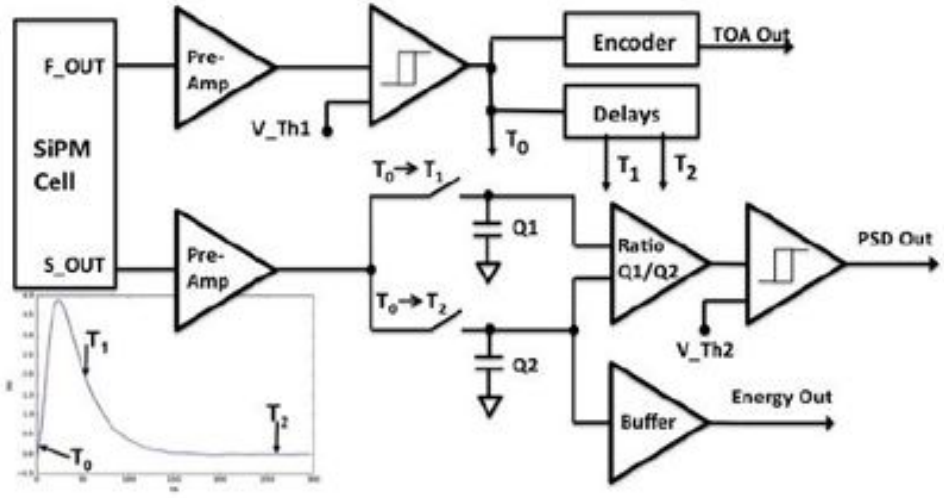
Prototype ASIC (PSD_CHIP) Design Goals

- **Allow for real-time rejection of gamma backgrounds**
  - addressed by our fast analog pulse shape discrimination (PSD) circuit design on chip
- **Be adaptable to different plastic/organic scintillator materials**
  - addressed by programmability and tunability provided on chip for selection of short and long integration windows
- **The ASIC front-end system should be designed to handle SensL SiPMs (two coupled outputs per SiPM)**
  - addressed by our custom front-end amplification stages
  - SiPMs were chosen as the photosensor because they are solid state devices that work at low voltage and power
- **Ensure maximum programmability/tunability of all parts of chip design for first prototype and all important nodes are available as external outputs**
  - Second chip design will be more practical and focused, using insight gained from testing of the prototype

Why a Fast, Analog PSD Method?

- **When targeting a low power, compact and mobile neutron imaging system, an analog system is a lower power option**
  - Existing techniques using ADCs + FPGAs consume a lot of power and are not suitable for longer term remote deployment
- **An efficient and fast analog PSD method will streamline data throughput in such a neutron imaging system's electronics**
  - We are able to classify neutron events in real time (with some efficiency)
  - The trick is in implementing the partial/total integration ratio using analog signal processing blocks (more in later slides)
- **We are developing a scalable custom ASIC that will deliver both the front-end system for SensL SiPM outputs and fast, analog PSD**

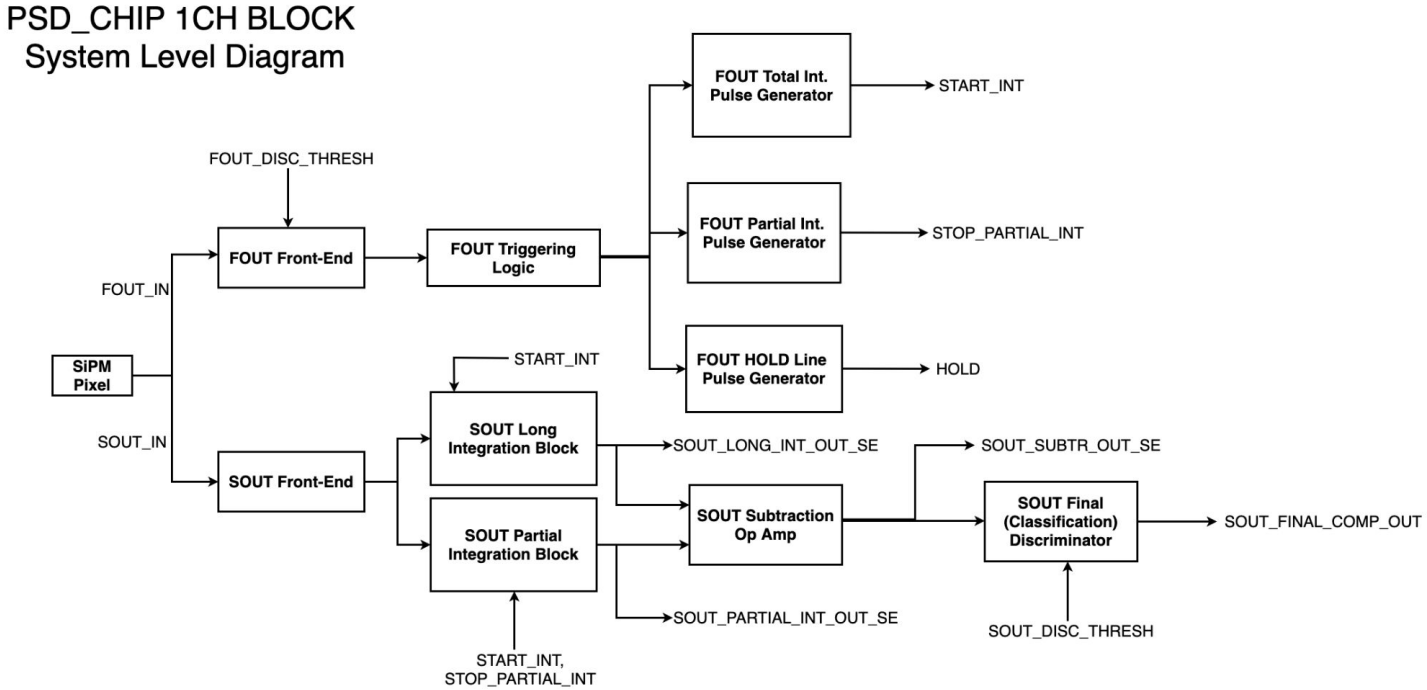
Conceptual Overview of PSD_CHIP 1CH Block



SensL SiPMs provide a capacitively coupled fast output (FOUT) and a resistively coupled standard output (SOUT)

PSD_CHIP is a 4 channel ASIC that takes in the dual FOUT, SOUT output lines of 4 SensL SiPMs

Detailed Overview of PSD_CHIP 1CH Block



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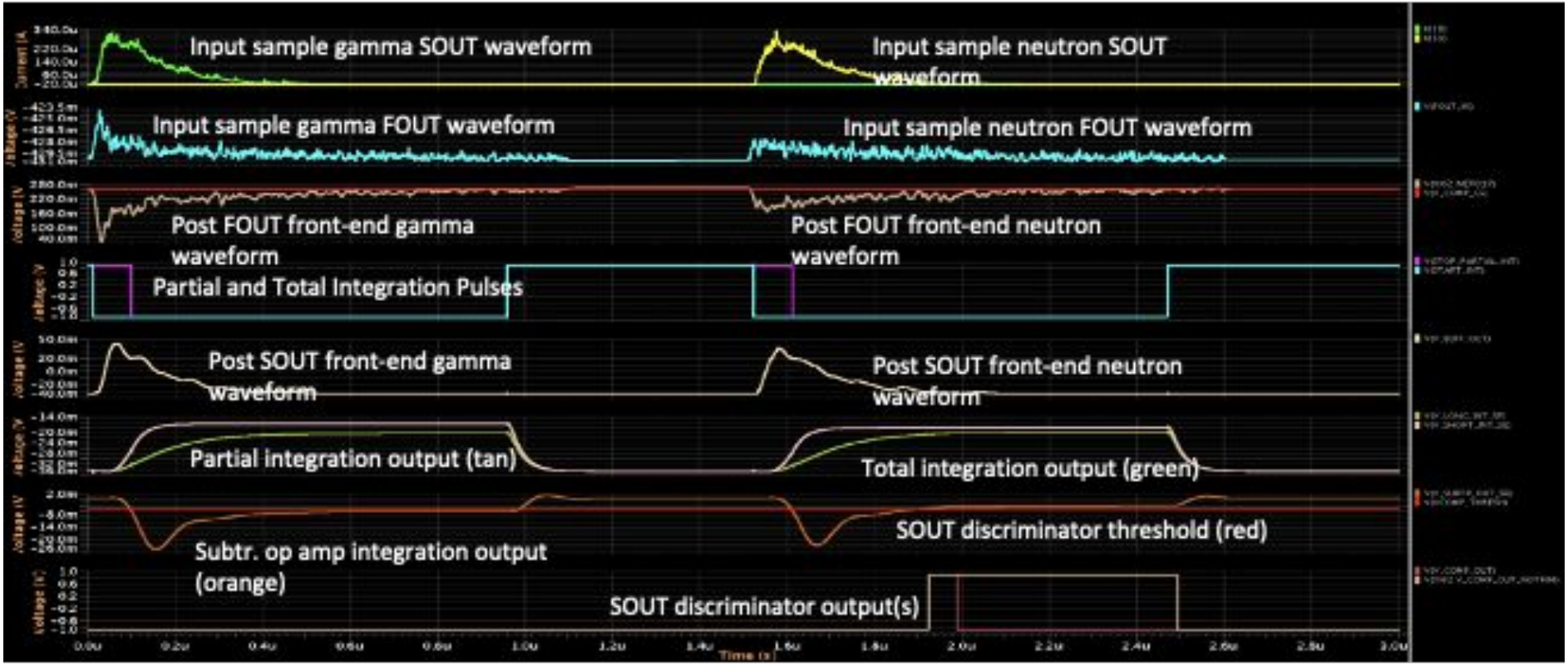
PSD_CHIP Fast Analog PSD Implementation

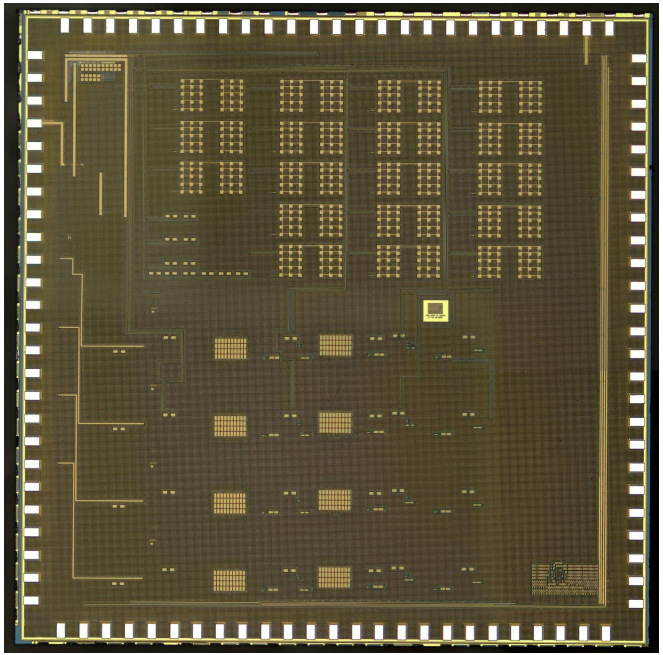
- Fast analog PSD is implemented using the SOUT line
- **Each SOUT signal is split into total and partial integration channels on chip**
- **Two-stage programmable system allows for fine tuning of total integration windows up to ~2.5us and ~200ns for partial integration (more details on later slide)**
- Tunable resistors on total integration channels allow for defining the expected ratio of partial/total integration values
- Subsequent subtraction op amps quantify differences from expected ratio for a given incident particle
- A discriminator w/ a highly tunable threshold triggers on that difference for fast neutron/gamma classification
- **All stages are available as external outputs per channel**

Sample SOUT Analog Signal Chain



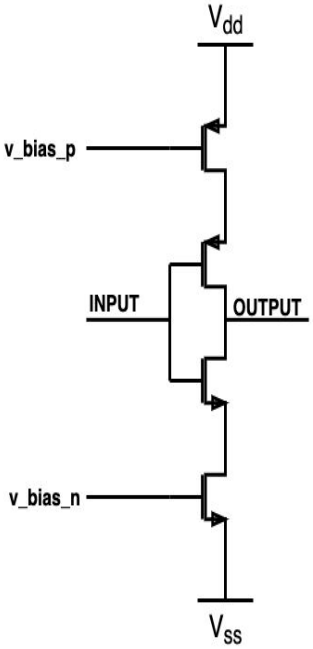
PSD_CHIP as Fabricated

- **The chip has both an analog and (synthesized) digital core**
- **Analog core is the heart; contains all signal processing for both SiPM outputs (for the four channels) as well as various biasing blocks, DACs, etc**
- **Digital core is responsible for all programmability/tunability selection on-chip**
  - This enables the use of different scintillators by allowing for tuning of short, long integration windows and tunable resistor values (more on later slide)



T1 and T2 Integration, Two-Stage Programmability

- **Chain of (different length) current starved inverters form the basis of short and long integration window tunability**
  - These inverters operate by limiting rise and fall times based on supplied bias current
  - Bias current is set by a 5-bit current DAC that takes as input the LSB current value
    - This value can be constant or set using an external DAC (it is an input pad to the chip)
- **Can theoretically hit any integration window length up to the max value (fixed by the length of the inverter chain)**
  - Step size/resolution set by external DAC specs and noise limitations
    - Important part of PSD_CHIP design we want to validate and characterize during initial testing of the fabricated chips
  - This, combined with the ability to select between 15 total integration resistor values, allows for maximal flexibility in adapting the chip for use with various scintillators



PSD_CHIP Programmability Cont.

- **PSD_CHIP digital core contains 40 8-bit registers**
  - Can be read/written to using simple UART (Universal Asynchronous Receiver/Transmitter)
  - Two interface modes (w/ chip always secondary)
    - POSI = Primary-Out-Secondary-In (data to chip)
    - PISO = Primary-In-Secondary-Out (data from chip)
- **Programmability includes control of:**
  - Reference voltages (for integration stage baselines)
    - Mitigation of DC baseline offset integration in parallel integration channels
  - Discriminator thresholds (for FOUT triggering using discriminator, and SOUT classification discriminator)
  - Total integration channel tunable resistor (15 selectable values)
  - Bias currents for current starved inverter delay lines (sets the lengths of the partial and total integration lines, etc)
- **Digital bits set in registers are control bits for various current and voltage DACs that generate appropriate analog thresholds, references, etc**

Current Status and Next Steps

- **Testing with the initial chips returned from foundry has shown issues with power routing on chip**
  - This has led to channel to channel variations in performance
  - Bench testing is currently ongoing in order to characterize this in detail as well as overall performance of the chip
- **A second prototype version of the chip, PSD_CHIP_v2 is currently being designed and will tape out at the end of March to both fix power routing, but in addition:**
  - A new dual polarity capable SOUT front end has been developed to provide flexibility to different biasing schemes of SiPMs and input dynamic range greater than 1MeV for EJ276 and Stilbene
  - FOUT front end has been improved as well (rise times under 1ns on chip)
  - A new method of generating the partial, total and hold line delays has been implemented on two of the channels that saves on area and power without compromising tunability