Design of Nupix-A1, a MAPS with timing and energy measurement for heavy-ion physics

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On behalf of the IMP&CCNU study group

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Outline

✓ Introduction on HIAF experiment

✓ MAPS development and the prototype
  ─ Sensor, front-end optimization, rolling-shutter readout mode
  ─ Column-level ADC and high speed of data transmission link at 5Gbps

✓ Summary
The new-generation High Intensity heavy-ion Accelerator Facility (HIAF) is being built by the Institute of Modern Physics, Chinese Academy of Sciences (IMP, CAS).

HIAF is an accelerator complex composed of the Superconducting Linac, the Booster Ring, the High Energy Fragment Separator, and the Spectrometer Ring.

HIAF will enable scientists to perform a large variety of modern nuclear physics experiments.
High performance vertex and tracking detectors are in great demanded by various experiments.

Monolithic Active Pixel Sensor (MAPS) with energy, time and position measurement will be used in these experiments.
Integrated sensor and readout electronics on the same silicon bulk with “standard” CMOS process: low material budget, low power consumption, low cost ...

Selected GSMC 130nm technology for Nupix-A1, featuring:

• Thin gate oxide: robust to total ionizing dose
• 1.2V power supply for digital circuit
• 7 metal layers
## MAPS for particle physics experiment

- **MAPS development context and the design goals of our attempt**

<table>
<thead>
<tr>
<th>Name</th>
<th>Structure</th>
<th>Pixel pitch</th>
<th>Integ.time</th>
<th>Power density</th>
<th>Spatial resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>MISTRAL (IPHC)</td>
<td>Column-level comparator, Rolling-shutter</td>
<td>22 × 33 (66) μm²</td>
<td>30 μs</td>
<td>200 (100) mW/cm²</td>
<td></td>
</tr>
<tr>
<td>ASTRAL (IPHC)</td>
<td>In-pixel comparator, Rolling-shutter</td>
<td>24 × 31(IB) μm²</td>
<td>20 μs</td>
<td>85 mW/cm²</td>
<td>≈ 5μm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>36 × 31 (OB) μm²</td>
<td></td>
<td>60 mW/cm²</td>
<td></td>
</tr>
<tr>
<td>ALPIDE (CERN,IN FN,CCNU, YONSEI)</td>
<td>In-pixel comparator, In-matrix zero compression readout</td>
<td>27 x 29 μm²</td>
<td>&lt; 4 μs</td>
<td>&lt; 39 mW/cm²</td>
<td></td>
</tr>
<tr>
<td>Attempt</td>
<td>rolling shutter</td>
<td>compact</td>
<td>&lt; 50 ns (time resolution)</td>
<td>&lt; 200 mW/cm²</td>
<td>&lt; 8μm</td>
</tr>
<tr>
<td></td>
<td>Can measure energy and time</td>
<td></td>
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</tbody>
</table>

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21/2/2022
First MAPS prototype design

- Design goals:
  - Pixel size: < 30x30 μm²
  - Time resolution: < 5 us
  - Power consumption: < 200 mW/cm²

- Pixel pitch: 30x30 μm
- The diode nwell size is 3x3 μm
- Collection Electrode is 10 μm × 10 μm
- Pixel array: 128 row x 64 col
- Front-end: current comparator, analog TAC and source follower
- Triggered readout
- DACs, bias
- 4 columns / 1 ADC (shared for energy and time)
- High speed data transmission: 5 Gbps
First MAPS prototype– energy measurement

- DC-coupled SF pixels: 3T structure
- two level source follower (nmos/pmos SF)
- Spacing = 3 μm, diameter = 3 μm, diode in Octagon shape

- Qin: 1k-100ke-, Gain approx 10μV/e-, tran noise about 3e-
- Linear error: < 2%
- Stabilization time before ADC: 100ns

Output Linearity
First MAPS prototype – time measurement

- ALPIDE-like front-end charge creates negative voltage step $\Delta V_{\text{PIX}_\text{IN}}$ at input node(PIX_IN). M1 acts as a follower and force source to follow gate.

- Threshold 265 e-: from OUT_A baseline voltage to point where discriminated output OUT_D flips when $I_{M8} > I_{DB}$.

$$\Delta V_{\text{OUT}_A} \approx C_z \cdot \Delta V_{\text{PIX}_\text{IN}} \approx \frac{C_z}{C_{\text{OUT}_A}} \cdot \frac{Q_{\text{in}}}{C_{\text{PIX}_\text{IN}}}$$

- Peaking time< 50 ns, time walk 86ns but 14ps after digital buffer, ENC < 8.5 e-
First MAPS prototype – time measurement

- TAC: adjustable charging current from 1nA to 10nA
- Large time measurement range: 3 μs to 100 μs
- Linearity error: < 30 LSB @3 μs, 1LSB = 3ns
Chip periphery: BG and DACs

BandGap: 1.25 V for voltage DACs

Voltage DAC
- 10 bits R-2R DAC, output range 0-3.02 V;
- Power consumption < 150uA.

Current DAC
- 8 bit (0 - 2.52uA), LSB=10 nA;
- The digital decoder is using 6bits thermometer and 2 bits binary to compromise the area and the accuracy.
Chip periphery: Column cyclic ADC

- 11-bit and covers a small area of 100μm x 300μm
- Power consumption is 7.6mW with 3.3V power supply
- Sampling rate 3.63 MSps, SNDR 66.25dB, ENOB 10.7bit
➢ Power supply is 1.2V, consist of 16b/20b encoder, 20:1 serializer, FFE driver, high speed receiver;

➢ 20:1 serializer consumes power:< 28 mA;

➢ The FFE driver consumes power:< 15 mA, work at 5 Gbps;

➢ The receiver is a hysteresis comparator, consume power:< 5 mA, work at 5Gbps;

➢ The power consumption of the whole data transmission link is 58 mA.

➢ The RMS jitter with DCC < 6ps
Summary

◆ This first prototype is under testing;

◆ Two versions of highly compact pixels were developed with rolling-shutter in 0.13 μm CIS CMOS technology;

- **Pixel Size**: $30 \times 30 \ \mu m^2$;

- **Speed**: $8 \ \mu s/\text{row}$;

- **Power**: $350 \ \text{nA/pixel}$, analog power supply is $3.3V$;

- Can measure energy, time and position;

- Power density is about $300\text{mW/cm}^2$;

◆ This chip is under testing, the accuracy needs to be improved in the next version.

*Thank you very much for your time!*