Design of Nupix-A1, a MAPS with timing and energy measurement for heavy-ion physics

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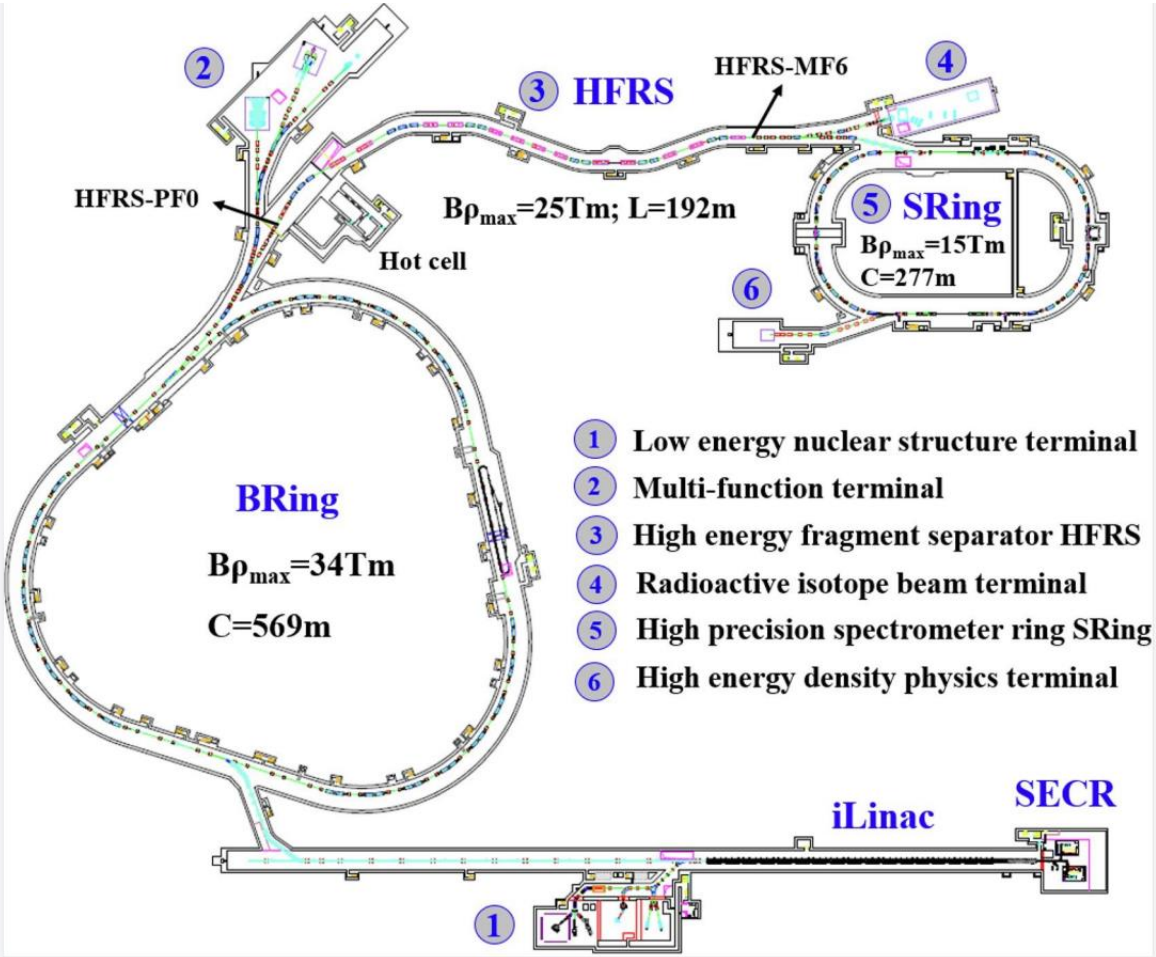
Outline

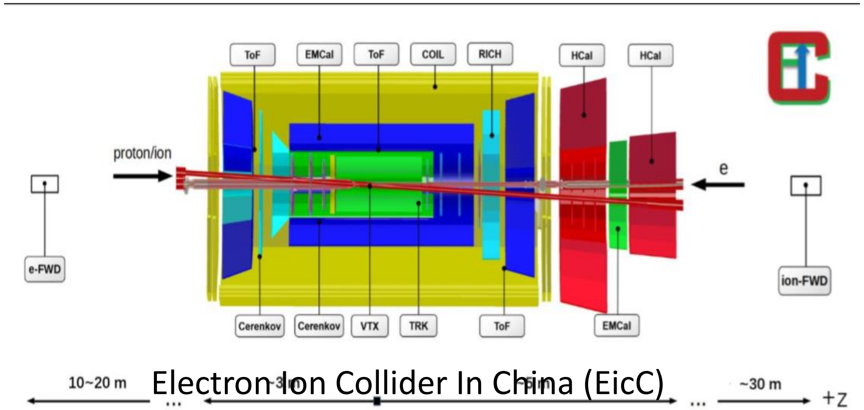
- ✓ Introduction on HIAF experiment
- ✓ MAPS development and the prototype
  - – Sensor, front-end optimization, rolling-shutter readout mode
  - – Column-level ADC and high speed of data transmission link at 5Gbps
- ✓ Summary

HIAF experiment

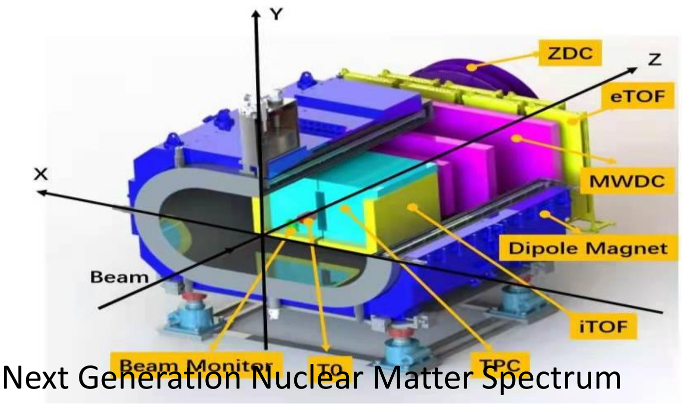


- The new-generation High Intensity heavy-ion Accelerator Facility (HIAF) is being built by the Institute of Modern Physics, Chinese Academy of Sciences (IMP, CAS)
- HIAF is an accelerator complex composed of the Superconducting Linac, the Booster Ring, the High Energy Fragment Separator, and the Spectrometer Ring.
- HIAF will enable scientists to perform a large variety of modern nuclear physics experiments

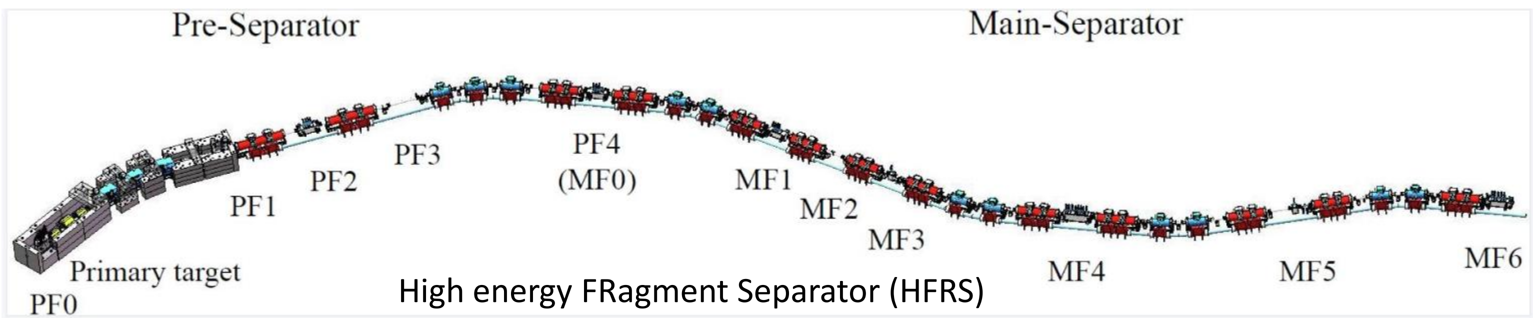
HIRFL-CSR



Electron Ion Collider In China (EicC)



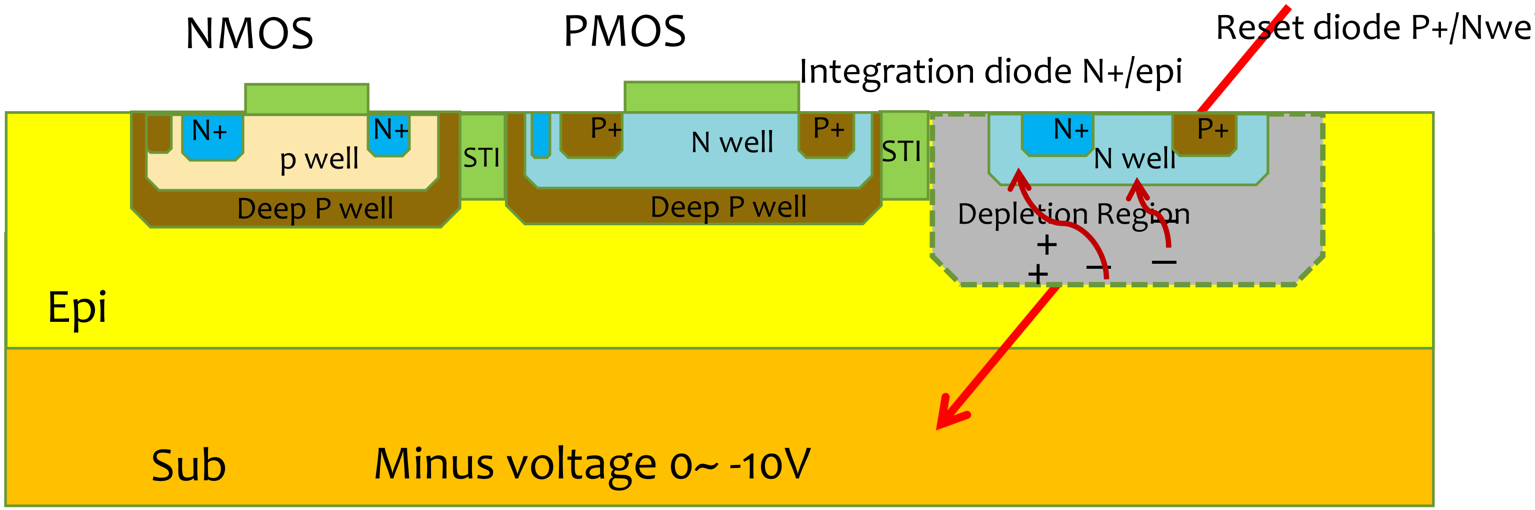
Next Generation Nuclear Matter Spectrum



High energy FRagment Separator (HFRS)

- High performance vertex and tracking detectors are in great demanded by various experiments
- Monolithic Active Pixel Sensor (MAPS) with energy, time and position measurement will be used in these experiments

CMOS pixel sensor and technology



- Integrated sensor and readout electronics on the same silicon bulk with "standard" CMOS process : low material budget, low power consumption, low cost ...

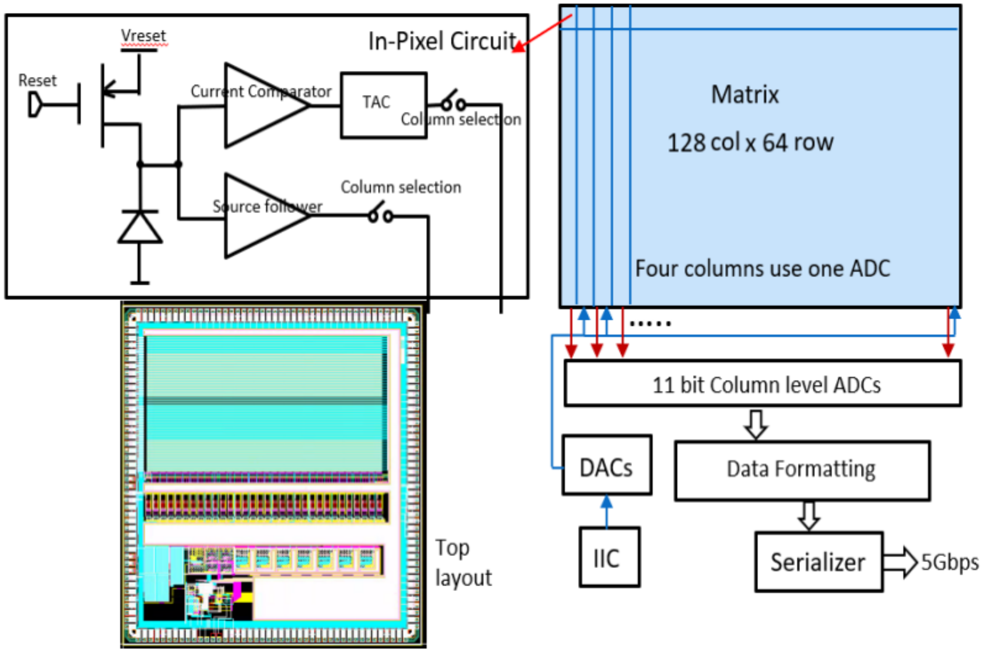
- Selected GSMC 130nm technology for Nupix-A1, featuring:
  - Thin gate oxide: robust to total ionizing dose
  - 1.2V power supply for digital circuit
  - 7 metal layers

MAPS for particle physics experiment

- MAPS development context and the design goals of our attempt

Name	Structure	Pixel pitch	Integ.time	Power density	Spatial resolution
MISTRAL (IPHC)	Column-level comparator, Rolling-shutter	22 × 33 (66) μm^2	30 μs	200 (100) mW/cm^2	$\approx 5\mu m$
ASTRAL (IPHC)	In-pixel comparator, Rolling-shutter	24 × 31(IB) μm^2 36 x 31 (OB) μm^2	20 μs	85 mW/cm^2 60 mW/cm^2	
ALPIDE (CERN,INFN,CCNU, YONSEI)	In-pixel comparator, In-matrix zero compression readout	27 x 29 μm^2	< 4 μs	< 39 mW/cm^2	
Attempt	rolling shutter Can measure energy and time	compact	< 50 ns (time resolution)	< 200 mW/cm^2	< 8μm

First MAPS prototype design



- Pixel pitch: 30x30 μm
- The diode nwell size is 3x3 μm
- Collection Electrode is 10 μm × 10 μm
- Pixel array:128 row x 64 col
- Front-end: current comparator, analog TAC and source follower
- Triggered readout
- DACs, bias
- 4 columns /1 ADC(shared for energy and time)
- high speed data transmission: 5 Gbps

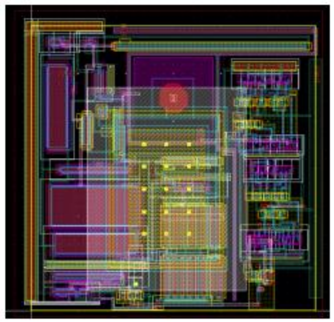
- Design goals:
  - Pixel size: < 30x30 um^2
  - time resolution: < 5 us
  - Power consumption: < 200 mW/cm^2

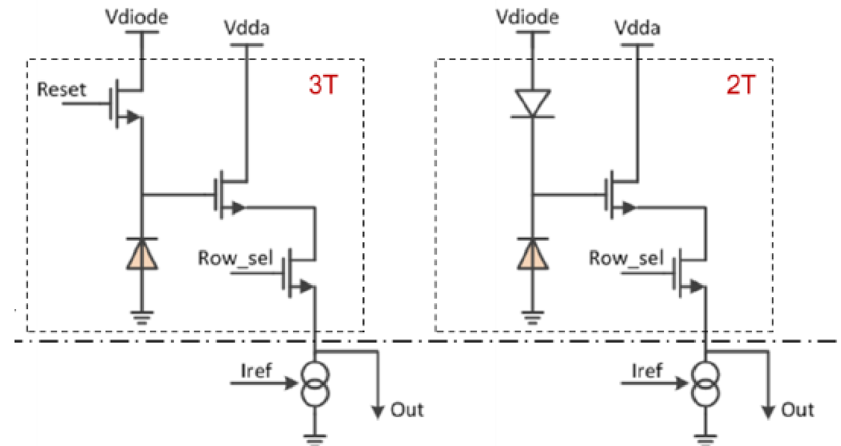
First MAPS prototype– energy measurement

– DC-coupled SF pixels: 3T structure

– two level source follower (nmos/pmos SF)

– Spacing = 3 µm, diameter = 3 µm, diode in Octagon shape

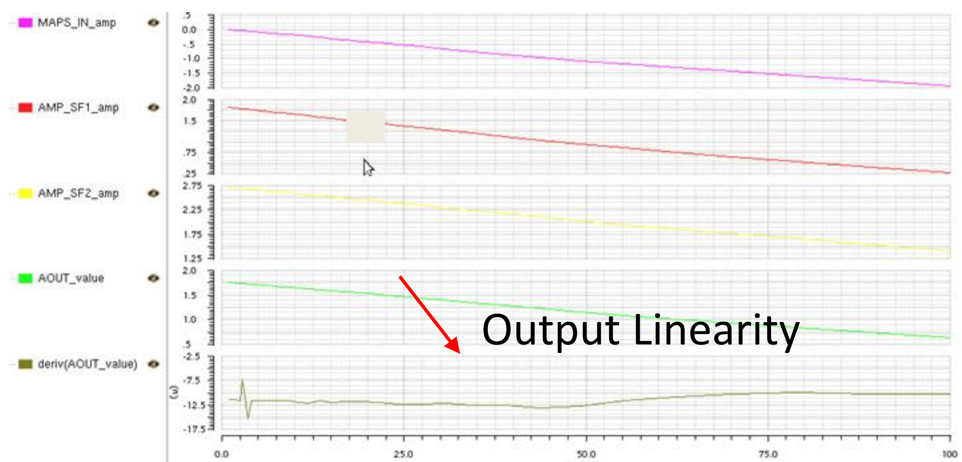




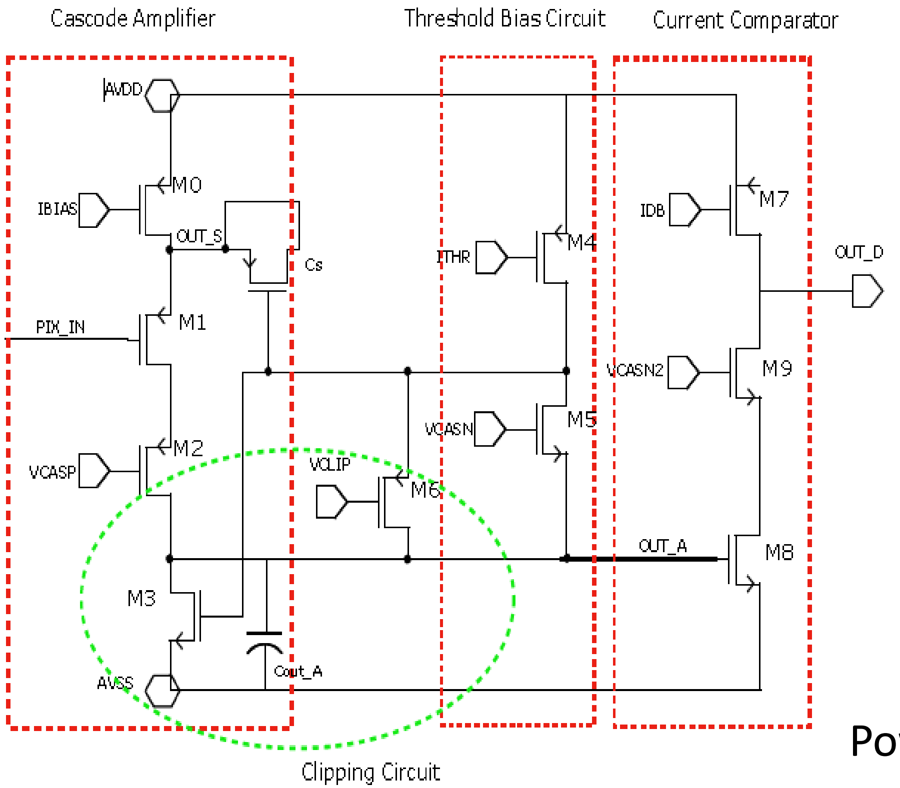
➢ Qin: 1k-100ke-, Gain approx 10uV/e-, tran noise about 3e-

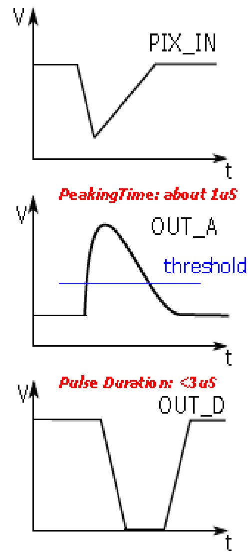
➢ Linear error: < 2%

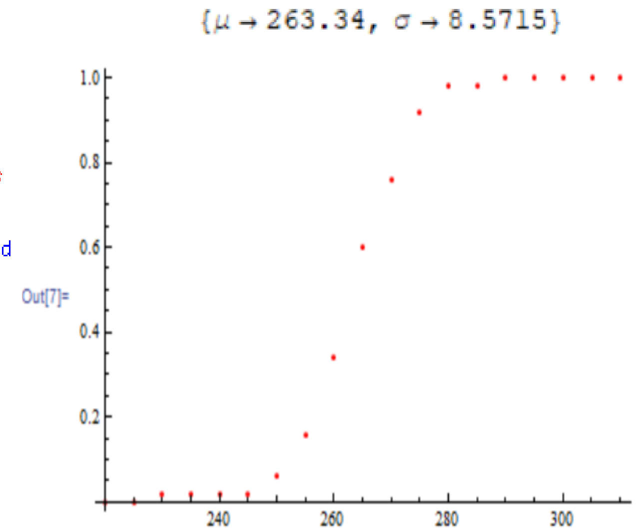
➢ Stabilization time before ADC： 100ns



First MAPS prototype– time measurement







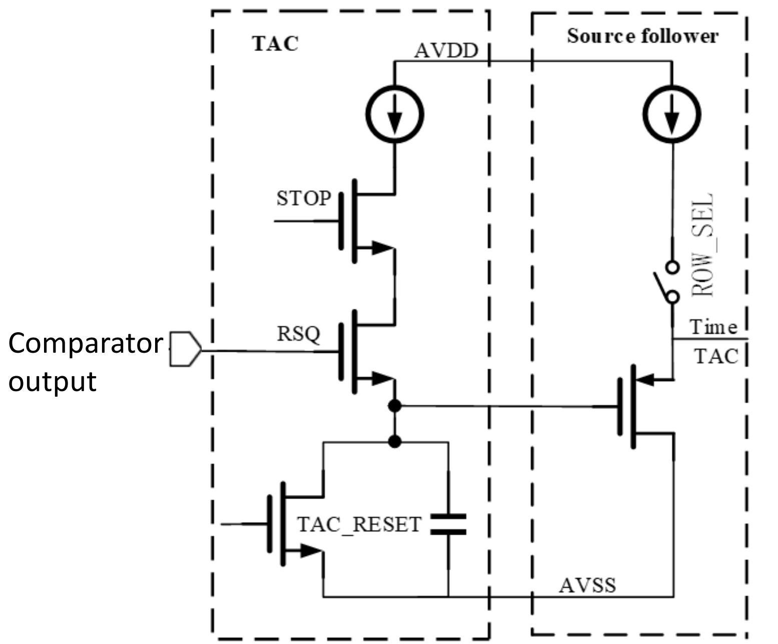
Power: 111nA/pixel

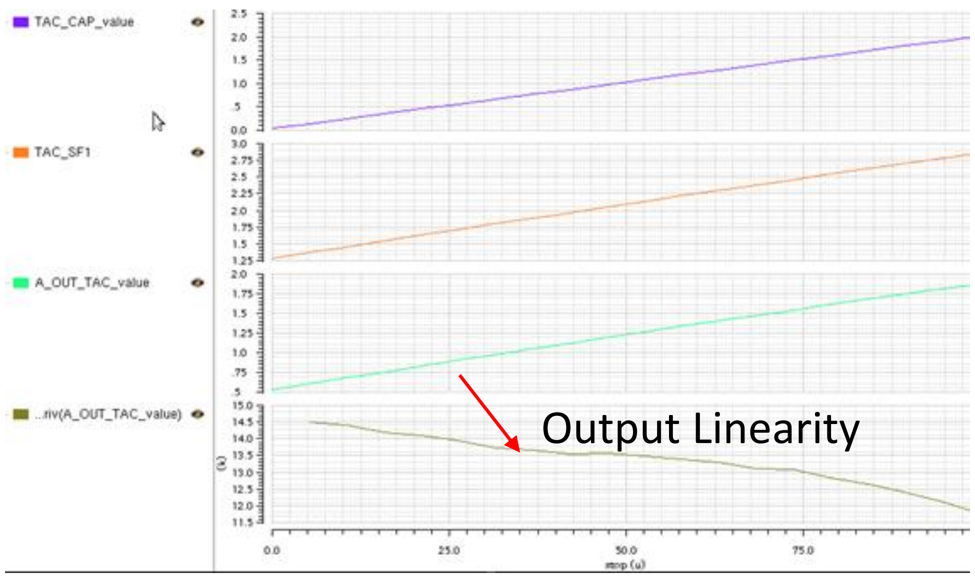
- ALPIDE-like front-end charge creates negative voltage step ΔV_{PIX_IN} at input node(PIX_IN). M1 acts as a follower and force source to follow gate.
- Threshold 265 e- : from OUT_A baseline voltage to point where discriminated output OUT_D flips when $I_{M8} > I_{DB}$.

$$\Delta V_{OUT\_A} \approx \frac{C_s \bullet \Delta V_{PIX\_IN}}{C_{OUT\_A}} = \frac{C_s}{C_{OUT\_A}} \bullet \frac{Q_{in}}{C_{PIX\_IN}}$$

- Peaking time< 50 ns, time walk 86ns but 14ps after digital buffer , ENC < 8.5 e-

First MAPS prototype– time measurement

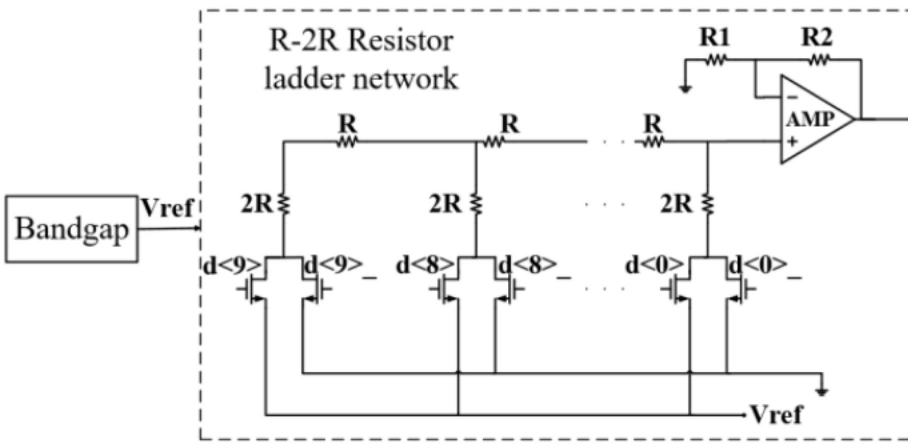


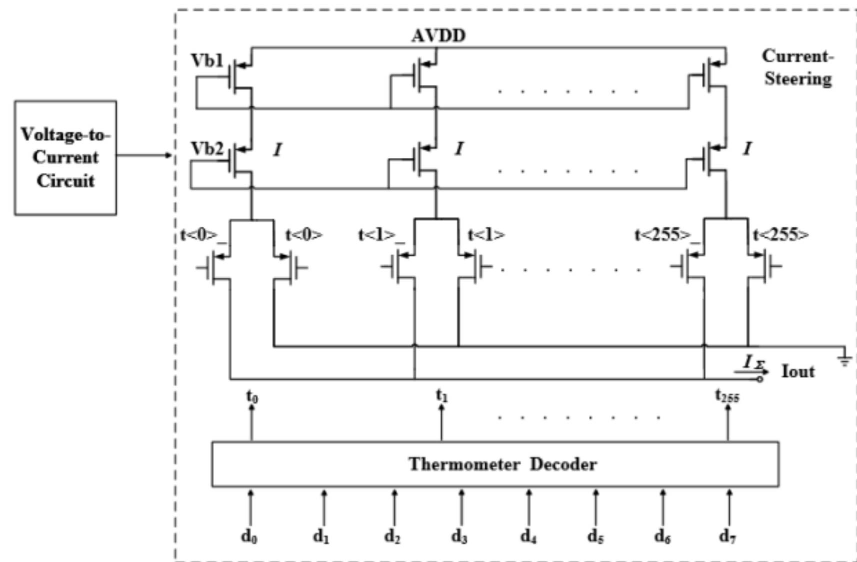


- TAC: adjustable charging current from 1nA to 10nA
- Large time measurement range: 3 µs to 100 µs
- Linearity error: < 30 LSB @3 µs, 1LSB = 3ns

Chip periphery: BG and DACs

BandGap: 1.25 V for voltage DACs





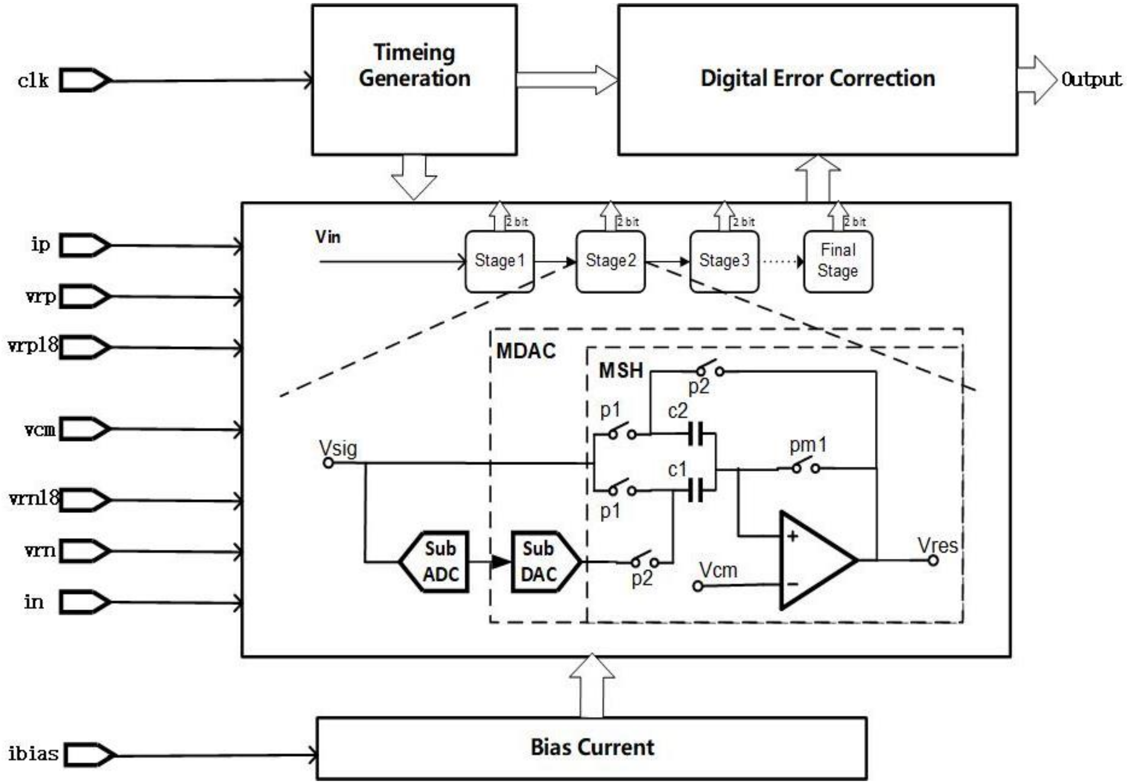
Voltage DAC

- 10 bits R-2R DAC, output range 0-3.02 V;
- Power consumption < 150uA.

Current DAC

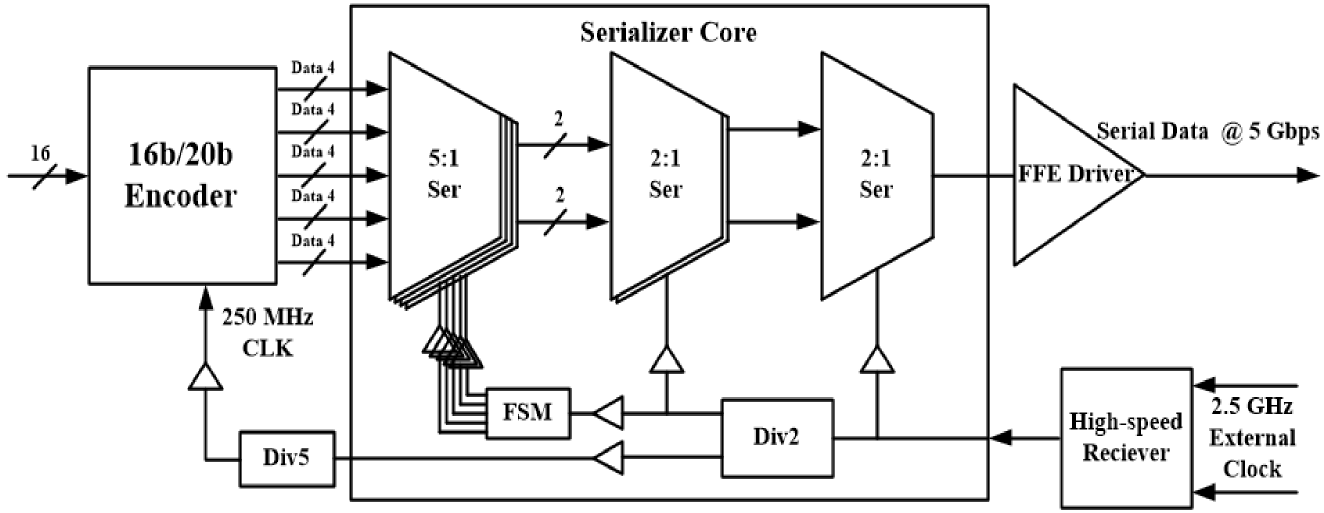
- 8 bit (0 - 2.52uA), LSB=10 nA;
- The digital decoder is using 6bits thermometer and 2 bits binary to compromise the area and the accuracy.

Chip periphery: Column cyclic ADC



- 11-bit and covers a small area of 100μm x 300μm
- Power consumption is7.6mW with 3.3V power supply
- sampling rate 3.63 MSps 、 SNDR 66.25dB、ENOB 10.7bit

Digital periphery



- Power supply is 1.2V, consist of 16b/20b encoder , 20:1 serializer ,

  FFE driver , high speed receiver;
- 20:1 serializer consumes power:< 28 mA;
- The FFE driver consumes power:< 15 mA, work at 5 Gbps;
- The receiver is a hysteresis comparator, consume power:< 5 mA, work at 5Gbps;
- The power consumption of the whole data transmission link is 58 mA.
- The RMS jitter with DCC < 6ps

Summary

- This first prototype is under testing;
- 2 versions of highly compact pixels was developed with rolling-shutter in 0.13 μm CIS CMOS technology;
  - **Pixel Size**: 30×30 μm^2;
  - **Speed**: 8 μs/row;
  - **Power**: 350 nA/pixel，analog power supply is 3.3V;
  - Can measure energy、time and position ;
  - Power density is about 300mW/cm^2;
- This chip is under testing, the accuracy need to be improved in the next version

Thank you very much for your time!