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Design of A 20 Gbps PAM4 VCSEL Driving ASIC for NICA Experiments

The Vertical cavity surface emitting laser (VCSEL) optical link has been prevalingly researched and used for the front-end data acquisition in high-energy physics experiments. As the increasing amount of data produced by the high-energy physics experiments, the bandwidth constraints imposed by the channel and ESD become more severe, which severely limits the development of the non-return-zero (NRZ) signaling. The 4-level pulse amplitude modulation (PAM4) is drawing widely attentions due to its two-fold bandwidth efficiency than NRZ signaling. In this paper, we present the design and the test results of a 20 Gbps PAM4 VCSEL driving ASIC fabricated in 55 nm CMOS technology. This ASIC is part of the optical link in the Nuclotron-based Ion Collider Facility (NICA) front-end readout electronics. The PAM4 VCSEL driving ASIC consists of two pre-driver stages, a 4PAM-core output driver stage and a SPI module. The two pre-driver stages receive two 10 Gbps NRZ bit streams MSB and LSB. The 4PAM-core output driver stage converts the high-speed voltage signal from the pre-drive stage into a 4-level current signal to the VCSEL. The optical test results show that the ratio level mismatch (RLM) of 20 Gbps eye diagram is 0.96 and the transmitter dispersion eye closure quaternary (TDECQ) is 0.63 dB, the optical modulation amplitude (OMA) is 761 uW. When working at 25 Gbps, the RLM is 0.94 with the TDECQ of 0.91 dB.

Primary experiment

Primary authors: ZHAO, Cong (Central China Normal University); GUO, Di (Central China Normal University)

Co-authors: CHEN, Qiangjun (Central China Normal University); Mr LIWEN, Yi (Central China Normal University); Ms ZENGTAO, Guo (Central China Normal University); Ms YUJING, Gan (Central China Normal University)

Presenters: ZHAO, Cong (Central China Normal University); GUO, Di (Central China Normal University)

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