MiniCACTUS: Sub-100ps timing with CMOS DMAPS

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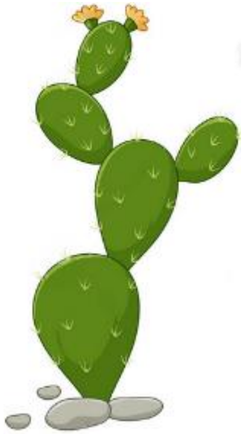
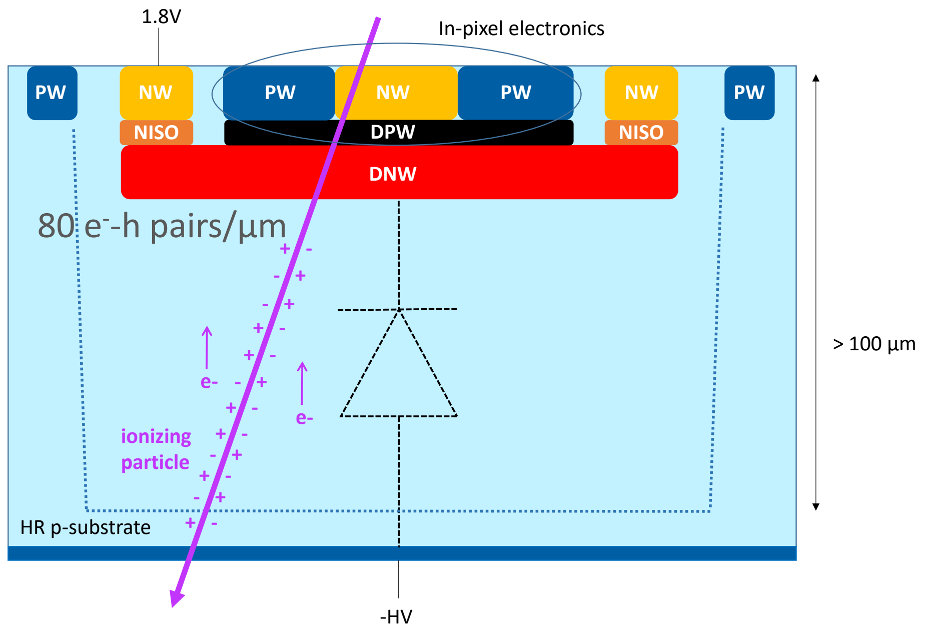


TIMING WITH HV-CMOS/DMAPS*

- The objective of this R&D is the development of a **monolithic timing sensor** in a **commercial HV-CMOS process** for future high energy physics experiments or for LHC upgrades (timing detectors, after phase 2 upgrades)
- **LFoundry 150 nm** HV-CMOS is one of the CMOS processes studied extensively for the CMOS option of the ATLAS Inner Tracker Upgrade
- Several large size demonstrators already designed and tested for tracking applications (**LF-CPIX**, **LF-MONOPIX1**, **LF-MONOPIX2**) in this process with proven **radiation hardness** (Bonn, IRFU and CPPM coll.)
- The monolithic sensors potentially cheaper and more reliable than dedicated hybrid solutions
- Possibility to integrate all functionalities (detection, analog + digital signal processing) on the same chip
- Wafers can be **thinned** and **backside processed** (for backside polarization and good charge collection uniformity)

HV-CMOS Sensor Pixel



- DNW/HR p-substrate charge collection diode
- HV (≥ 300 V) applied on the substrate (from top or back)
- Large depletion depth (≥ 300 µm)
- **Charge collection by drift (fast)**
- **No internal amplification**
- Electronics can be integrated inside charge collection diode

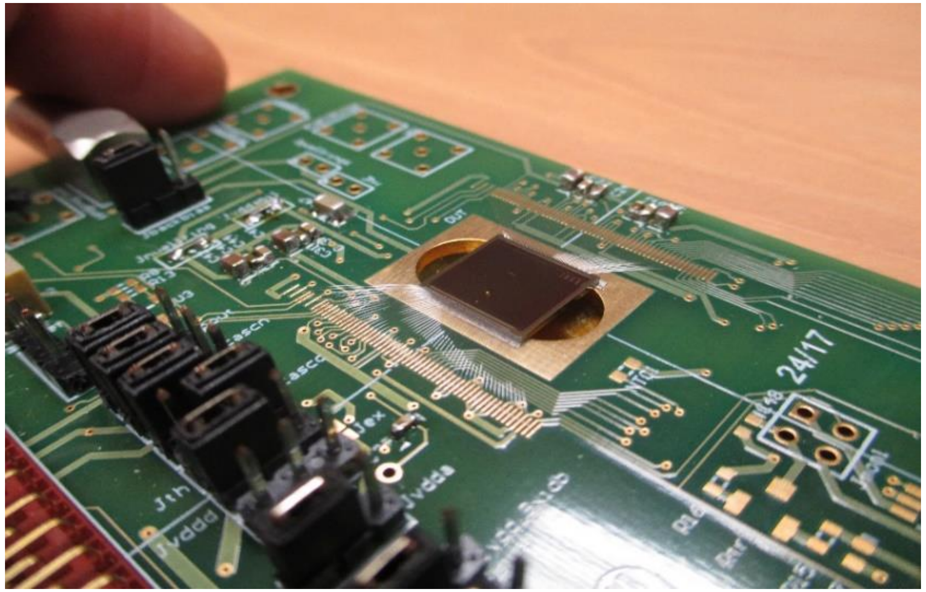
→ **Particularly suitable for timing**

*Depleted **MAPS**

CACTUS* DEVELOPMENT

- The first demonstrator called **CACTUS** for timing in LF 150 nm process designed in 2019
- The front-end in CACTUS is based on an **in-pixel fast preamplifier** followed by a **leading edge discriminator**
- Time walk corrections done off-line by **ToT measurement**
- Expected timing resolution from Cadence & TCAD simulations: 50-100 ps
- Promising results obtained with the CACTUS detector developed in this process (high breakdown voltage, homogenous charge collection, deep depletion depth, good yield), but **very low S/N** observed
- Very long & large power rails needed to distribute power into pixels increased significantly detector capacitance in CACTUS
- Timing possible only with **high thresholds** (leading to very low efficiency)

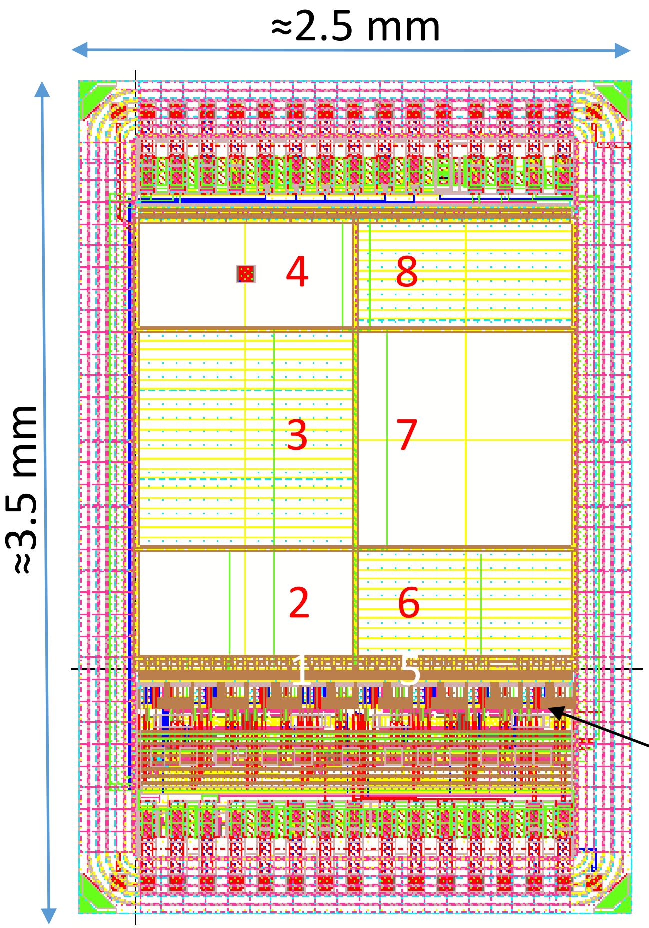
[Y. Degerli et al. JINST 15, 2020]



The CACTUS demonstrator on PCB
(chip size : 1 cm x 1 cm)

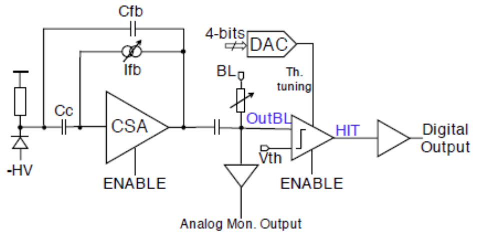
*CMOS ACtive Timing µSensor

MiniCACTUS Sensor Chip



Layout of MiniCACTUS chip

- **MiniCACTUS** is a smaller detector prototype designed in order to address the *low S/N issue* of CACTUS
- Main change in MiniCACTUS: FE integrated at column level, pixels mostly passive
- FE parameters programmable through on-chip Slow Control
- 2 digital (LVDS) and 2 analog monitoring (*slower than CSA output*) outputs for 2 columns

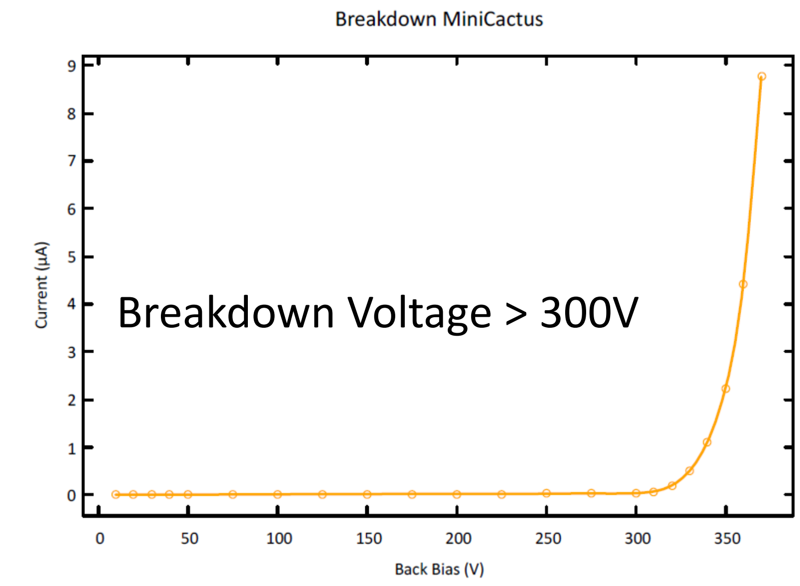


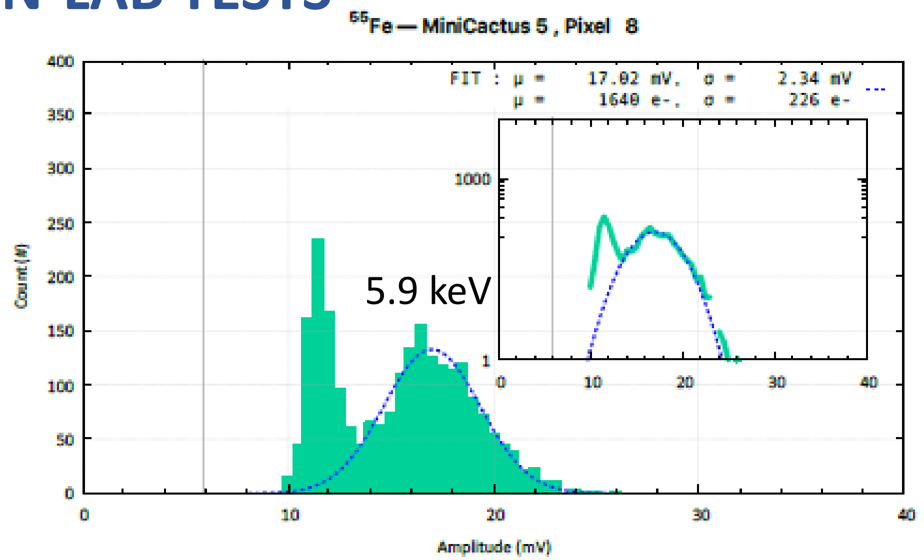
FE (1/pixel)

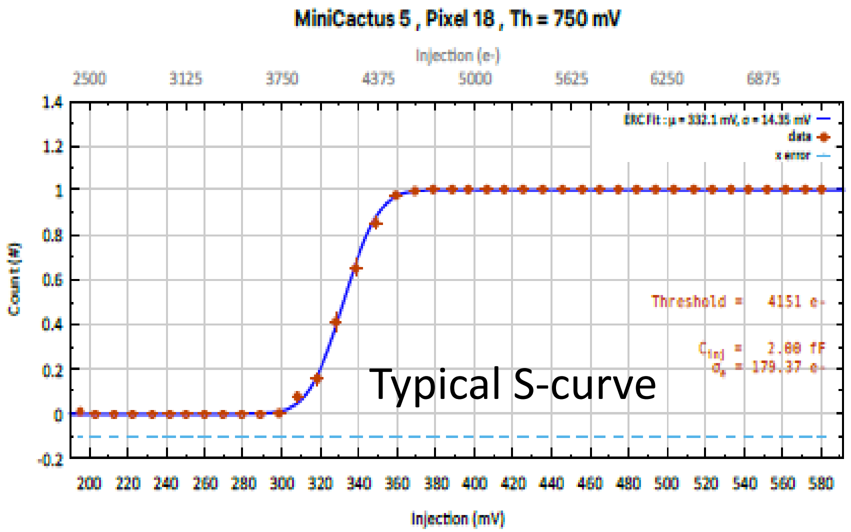
Pixel Flavors :
Pixels 3 & 7 : 1 mm x 1 mm baseline pixels
Pixels 2, 4, 6 & 8 : 0.5 mm x 1 mm pixels
Pixel 8 : 0.5 mm x 1 mm pixel with in-pixel AC coupling capacitor (20pF)
Pixels 1 : 50 µm x 50 µm test pixel
Pixels 5 : 50 µm x 150 µm test pixel

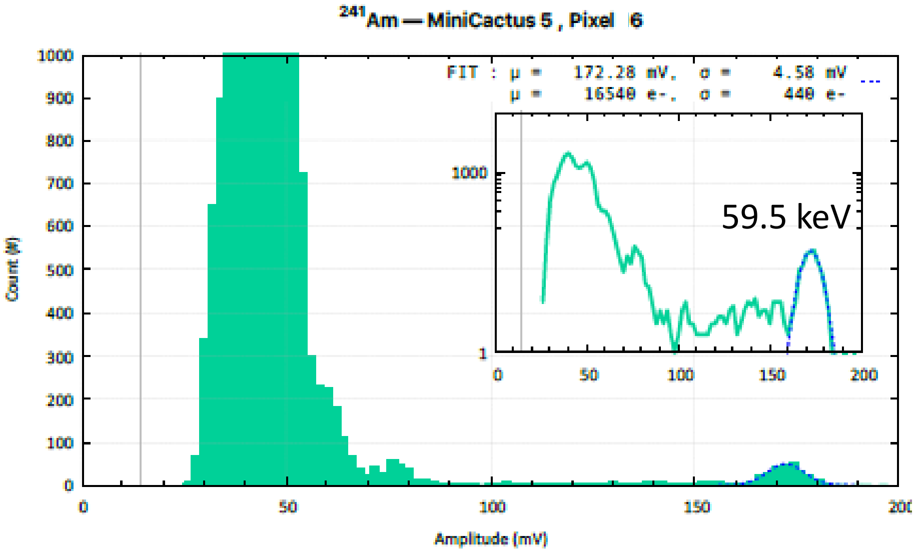
- ❑ **Front-end mostly optimized for 1 mm² pixels** with peaking time of 1-2 ns @ 1-2pF (Ibias_total=800µA → P ≈ 150mW/cm²)
- ❑ Small pixels can be seen as test structures to study charge collection (no power optimized FE available)
- ❑ Some detectors thinned to 100µm/200µm and than post-processed for backside polarization after fabrication

IN-LAB TESTS



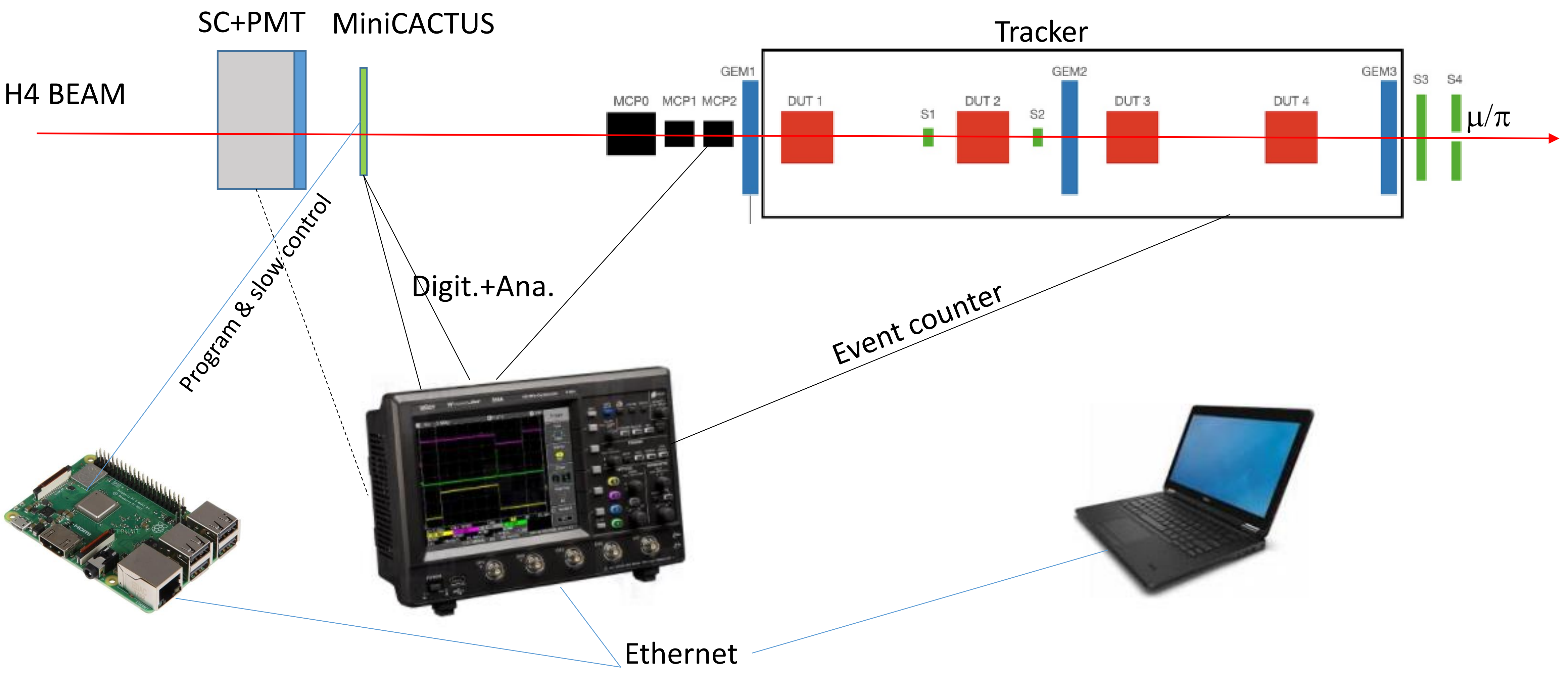






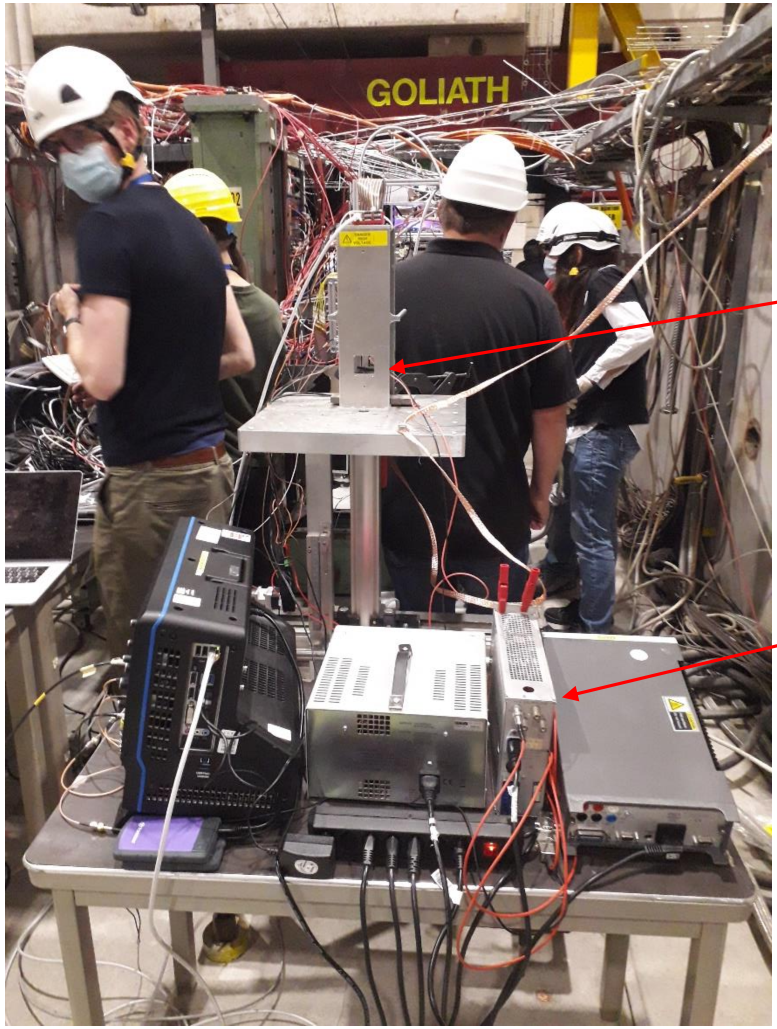
- → Best S/N observed on pixel 8 (0.5mm²) among large pixels
- → Sensors can be biased safely @ -300V (checked on several chips with different thicknesses: 100 µm, 200µm, unthinned)
- → $Noise_{DigOut}$:
  179.4e- (chip#5_200µm)
  155.9e- (chip#8_100µm)

TESTBENCH OF MINICACTUS IN TESTBEAM



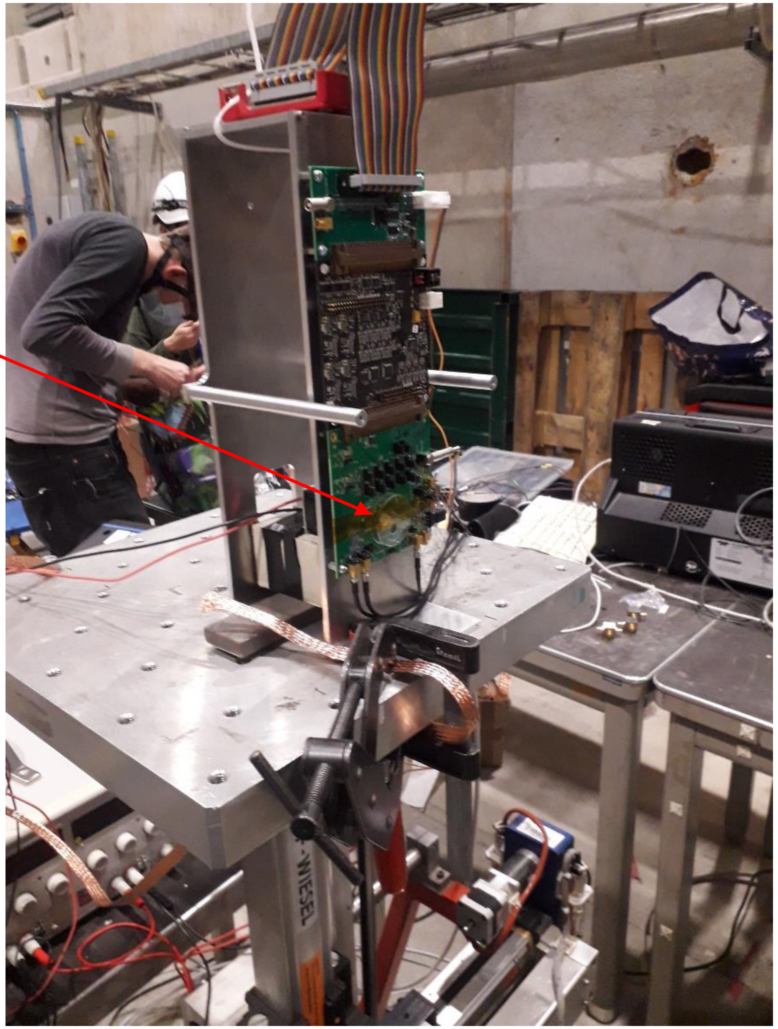
Setup installed on H4 line at SPS-CERN during **RD-51** test-beam period in **parasitic** mode (October 2021)

TESTBENCH OF MINICACTUS IN TESTBEAM



MiniCACTUS

Power Supplies
(LV and HV)



Setup installed on H4 line at SPS-CERN during **RD-51** test-beam period in **parasitic** mode (October 2021)

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DETECTORS TESTED AND DATA TAKEN DURING TEST-BEAM

- Several pixels from 2 different detectors with various HV (200V, 280V) and bias conditions tested during the 2 weeks:
  - **1 detector** with **200 µm** thickness (chip#5) **running almost continuously during ~12 days** (muons and pions)
  - 1 detector with 100 µm thickness (chip#8) running during the last 2 days

- 190 k triggers collected (μ,π) → allows to study energy deposits, Landau distributions, noise

- 115 k triggers are in coincidence with beamline **MCP** → time resolution studies

- 8k triggers are in coincidence with beam telescope → uniformity studies (to be done…)

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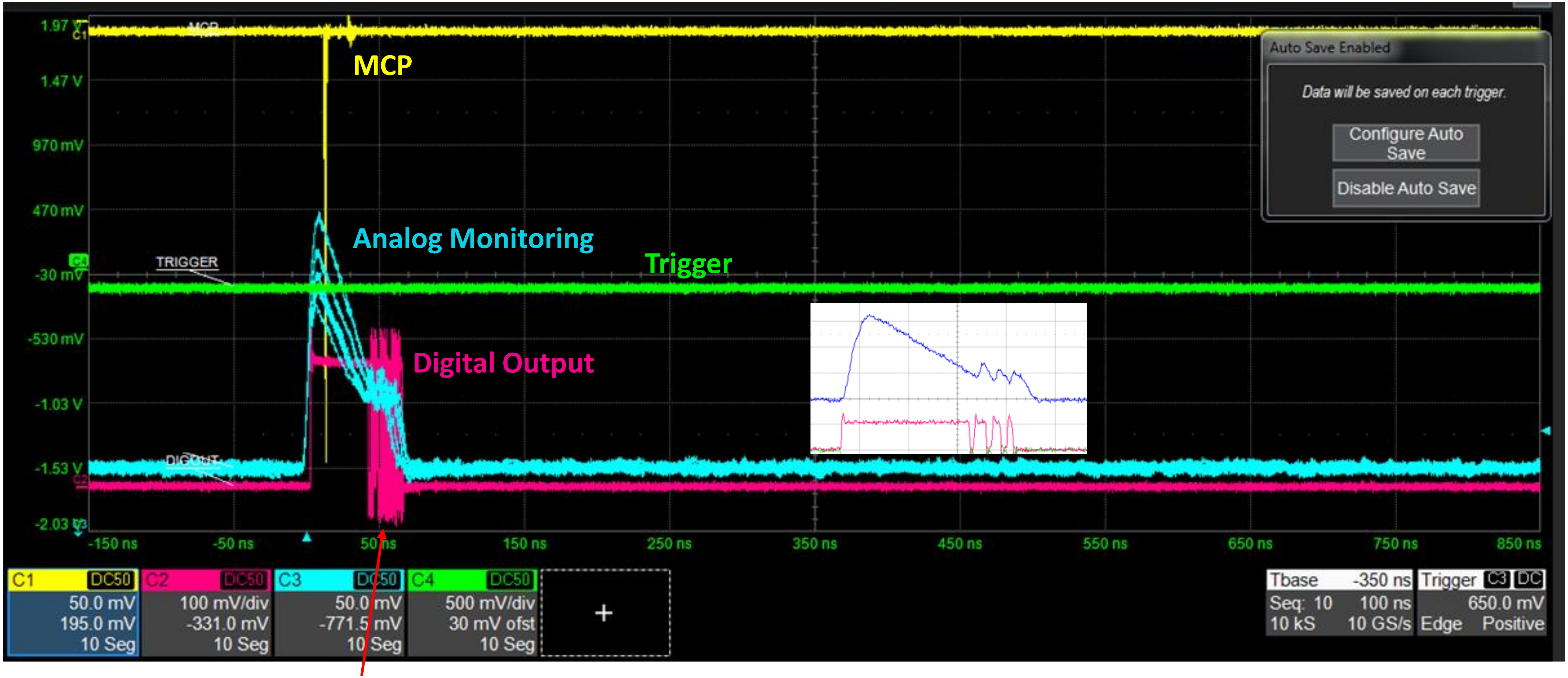
TYPICAL WAVEFORMS OBSERVED DURING TESTBEAM

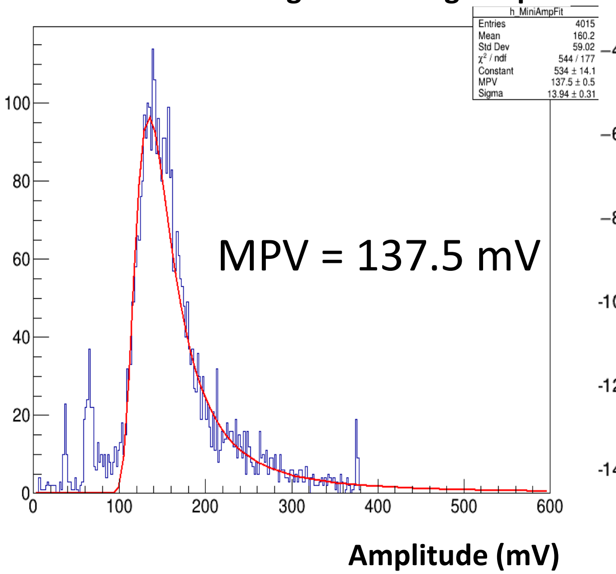


→ Ringing on Digital Output due to coupling from the digital buffers
(known problem from in-lab tests, negative impact on TW corrections from digital ToT)

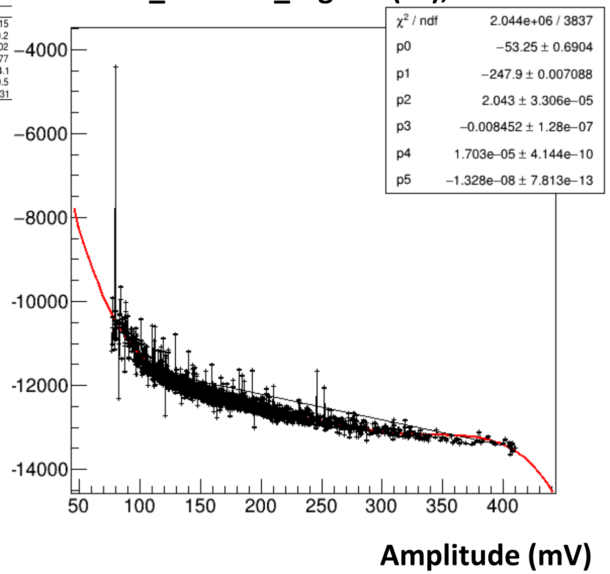
REFERENCE PERFORMANCE PLOTS

Chip#5, pixel 8**, 0.5 x 1 mm², 200 µm**, **-280V** (Back-side pol.)

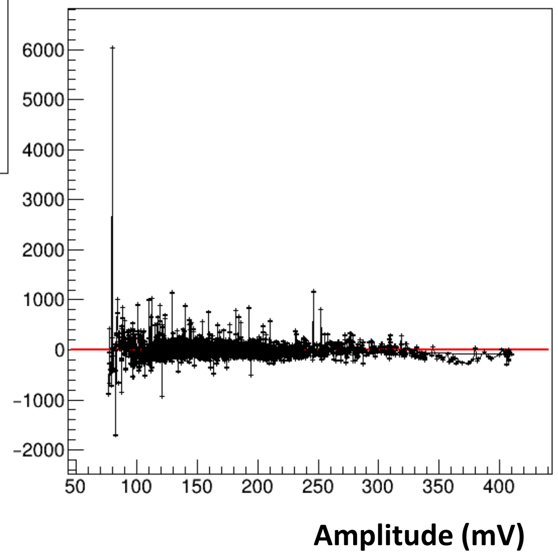
MiniCACTUS Analog Monitoring Output



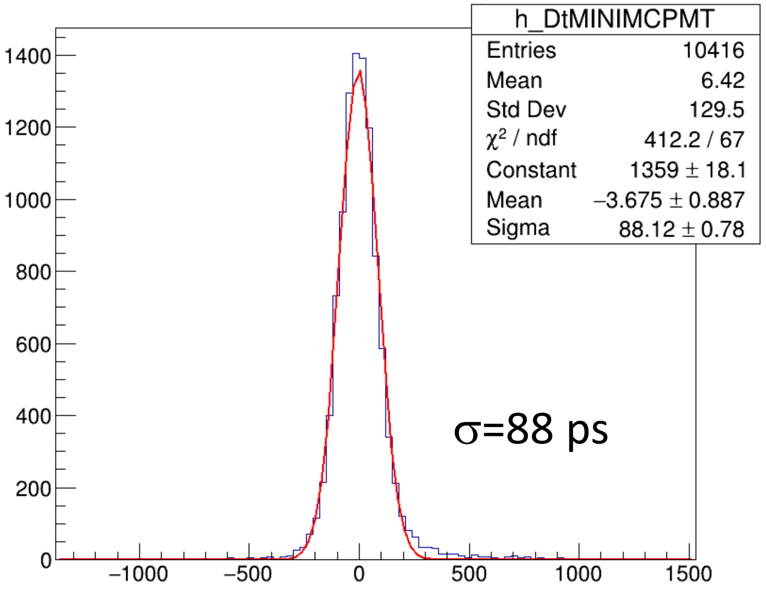
Fit T_MCP – T_DigOut (ns), no corr.



Fit T_MCP – T_DigOut (ns), TW corr.



T_MCP – T_DigOut (ps) after TW correction



- Measured timing resolution : **88 ps** (MCP resolution negligible)
- Worse timing resolution measured with 100 µm sensor (*lower S/N* and *ringing from digital*)
- Small pixels have worse performance, probably due to charge sharing effects (*pixel 5 tested in testbeam*)

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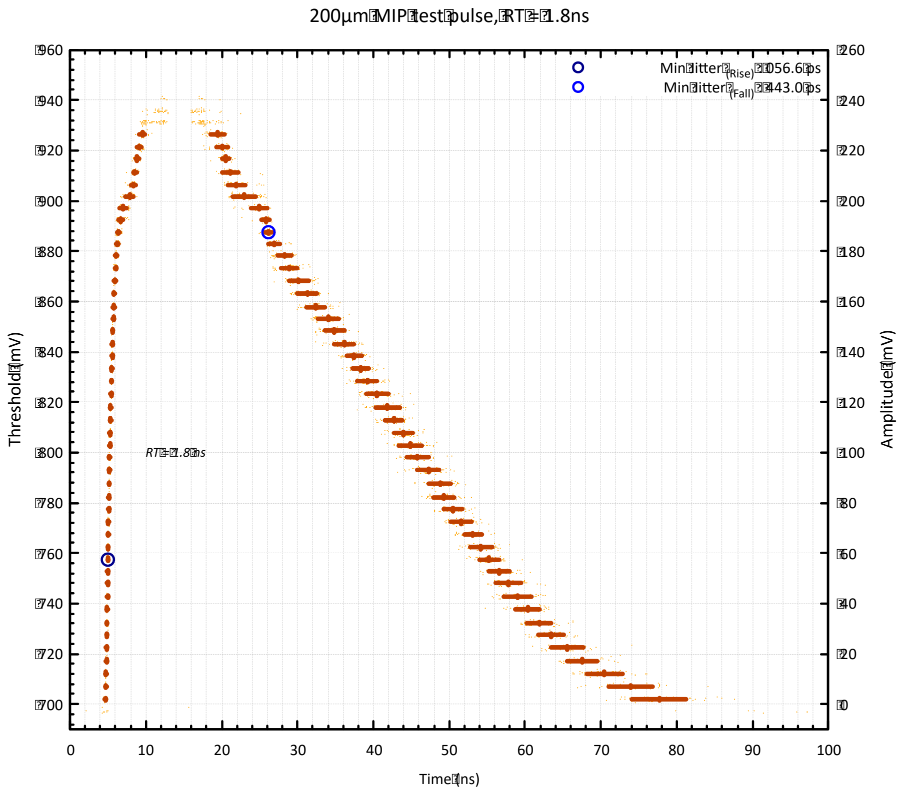
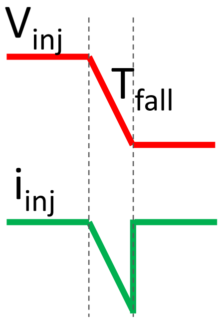
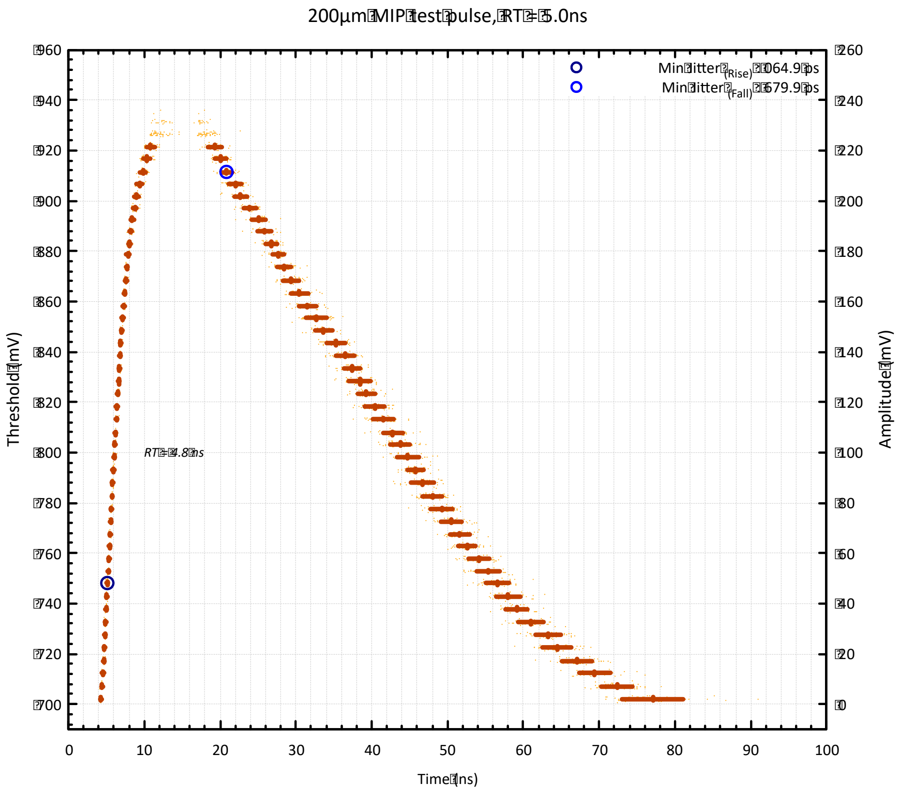
POST-TESTBEAM IN-LAB TESTS

- In order to understand limiting factors for timing, in-lab tests still going on
- Reconstruction of the **internal analog signal** to get an idea of the charge collection time (or rise time)
- Timing measurements using the ^{90}Sr source with different FE parameters to look for an optimal parameter set
- The noise seems currently the main limiting factor with the current FE, the timing improves when noise is filtered
- We plan to try also higher substrate thicknesses (**300 µm**) to increase the signal level
- We know from signal amplitude measurements on 100 µm sensors and 200 µm sensors that we will be able to deplete completely a 300 µm thick sensor
- A new test-beam campaign is planned in April 2022

INTERNAL ANALOG PULSESHAPE RECONSTRUCTION FROM DIGITAL OUTPUT





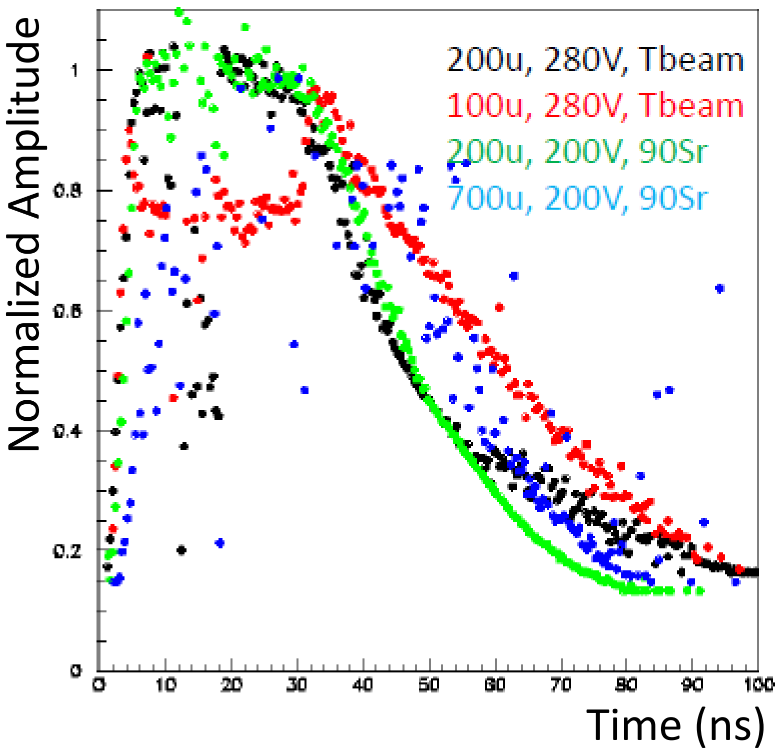


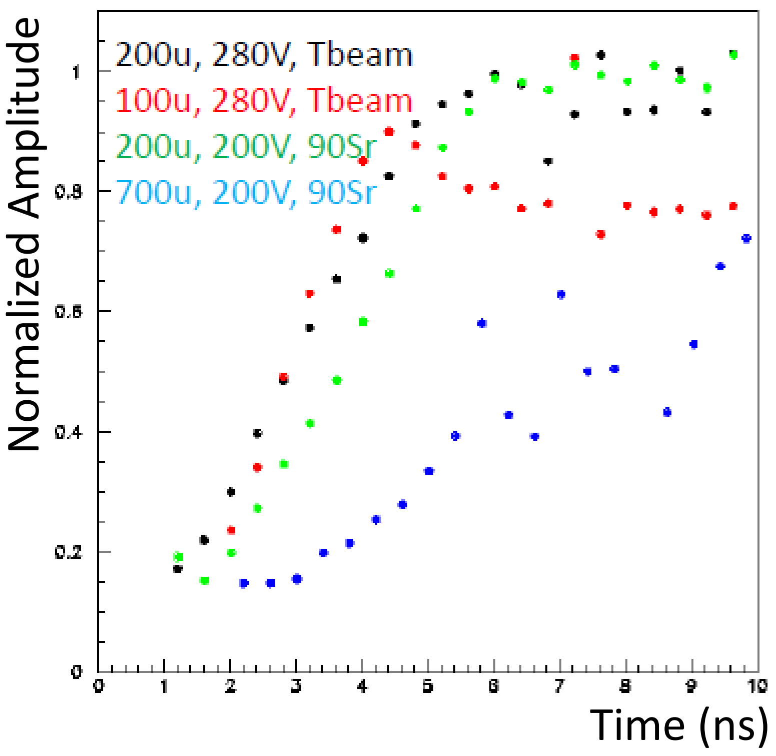
- Charge Injection → Vpeak AmpOut ~ 150 mV (MPV of MIPs for a 200 µm thick sensor)
- Input injection pulse Rise/Fall Time = 1.8 ns
- FE Internal Pulse Rise Time ≈ 1.7 ns
- Jitter : 22.6 ps

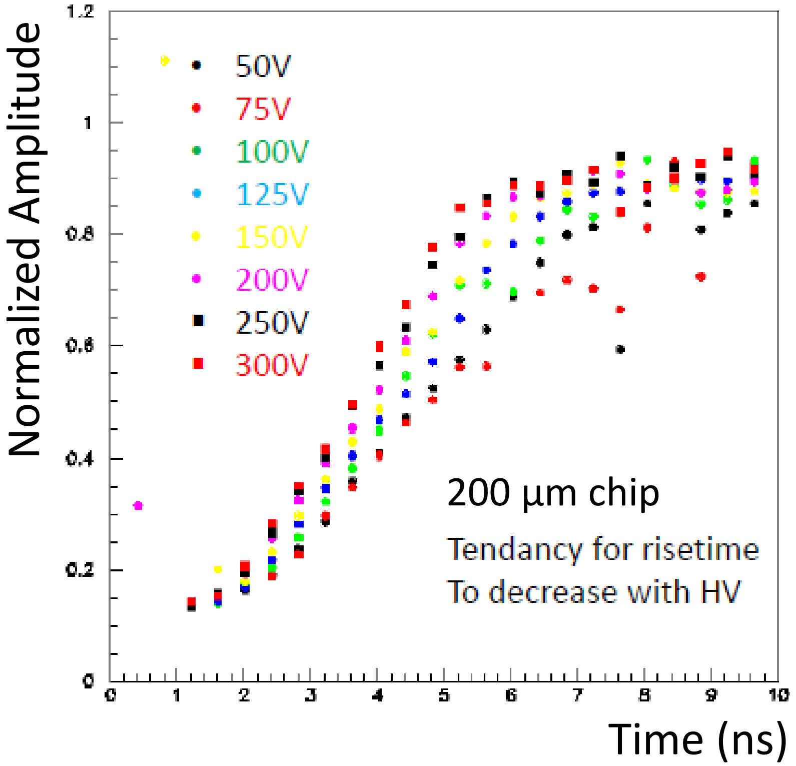
- Charge Injection → Vpeak AmpOut ~ 150 mV
- Input Rise/Fall Time = 5.0 ns
- Pulse Rise Time ≈ 4.8 ns
- Jitter : 64.9 ps

→ The FE follows well a 1.8 ns falling edge digital injection pulse

INTERNAL ANALOG PULSESHAPE RECONSTRUCTION ATTEMP



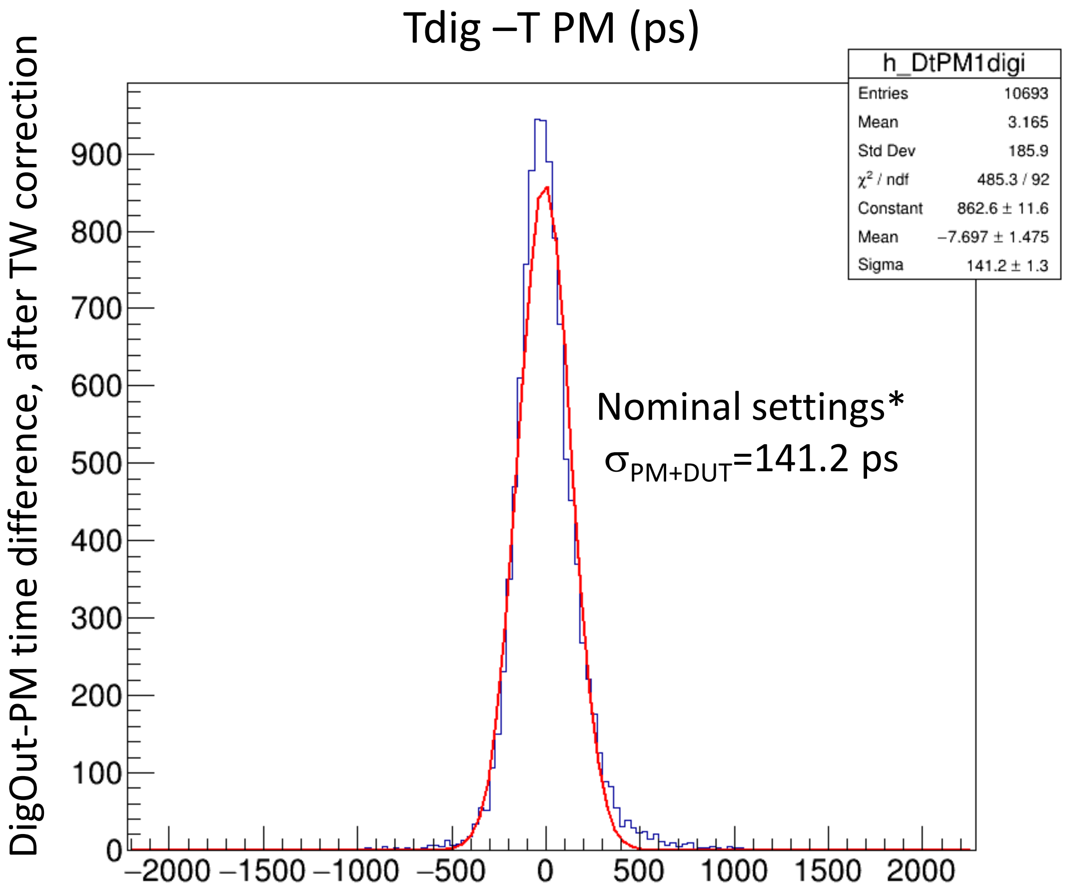


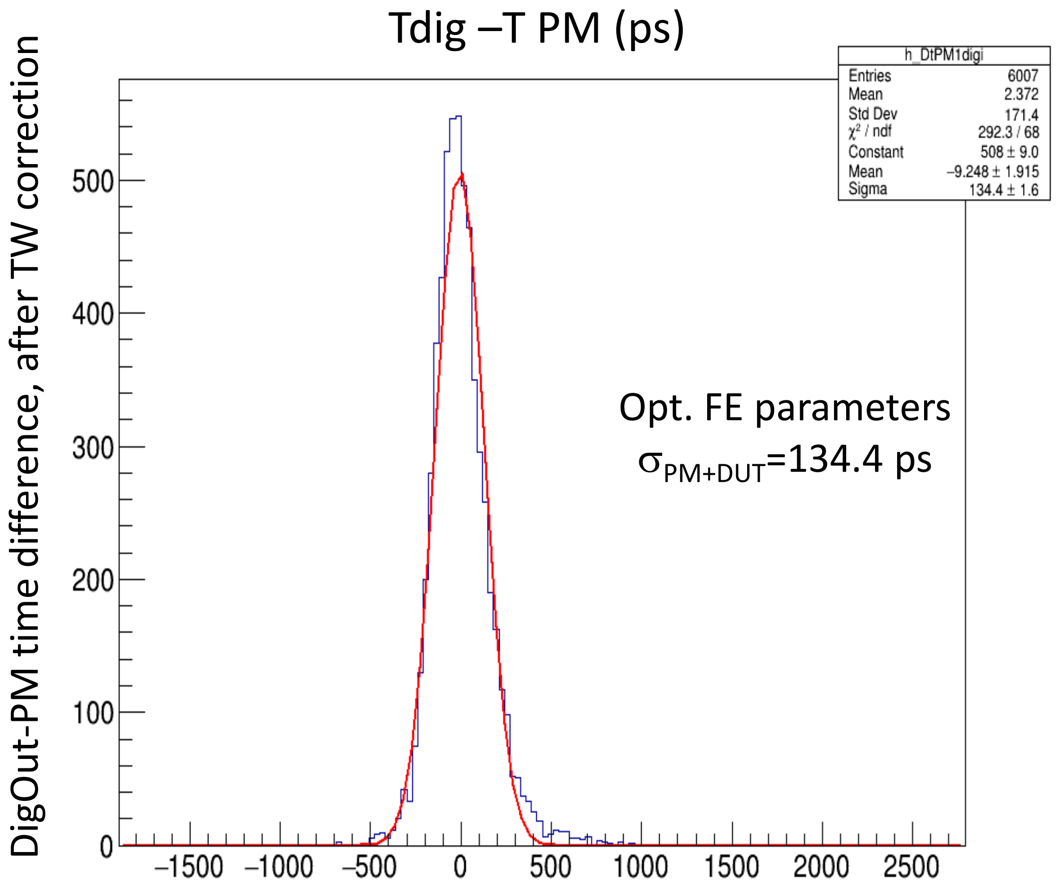


- Internal pulseshape reconstruction not very precise, but enough to get an idea of the shape and the rise time
- Rise time is of the order of **4-5 ns** for 200 µm and 100 µm
- The unthinned 700 µm chip are clearly slower
- Rise time decreases somewhat with HV
- With these results, for a given thickness, **the noise of the FE seems to be the limiting factor of the current timing resolution**

IN-LAB TIMING MEASUREMENTS WITH PM AND ^{90}Sr SOURCE

Chip#5, pixel 8**, 0.5 x 1 mm², 200 µm**, **-200V**





→ The global timing (PM+DUT) improves after optimization of FE parameters (σ_{PM}>100 ps)

→ Should give improvement of ~10 ps on the DUT (to be confirmed in testbeam)

*Nominal FE parameters used in testbeam giving ~88 ps resolution for the MiniCACTUS

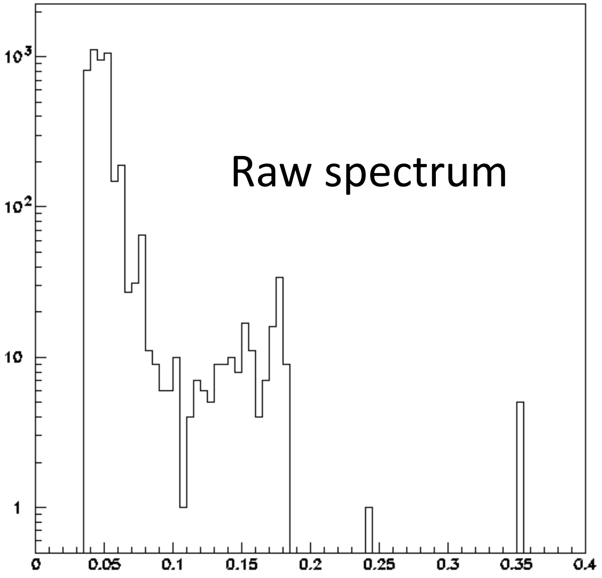
CONCLUSIONS AND NEXT STEPS

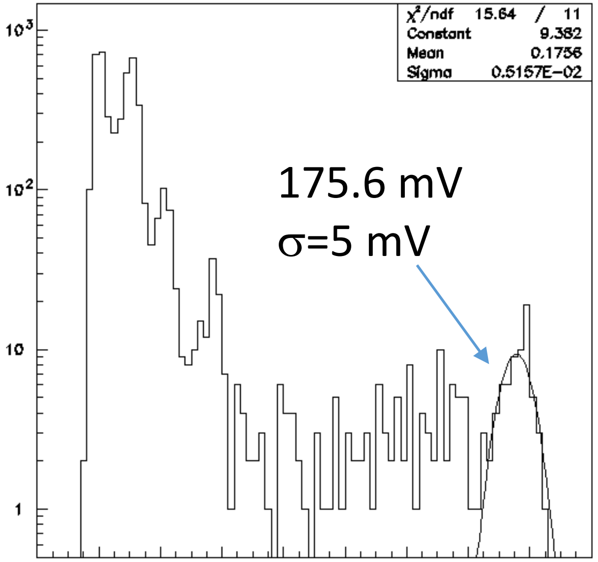
- Present test-beam results of MiniCACTUS prototype consistent with in-lab results obtained using ^{90}Sr source
- Significant improvements observed on **MiniCACTUS** compared with the previous **CACTUS** demonstrator
- Up to now, best timing results obtained in test-beam with **200 µm** sample, 500 µm ×1000 µm pixel (~**88 ps**), including the **on-chip analog front-end** and the **discriminator**.
- The timing resolution of 100 µm sample is not better due to the *lower signal level* and *ringing from digital*
- These results, plus understanding of the internal pulseshapes, collection time, gives directions for FE re-optimization and design evolution of the CACTUS concept

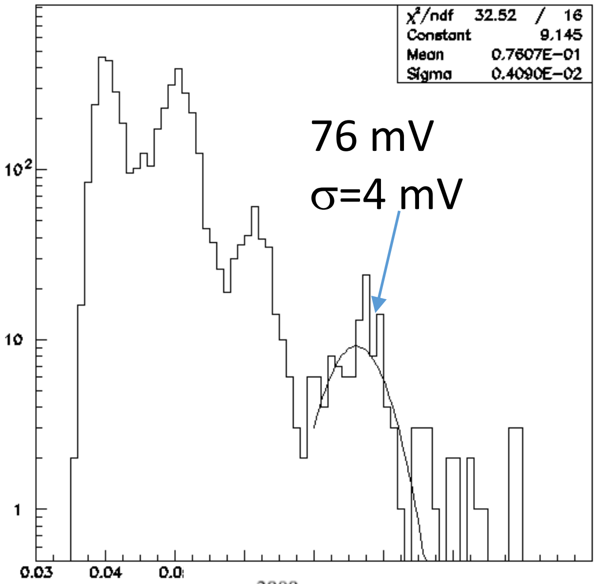
- Short term: A new testbeam campaign planned in April 2022 :
  - → tests of **200 µm** samples *with optimized FE parameters*
  - → tests of **300 µm** samples if in-lab tests promising
- Medium term: Irradiation tests to confirm radiation tolerance of the technology
- A new prototype submission is planned this year with
  - → **optimized FE** (CSA + Discriminator)
  - → **improved digital buffering** to address ringing issue

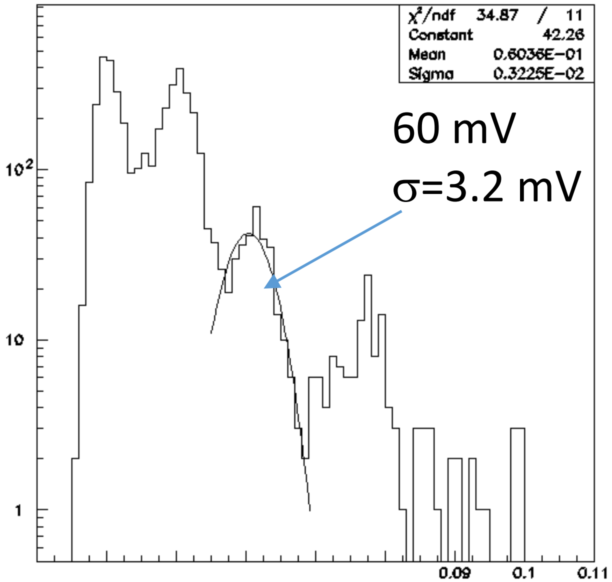
ANNEXES

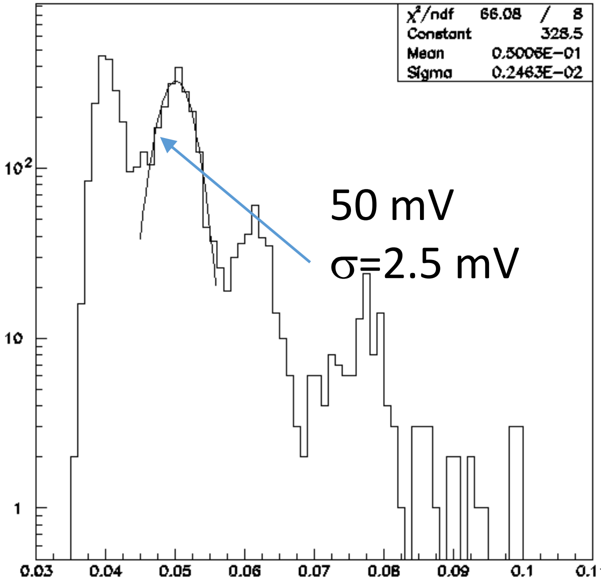
241Am Amplitude Spectrum (pixel 5, 50 µm x 150 µm)

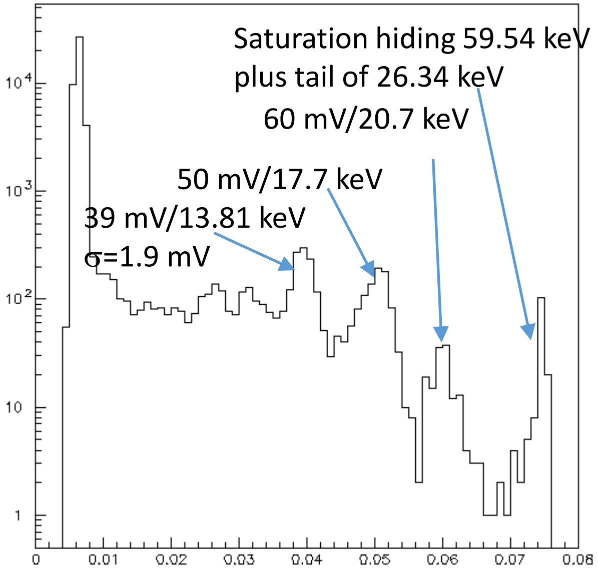


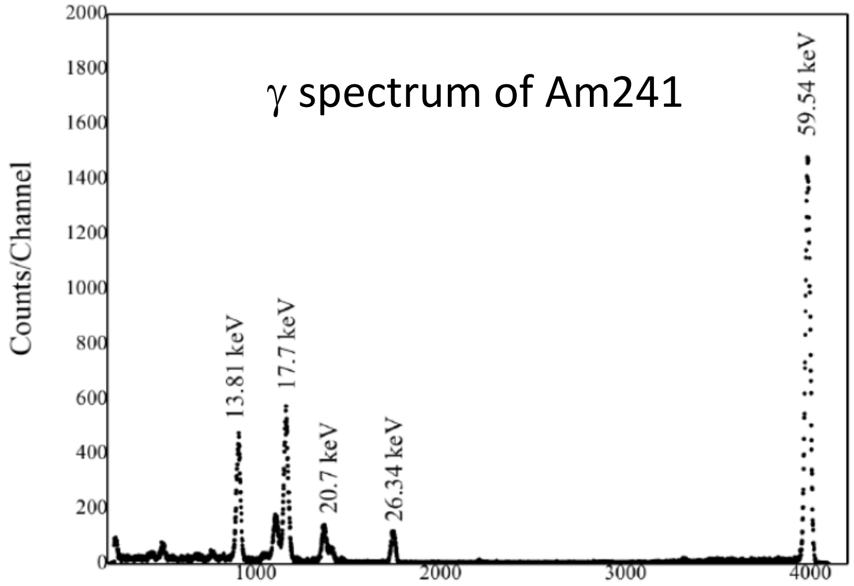






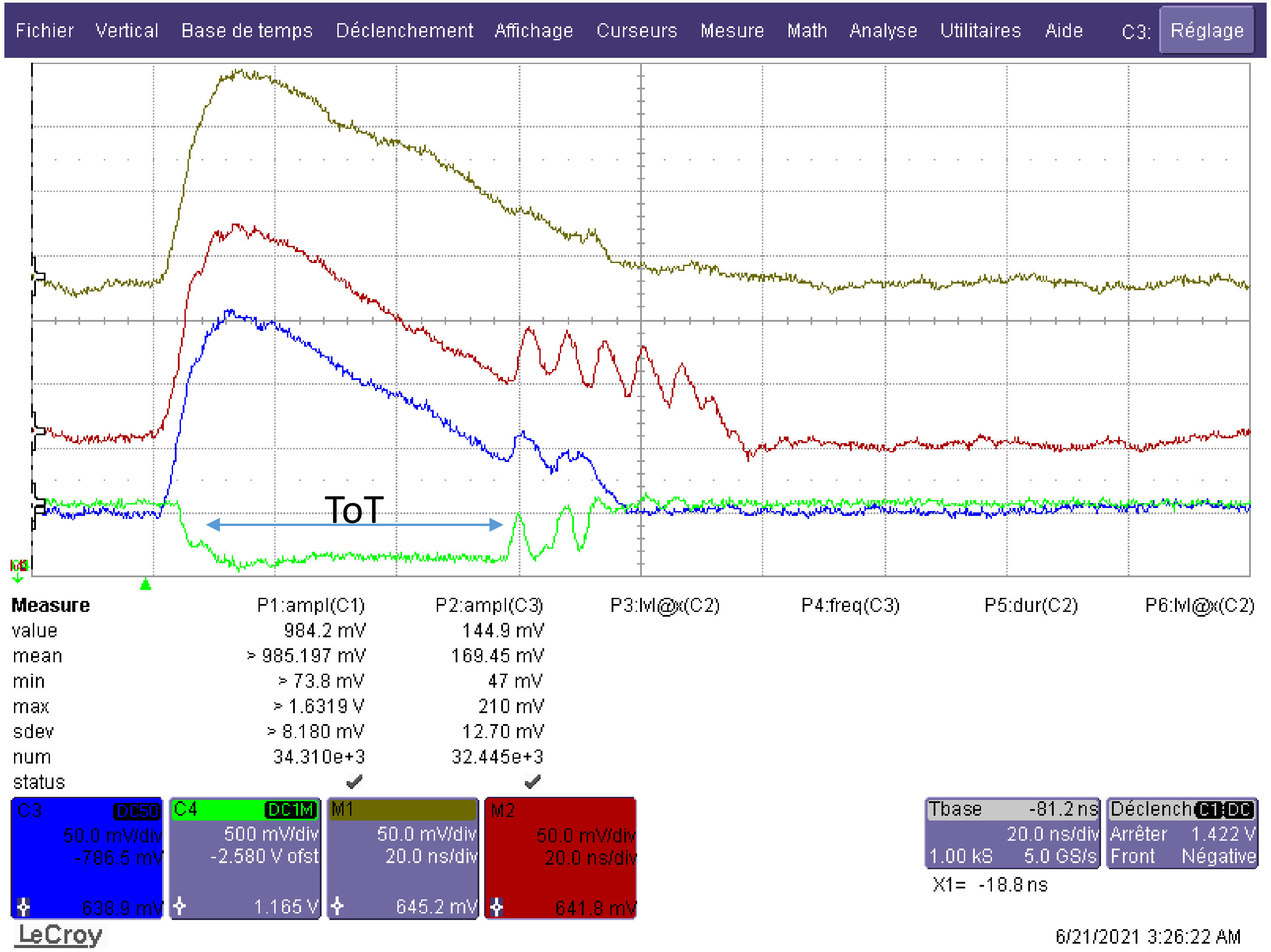






COUPLING FROM DIGITAL BUFFERS

(Chip#4, pixel 8)



Discri ON, CMOS buffers OFF

Discri ON, (VTH=0.75V)

Discri ON, vdd_cmos_buffers=1.5V

Minicactus LVDS output (100Ω-terminated)

→ Clean leading edge
→ Reducing vdd_cmos_buffers improves slightly oscillations