Detector Developments for the High Luminosity LHC Era

Lecture 3:
Vertex Detectors

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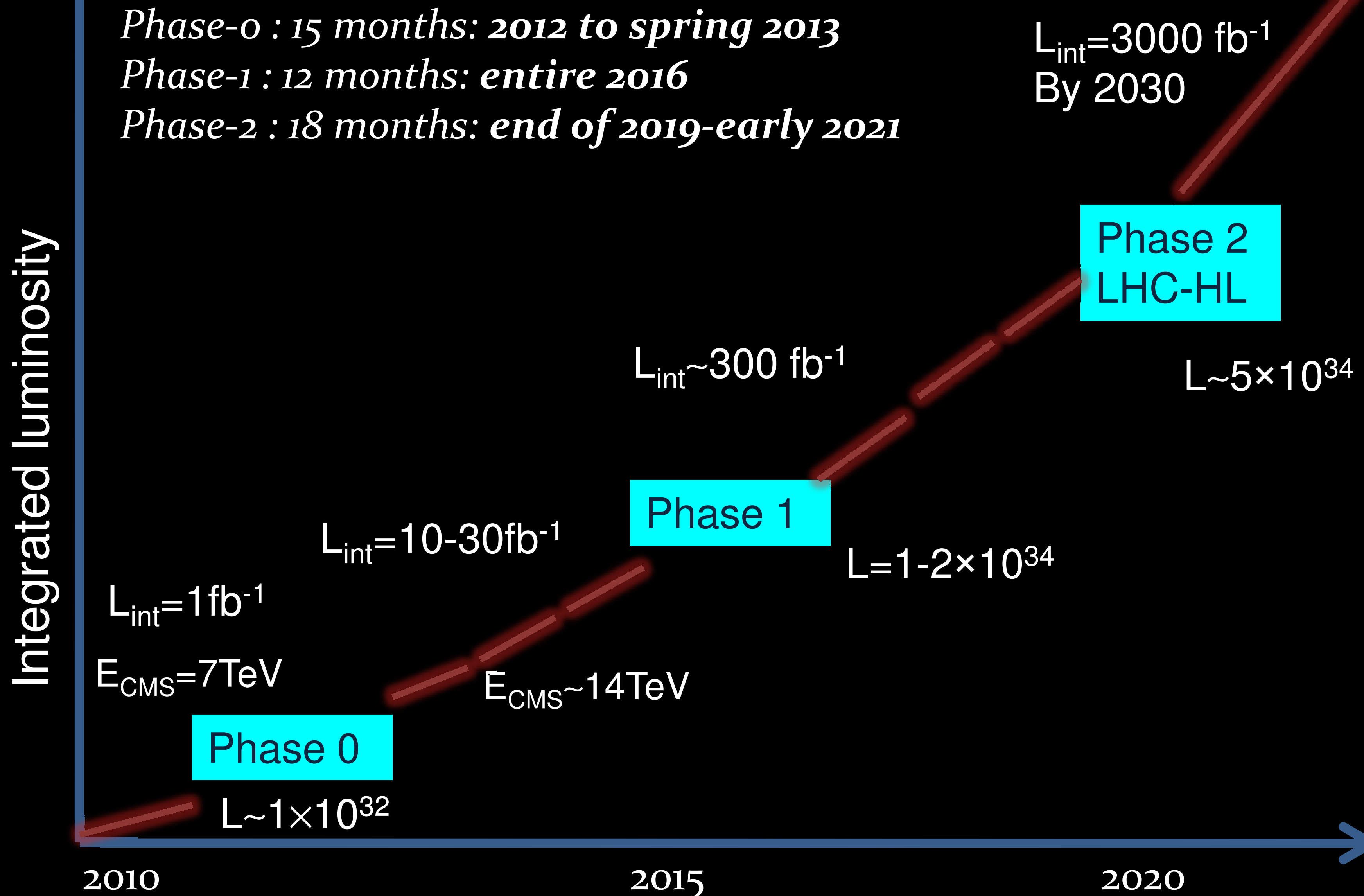
The LHC and the High Luminosity LHC ERA

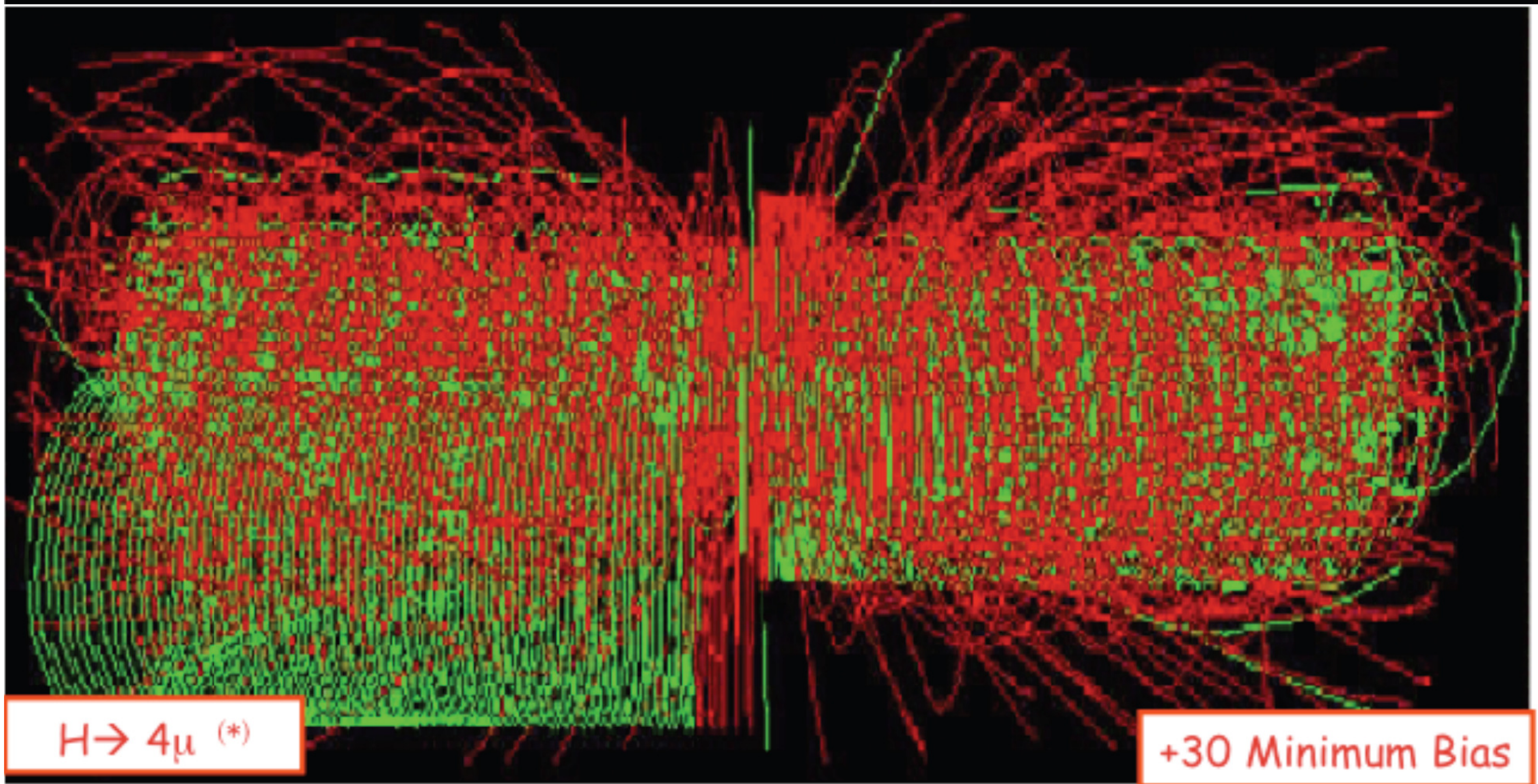
- The LHC is a discovery machine built to study
  - **Electroweak symmetry breaking**
    - **The Higgs mechanism**
  - **The short comings of the standard model**
    - **Dark matter (SUSY or due to another theory)**
    - **Hierarchy problem**
    - **CP violation**
- The discovery potential of the LHC can be enhanced by increasing its luminosity
- To distinguish between different new physics scenarios and solve the "LHC inverse problem" we need very large data sample
- To take advantage of this increase we must maintain or improve the performance of the LHC detectors including vertexing and tracking

The machine upgrade path

*Phase-0 : 15 months: **2012 to spring 2013***
*Phase-1 : 12 months: **entire 2016***
*Phase-2 : 18 months: **end of 2019-early 2021***

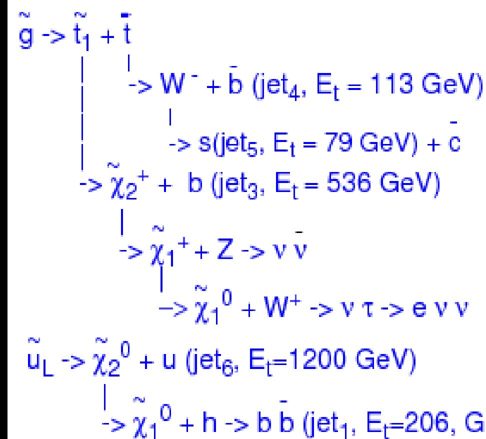


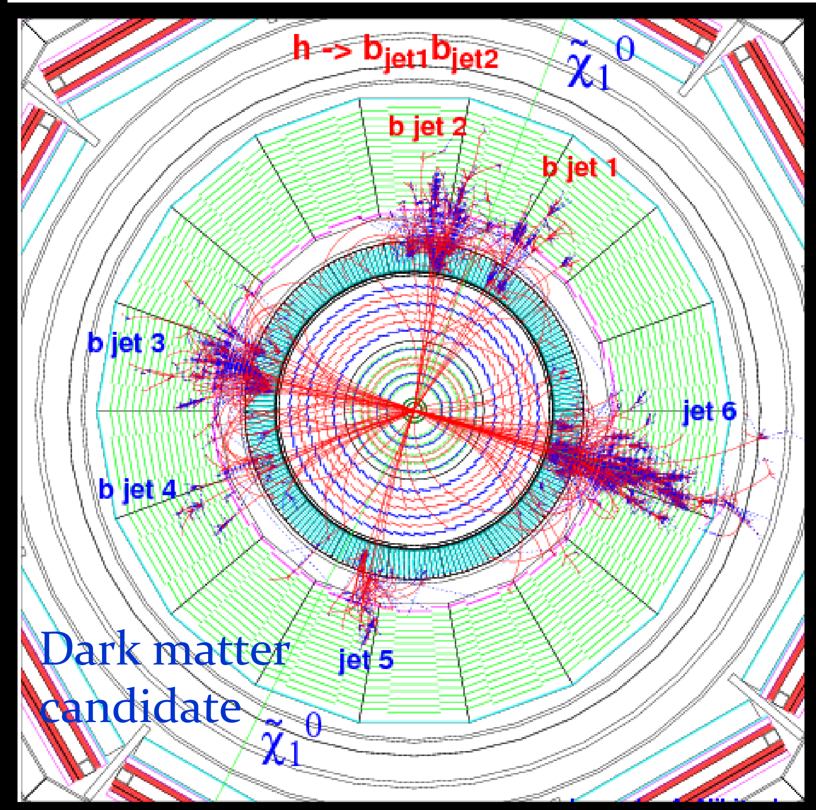
Increasing challenge



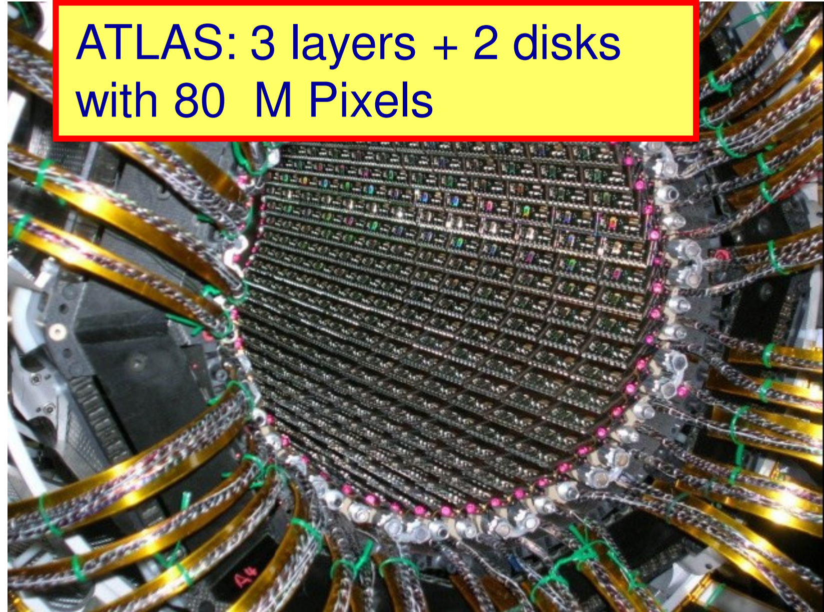
Vertex Detectors Physics Design requirements

- Precise vertex determination
  - b and tau identification
- Important role in pattern recognition/ track reconstruction
  - More layers? less material?
- Issues:
  - Material minimization
    - Thin/small beam-pipe
    - Ultra-light detectors
    - New powering concepts (serial, DC-DC)
  - High-precision detectors very close to IP
    - Ultra radiation hard detectors
    - Radiation hardness up to ~10^{16} 1MeV neutron/cm^2 @ innermost layers by phase 2
  - Many channels to reduce occupancy
    - High data rates⇒ Output rate at innermost layer = 320 MHz = 4 x LHC already in Phase 1
  - Triggering ?



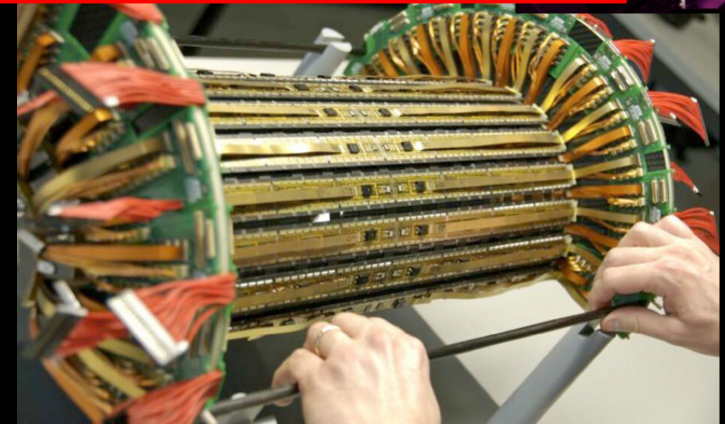


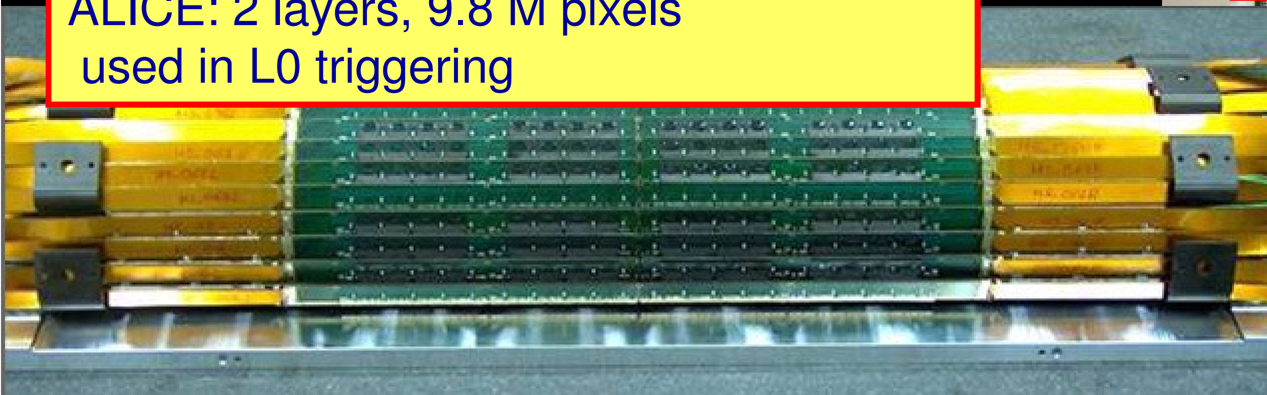
The LHC vertex detectors



ATLAS: 3 layers + 2 disks with 80 M Pixels

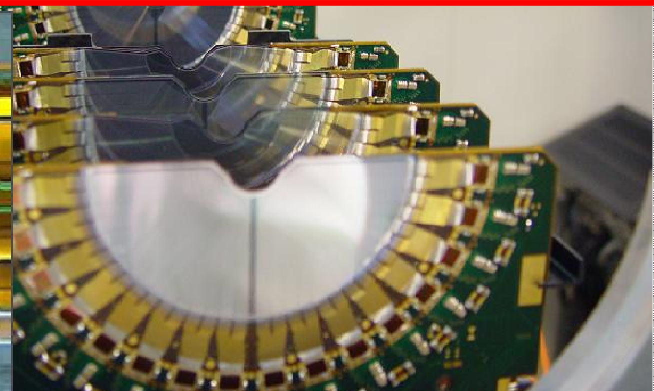
CMS: 3 layers and 2 disks for 66 M pixels





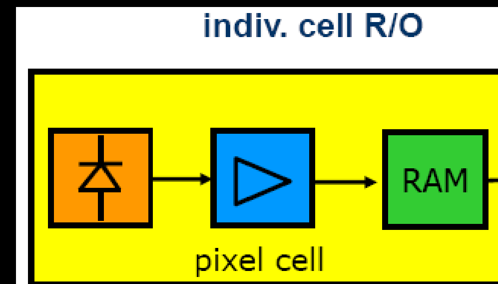
ALICE: 2 layers, 9.8 M pixels used in L0 triggering

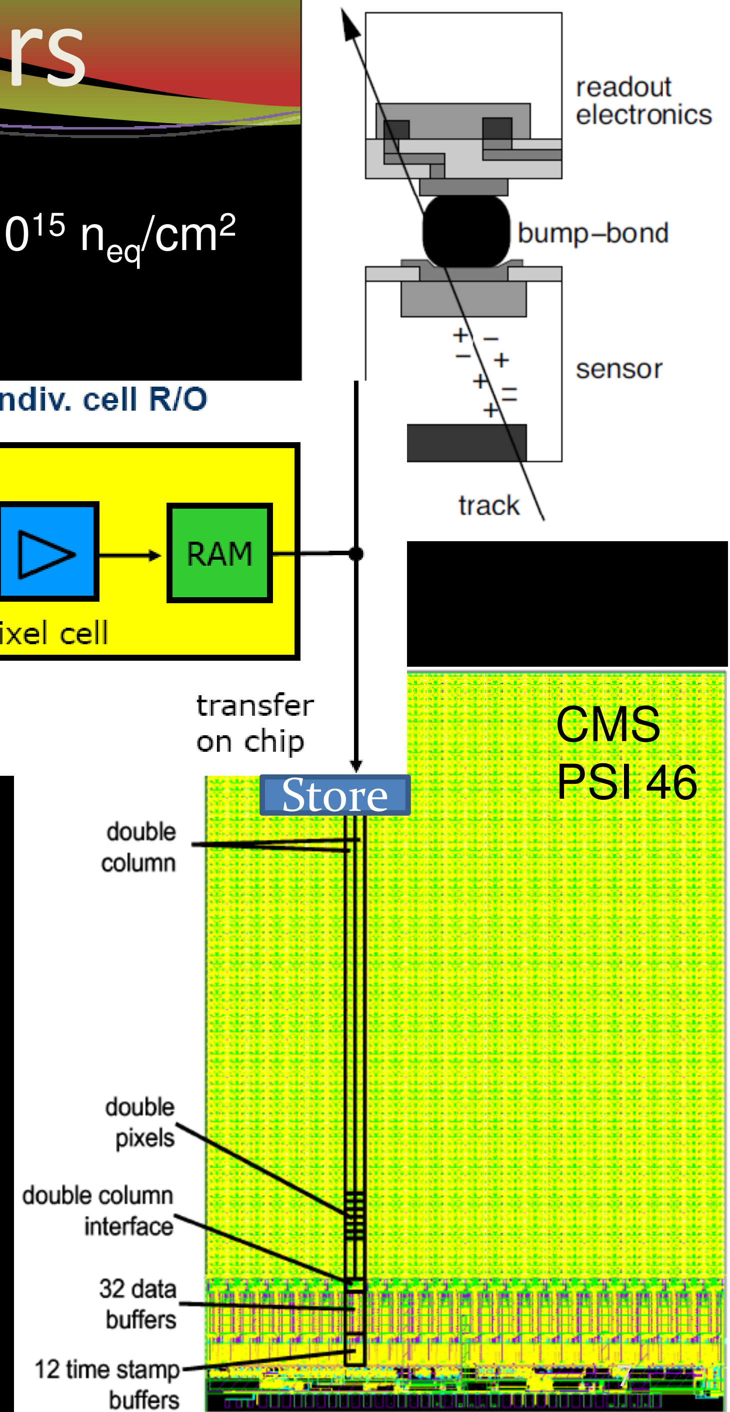
LHCb: 176 k strips pileup Veto trigger, CO_2 cooling



LHC Hybrid Pixel detectors

- Hybrid pixel detectors meet LHC detectors need:
  - High rate capability and radiation hardness to~ 10^{15} n_{eq}/cm^2
- Charge generation in sensor, integration in FE-chip
- Require bump-bonding
- Trigger driven readout of individual hits
  - pn-diode $\rightarrow Q_{signal}$
  - amplification and filtering$\rightarrow$Vout
  - Pixel storage: address, charge, BX
  - column-wise R/O
  - transfer information to End of Colum (wait for trigger)
- Current implementation:
  - 250 nm CMOS technology
  - Material budget ~2-3%X/X_0/layer
  - Resolution ~10 μm due to pixel size (50 μm×400 μm, 100 μm×150 μm)
  - ATLAS: Digital I/O
  - CMS: Analog I/O

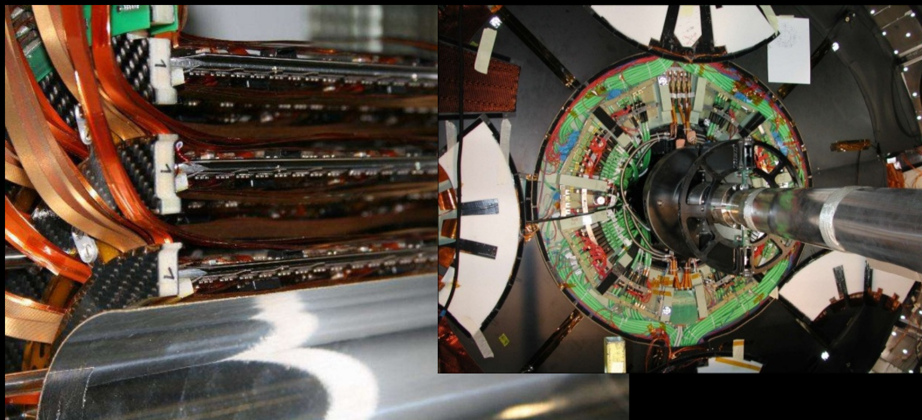




Lesson learned from the pixels

CMS

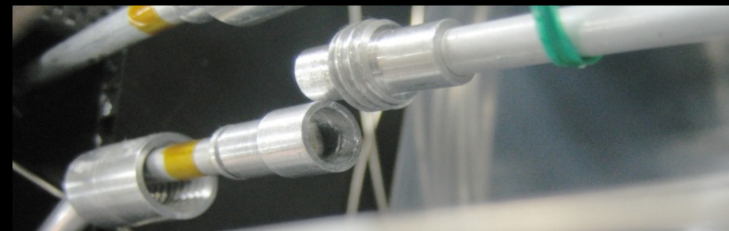
- Some modules in barrel pixel were bad before installation. Difficult to replace a module
- The layout of the fibers and the connections at patch panels were difficult



- Power (CAEN Easy series)
  - Mechanical problems with connectors

ATLAS

- Aluminum tubes corroded during production and were replaced
- Leaks in custom low mass fittings
  - 3 inside the detector can not be accessed



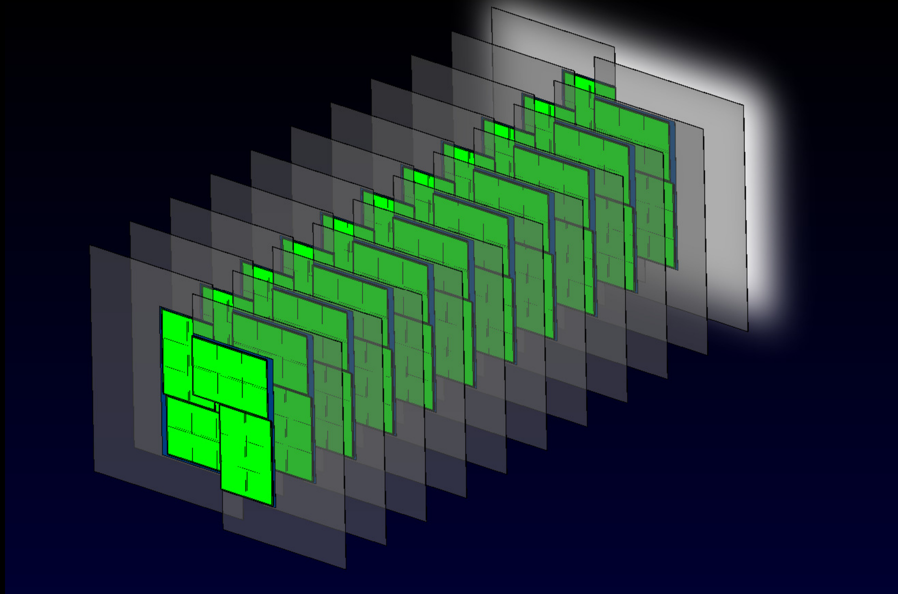
- VCSEL LASER array response are temperature dependent (similar problem in CMS Analog opto Hybrids)
  - Add resistive heaters to on-detector optical boards to control temperature

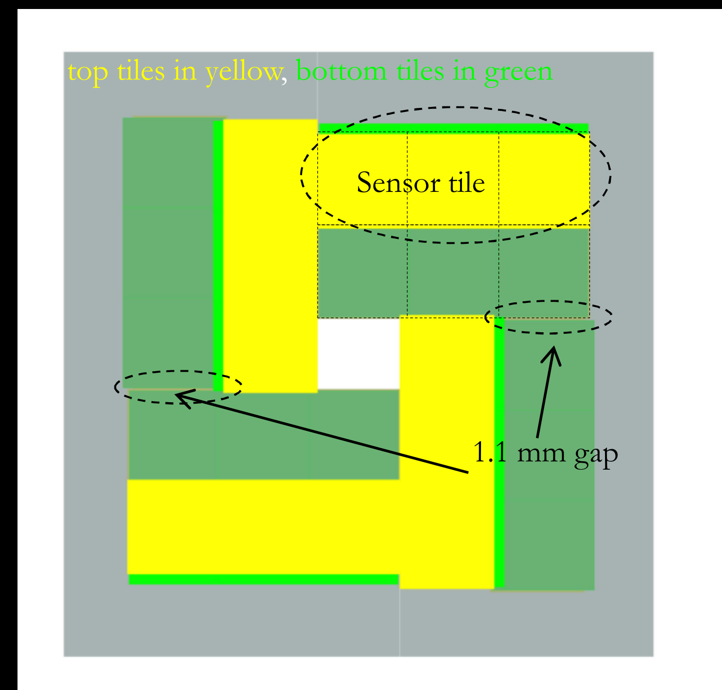
- R&D must cover also these areas to built detectors that can maintain or improve the performance of the current detectors

The LHCb VELO upgrade plan

- Run existing LHCb and collect 10 fb^{-1} in 5 years at L = 2 x 10^{32} $cm^{-2}s^{-1}$
- UPGRADE
  - Collect 100 fb^{-1} in 5 years at L = 2 x 10^{33} $cm^{-2}s^{-1}$
- A 'station' is made of 8 sensor tiles.
  - active area is near 100% (except small gaps).
  - Closest pixel is at 7.5 mm from the beam center.

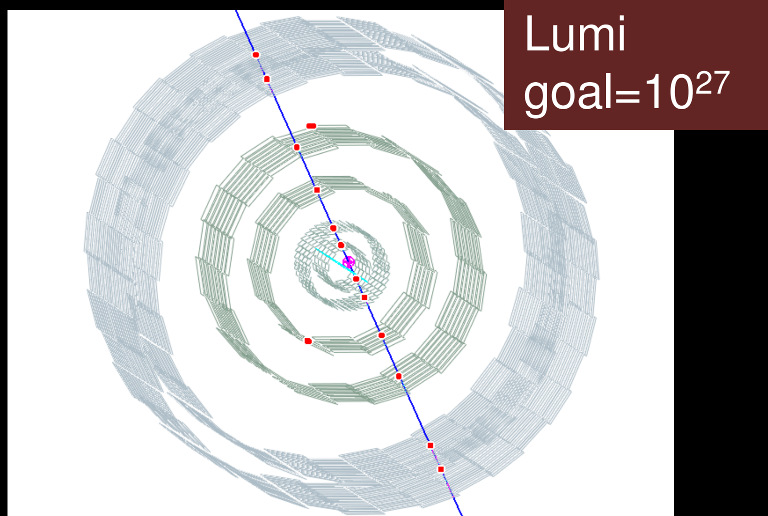
- The full detector is composed of 26 stations.
- The modules on either side of the beam are staggered to create overlap regions.





Alice Upgrade inner tracking system

- Present 6 detector layers based on three silicon technologies:
  - 2 layers SPD (pixels)
  - 2 layers SDD (Si Drift)
  - 2 layers SSD (Si strips)



Lumi goal=10^{27}

Radii: 4, 7, 15, 24, 39, and 44 cm
Total material budget of $7\% X_0$ (normal incidence)
Pixel size 50 μm x 425 μm
Beam pipe radius 2.98 cm

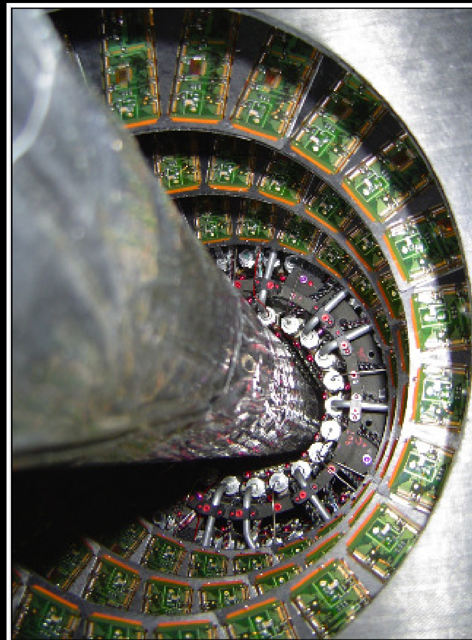
- 6/7 cylindrical layers
- First layer as close as possible to the interaction point
  - smaller and thinner beam-pipe (present 29/0.8mm)
  - goal: 20mm radius or smaller
- Extend the use of pixel detectors to larger radii (replace SDD, slowest det in ITS)
  - strips where pixels not affordable
  - re-use of the existing pixel and/or strip layers being considered
- Extremely low material budget, trigger capability, granularity, fast readout
- New mechanics and cooling
- ➢ Target dates defined by the LHC shutdown schedule: 2017-18

- Physics Goal: a factor of 2 improvement in impact parameter resolution
- Secondary goal: improve stand-alone tracking capability

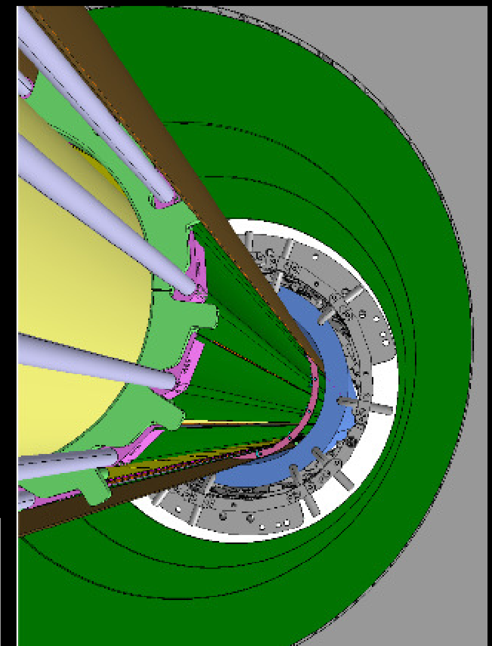
ATLAS phase 1 upgrade plans

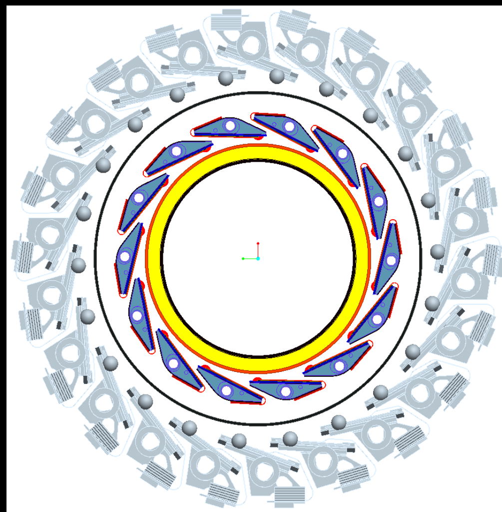
- Insertable pixel B Layer (IBL) to Improve Physics performance of the present Pixel Detector:
  - Reduce material budget to an “aggressive” 50% of the present inner most pixel layer, i.e. <1.5% X/X_0 at $\eta=0$.
  - Have low R/O inefficiencies at LHC ultimate luminosity and above (i.e. $3x10^{34}$ $cm^{-2}s^{-1}$).
  - Increase radiation hardness by a factor of five to $5x10^{15}$ 1MeV neutrons/cm^2

- Installation schedule, 2016



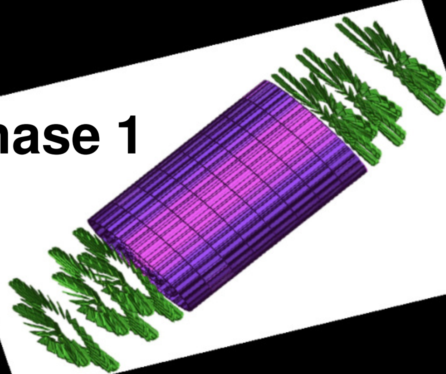
- Current b -layer





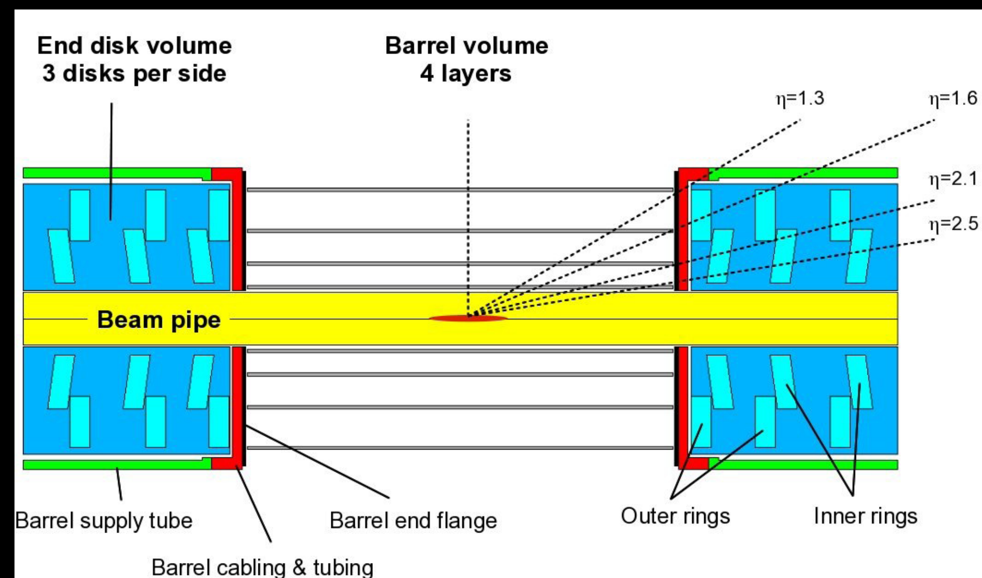
- IBL

CMS Phase 1 Plan



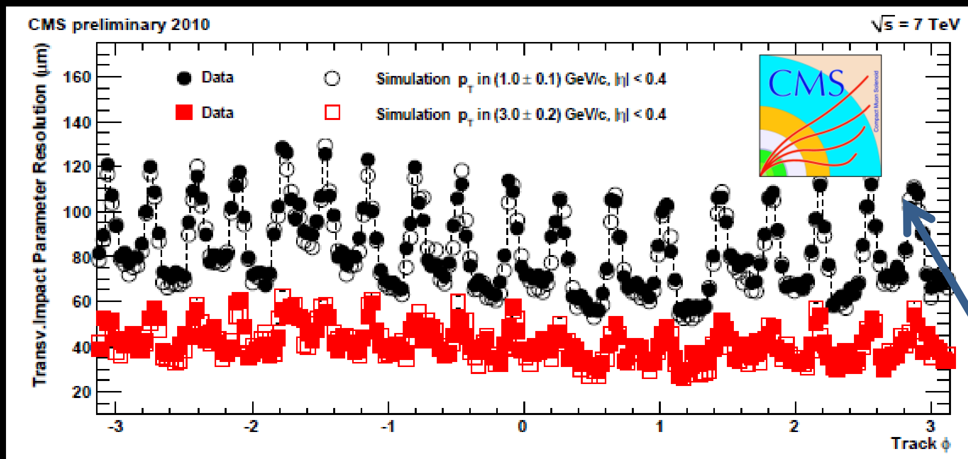
- Improve hit detection efficiency, track seeding, and pattern recognition at $L=2x10^{34}$ $cm^{-2}s^{-1}$ (and 50 pile-up events):
  - Minimize data losses at high luminosity
  - Maximize 4-hit coverage over the full pseudorapidity range
- Improve track parameter resolution :
  - Minimize radius of innermost layer
  - Reduce passive material in the tracking region
- Use current CMS cabling and connections and simplify module production

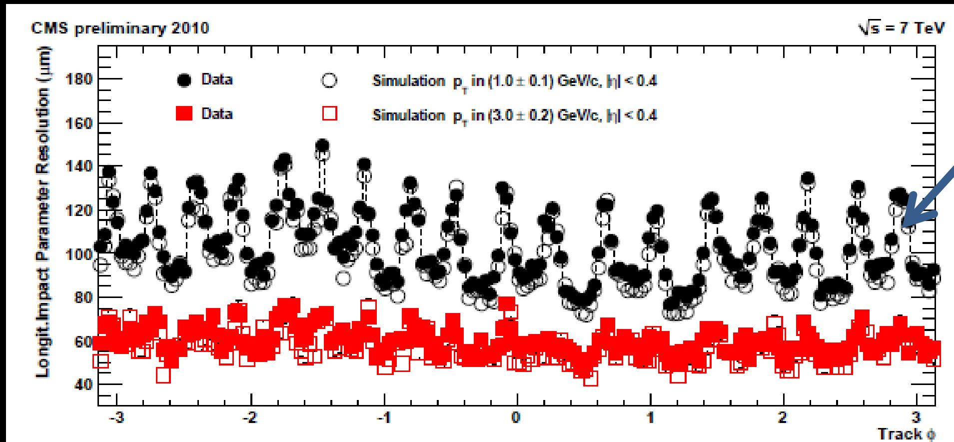
- Main Features of the new detector:
  - 4 barrel layers and 3 endcap disks at each side
  - New readout chip with expanded buffers, embedded digitization and high speed data-links
  - CO2 two-phases cooling and displaced optical transceivers
  - Powering based on DC-DC converters

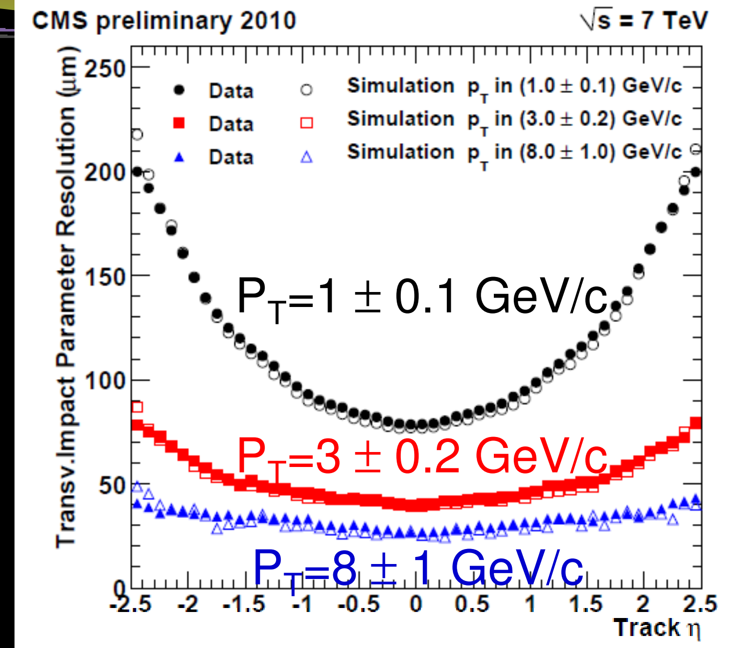


Material effects

- Transverse and longitudinal Impact parameter resolution as a function of η



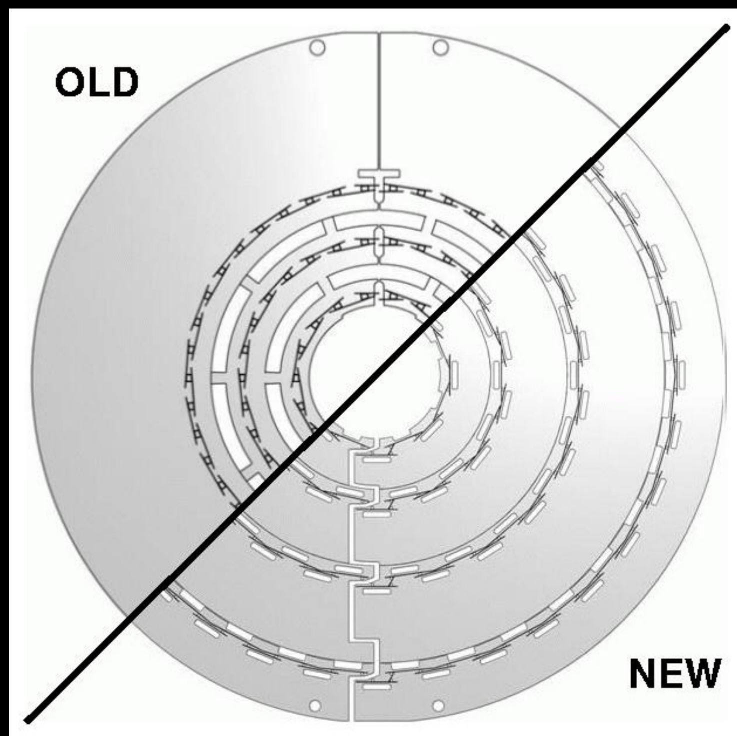




- The effect of the 18 innermost pixel layer cooling lines on the transverse and the longitudinal impact parameter is clearly seen

CMS material reduction plans

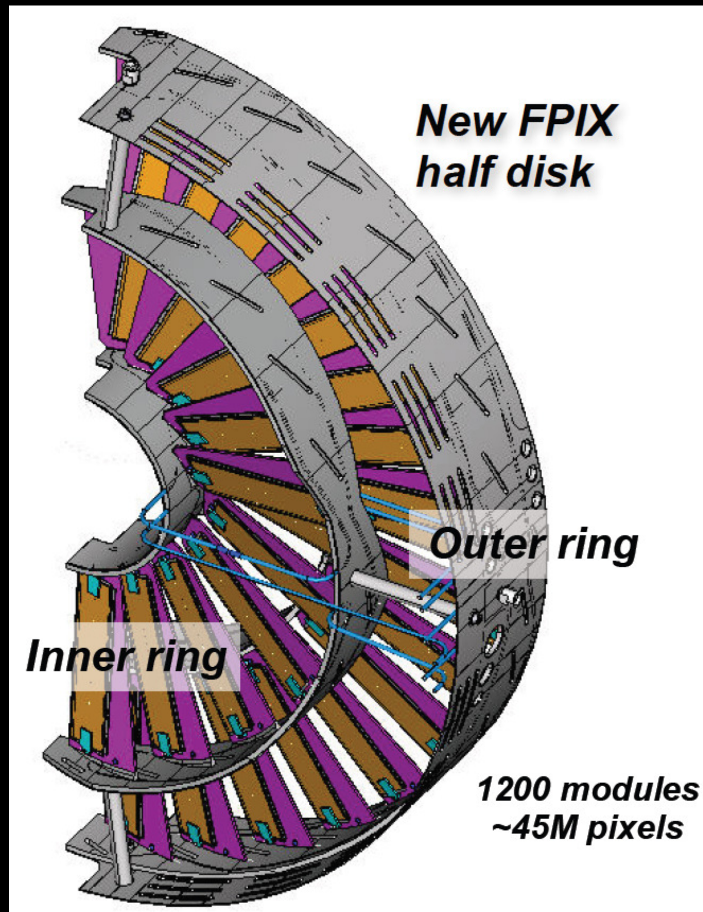
BARREL



- Ultra-light support structure:
- 200 μm carbon fiber
- 4mm Airex foam filler
- Stainless steel tubes (1.5 mm OD, 50μm wall thickness)
- Innermost layer with reduced radius (39mm)
- Additional outermost layer at 160mm
- ~2x radial acceptance
- ~65% more pixels

The total weight of the 4 barrel layers plus supply tube within this *is* 7 kg, about a factor 2.4 less than the current BPIX detector with only 3 layers.

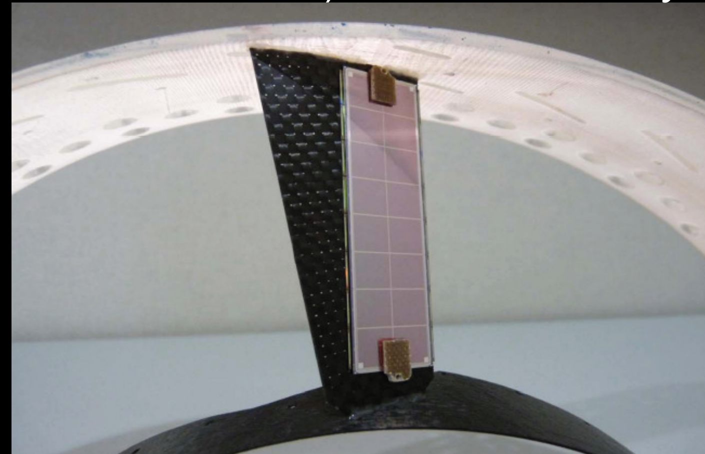
CMS material reduction plans FORWARD



- Half disks divided in inner and outer rings for easier replacement
- 1 type 8x2 ROC modules 18M -> 45M pixel

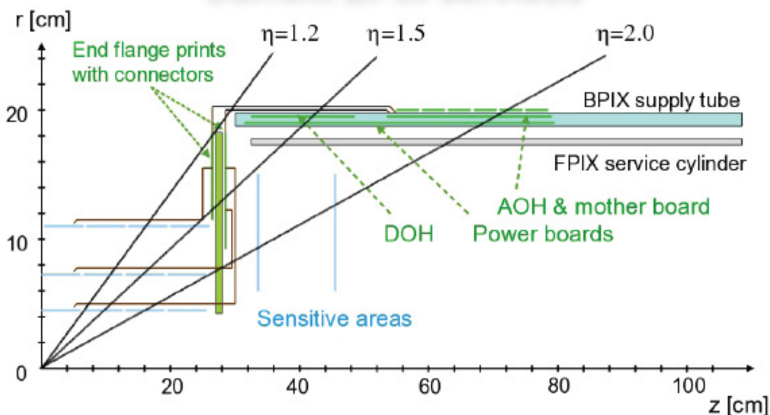
Ultra light support

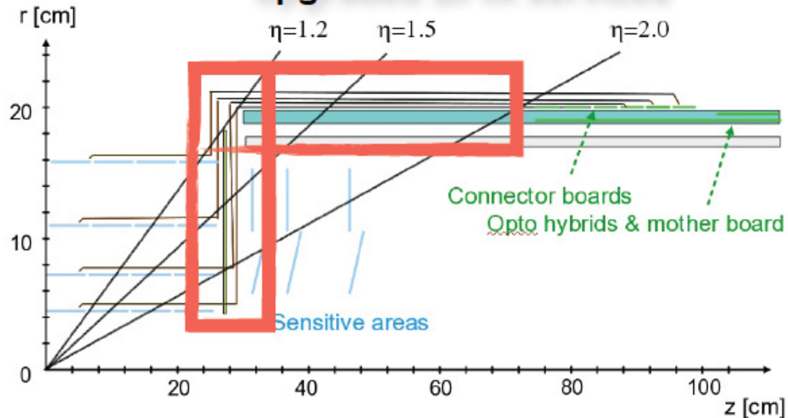
- One ply of Carbon Fiber Reinforced Polymer on Thermal Pyrolytic Graphite as facing sheet.
- CF encapsulation on both sides of TPG,
- TPG has a high thermal conductivity (in-plane k = up to 1700 W/m-K) and low density (2.26 g/cc)

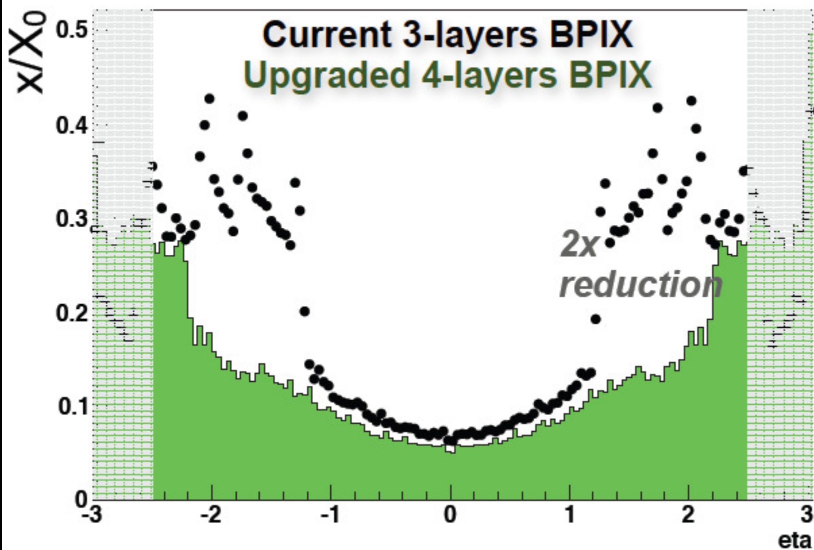


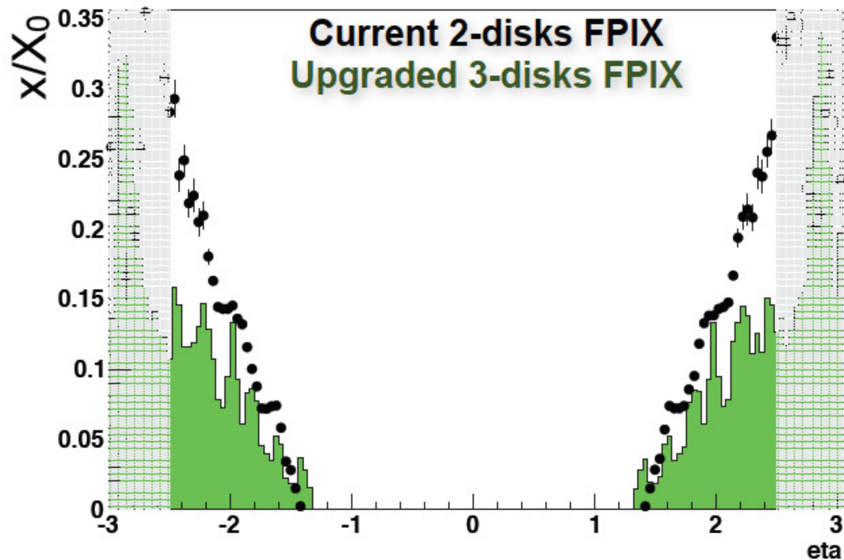
The weight of the new half-disk is estimated to be 420 g, to be compared with the present 607 g. Within η *< 2.5, the total weight of each half cylinder, including the* three half-disks, cables, and cooling lines, is estimated to be 1.82 kg.

CMS Pixel Material



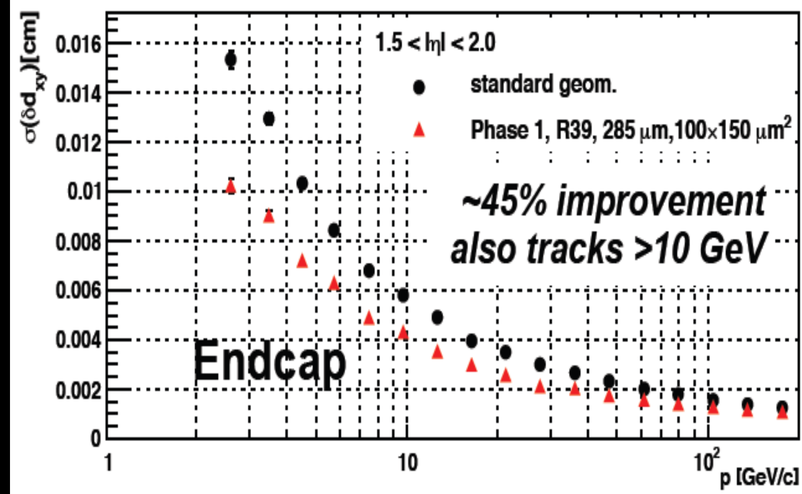


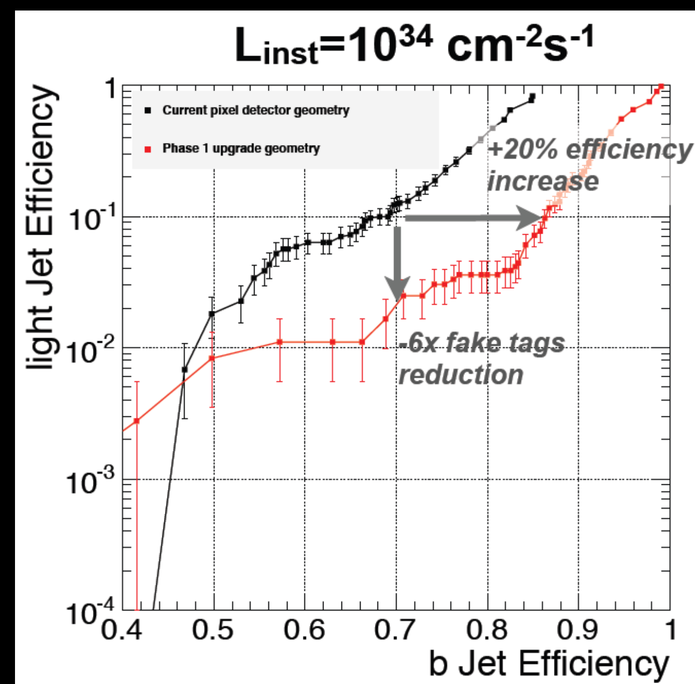




Performance improvements

- Reduced material and larger lever (2x)arm improves track parameter and vertex resolution at High Level Trigger
- Iterative tracking can use seeding based on quadruplets & triplets
  - Reduce fake rate
  - Increasing tracking efficiency
  - Both critical for high pile-up events
- Reduced distance between outermost pixel layer and innermost strip layer ⇒ smaller track extrapolation
- 4x better p_T resolution
  - Both can reduced combinatorics and lead to faster pattern recognition
- Reduced material improves electron reconstruction and reduces fake tracks from photon conversions and nuclear interactions



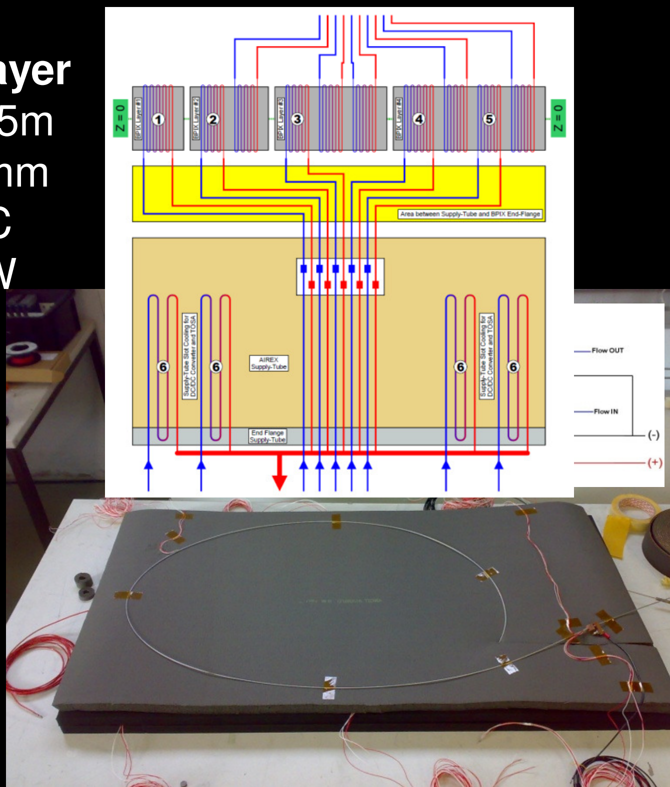


CO2 cooling R&D

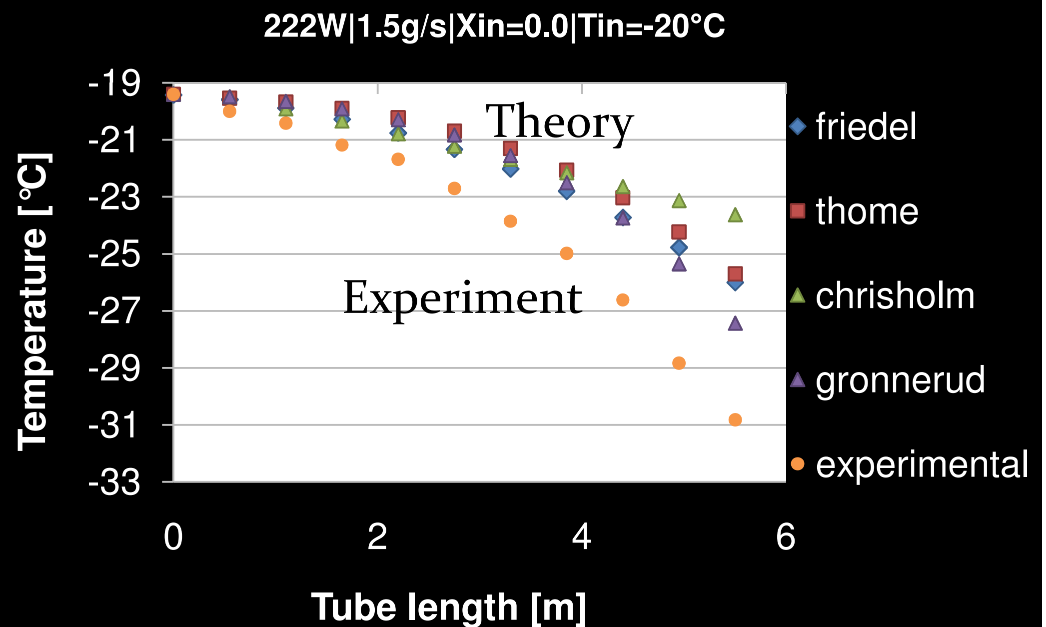
- Implementation of CO_2 cooling is critical to achieve reduction in material
- The pixel detector cooling uses miniature pipes involve a domain of CO_2 heat transfer and two-phase flow for which there are few experiment measurements and poor agreement between experimental measurements and theory

BPix Cooling Layout

BPix Layer #1 L=5.5m
ID=1.4mm
T=-20℃
P=150W

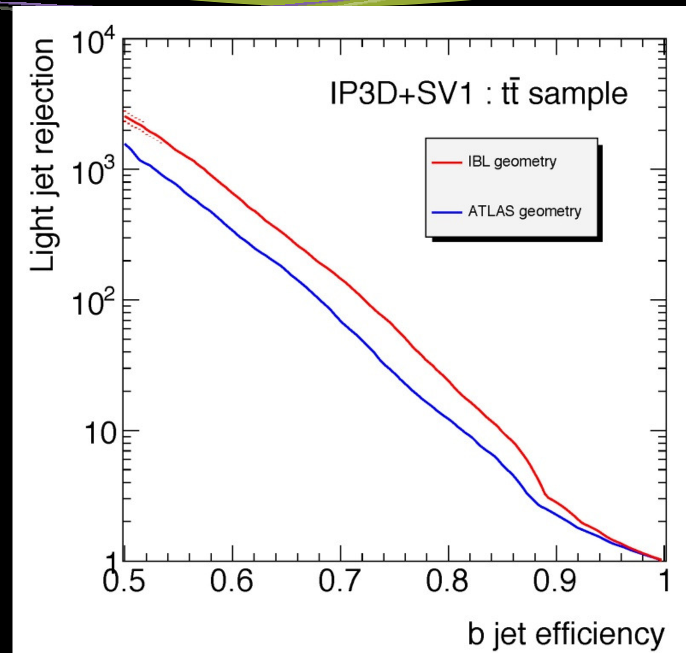


Experimental vs Theoretica:

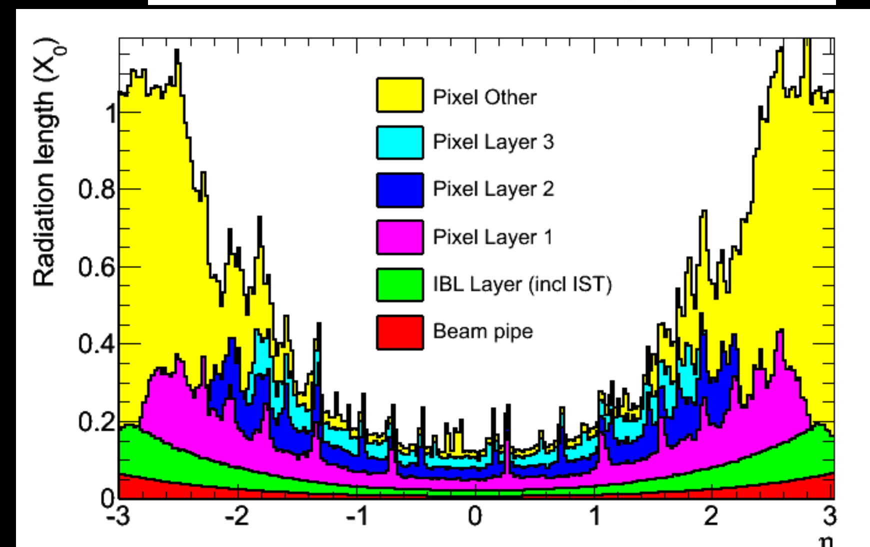


ATLAS IBL Material reduction

- Developed new carbon foam material collaboration with industry (LBNL)
- Material is machineable, has low-density, high thermal conductivity, and strong.
- Baseline for all future ATLAS pixel mechanics designs. Can be applied in other future experiments.
- Current detector 3.5% X0 per layer
- Insertable B-Layer (IBL): current estimate 1.5% X0



Component	% X_0
beam-pipe	0.6
New BL @ R=3.2 cm	1.5
Old BL @ R=5 cm	2.7
L1 @ R=8 cm	2.7
L2 + Serv. @ R=12 cm	3.5
Total	11.0

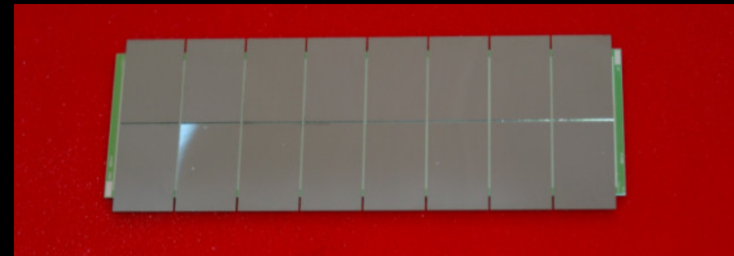


Thinning of Hybrid pixels

Bonn and IZM

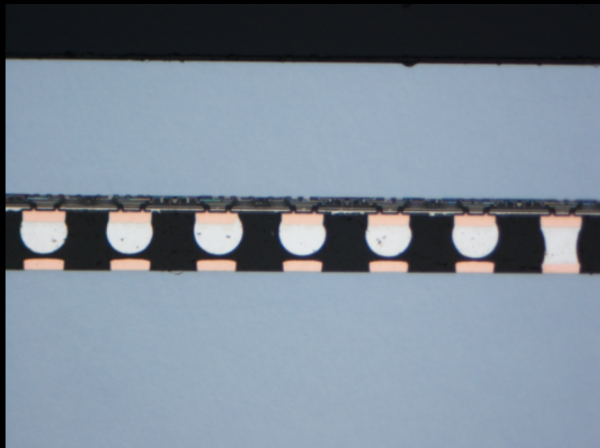
- Current flip chip technique: IZM solder SnAg
- Chip bow during flip chip
- New techniques using handle-wafers during flip chip and lift-off after flip chipping are needed
  - 3 methods studied so far with IZM Berlin

1st method: wax



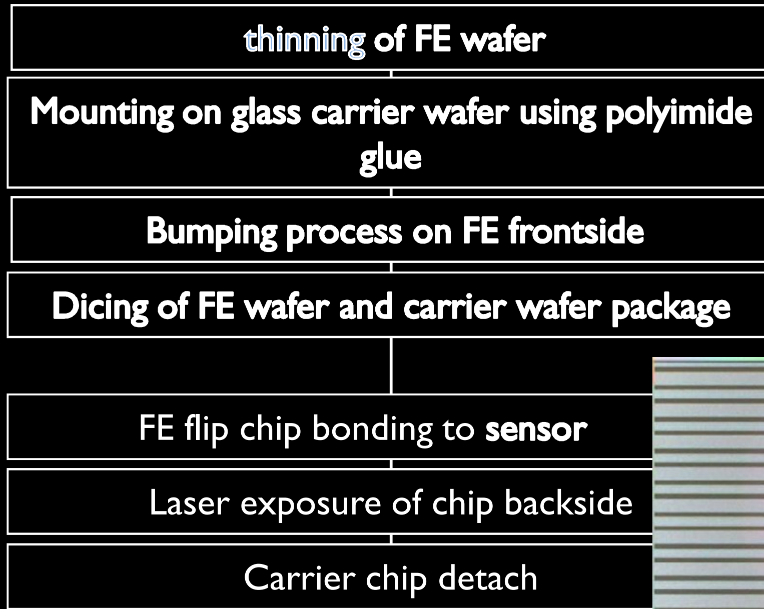
ATLAS pixel module with **90 µm** thick FE-I2

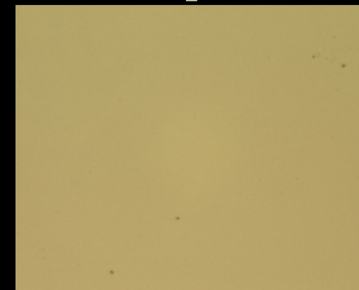
2nd method Brewer glue



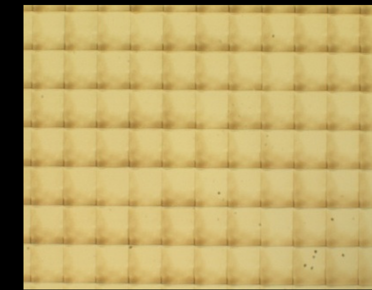
- Not successful
  - thinning ok, but chips bent up at the corners, opposite to the End Of Column region
  - Bump bonds do not connect in this area

Thinning of Hybrid pixels





Glass carrier on Si test chip before laser exposure_25x



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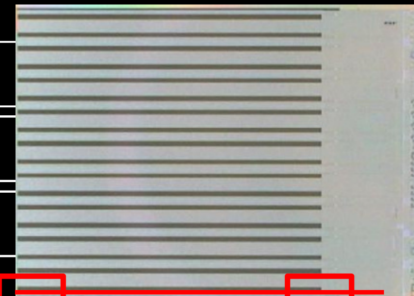
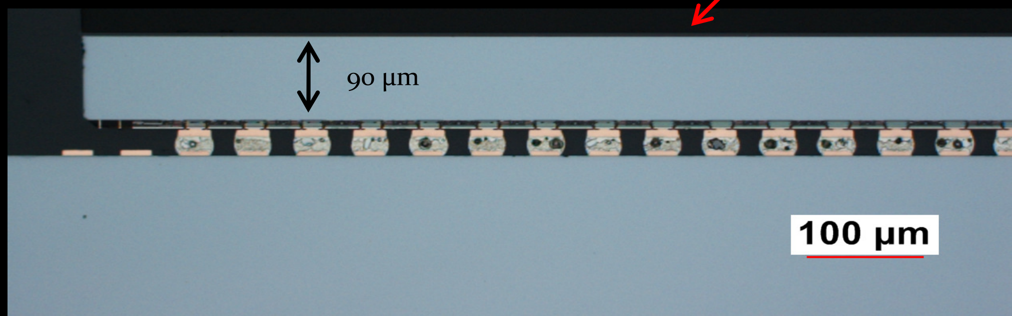
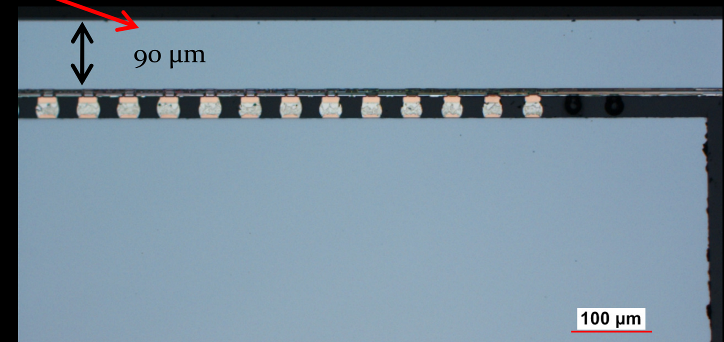


2x2 FE-I2 array, **90um**, on dummy sensor
Cross section cut of first column → **all bumps are connected!!!**



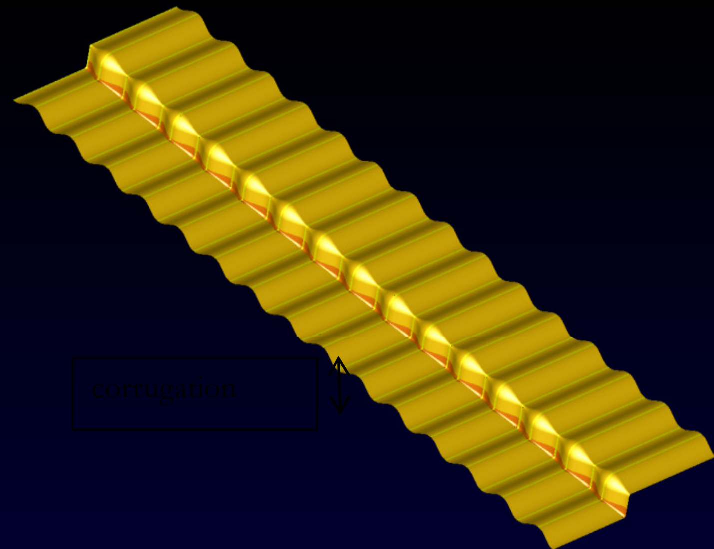


LHCb RF foil

- Provide separation from extreme-high-vacuum of LHC from Detector vacuum and Protects against RF effects
- Very diverse & severe requirements !
    - Vacuum tight.
    - Radiation hard.
    - Low mass. (dominant in X_0 contribution), but rigid
    - Electrical conductive

      (beam mirror currents and shield front-end electronics)
    - Thermally stable and conductive

      (heat load from beam)

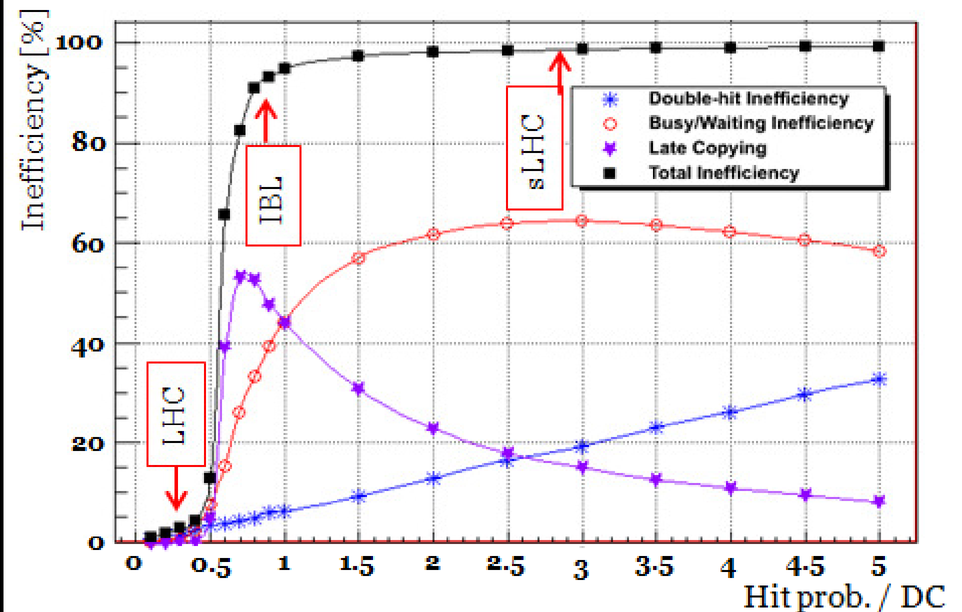


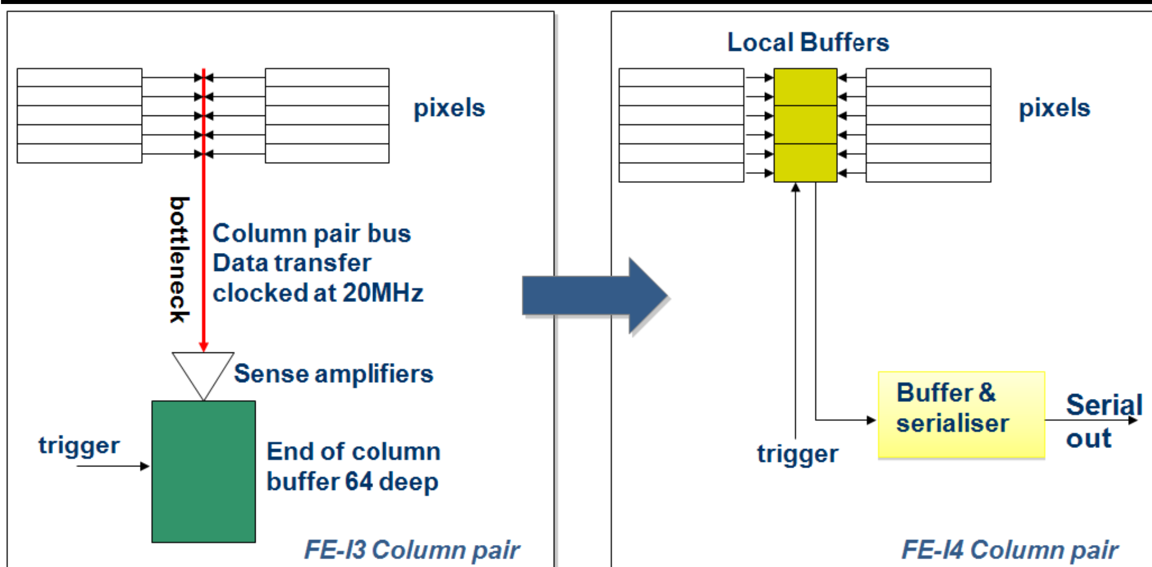
- Material and manufacturing options:
    - Aluminium: 200-350 um thickness.
        - Formed by superplastic deformation as used in present foils.
    - CF composite, coated with Aluminium.
        - Could reduce X_0
        - Prototype work started (CMA, Tucson, AZ.)

Pixel Readout R&D

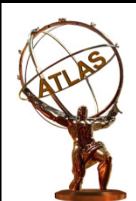
- Hit inefficiency rises steeply with the hit rate
- Dead time due to congestion in double-column readout
  - Example data loss of CMS PSI46 at 10^{34} at 4 cm =3.8%
- Possible solution: more local in-pixel storage (130 nm !)
  - >99% of hits are not triggered → No need to move them

Current ATLAS CHIP FE-I3





- FE-I4 new digital architecture: local regional memories
- FE-I4 has smaller pixel size 50μm×250μm

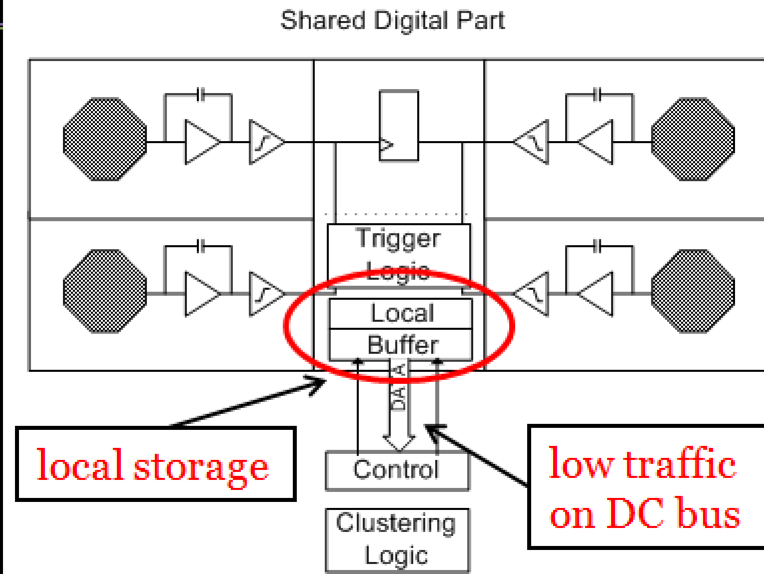


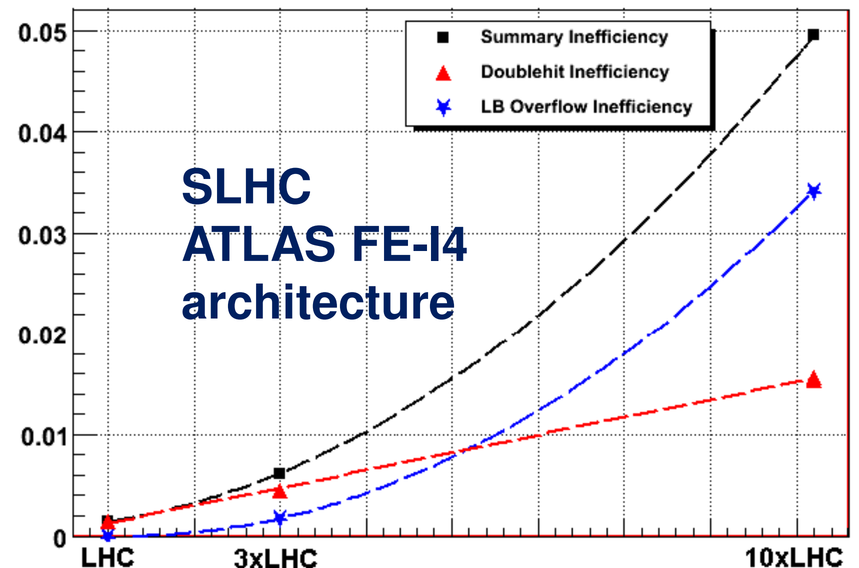
FE-I4A R&D

- Store hits locally in region until L1T.
- Only 0.25% of pixel hits are shipped to EoC → DC bus traffic “low”.
- Each pixel is tied to its neighbors -time info- (clustered nature of real hits). Small hits are close to large hits! To record small hits, use position instead of time.

Consequences:

- Spatial association of digital hit Lowers digital power consumption (below 10 μW / pixel at IBL occupancy).
- Physics simulation → Efficient architecture



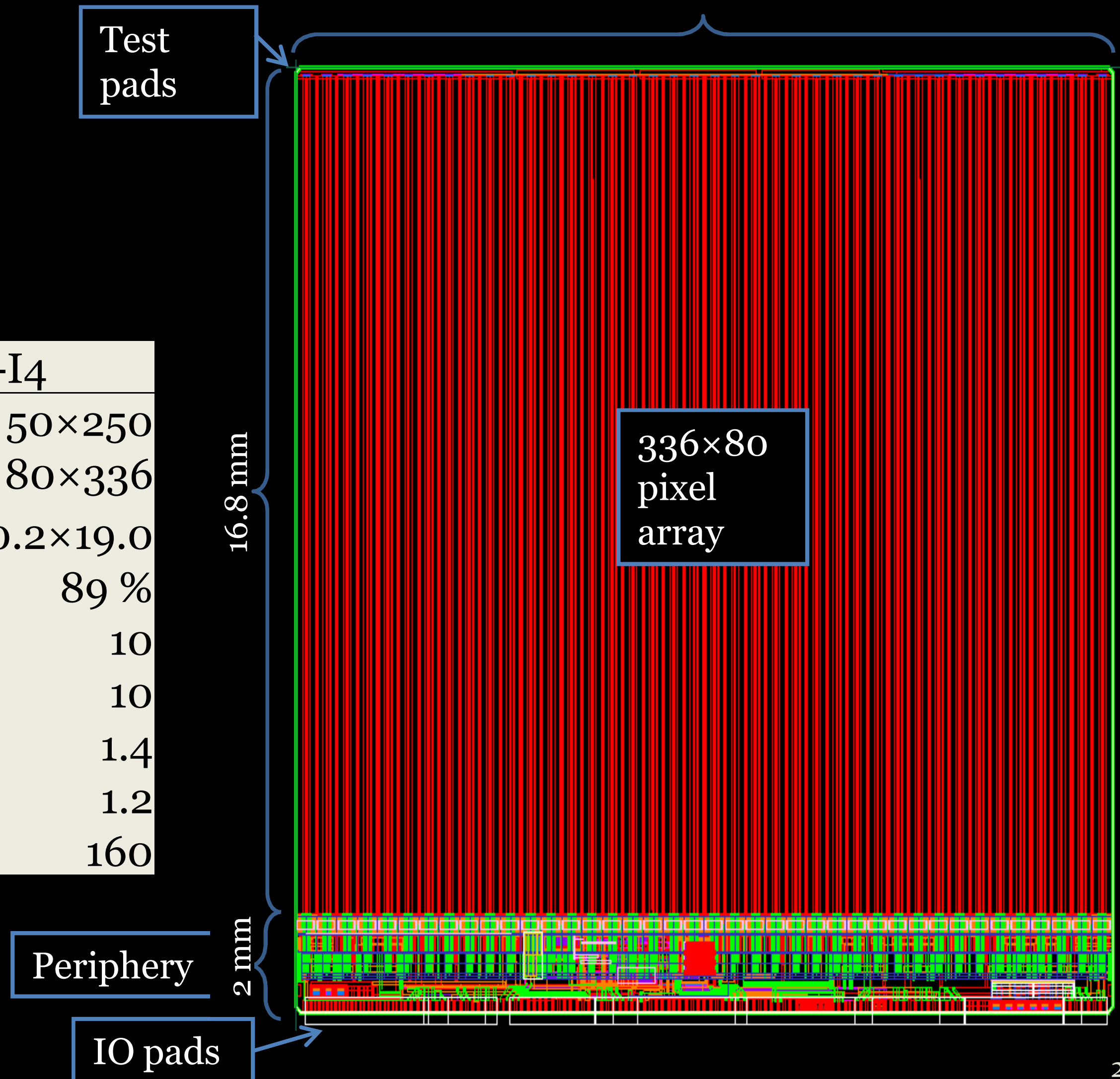


FE-I4A

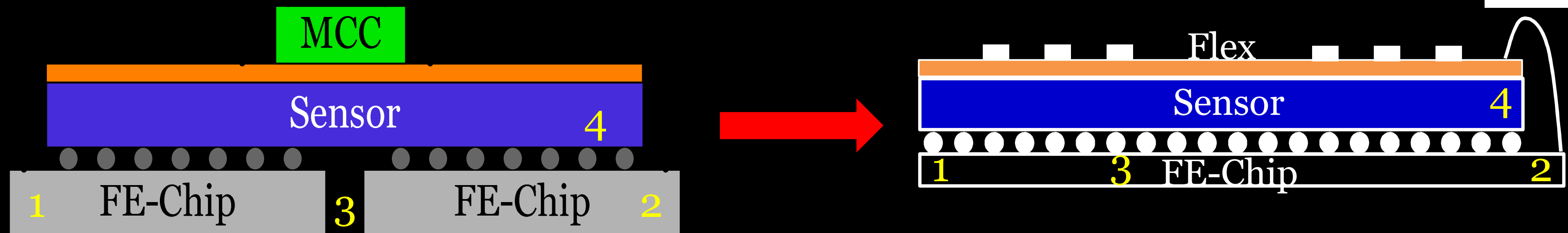
- Rad.-hardness: >250 MRad ionizing dose (FE-I3: >50 Mrad).
- Minimal guidelines: no Enclosed Layout Transistors, minimal size and guard rings only for analog & sensitive digital circuitry.
- DC leakage current tolerant to > 100 nA.
- ToT coded on 4 bits.

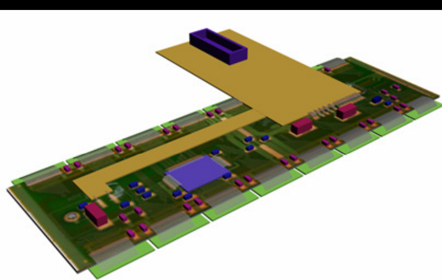
- Full scale prototype.
- Many test features provided.
- Submitted August 2010.
- Wafer ship date September 14th.

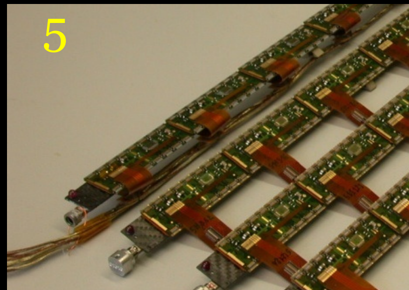
	FE-I3	FE-I4
Pixel Size [μm²]	50×400	50×250
Pixel Array	18×160	80×336
Chip Size [mm²]	7.6×10.8	20.2×19.0
Active Fraction	74 %	89 %
Analog Current [μA/pix]	26	10
Digital Current [μA/pix]	17	10
Analog Voltage [V]	1.6	1.4
Digital Voltage [V]	2	1.2
pseudo-LVDS out [Mb/s]	40	160



FE-I4 R&D





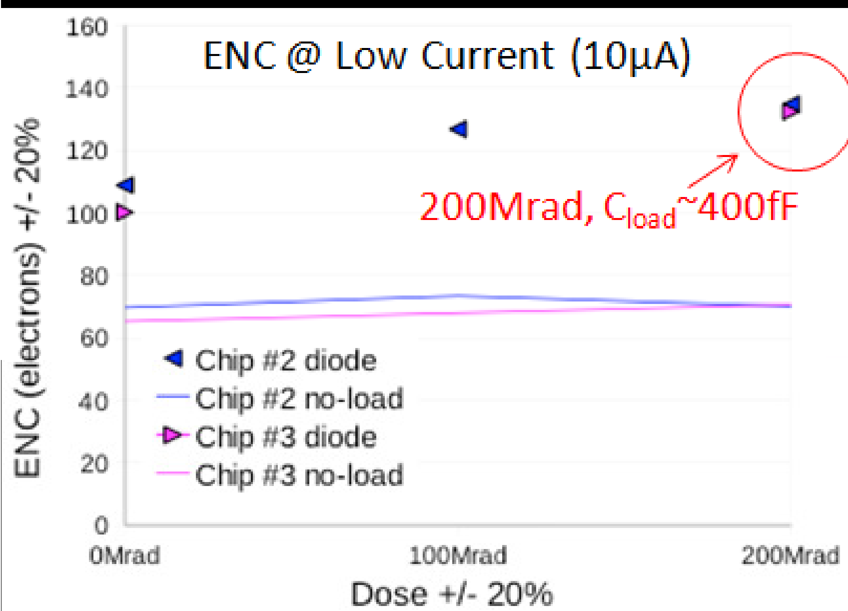


1) Big chip (periphery on one side of module).
2) Reduce size of periphery (2.8 mm→2 mm).
3) Thin down FE chips (190 μm→90 μm).
4) Thin down the sensor (250 μm →200 μm)?
5) Less cables (powering scheme)?

- Big FE (~2x2cm!) with increased active area: from less than 75 % to ~90 %:
  → Reduced periphery; <u>bigger IC</u>; cost reduction (main driver is flip-chip costs per chip).
- No Module Controller Chip:
  → More digital functionality in the IC.
- Power:
  → Analog design for reduced currents; decrease of digital activity (digital logic sharing for neighbor pixels); new powering concepts. 8 metal layers [2 thick Alu.] → power routing.

FE-I4A R&D

- Good noise/radiation hardness for analog pixel



- Novel CHIP development setup
  - Collaborate remotely using Cliosoft.com platform.
  - Participating institutes:

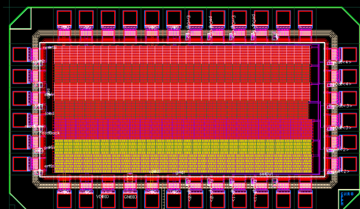
    Bonn: D. Arutinov, M. Barbero, T. Hemperek, A. Kruth, M. Karagounis.

    CPPM: D. Fougeron, F. Gensolen, M. Menouni.

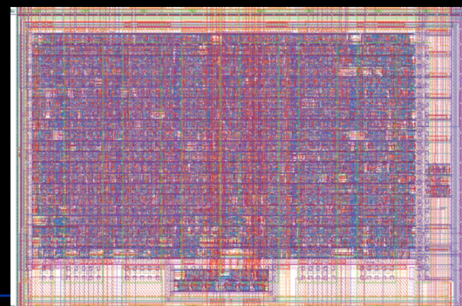
    Genova: R. Beccherle, G. Darbo.

    LBNL: S. Dube, D. Elledge, J. Fleury (LAL), M. Garcia-Sciveres, D. Gnani, F. Jensen, A. Mekkaoui.

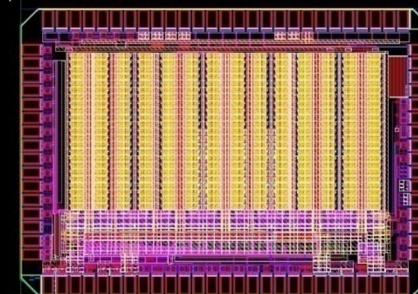
    NIKHEF: V. Gromov, R. Kluit, J.D. Schipper, V. Zivkovic.



SEU test IC



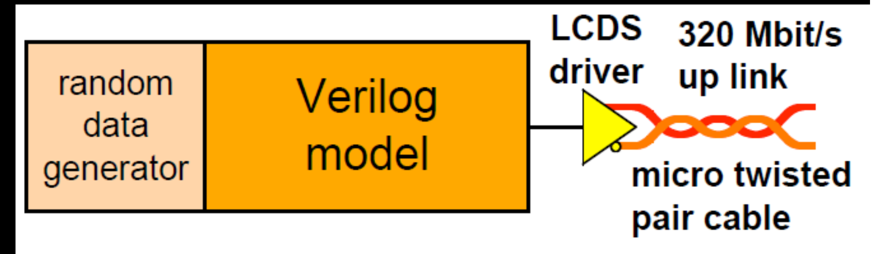
4-pixel digital region

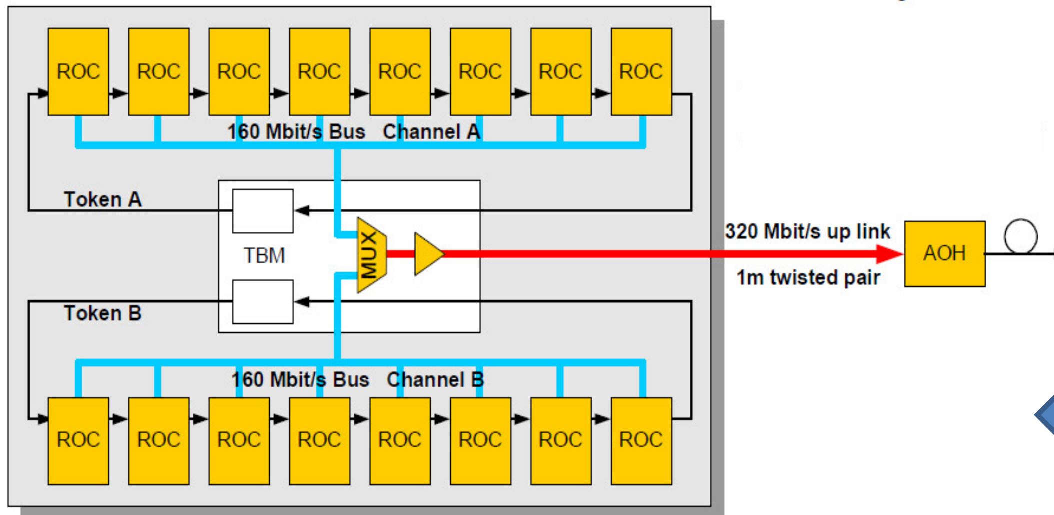


low power discri.

CMS Pixel ROC upgrade

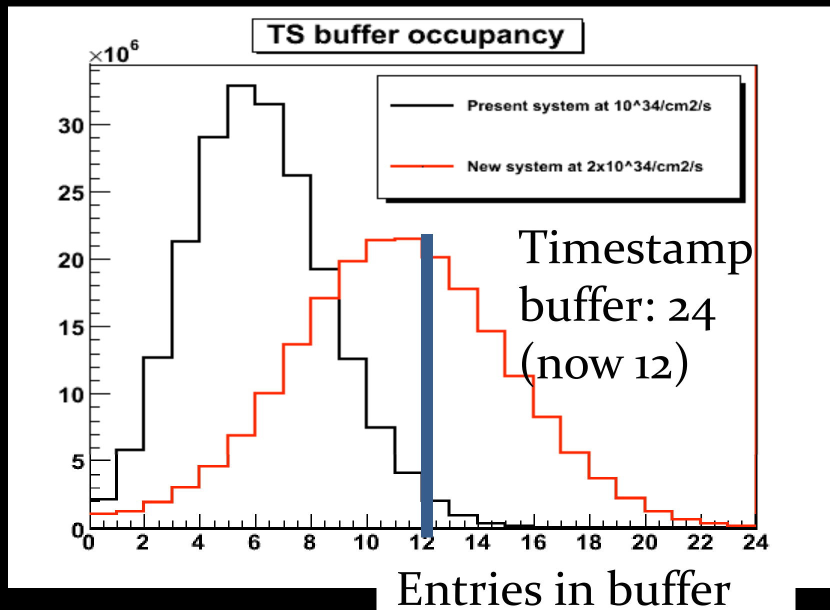
- New chip 250 nm ROC based on present readout chip.
- In Phase 1 CMS will have:
  - Higher luminosity ($2x10^{34}$ cm^{-2} s^{-1} peak)
  - Same number of fibres to counting room (+ spares)
  - Higher data rates requires digital uplink
    - →320 Mbit/s
    - →increase size of data buffers

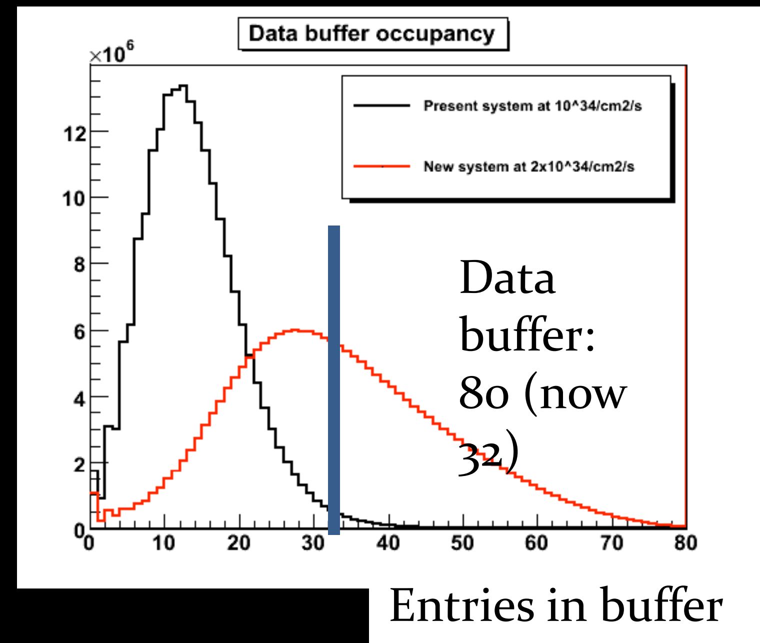


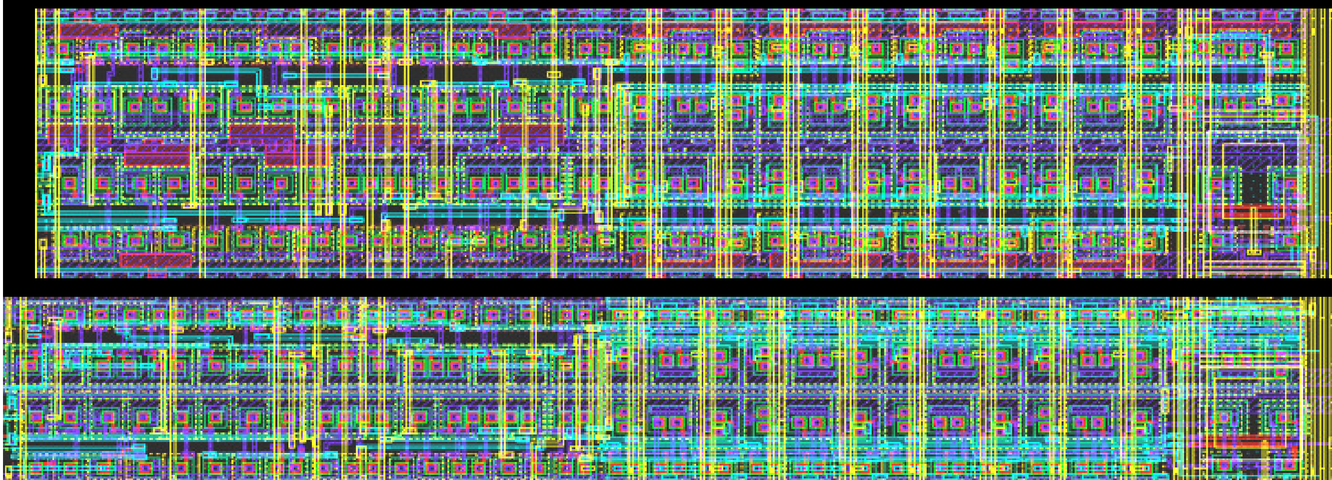


ROC with digital readout & data buffers
- 160 Mbit/s: ROC to TBM
- Digital multiplexer in TBM

CMS ROC upgrade







OLD buffer cell

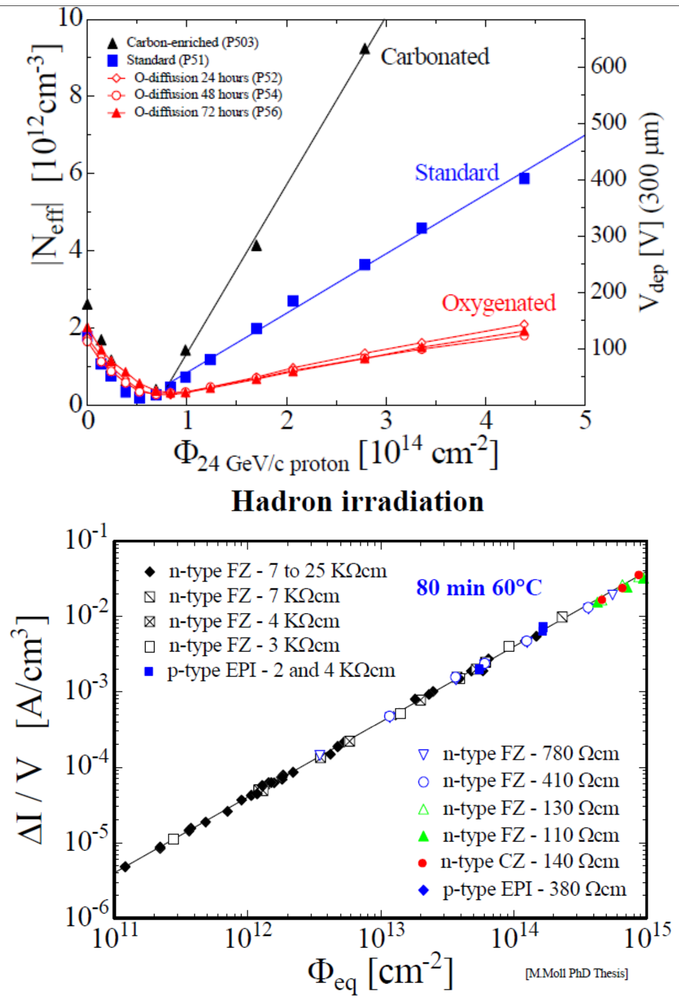
36 μm

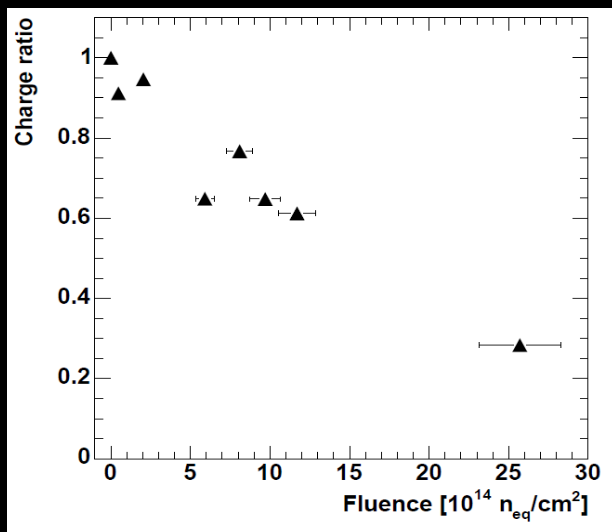
NEW denser buffer cell

22.4 μm

Radiation damage

- Bulk damage due to Non Ionizing Energy Loss (NIEL) causes displacement damage and built up of crystal defects
  - Change of effective doping concentration (higher depletion voltage, under- depletion)
  - Increase of leakage current (increase of shot noise, thermal runaway)
  - Increase of charge carrier trapping (loss of charge) most important effect at $\Phi > 10^{15}$ 1MeV neutron/cm^2





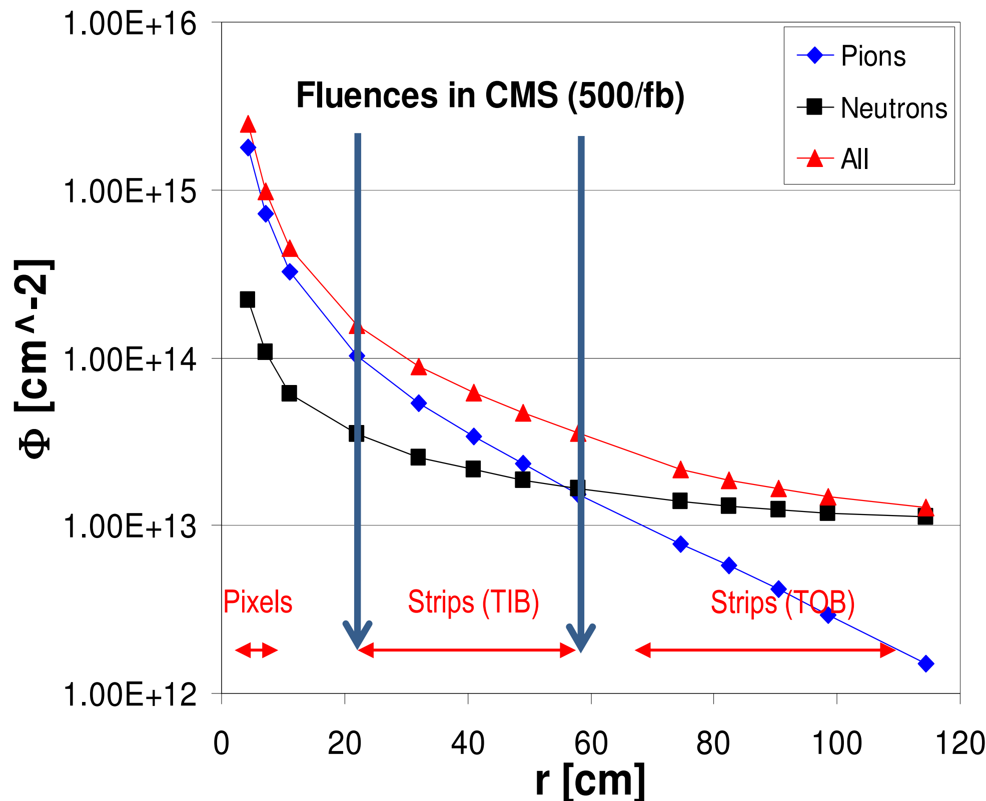
- Surface damage due to Ionizing Energy Loss (IEL) accumulation of positive in the oxide (SiO_2) and the Si/SiO_2 interface which affects interstrip capacitance (noise factor), breakdown behavior and therefore the detector performance

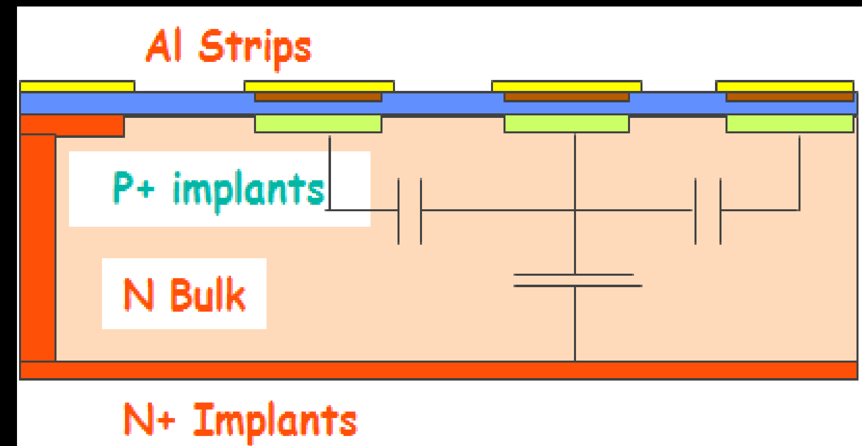
Signal/Threshold ratio is the quantity to watch

Silicon at the LHC

R>20 cm $\Phi<2\times10^{14}$ cm^{-2}

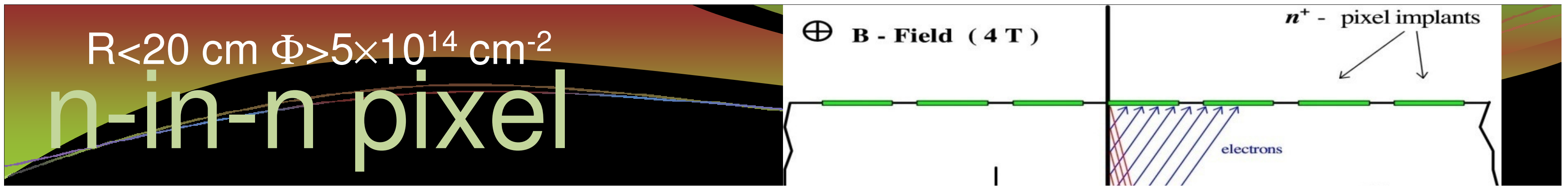
STRIPS: p-on-n

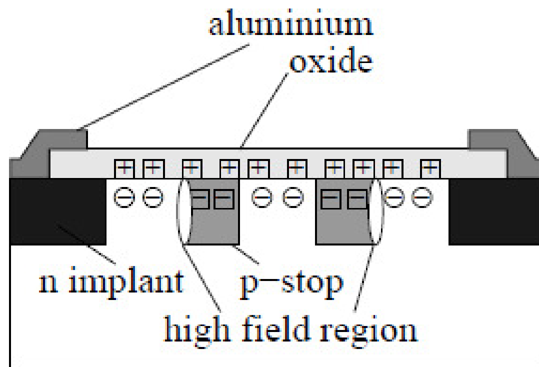




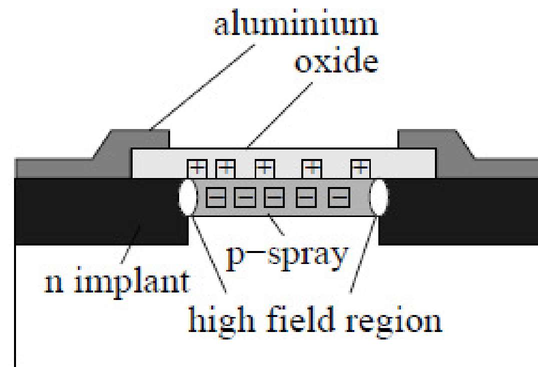
- p-on-n sensors work after bulk type inversion if they are biased above depletion
  - Optimize design to achieve much higher V_{break} to operate at higher V_{bias}
  - Strip width/pitch ~ 0.25: reduce C_{tot} and therefore the noise
  - Optimal edge processing for stable high bias voltage operation

R<20 cm Φ>5×10^{14} cm^{-2} n-in-n pixel

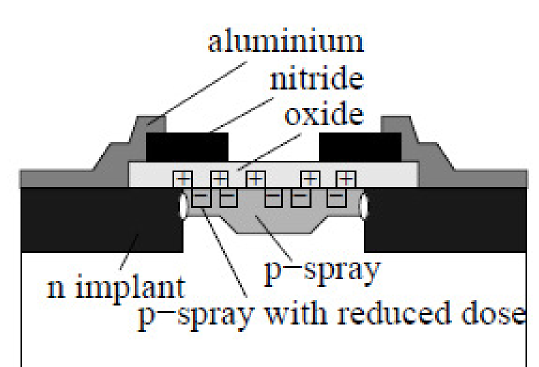




(a) *p*-Stops

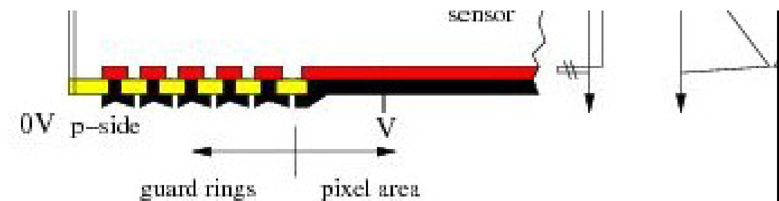


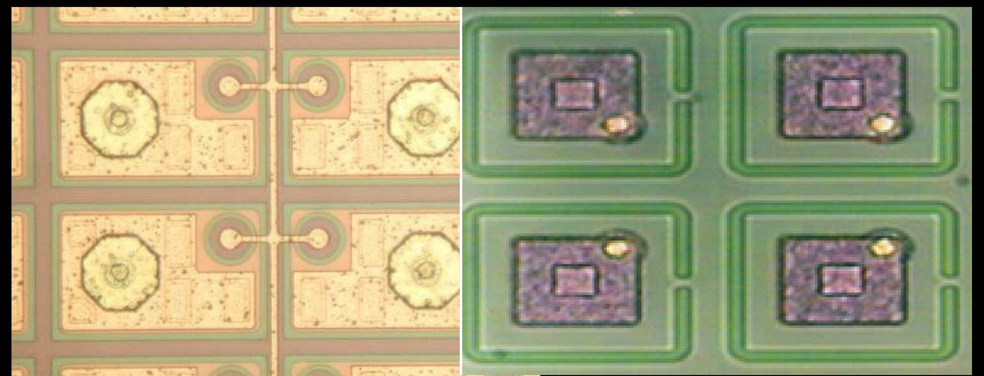
(b) *p*-Spray



(c) moderated *p*-Spray

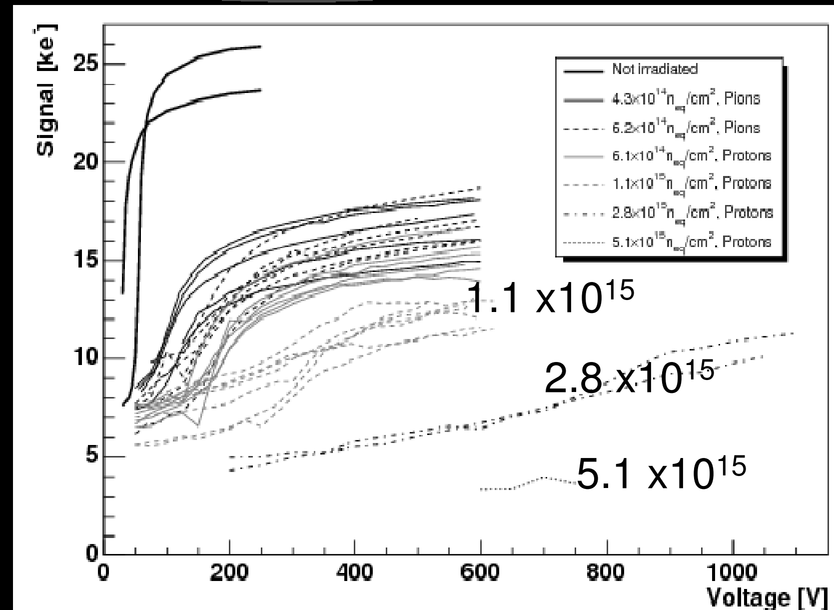
- **Isolation**
  - CMS BPIX and ATLAS
    - Moderated p-spray with bias grid
    - Small gaps, homogenous drift field, higher C ~ 80fF
  - CMS FPIX
    - Open p-stops, some over-depletion needed to separate channels
    - large gaps, smaller C

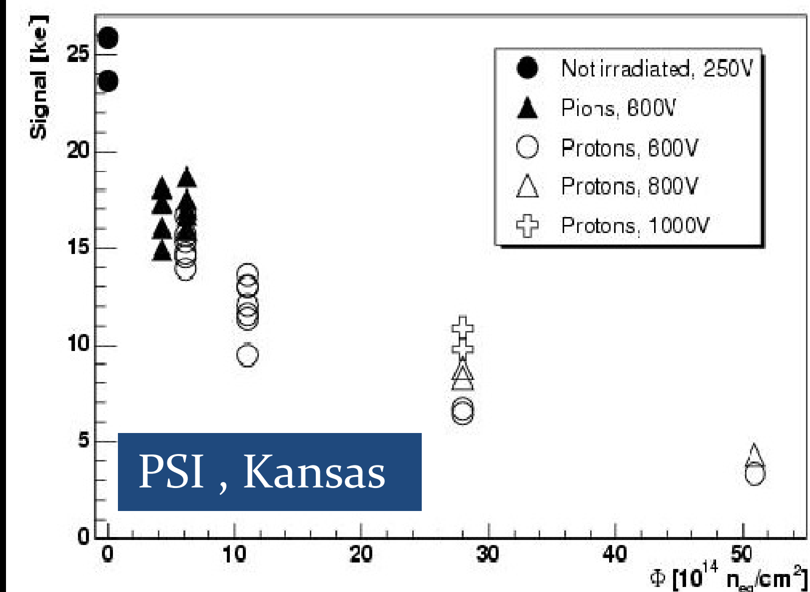




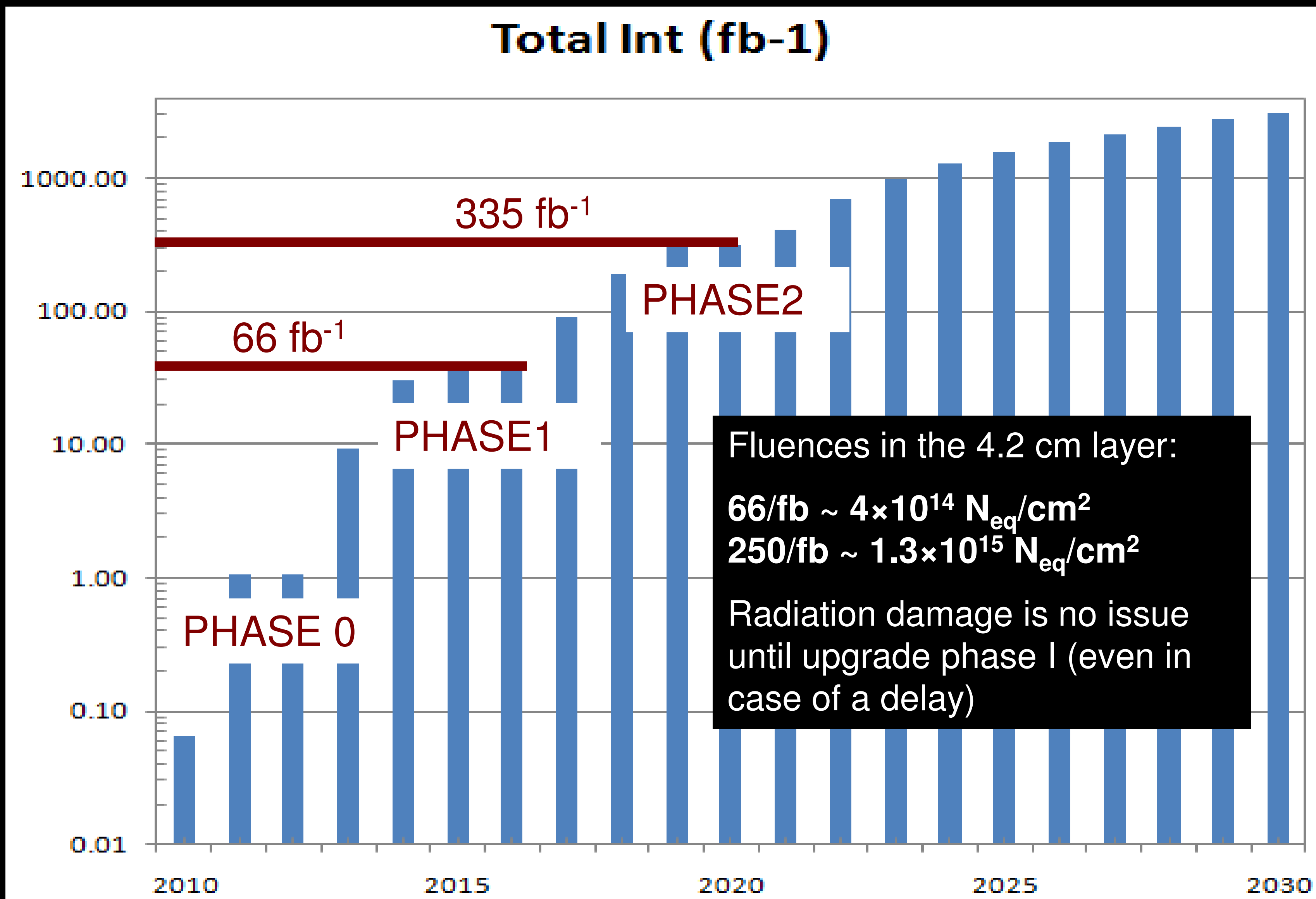
Performance of highly irradiated n-in-n

- Highly irradiated sensors operate up to 1kV
- No signal saturation with bias for $\Phi > 2\times10^{15} n_{eq}/cm^2$
  - Charge multiplication?
- Sensors exposed $2.8\times10^{15} n_{eq}/cm^2$ yield > 7ke (at 800V)
  - High voltage is limited in both CMS and ATLAS by connectors, cables and power supplies to about 500-600 V
  - Increase in bias voltage and decrease in signal worsen spatial resolution
- Detector might become "useless" for impact parameter measurement although detection efficiency is still high (>95%)
  - Present operational limit 1.2×10^{15} N_{eq} (~250 fb^{-1}, 4cm layer) reachable
- Any higher demand requires a smaller pitch in r-Φ





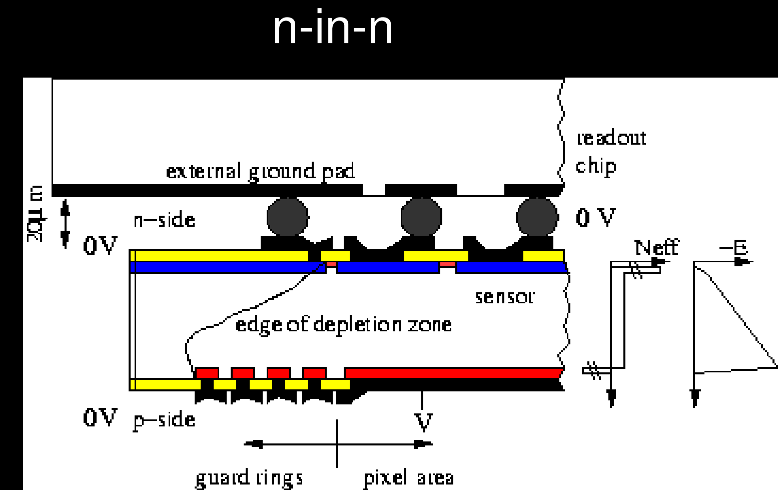
Estimated integrated luminosity



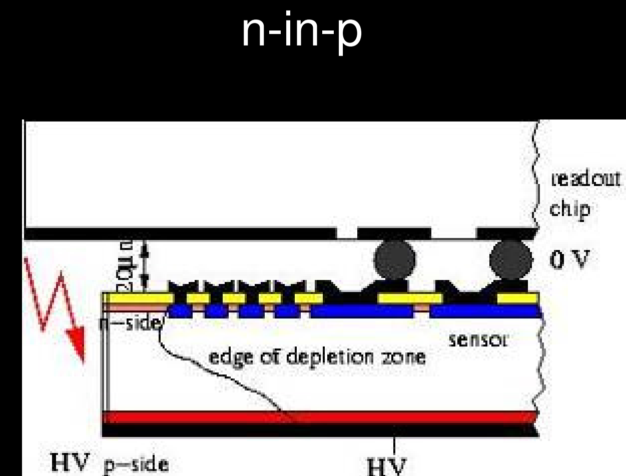
Exploring n-in-p pixels

- **Present CMS pixel detector uses n-in-n-sensors**
  - double sided processing (back side is structured)
  - all sensor edges on ground
  - most expensive part of the module (only bump bonding is more expensive)
- **Exploring n-in-p sensors as alternative**
  - recent studies show radiation hardness
  - single sided process promise prize benefit of factor 2-3
    - important since the CMS pixel area will be doubled in Phase 1
  - Absence of guard rings on back side lead to the risk of (destructive) sparking to the ROC

n-in-n



n-in-p



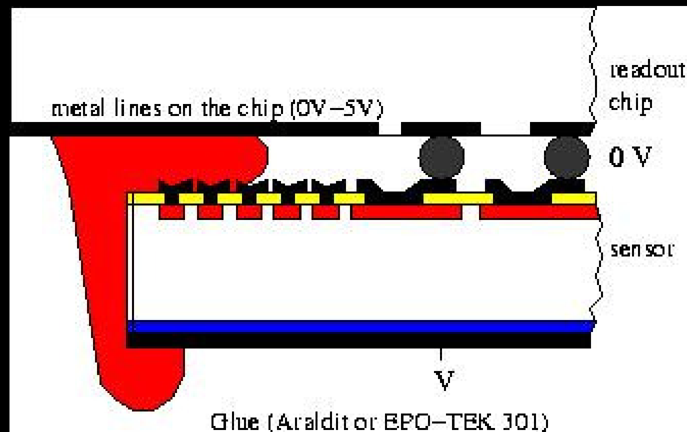
Exploring n-in-p pixels

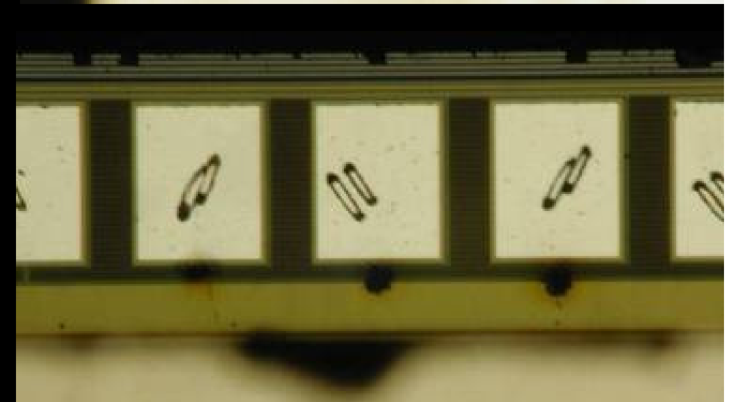
PSI

- Applied V_{bias} to the sensor while ROC was grounded
- Breakdown occurs at ~500V
  - Grounded pad on ROC completely destroyed
  - Other pads also damaged
  - Voltage surprisingly high aluminium also evaporated on sensor backside

Passivation of the edges with glues

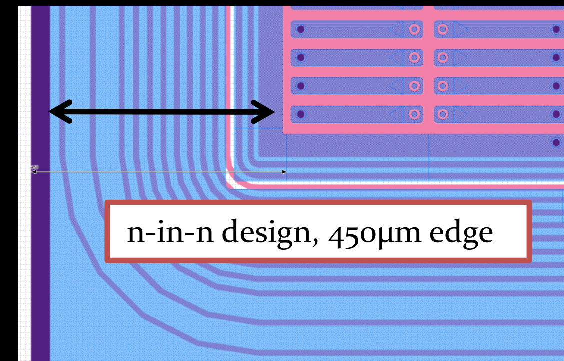
- Araldit used in CMS module production
  – no change of break down voltage
- EPO-TEK 301 very liquid, fills part of the gap
  – break down at ~700V

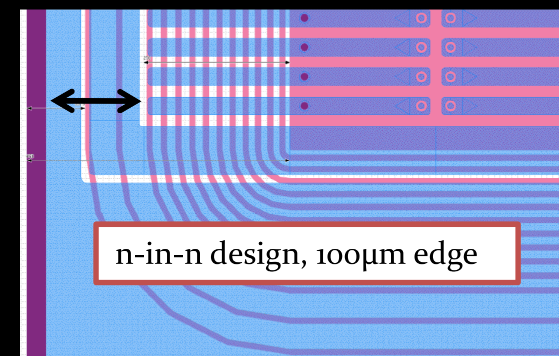


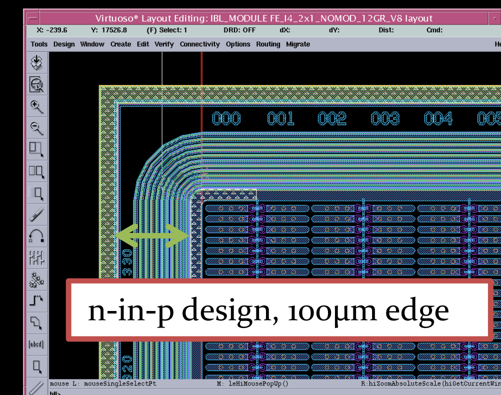


Thin edge R&D

- Planar n-in-n silicon sensors R&D for ATLAS IBL:
  - Similiar design as for ATLAS Pixel.
  - Radiation tolerance proven to several $10^{15} n_{eq}/cm^2$.
  - Main focus in development of slim edges.
- Planar n-in-p silicon sensors, thinned to 150µm:
  - Utilize the advantages of thinned sensors at a given maximum bias voltage
  - Standard 450µm wide inactive edge
  - Special passivation layer (BCB) needed for HV operation



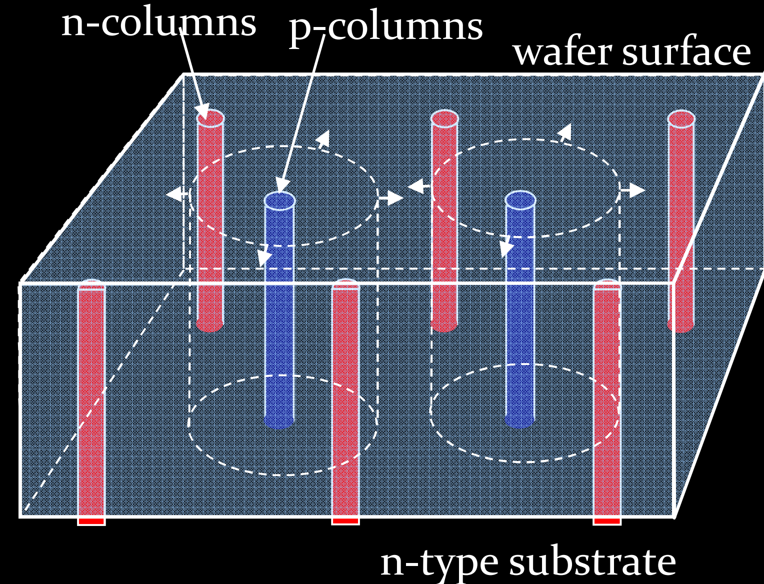


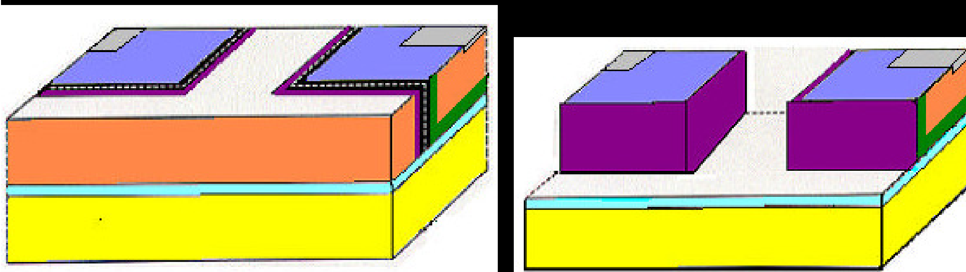


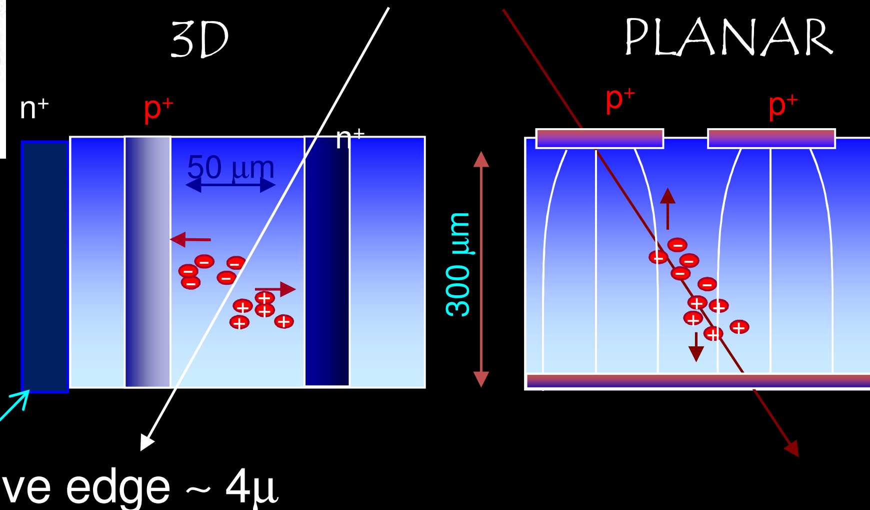
3D detectors

- Shorter drift distance and fast collection
- Lower depletion voltages
- Better radiation tolerance
- Sensor edge can be an electrode (Interesting for forward physics experiments)
- Inefficient in electrode area
- Non standard manufacturing
  - Deep Reactive Ion Etching (DRIE)
  - **Support wafer essential to fabricate active edge and use plasma etching**

3D
S. Parker 1995





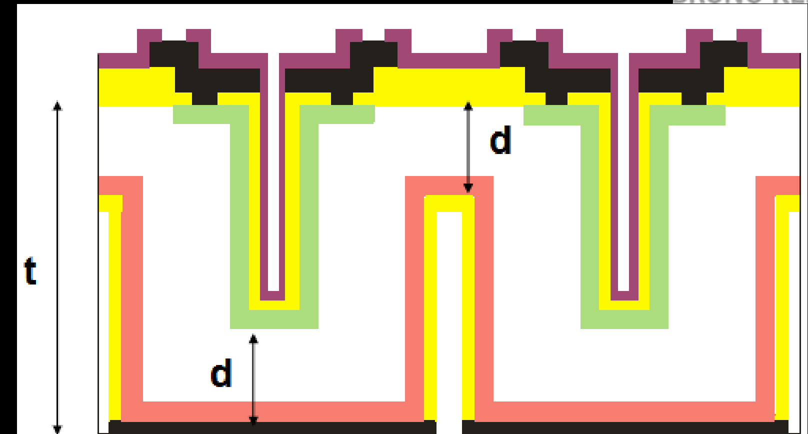


Active edge ~ 4µ

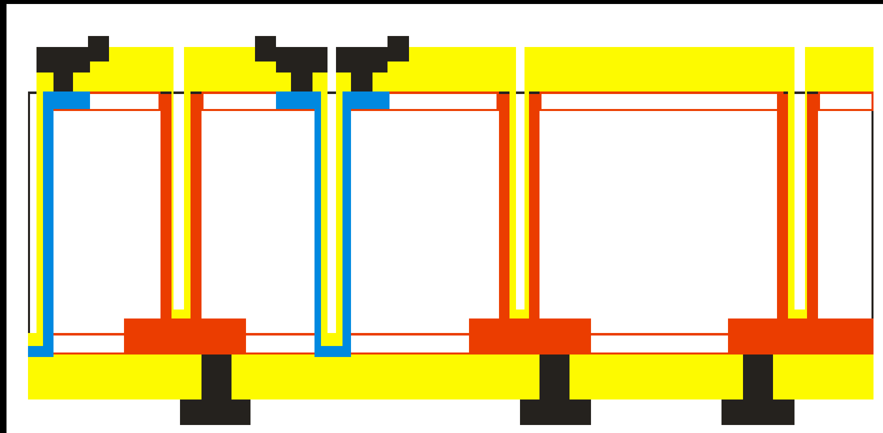
  - Poorly known yield & costs
- On going effort on industrialization:
  - **SINTEF (Oslo), FBK(Trento), CNM (Barcelona), VTT (Finland)**

3D-DDTC+ : passing through columns

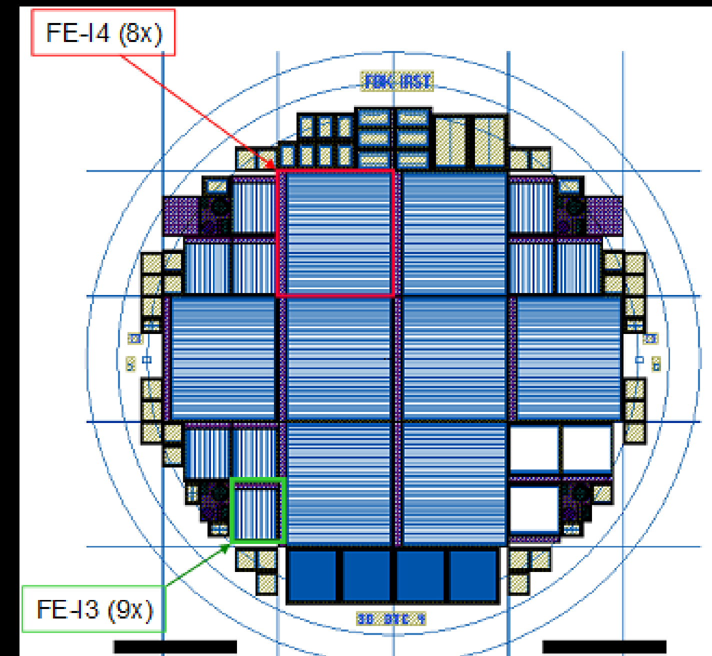
- Double-sided approach (3D-DDTC)
  - Hole etching by DRIE
  - Wide superficial diffusions around holes
  - Contacts at surface only
  - Passivation of holes with oxide:
    - Holes are empty (dead regions)



- Modified 3D-DDTC technology approach
- No support wafer, back-side accessible
- suitable for dual-readout pixel/strip
- Allows for "slim-edge" (~200 mm) detectors



- Two batches under fabrication at FBK one for ATLAS IBL prototypes



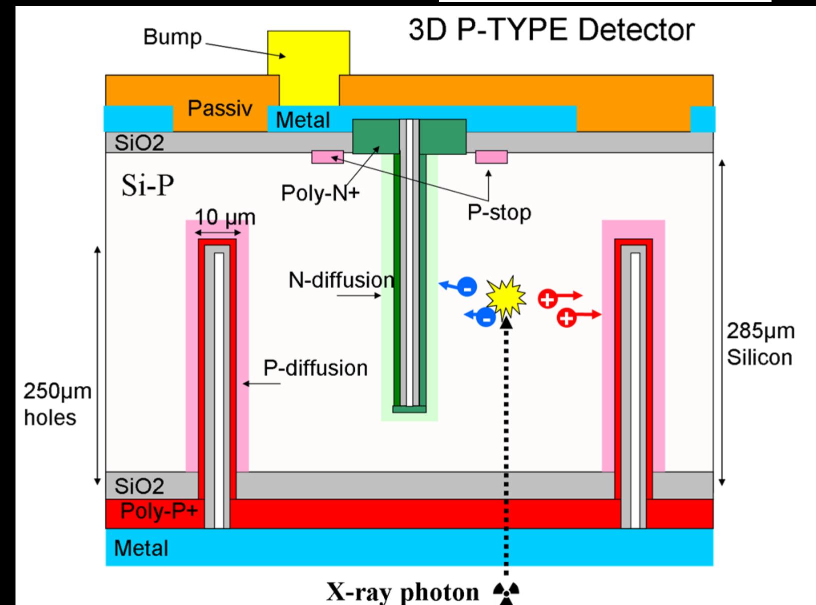
Double-sided 3D at CNM

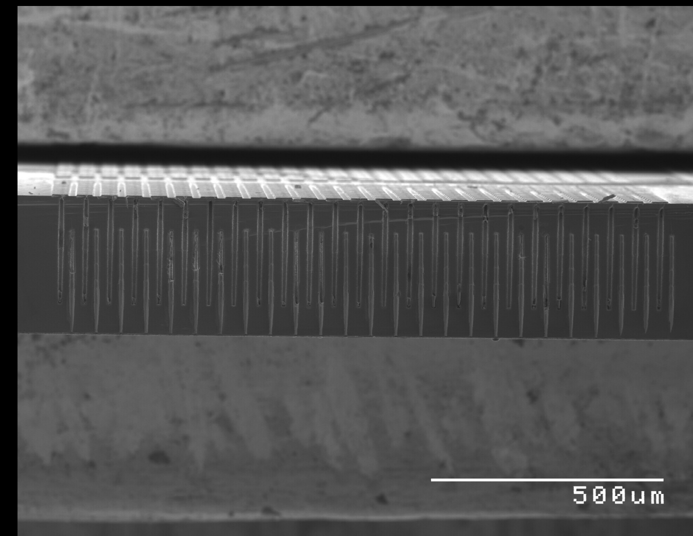
- Columns etched from opposite sides of substrate and don't pass through full thickness
- All fabrication done in-house using Inductively Coupled Plasma etching
- ICP is a reliable and repeatable process (many successful runs)

Electrode fabrication:

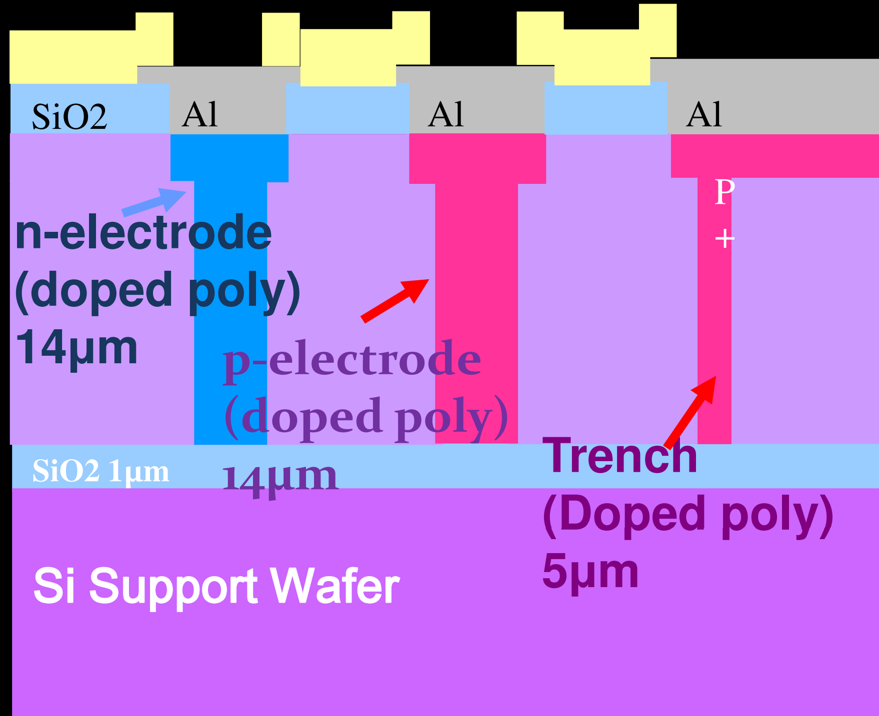
1. ICP etching of the holes: Bosch process, ALCATEL 601-E
2. Holes partially filled with 3 µm Low Pressure Chemical Vapour Deposition poly
3. Doping with P or B
4. Holes passivated with TEOS SiO_2

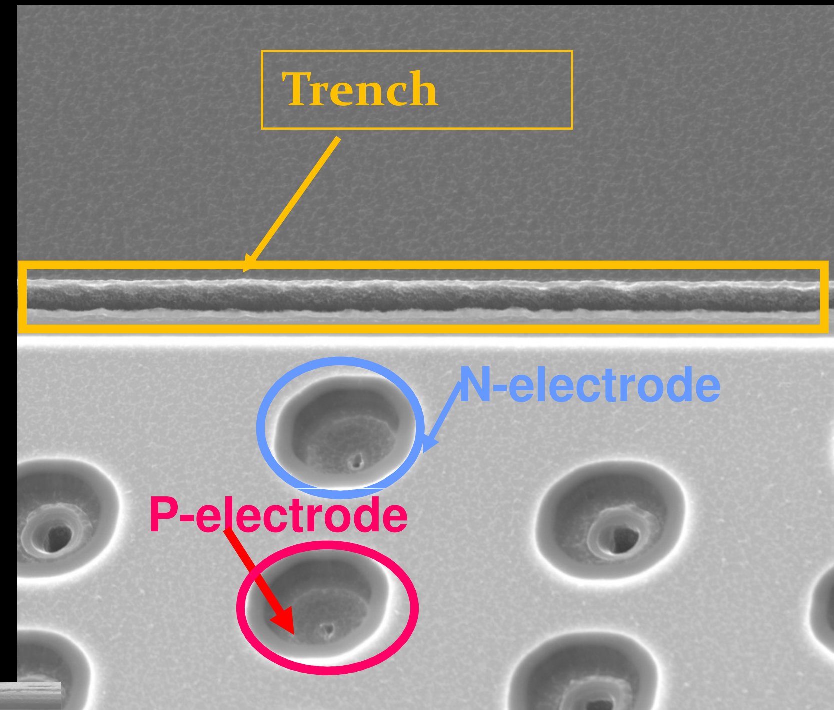
Hole aspect ratio 25:1
10µm diameter, 250µm deep
P- and N-type substrates, 285µm thick





SINTEF/Stanford process



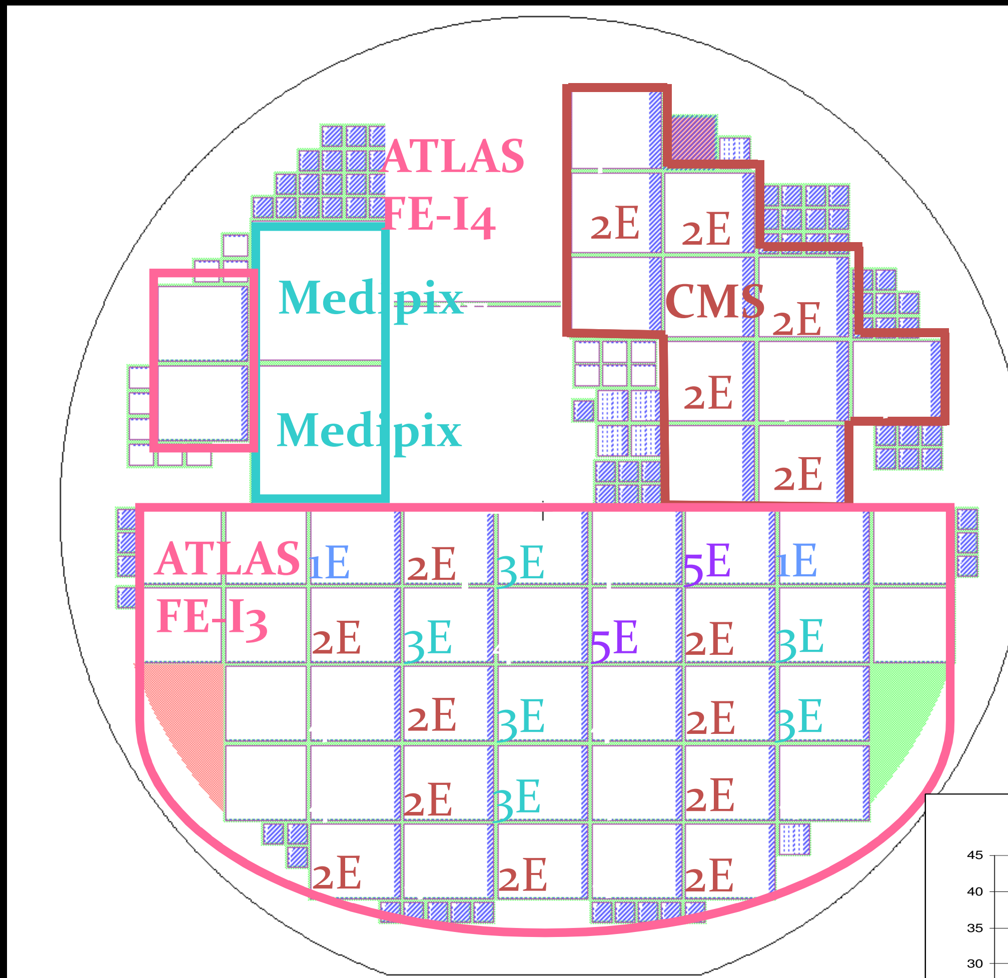


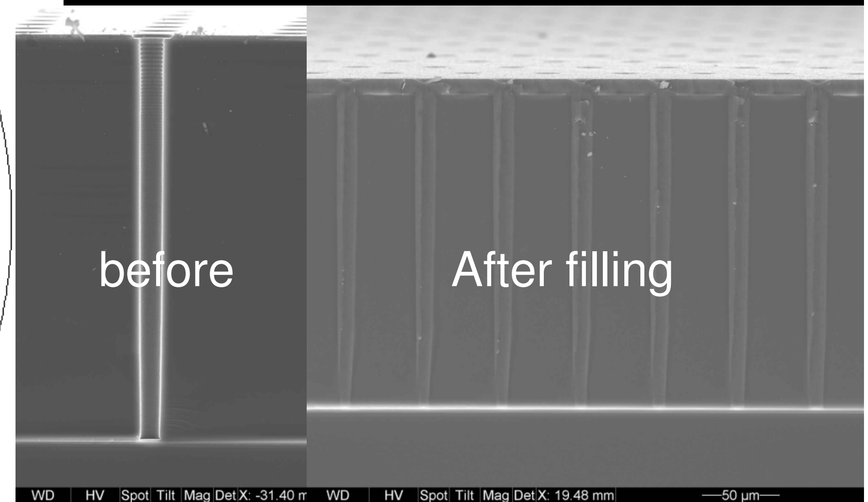
Holes and trenches filled with doped poly to form electrodes and active edge

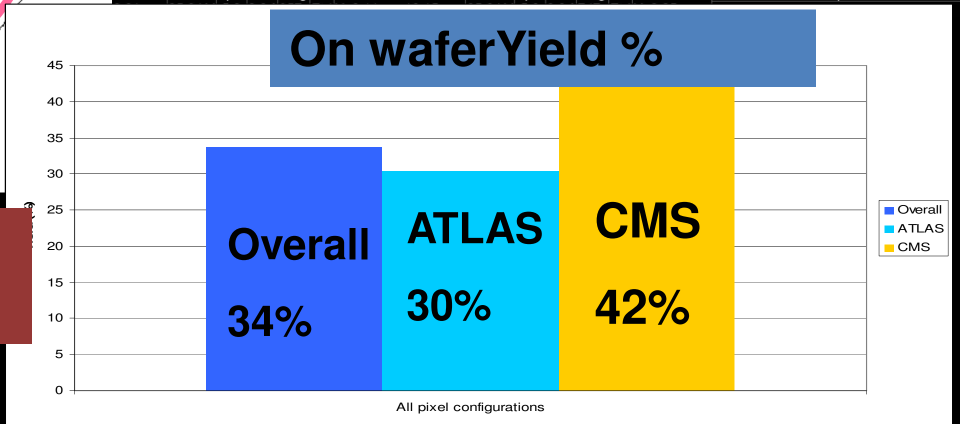
- Support wafer required
- Through wafer electrode
- Active electrodes and active edges
- Electrodes filled with poly

3D SINTEF

- Two runs. Improvements in the second run
  - Narrower trenches
  - Improved hole profiles
  - Extra nitride layer
  - Polyfilling at Stanford wth Oxygen free (diborane doping) at Stanford to improve electrode efficiency



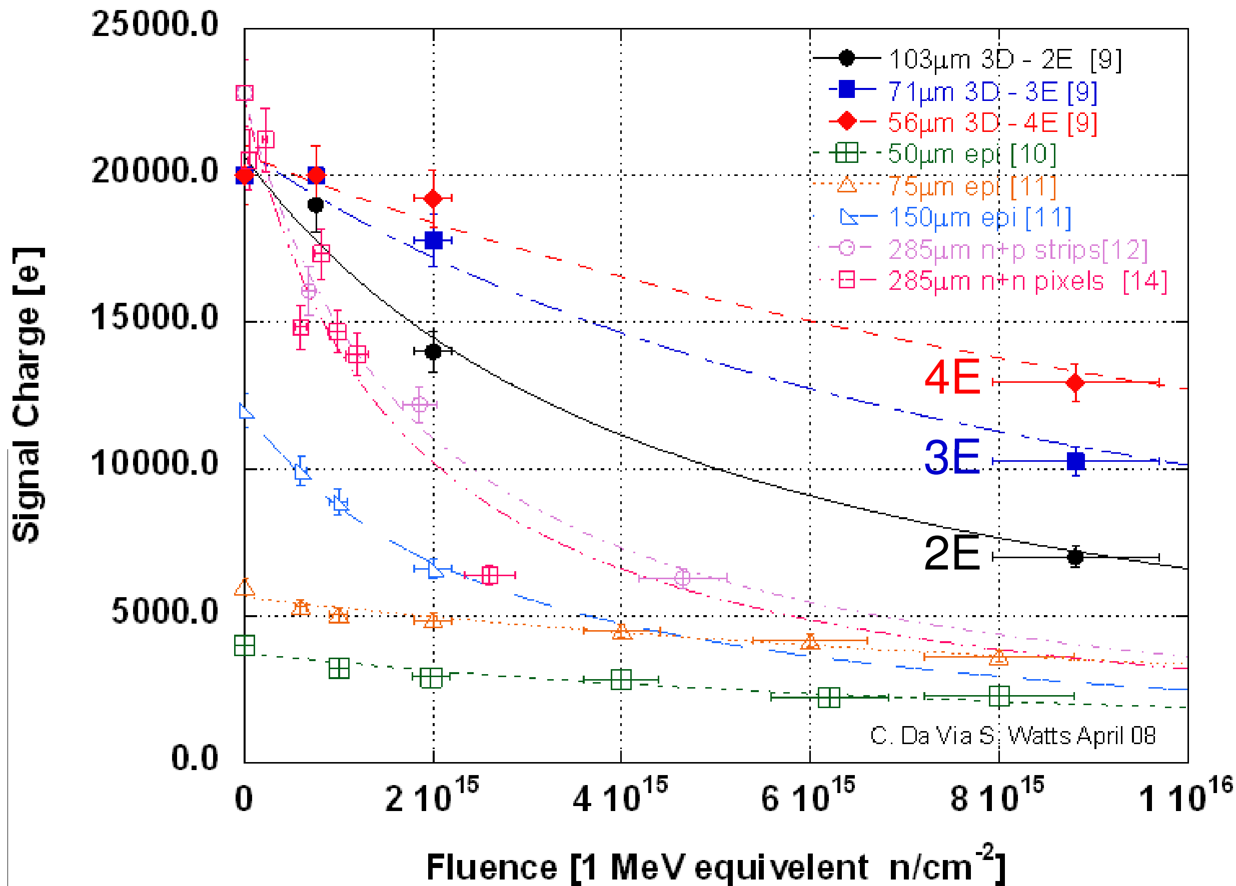


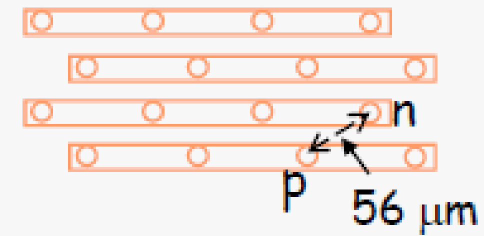


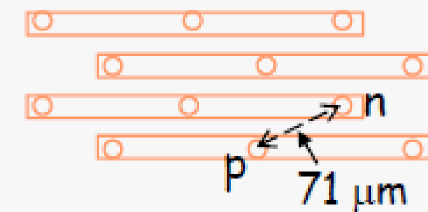
Very poor yield after Bump bonding on Atlas devices, ok for CMS devices

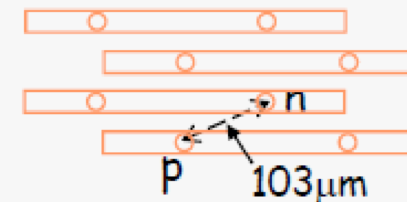
D. Bortoletto

3D Optimization







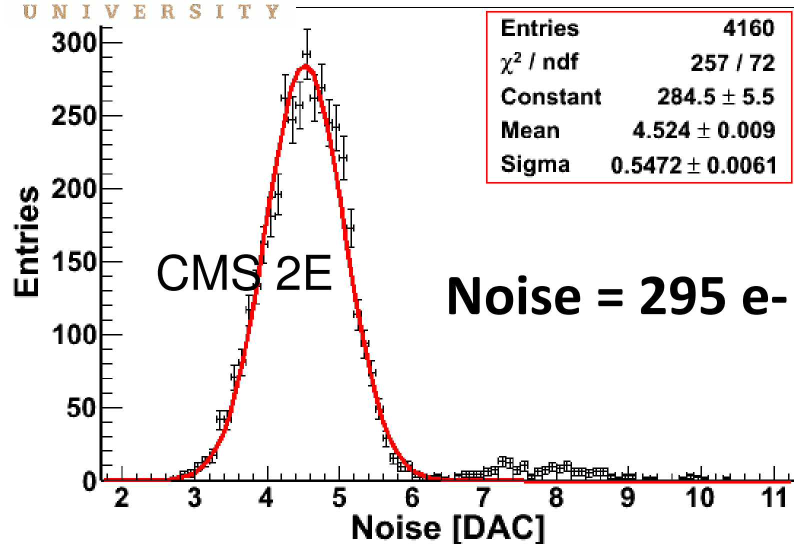


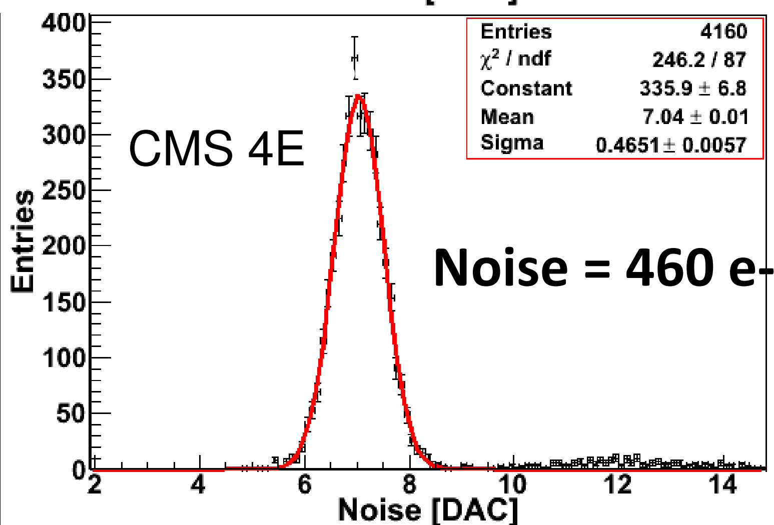
- But remember that what is important is the signal above threshold

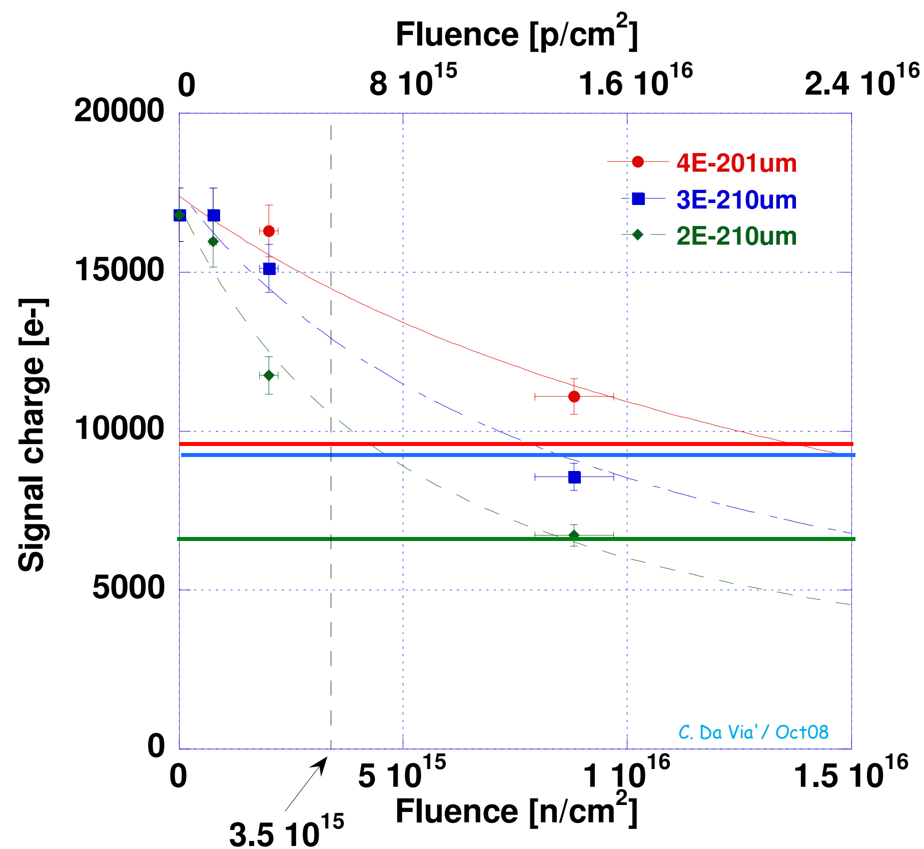
SINTEF 3D

PURDUE UNIVERSITY

Signal/Threshold optimization







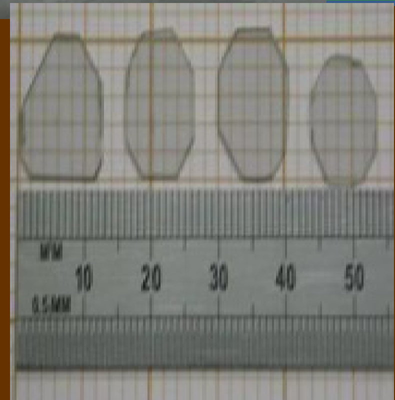
RD42: Diamond

DIAMOND DETECTORS LIMITED

- Poly crystalline and single crystal
- Competitive (to Si), used in several radiation monitor detectors
- Large band gap (x5 Si)
  - no leakage current
  - no shot noise
- Smaller ε_r (x 0.5 Si)
  - lower input capacitance
  - lower thermal and 1/f noise
- Small Z=6 →large radiation length (x2 in g/cm^2)
- Narrower Landau distribution (by 10%)
- Excellent thermal conductivity (x15)
- Large w_i (x 3.6) →smaller signal charge

- poly-CVD diamond wafers can be grown >12 cm diameter, >2 mm thickness.
- Wafer collection distance now typically 250μm (edge) to 310μm (center).
- 16 chip diamond ATLAS modules

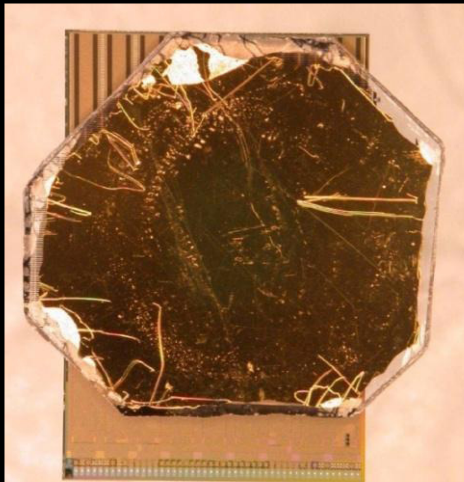
- sc-CVD sensors of few cm^2 size used as pixel detectors
- High quality scCVD diamond can collect full charge for thickness 880μm

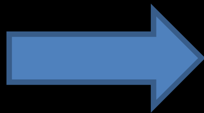


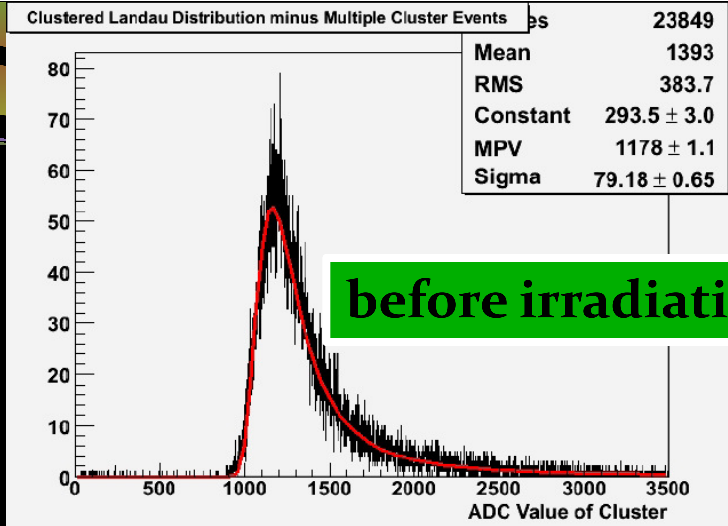
- Industrialize metallization and bump-bonding
  - Full-size ATLAS pixel module assembled by industrial partner (IZM)

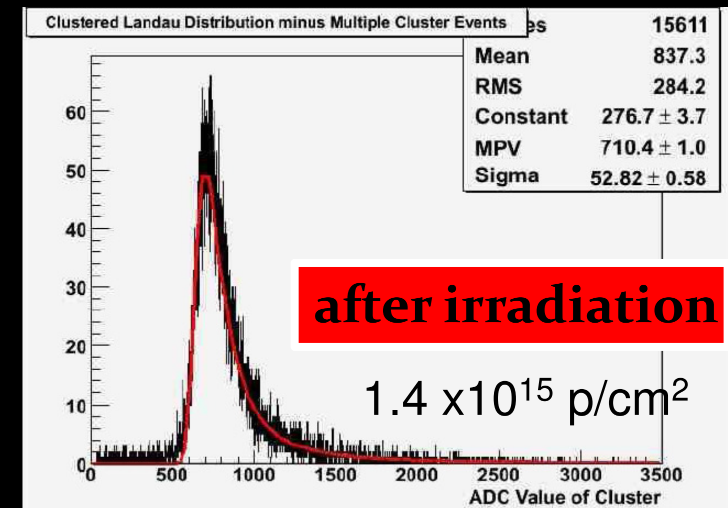
Diamond

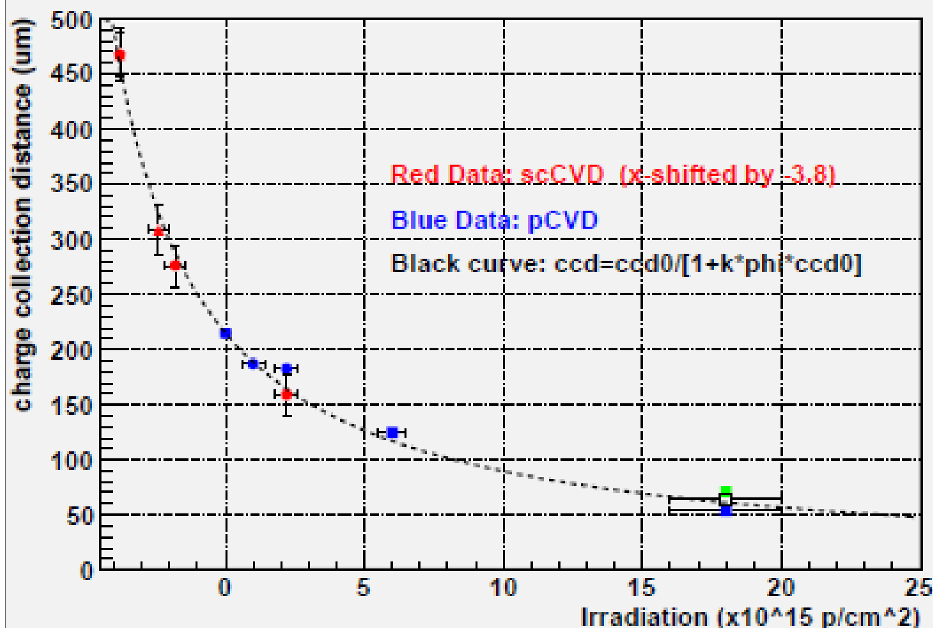
- Single crystal diamond pixel detector









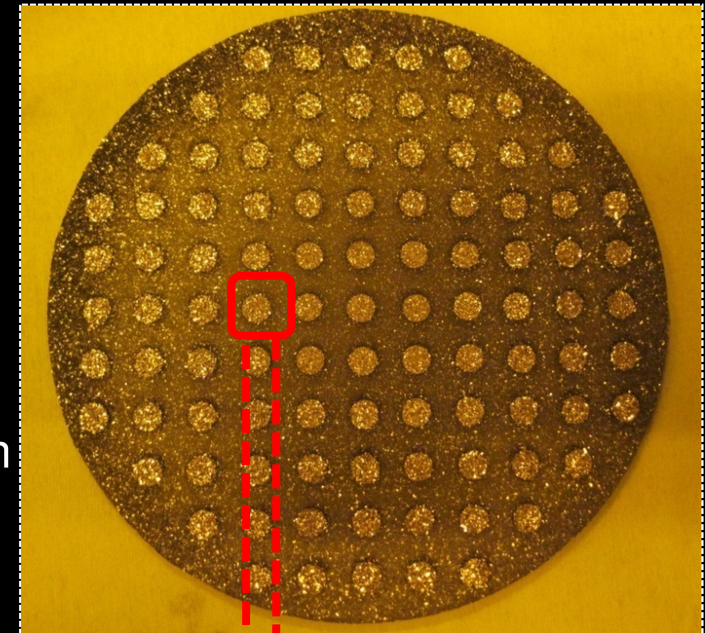


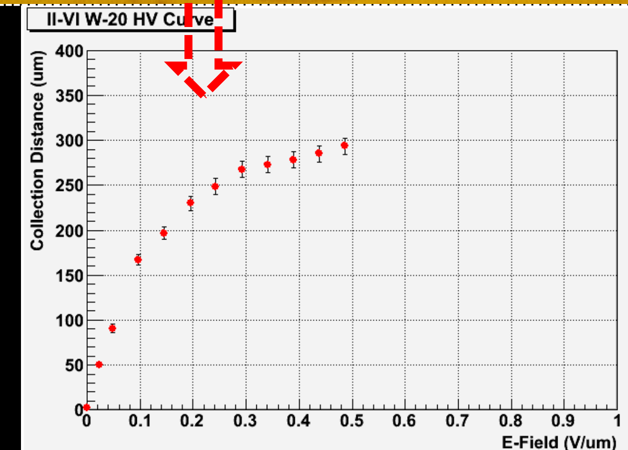
- Studies of pCVD (blue) and scCVD diamond (red) at E=1V/μm up to 1.8×10^{16} p/cm^2.
- pCVD and scCVD diamond follow the same damage curve:

$$1/ccd = 1/ccd0 + k\,\varphi.$$

Diamond vendors

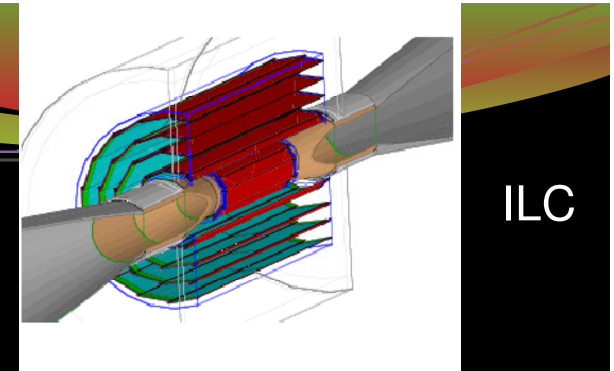
- DDL (E6) long-term supplier (pCVD and scCVD)
  - Reproducible material
  - Quote for 500 pcs (900 kGBP)
  - ATLAS-FE-I4 shaped sensors at hand 17.4 mm x 20.6 mm
  - Measured CCD between 240 and 260 µm
- New US producer II-VI Incorporated (pCVD)
  - Large company based in Saxonburg, PA
  - Interested in electronic grade diamonds to enrich their product line
  - Working closely with OSU on development for HEP
  - 300 USD/cm², 300 µm CCD, 300 µm thick
  - Spectacular CCD results
    - 300 µm at 0.5 V/µm !
- The Diamond Research Center at the National Institute of Advanced Industrial Science and Technology (AIST) in Japan has recently fabricated one-inch square Mosaic Single Crystals.
- Diamond Materials (Freiberg) and the Laboratoire d'Ingénierie des Matériaux et des Hautes Pressions (LIMHP) in Paris.



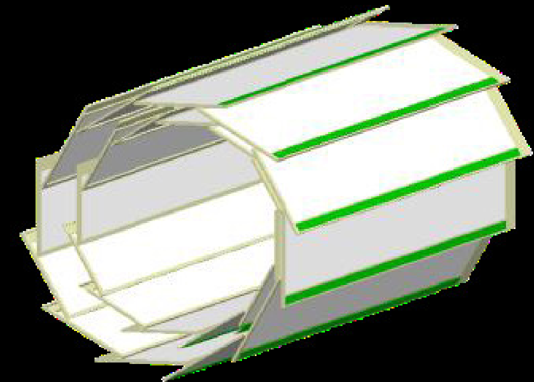


Monolithic Pixels

	LHC	ILC
Event rates	1GHz	1KHz
Beam Structure	25 ns, cont	340ns, 0.5% Duty Factor
Triggering L1 L3	40 MHz 100Hz	no hardware 15kHz → 100Hz
Radiation	10..50Mrad/year	10..50Krad/year
Resolution	10 μm	3 μm

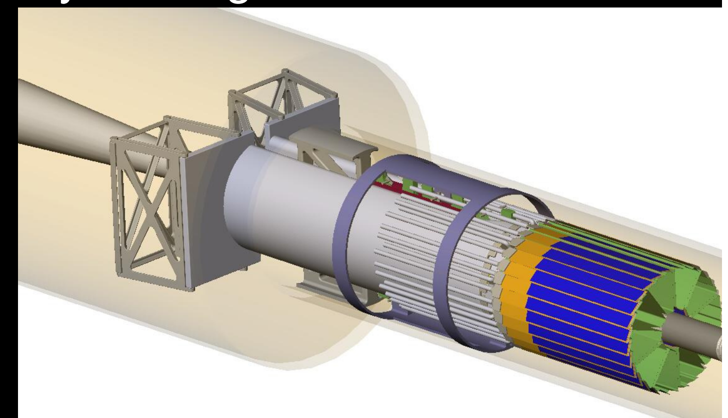


ILC



Belle New central pixel double-layer using **DEPFET**

- R&D (for ILC) ongoing for >10 years
  - DEPFET
    - recently (2008): baseline for a 2 layer detector for SuperBelle
  - Monolithic Active Pixels (MAPS-epi)
    - 2 (or 3) pixel layer detector for STAR@RHIC
    - EUDET
    - Layer 0 of the SuperB SVT
  - Monolithic Active Pixels (MAPS-SoI)



STAR Pixel upgrade (MIMOSTAR) total area: 0.16m^2

Monolithic devices

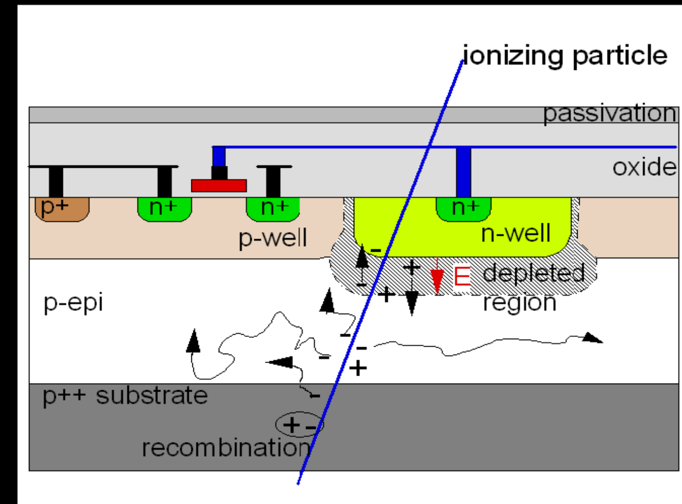
IPHC STRASBURG

ALICE

- Monolithic devices in standard deep submicron CMOS technology could yields many advantages: cost, material budget, yield, low capacitance of the collection electrode allowing very favorable power/signal-to-noise ratios

MIMOSA: 'traditional' monolithic detectors, MAPS-based with serial readout

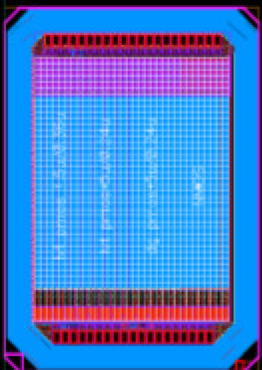
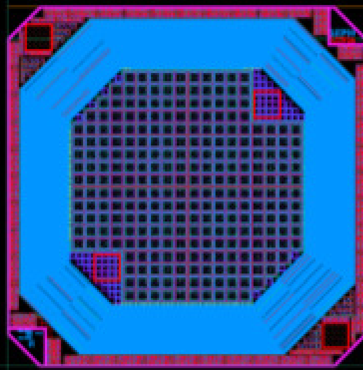
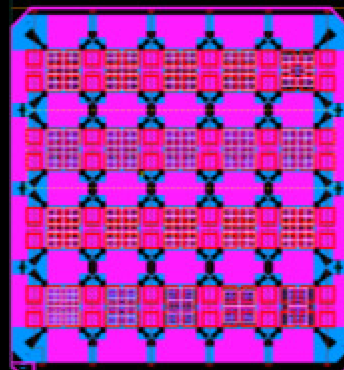
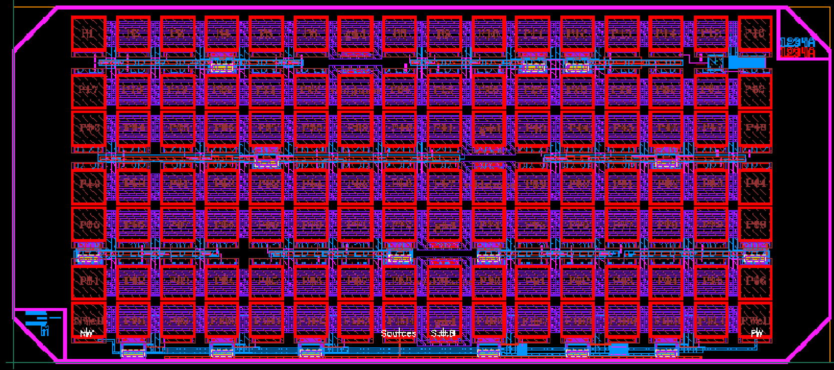
- P-type low-resistivity Si with n-type "charge collectors"
  - signal created in epitaxial layer (low doping)
  - Q ~ 80 e-h/µm → signal ≤ 1000 e^-
  - charge sensing through n-well/p-epi junction
  - Carriers propagate (thermally) to diode
- High granularity: pixel size ≤ 10 µm x10 µm
- Reduced material budget: total thickness ≤ 50 µm
- MIMOSA-22, binary output, integrated zero suppression 18.4 µ m pitch, 1152 columns x 576 rows, ~110ms readout time



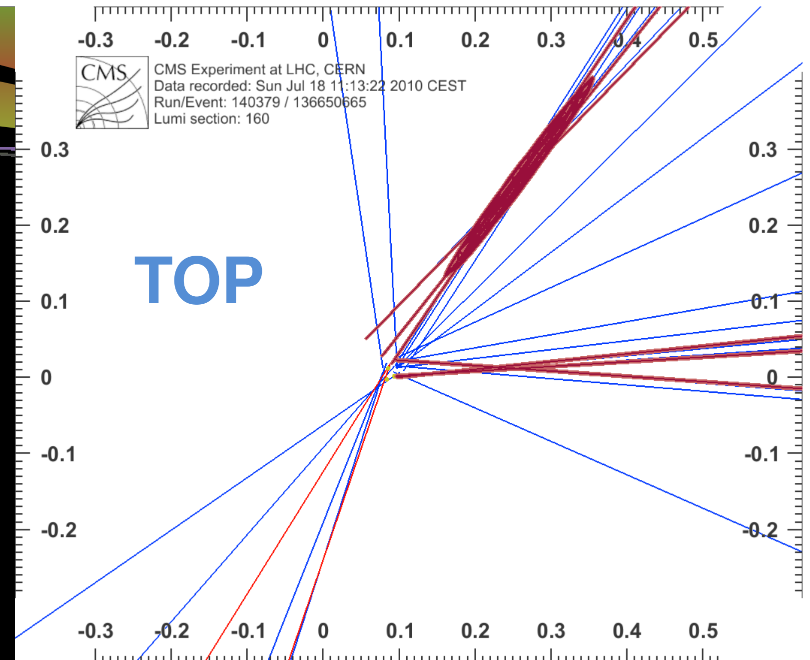
- BUT :
  - Very thin sensitive volume impact on signal magnitude (mV !)
  - Sensitive volume almost undepleted impact on radiation tolerance & speed
  - Commercial fabrication impact on sensing performances & radiation tolerance
  - N_{WELL} used for charge coll. →restricted use of P_{MOS} transistors

Monolithic Devices LePIX

- **LePix: non-standard processing on high resistivity substrate**
- Advanced CMOS deep submicron technologies (130 nm and beyond) can be implemented on ≥100 Wcm (~ 30µm depletion at 100 V)
  - Radiation hard
  - Charge collection by drift
- Low power consumption (target 20 mW/cm^{2})
- High production rate (20 m^2 per day…) and low cost per unit area (less than traditional detectors)
- High granularity
- Reduced material budget
- Prototype: test structures and matrices submission end of February 2010

Conclusions



- The construction of vertex detectors for the LHC upgrade is very challenging.
- R&D for Phase 1 is progressing well but it is important to keep in mind integration issues.
  - Material, cooling, cabling
- Warning
  - We do not have a proven solution for ultra-radiation sensors that can operate up to10^{16} neq/cm^2
  - We need ideas on how to implement pixel readout with lower thresholds
- "Ultimate goal remains a massless, cheap, infinite granularity, 100% hermetic and efficient, infinite bandwidth, long lifetime detector"

(Muenstermann, after Garcia-Sciveres)

- Further reading ICFA detector schools, previous academic training
  - Latest ICFA detector school
  - http://particulas.cnea.gov.ar/workshops/icfa/wiki/index.php/Main_Page