The Fake Sector Logic for the ATLAS Muon Trigger system

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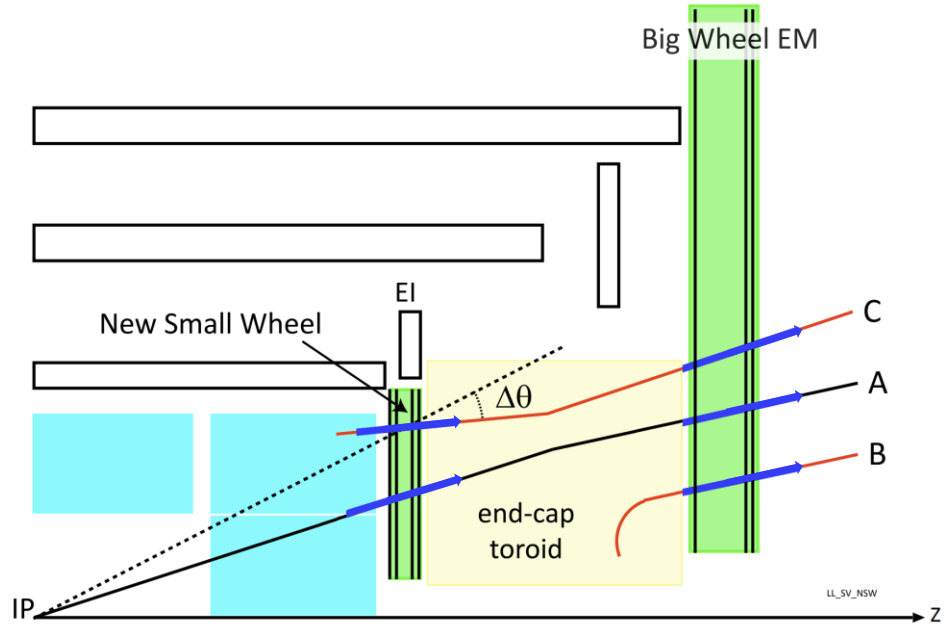
Overview of the NSW Trigger

- The New Small Wheel Trigger aims to reduce fake triggers from particles that are not high-p_T muons originating in the interaction point.
- Validates Big Wheel Trigger candidates on the Sector Logic.

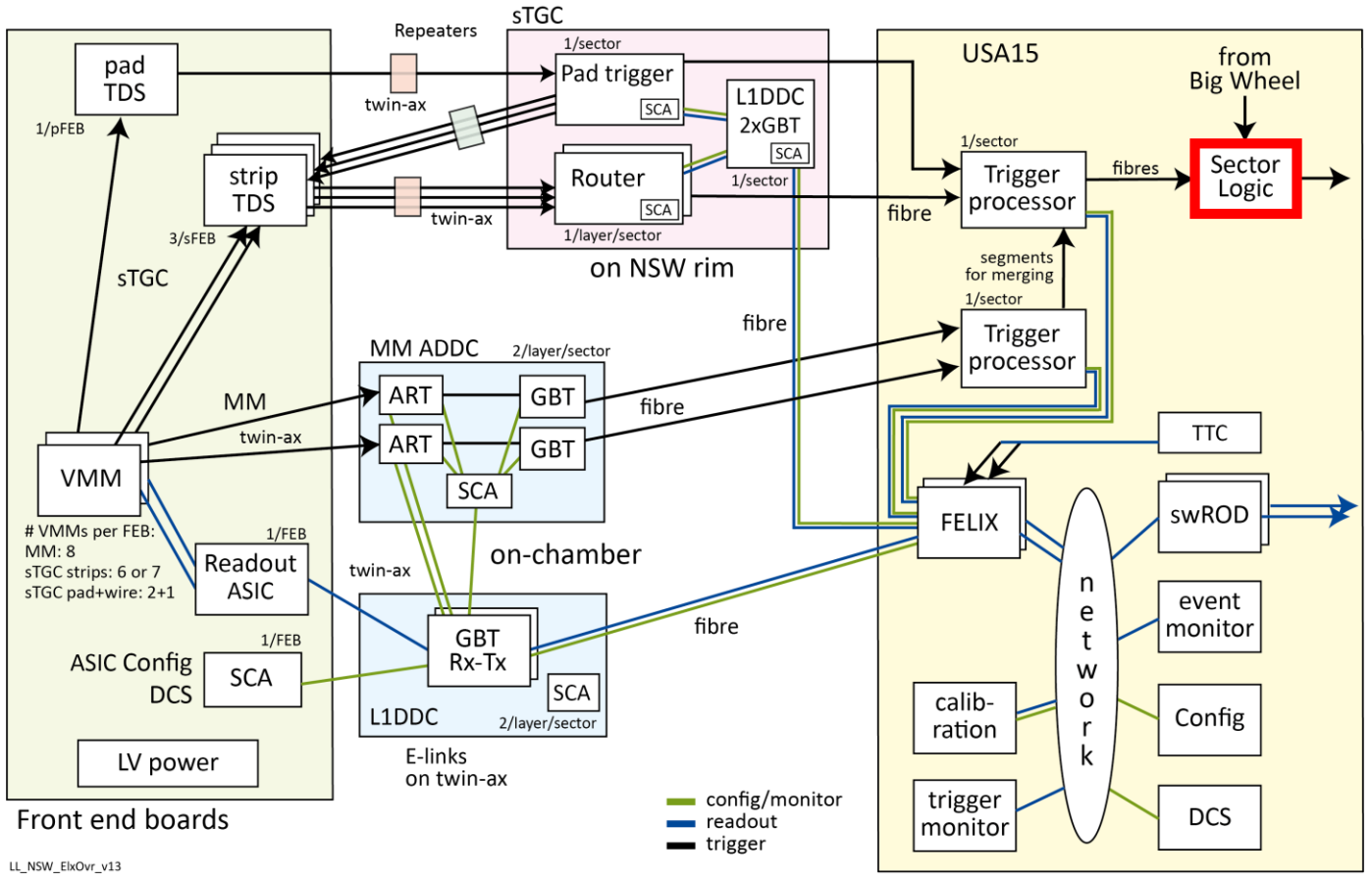
- Tracks A,B,C are accepted by the Big Wheel.
- Track C is rejected by NSW since its track does not correspond to the IP.
- Track B is rejected by NSW since it doesn't have track information.
- Track A is accepted by NSW and BW and is a valid Trigger candidate.



Schematic of the muon endcap trigger, adapted from [1]

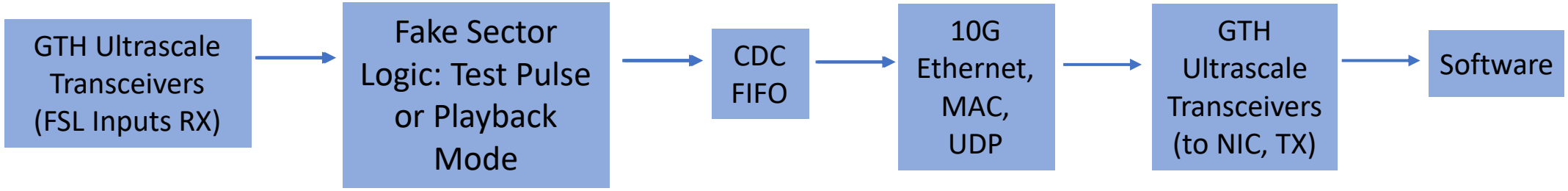
Overview of the NSW Electronics

- Data from the sTGC detector are sent to the Pad Trigger for a coincidence check.
- If data meets the conditions, it is sent to the Trigger Processor, and is merged with the MM detector data before being sent to the Sector Logic.



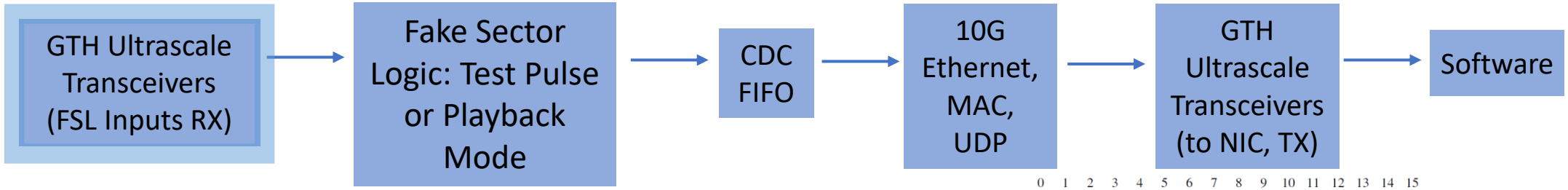
NSW Electronics overview [2]

Outline of the Fake Sector Logic

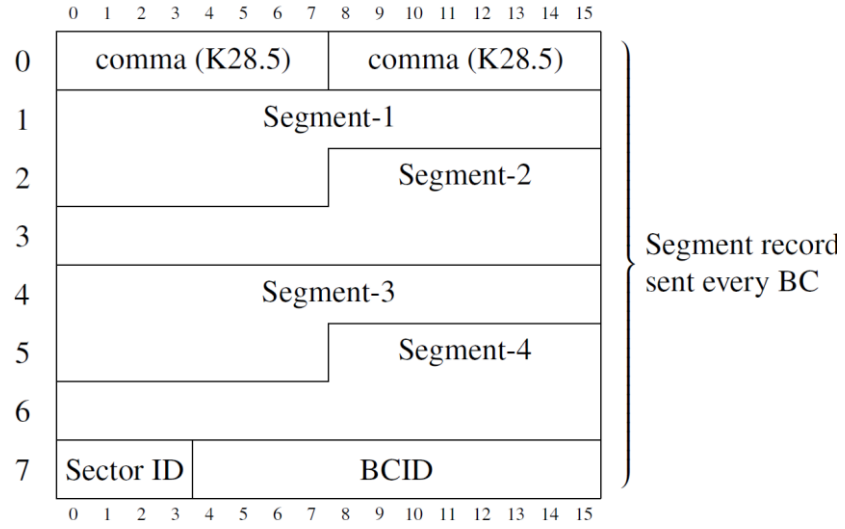


- ATLAS Work in progress.
- Inputs: Two Fibers from the Trigger Processor.
- Fake Sector Logic: processes data according to the type of measurements required as outputs.
- CDC FIFO is for Clock Domain Crossing between the 10G Ethernet Logic and the Fake Sector Logic.
- 10G Ethernet Logic transforms a part of the FPGA into a NI Card.
  - Data are packaged with headers, information, MAC address etc. to be sent to a local PC.
  - Connection is performed with optical fibers and is point-to-point connection.
- Output: One Fiber to NIC.
- Software/Scripts required to connect with FPGA, store and process data.

Inputs to Fake Sector Logic



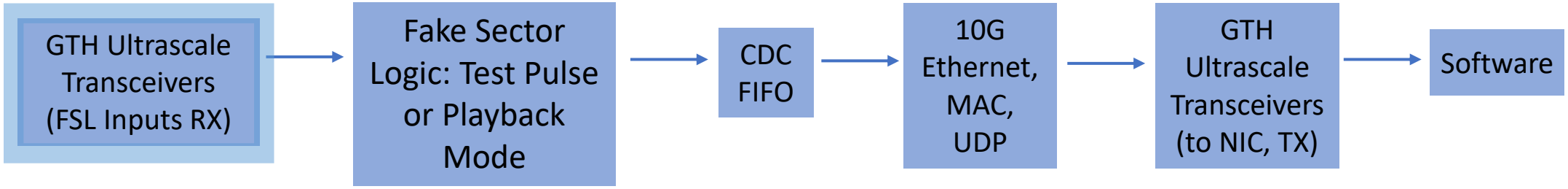
- Segment Records and the resolution and track location data they contain.
- Δθ field is the most important field for the FSL.



Data format from the NSW Trigger Processor to the Sector Logic [3]

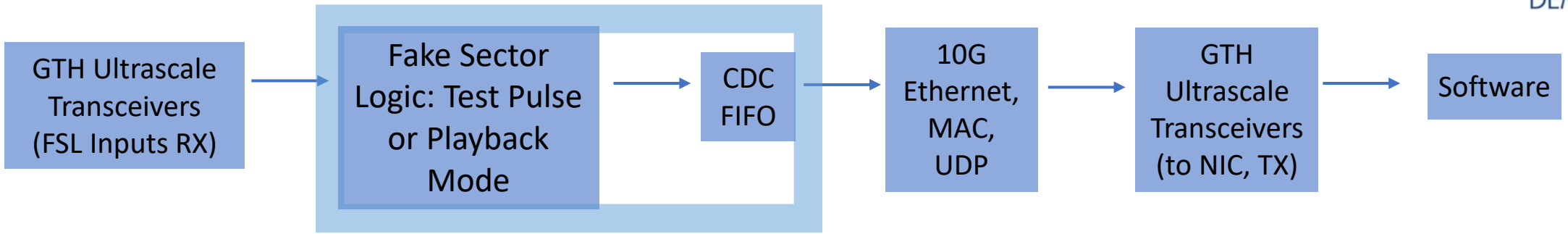
Field:	Monitor	Spare	Low Res.	Phi Res.	Δθ (mrad)	Phi Index	R Index
# of Bits	1	2	1	1	5	6	8
Stream Bit #	23	22:21	20	19	18:14	13:8	7:0

Inputs to Fake Sector Logic



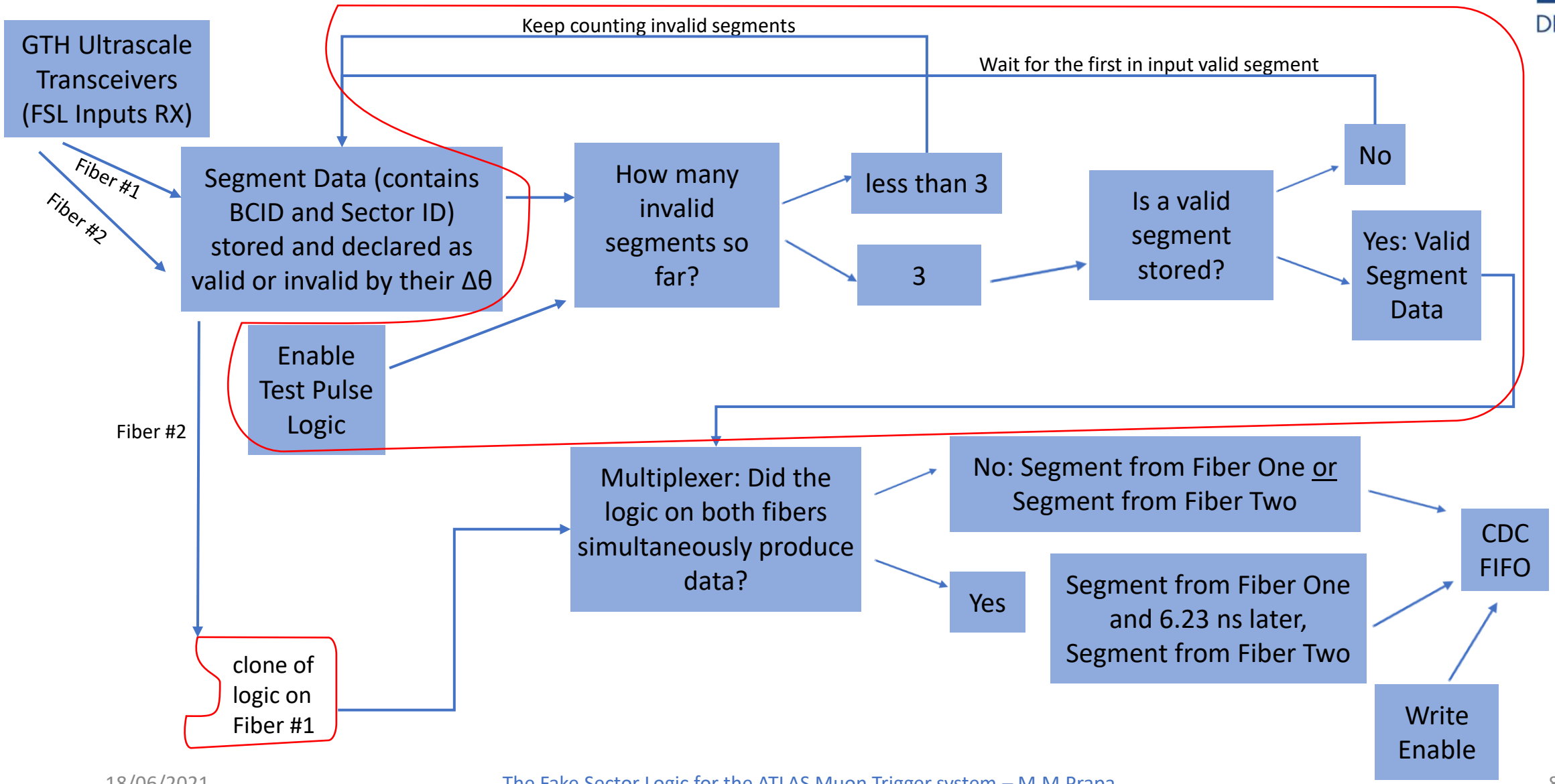
- In testing sessions, segment inputs come in two different forms:
  - Test Pulse Mode: 1 segment record packet containing 4 valid segments comes in per 3563 segment record packets or one orbit. The rest of the packets are empty or invalid.
  - Playback Mode: segment record packet contents change per second. Regardless of the segment content, the same segment record packet will be input for 1s before changing to a different packet.

Fake Sector Logic

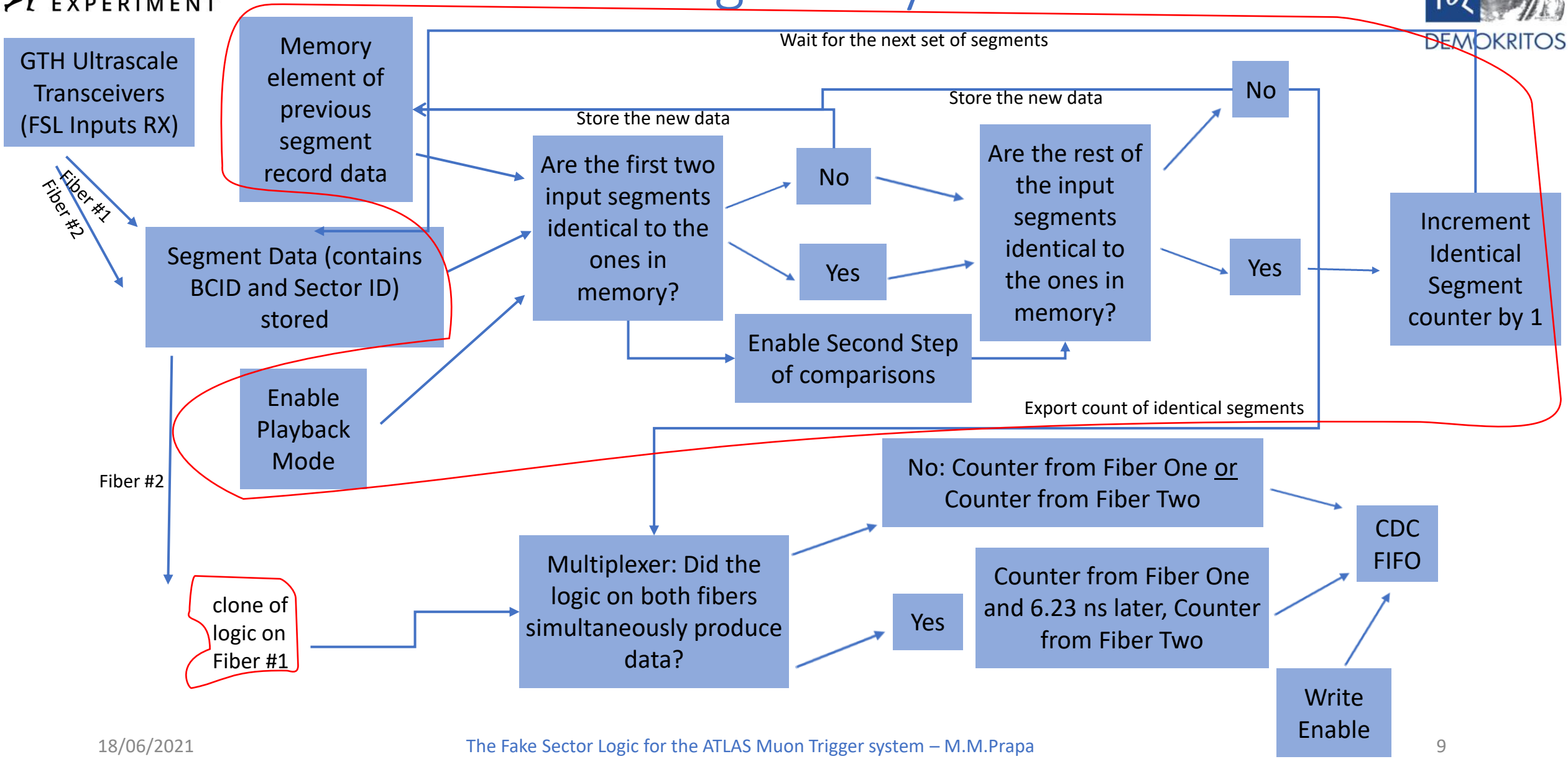


- Data from the Receivers is stored and processed based on the selected mode as well as their content.
- Invalid segments are identified and counted prior to data propagated to the architecture branch that is defined by the selected mode.
- The storage process, the CDC FIFO and the multiplexer logic are shared between the two modes.
- Each mode features a different method to produce the requested outputs.

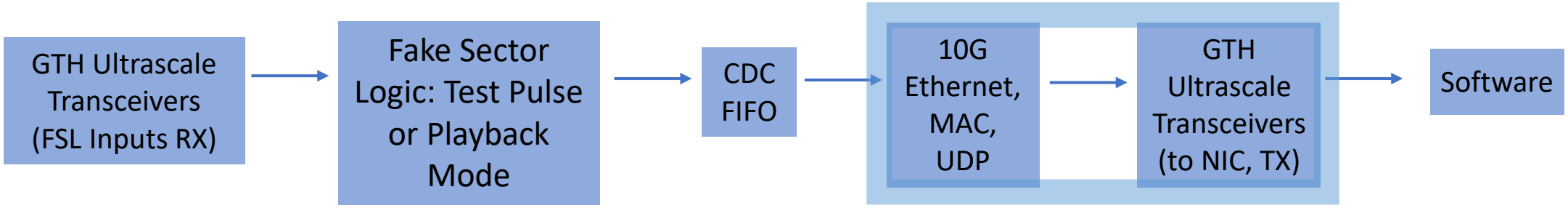
Fake Sector Logic: Test Pulse Mode



Fake Sector Logic: Playback Mode



10G Ethernet



64-1518 Bytes

Number of Bytes	7	1	6	6	2	0-1500	0-46	4
Content	Preamble	SFD	Destination Address	Source Address	Length/Type	Data	Pad	FCS

Standard Ethernet Frame Format as per the IEEE 802.3 Standard

- The 10G Ethernet uses IP components, to package and export data using the UDP protocol.
- While data arriving back-to-back will be processed concurrently, headers and packaging of each data packet are performed sequentially.
- This design was created based on an 1G Ethernet project and complies to the IEEE 802.3 standard for 10G Ethernet.

Summary

- Architectures have been tested and perform as always expected; any corruption of data halts the logic, until problems are resolved. Such problems usually require some minimum user intervention, like a reset.
- All results produced from this design can be processed further using software methods.
- Development using best design practices, makes full usage of the Ultrascale device functionalities, keeps resource utilization as minimum as possible and is easy to maintain, debug or modify for production of additional data.

…any questions?

References

[1]: Trigger Processor Design Review Report, The NSW Trigger Processor Working Group, ATLAS Note, 2018

[2]: Image made by Lorne Levinson, for the ATLAS NSW Trigger Processor group

[3]:New Small Wheel Trigger Processor Firmware Requirements & Implementation, NSW Trigger Processor Group, ATLAS Note, 2019