# Operational experience of the CMS Tracker

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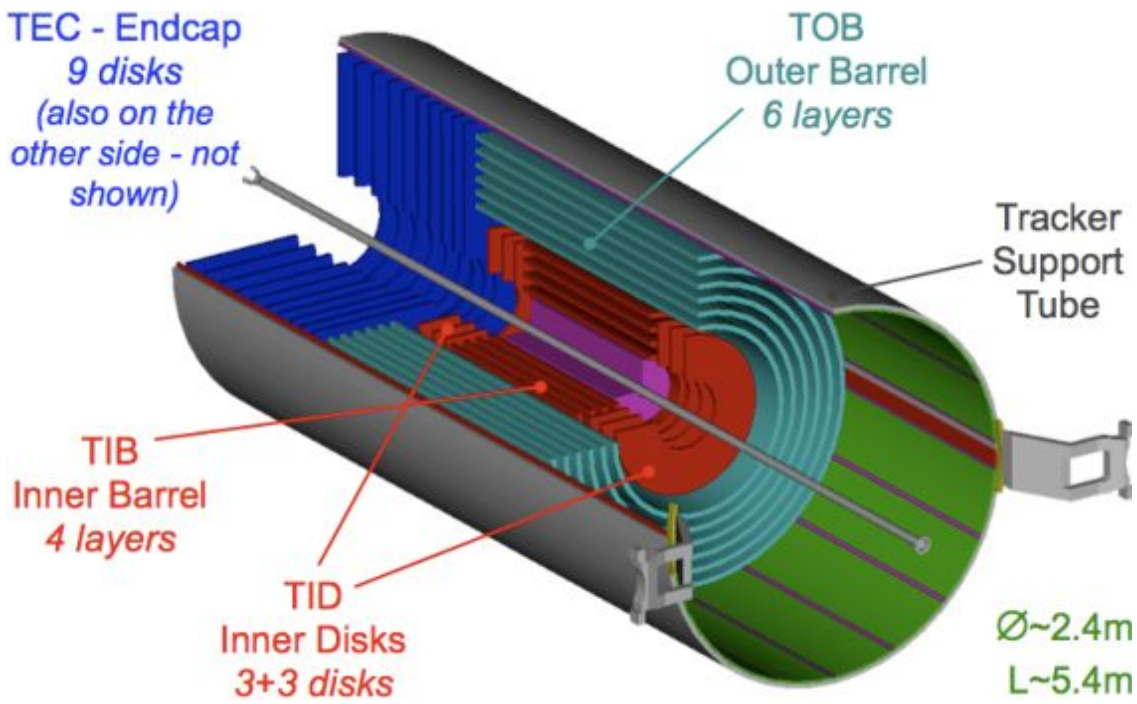
**Vertex 2021**

27th September 2021

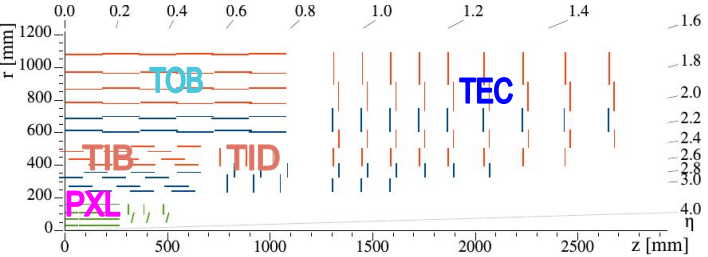

# The CMS Tracker

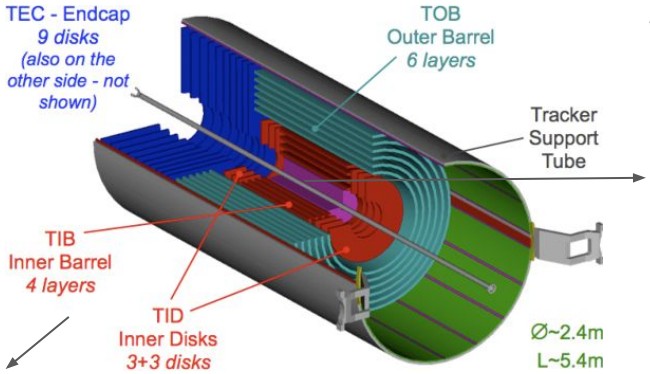
- Largest silicon tracker ever built.
- ~200 $m^2$ active material
- 5.6 m length, 2.5 m diameter
- $|\eta| < 2.5$ acceptance



# The CMS Tracker

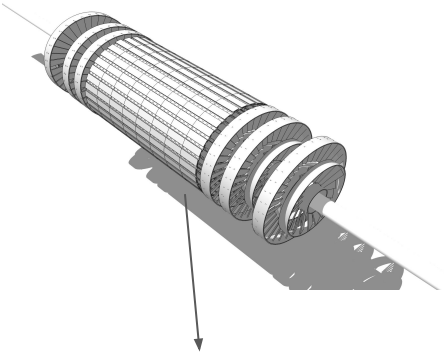
## Outer Tracker (Strip Tracker)

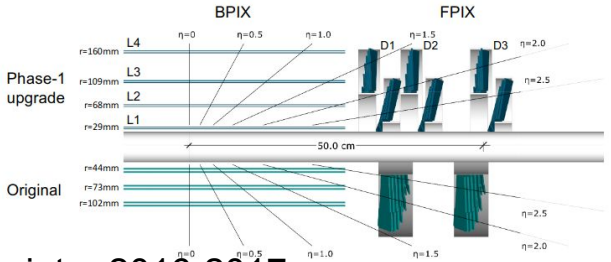



- Inner Barrel (TIB) : 4 layers
- Inner Disks (TID): 3(x2) disks
- Outer Barrel (TOB): 6 layers
- EndCap (TEC) : 9 (x2) disks
- Stereo module: 4 layers (3 rings) in Barrel (Endcap)

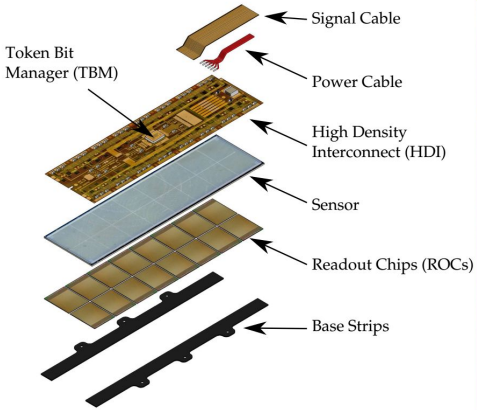
## Inner Tracker (Pixel Detector)

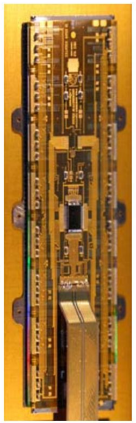





- Installed in winter 2016-2017
- Barrel : 4 layers (BPix)
- Endcap: 3 (x2) disks (FPix)
- Layer-1 closer to IP
- 4 hit coverage up to $|\eta| < 3$
- **Newest Layer 1 Installed during LS2 (2021)**

# Readout of the Pixel Detector




- Same as Phase 0 (2009- 2016) detector

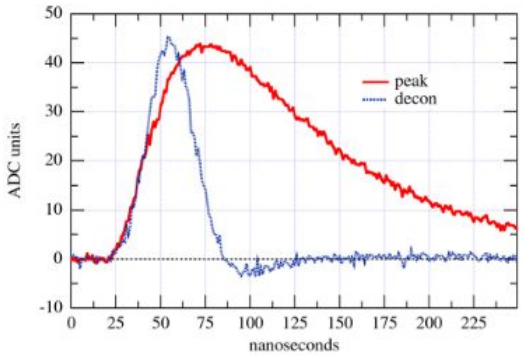
- **PSI46dig**
  - Same architecture as Phase 0
  - Digital readout and double column drain
  - **>90% efficiency up to 400MHz hit rate**
- **PROC600**
  - Dedicated for Layer 1
  - Dynamic cluster drain
  - **>90% efficiency up to 600MHz hit rate**

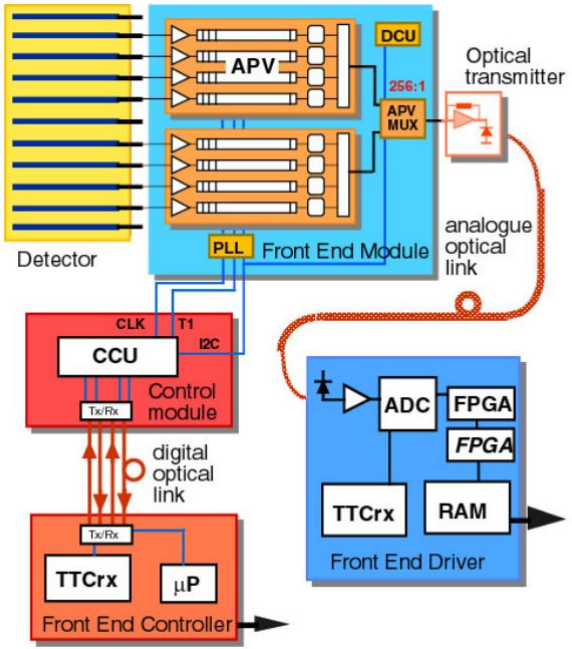
- **New digital TBM**
  - Old: 40MHz analog coding
  - New: **160Mbit/s digital**
- Module out-bound data stream: **400Mbit/s**

# Readout of the Strip Tracker

**APV25 Chips:** Analog readout

- 0.25 $\mu$m, 128 channels each with
  - Pre-amplifier, 50 ns CR-RC shaper, 192 cell analog pipeline
- Readout can be in two modes
  - **Peak mode** - one sample corresponding to the peak voltage of CR-RC shaper
  - **Deconvolution mode** - weighted sum of three consecutive samples
- Signals from APV25 chips are multiplexed by the APVMUX and sent to the laser drivers
- Analog to optical conversion happens on the Analog-optohybrid (AOH)
- Optical signal eventually transferred to off-detector readout electronics



# Operational Challenges of the Pixel Detector

## Crosstalk

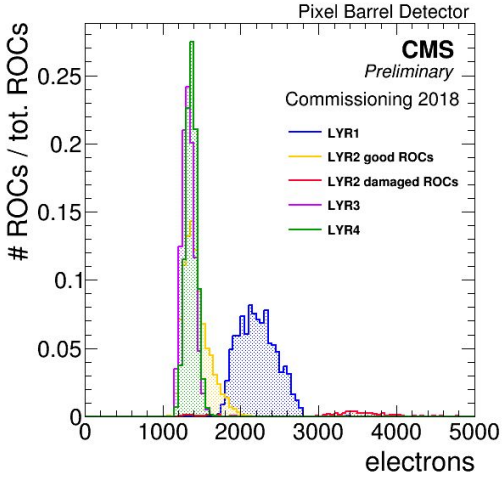
- Layer 1 has higher threshold than expected, mainly due to electronics crosstalk.
- **Problem addressed in the new version of PROC600v4.**

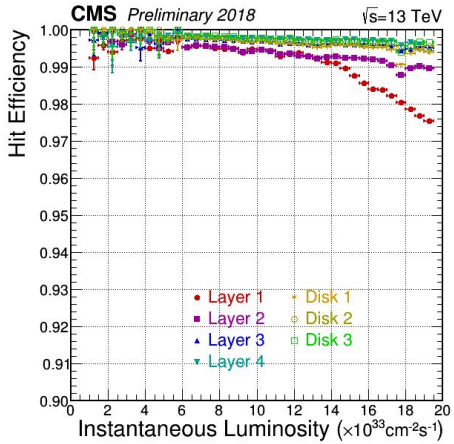
## Dynamic Inefficiency

- Hits are stored in chip periphery
  - timestamp- timestamp buffer
  - data - data buffer
- Due to a glitch we lose synchronization between data and time, leading to loss of data.
- **Problem addressed in the new PROC600v4.**

## DCDC converters failure

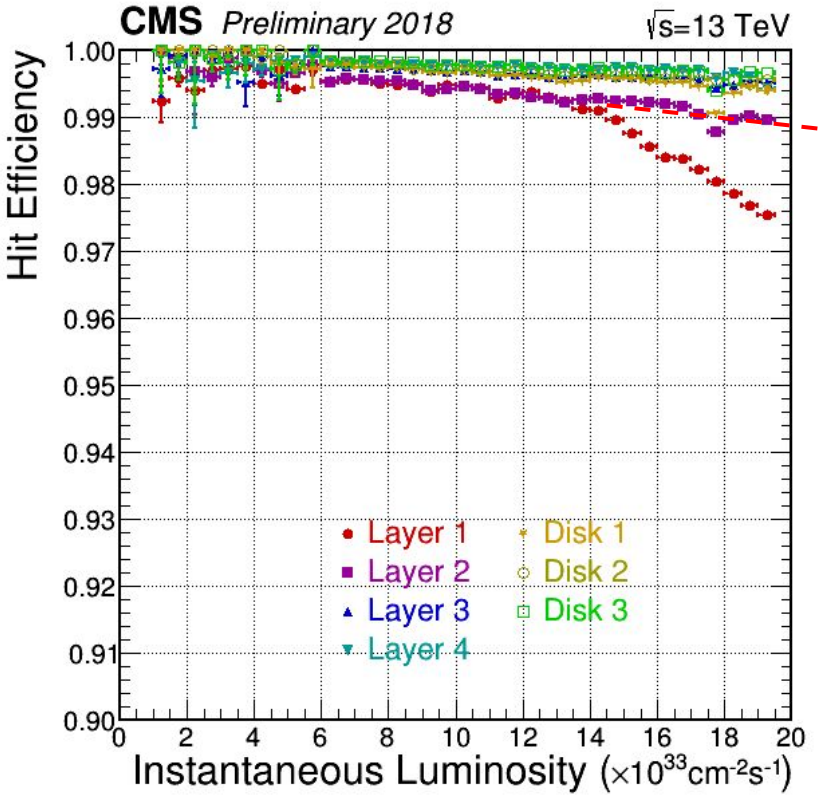
- Resulted from a fault in the **FEAST** chip design.
- **Impact on Run 2** - 5% DCDC converter not working, 11% detector fraction inactive.
- **New production of DCDC converters with new version of FEAST chips for Run 3.**



# Performance - Pixel Detector

## Hit efficiency

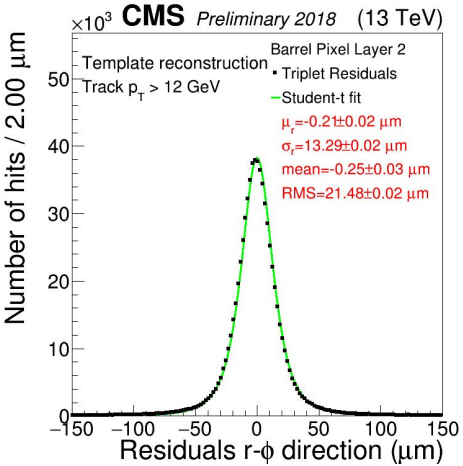


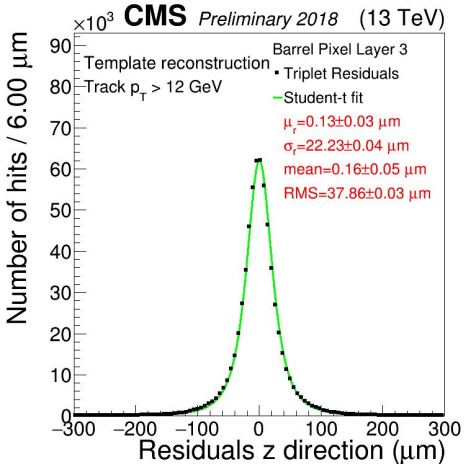

expected new Layer-1

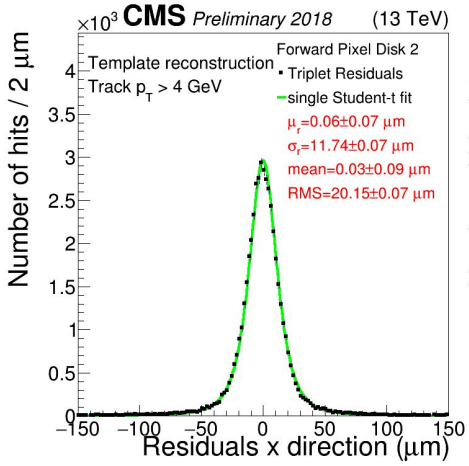
- Overall excellent efficiency from Phase-1 Pixel detector.
- We have now a new Layer-1 which will improve performance substantially.

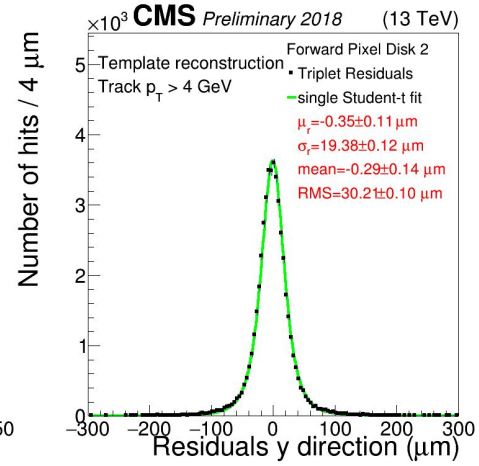
# Performance - Pixel Detector

## Residuals/Resolutions




Resolution in r-Φ: 13 $\mu$m

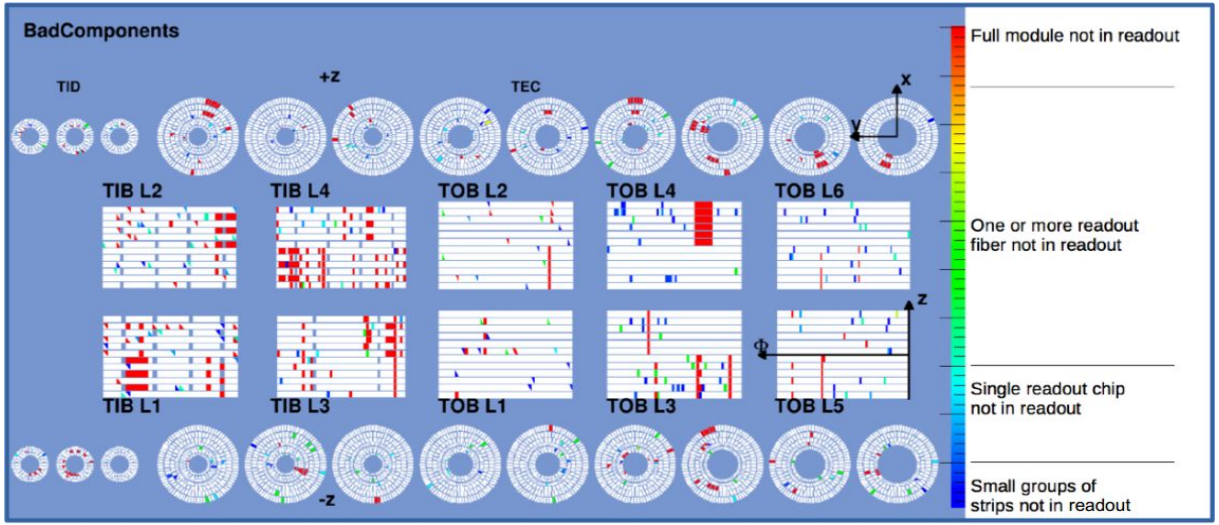
Resolution in z: 22 $\mu$m

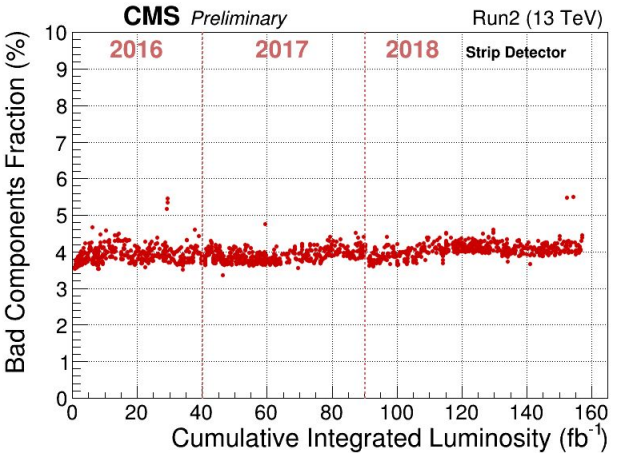
Resolution in x: 12 $\mu$m

Resolution in y : 19 $\mu$m

**Excellent resolution both in the barrel and the forward pixel.**

# Status of the Strips Tracker

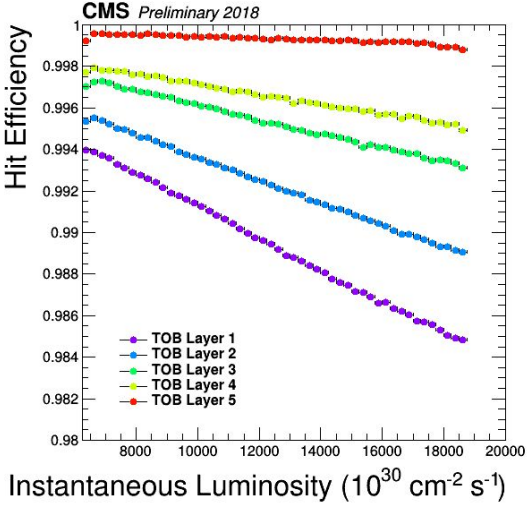


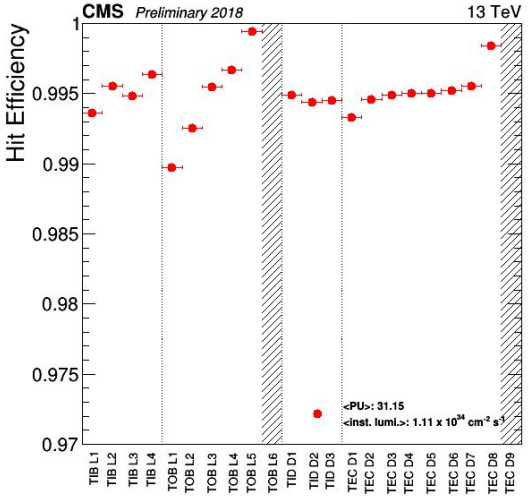



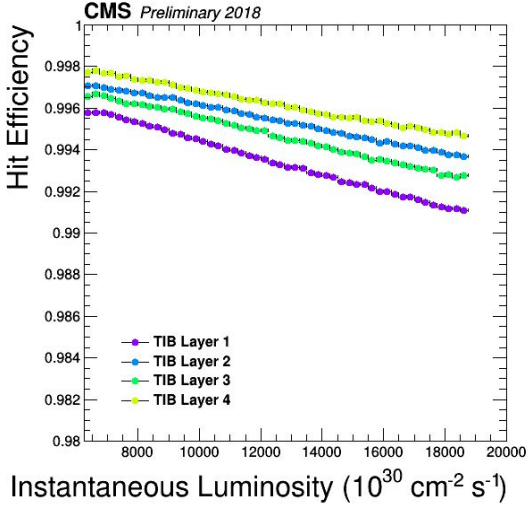

- Fraction of active components **~96 %** in Run 2.
- Bad components include:
  - Read-out channels excluded from the cabling (typically FEDs)
  - Unpowered groups of modules
  - Single APV25 chip or groups of strips masked from the offline reconstruction by a Prompt Calibration Loop algorithm (noisy channels)
- **Active fraction has not changed since then.**

# Performance - Strips Tracker

## Hit Efficiency



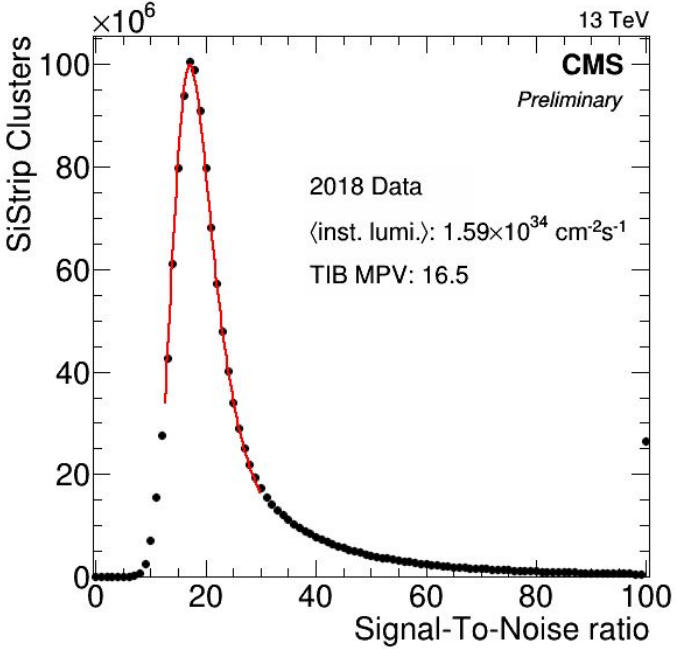



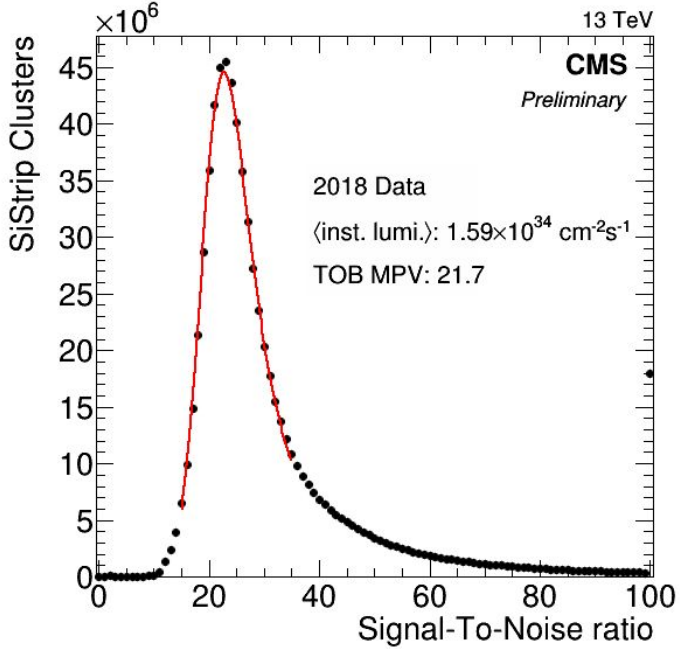




- Hit Efficiency still > 98%  at the highest instantaneous luminosity.
- The efficiency varies linearly with the instantaneous luminosity and is layer dependant.

# Performance - Strips Tracker

## Signal to Noise Ratio



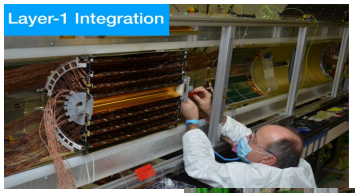

| | TIB | TOB | TID | TEC (thin) | TEC(thick) |
|---|---|---|---|---|---|
| **2018 - ∫Ldt= 11.5 fb$^{-1}$** | 16.5 | 21.7 | 16.0 | 16.9 | 21.8 |

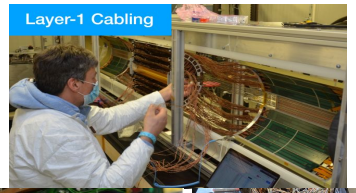
**High signal to noise ratio**

# Refurbishment, Re-installation and Commissioning

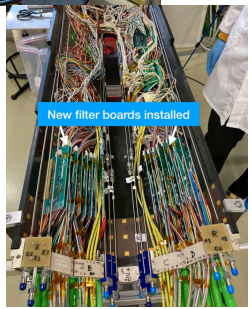
## Pixel

- BPix
  - New Layer-1 with **PROC600v4** readout chip, new TBM (**TBM10d**), new HDI design.
  - Replacement of accessible DCDC-damaged modules in Layer-2.
  - Installation of new DCDC converters (with FEAST v2.3).
- FPix
  - Fixing broken cooling pipes with custom **VCR fitting**.
  - Installation of new DCDC converters.
  - Fixing of broken FED fibre bundle.
  - Replacement of filter boards.
  - Replacement of DCDC converter cooling bridges.






## Strip

- No structural changes.
- Refurbishment of dry gas distribution racks.
- New membranes installed on membrane plant.
- Refurbishment of dry air system for better dew points.

**Pixel was re-installed in June 2021!!**

# Summary

- The CMS Tracker has performed well.
  - Signal-to-noise and hit efficiency for outer tracker are very good and in agreement with expectation.
  - Excellent position resolution and hit efficiency for pixel detector in 2018.
- Pixel detector has new Layer 1, installed and fully commissioned for Run 3.
- Strip tracker remained structurally same as Run 2, the only difference being the operational temperature which changed from -20°C to -25°C, to mitigate radiation damage.
- Expecting excellent performance for Run 3.

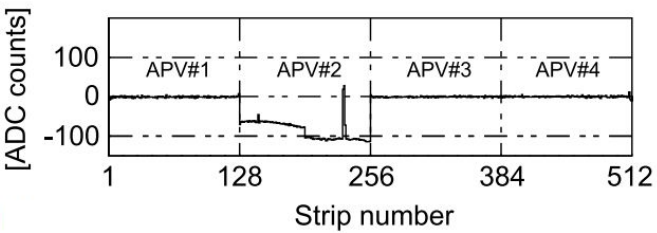
# Thank You!!!!

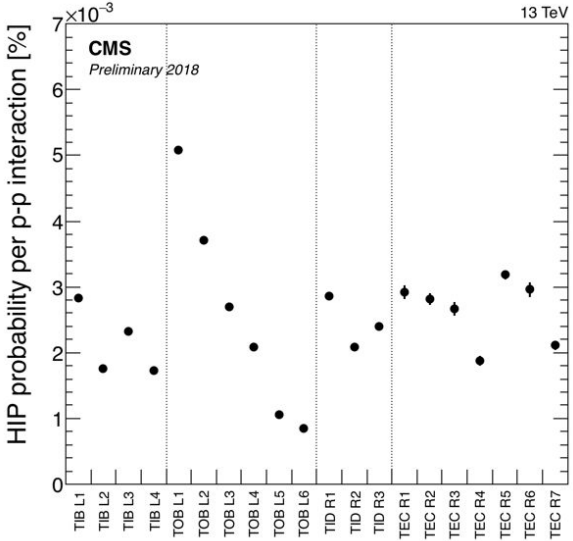
# Back up

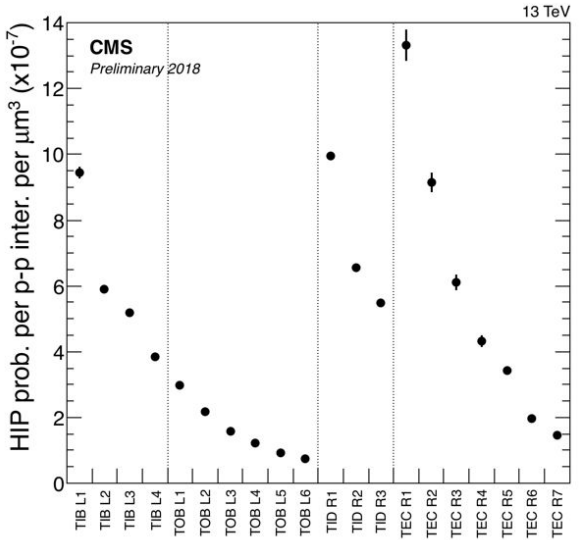
# Operational Challenges of the Strip Tracker

## Highly Ionizing Particles (HIP)

- Inelastic hardronic interactions between incident particle and silicon sensors create HIPs.
- An order of ~1000 times larger energy deposition than a MIP.
- Energy is deposited among few APV strips causes the APV baseline to drop.
- APV becomes insensitive to MIPs  and baseline recovery may take several BXs.
- Leads to the loss of efficiency.



# Operational Challenges of the Pixel Detector

## DCDC converters

- Resulted from the fault in the **FEAST** chip design.
- In disable state, charge build up on the circuit due to irradiation(>10kGy) caused the circuit to break.
- The problem wasn't understood until **Mid 2018.**

| May 2017 | 5th Oct 2017 | Dec. 2017 | YETS 2017/2018 | May. 2018 |
|---|---|---|---|---|
| Phase 1 upgrade done 96.6 % active detector | 1st DCDC converter Broke | 5% converters not working, 11% detector not working | Detector extracted, Replaced all DCDC with bigger fuse,problem not understood yet | Problem reproduced at lab (irad, xray), reason known |

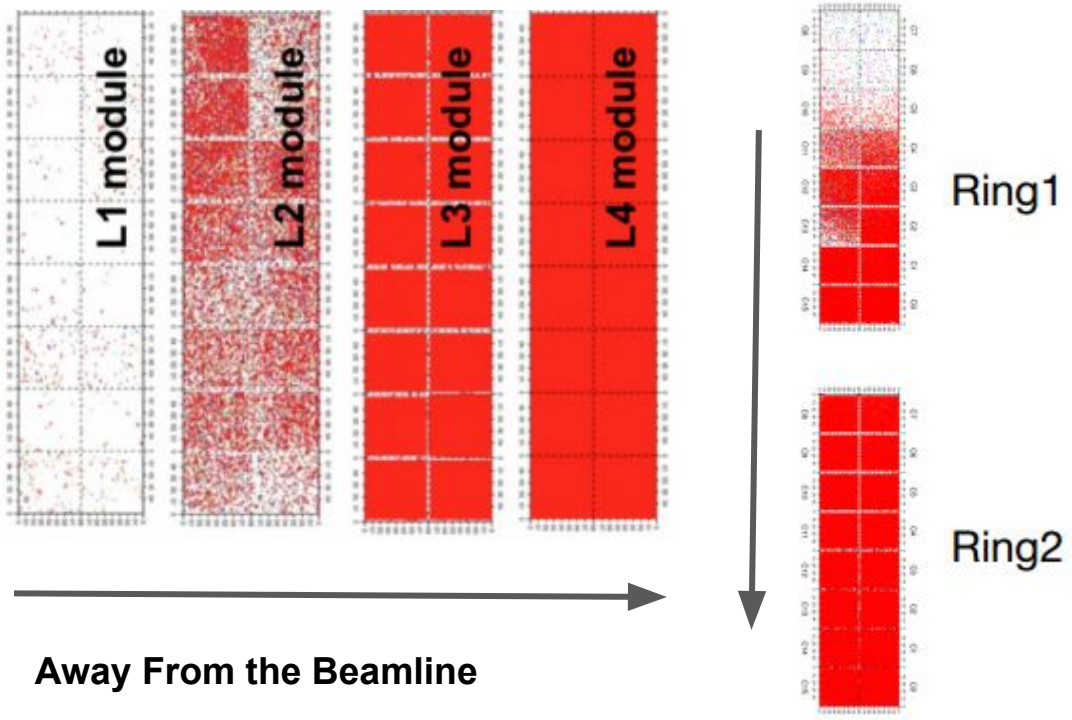
**Impact on operations (2018)**

- Converters not used to power cycle during run, stuck TBM accumulated.
- Power supplies (CAEN) used to power cycle in between beams.
- High current trips in power groups with higher share of modules.
- Raised trip limits, programmed to reduce start up current in power groups.
- Selective disabling of a few DCDC converters to prevent trips.

# Operational Challenges of the Pixel Detector

## DCDC damaged modules

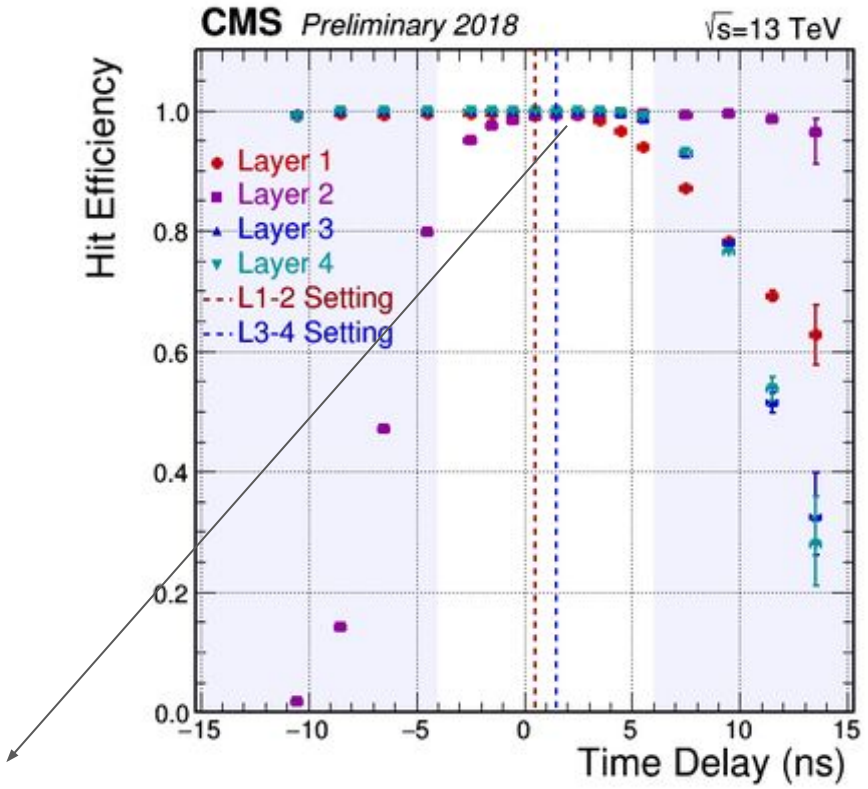
- DCDC damaged modules were not correctly powered.
- Sensor leakage current cannot be drained efficiently if the ROC is not powered.
- With Bias voltage **(HV) ON** and module power power (LV) **OFF** leads to bad grounding.
- The leakage current is **drained** through the pre-amplifier,**damaging the pre-amplifier and the module.**
- The damage seem to be accumulates radiation and **distance from beamline**.
- **6 (accessible) Layer-1 modules replaced during 2017-18 YETS out of total 8 damaged modules in Layer-1**
- **Accessible DCDC-damaged modules in Layer-2, were replaced during LS2.**



# Operational Challenges of the Pixel Detector

## Pixel Timing Problem

- Layer 1 ROC is shifted by ~12ns with respect to layer 2-4 ROC -> PROC600 is faster than PSIdigv2.
- Layers 1 and 2 are on the **same clockline** and have the same timing shift. ( same delay 25 chip)
- No adjustable delay between Layer 1 and 2 and leads to sub-optimal performance in terms of efficiency and resolution.
- **The New TBM (TBM10d) of the new Layer 1, solves this problem.**
  - Has a delay register that can delay the clock by 32 - 1 ns steps.
  - **An additional, adjustable delay between Layer 1 and 2.**

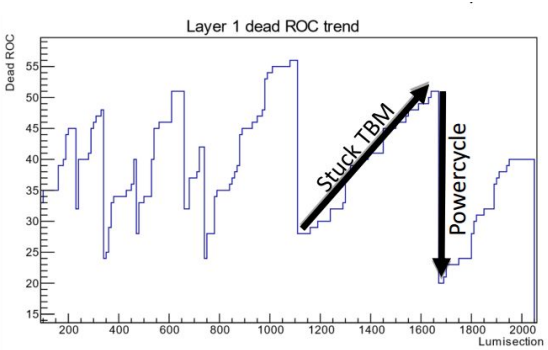



**On the edge for Layer 1+2**

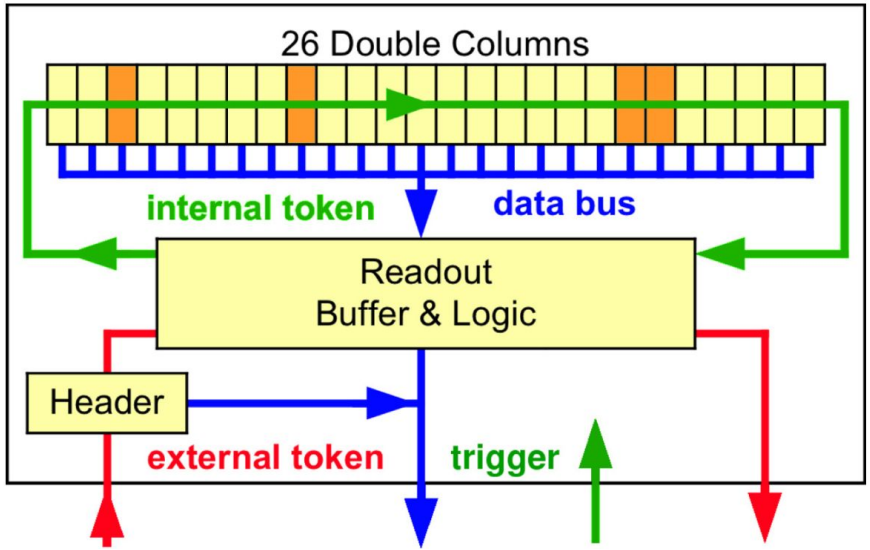
# Operational Challenges of the Pixel Detector

## Stuck TBMs

- 30 (SEUs)/fb$^{-1}$ in L1 transistor in TBM latch sets TBM to 'no readout' mode: "**Stuck TBMs".**
- This leads to the loss of data.
- The only way to recover this is through a **power cycle.**




- **New TBM for Layer 1 (TBM 10d) solves this problem**
  - **Reset of the TBM is possible in the new Layer 1**




- After receiving the L1A signal TBM orchestrated the readout of data from all the Readout chips.
- Sends it to the FED eventually.
- It is affected by SEU's **(Single Event Upsets)**