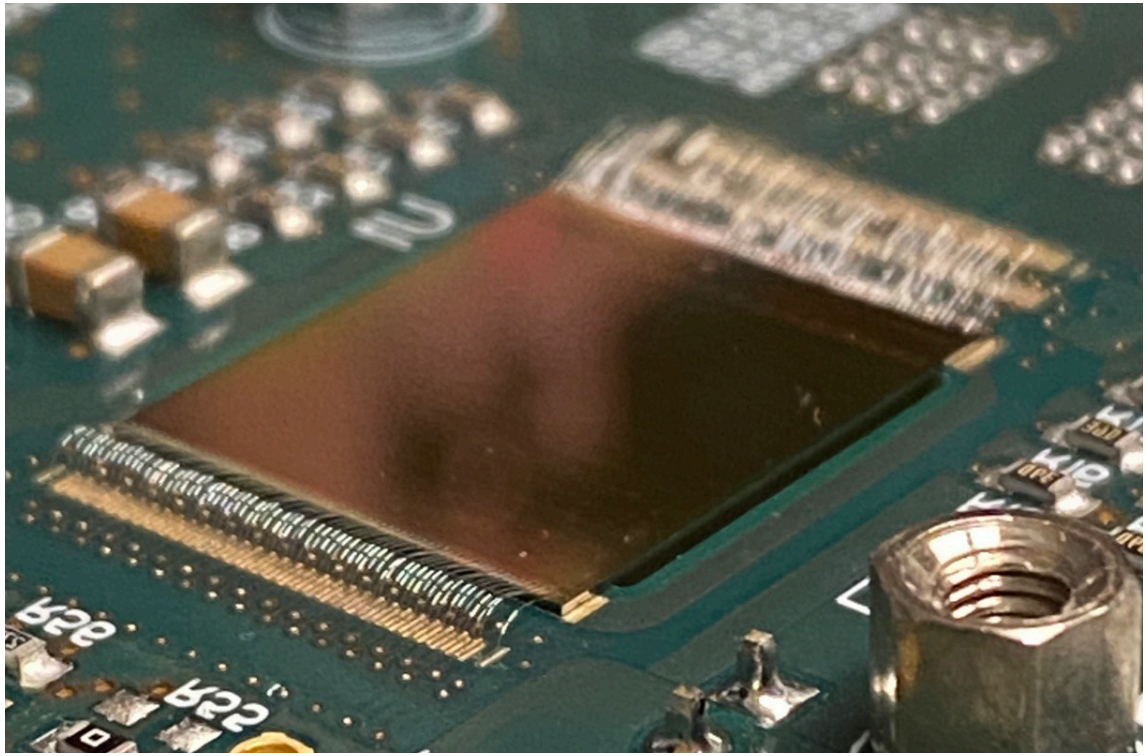
Istituto Nazionale di Fisica Nucleare

ARCADIA

ARCADIA: technology platform and system-grade demonstrator architecture



Vertex 2021

Oxford, UK (Virtual)

September 29th, 2020

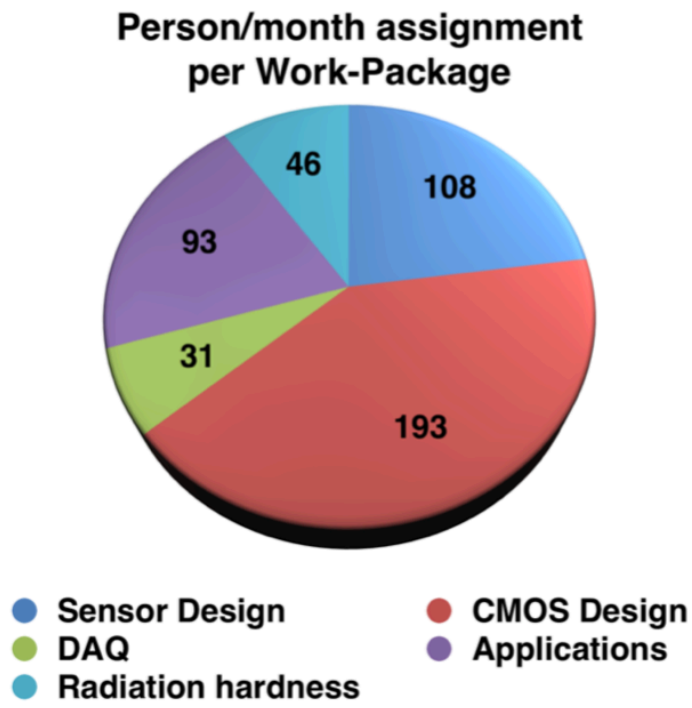
Andrea Paternò
on behalf of the ARCADIA Collaboration

ARCADIA (INFN CSNV Call Project)

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

INFN - Bologna, Milano, Padova, Perugia, Pavia, TIFPA, Torino

F. Alfonsi, G. Ambrosi, A. Andreazza, E. Bianco, G. Balbi, S. Beolè, M. Caccia, A. Candelori, D. Chiappara, T. Corradino, T. Croci, M. Da Rocha Rolo, G. F. Dalla Betta, A. De Angelis, G. Dellacasa, N. Demaria, L. De Cilladi, B. Di Ruzza, A. Di Salvo, D. Falchieri, M. Favaro, A. Gabrielli, L. Gaioni, S. Garbolino, G. Gebbia, R. Giampaolo, N. Giangiacomi , P. Giubilato, R. Iuppa, M. Mandurrino, M. Manghisoni, S. Mattiazzo, M. Mignone, C. Neubüser, F. Nozzoli, J. Olave, L. Pancheri, D. Passeri, A. Paternò, M. Pezzoli, P. Placidi, L. Ratti, E. Ricci, S. B. Ricciarini, A. Rivetti, R. Santoro, A. Scorzoni, L. Servoli, F. Tosello, G. Traversi, C. Vacchi, R. Wheadon, J. Wyss, P. Zuccon



- 3-year >1M€ R&D project 2019-2021
- Sensor&CMOS design, DAQ, System characterisation (medical, future colliders, space)

ARCADIA (INFN CSNV Call Project)

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

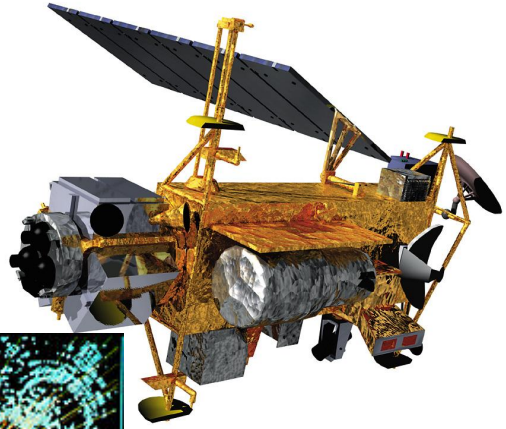
CMOS sensor design and fabrication platform allowing for:

- Active sensor thickness in the range 50 µm to 500 µm
- Operation in full depletion with fast charge collection only by drift
- Small charge collecting electrode for optimal signal-to-noise ratio
- Scalable readout architecture with ultra-low power capability (~20 mW/cm2)
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)
- Use of a deep sub-micron 110nm CMOS node for higher gate density

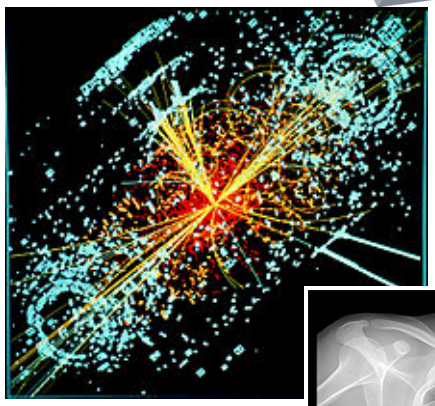
Specifications

Apply the experience developed with SEED to a versatile, full-chip prototype

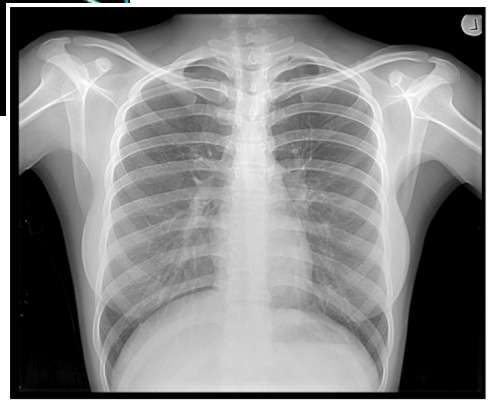
Targeting most stringent requirements for a number of applications:



- Low power → O(20 mW cm^{-2})
  - Scale down to O(10 mW cm^{-2}) in Low Rate mode

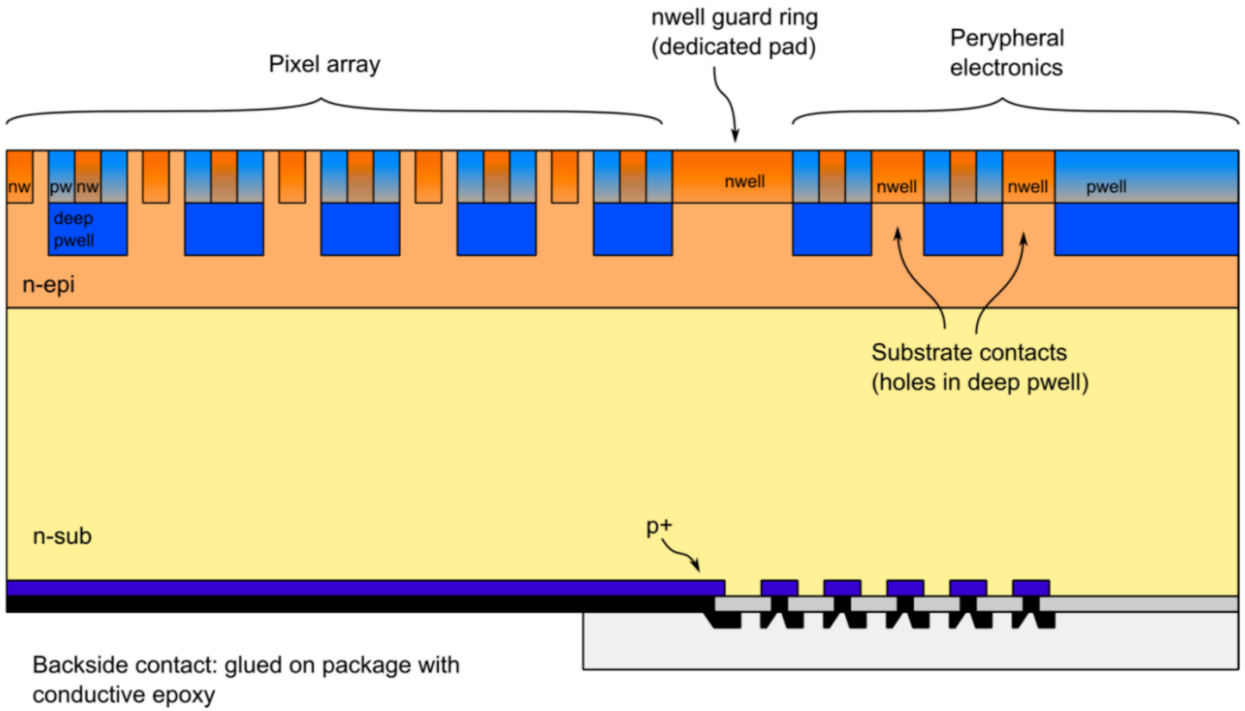


- Small pixel pitch → 25 × 25 μm^2
- Thin sensors → 100μm



- Scalability to large area → up to 4 × 4 cm^2
- High particle rate → up to 100 MHz cm^{-2}
- Timing resolution → O(1μs)
  - Investigating more advanced solutions for O(10 ns) timing

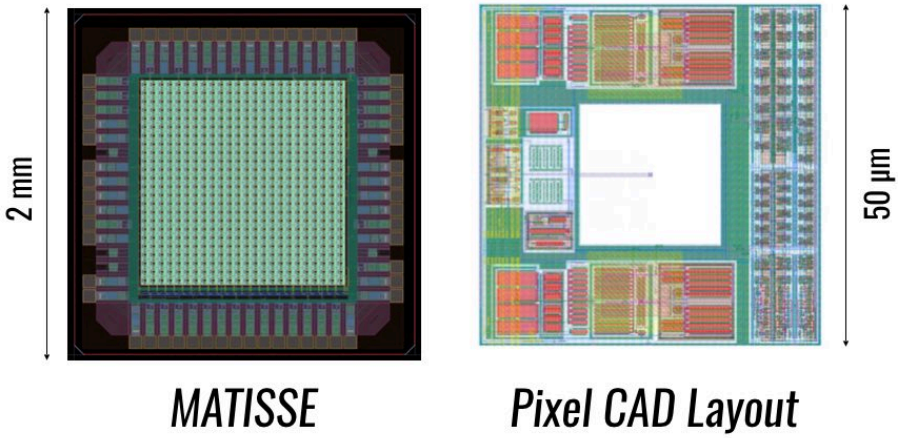
The Sensor



- Prototypes: Pixel sensor w/ electronics (MATISSE) and passive test structures (Pseudo-Matrix)
- Technology: 110 nm CMOS CIS technology (quad-well, both PMOS and NMOS), high-resistivity bulk
- Backside: diode surrounded by a guard-ring, custom patterning, process developed with LFoundry
- Process, back-side pattern and geometry validated in silicon

Prototypes

Small-scale demo: MATISSE



Pixels: Analog-only

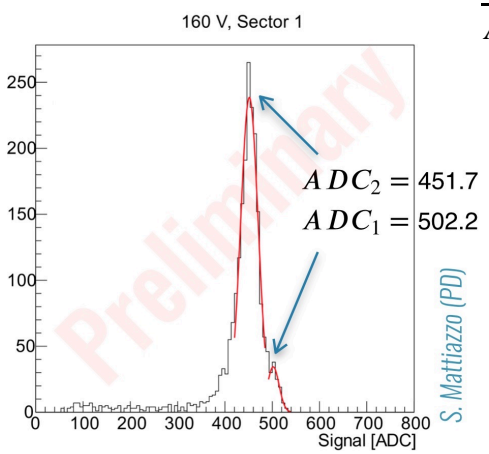
Matrix: 24x24 pixels

Dynamic range: up to 40ke-

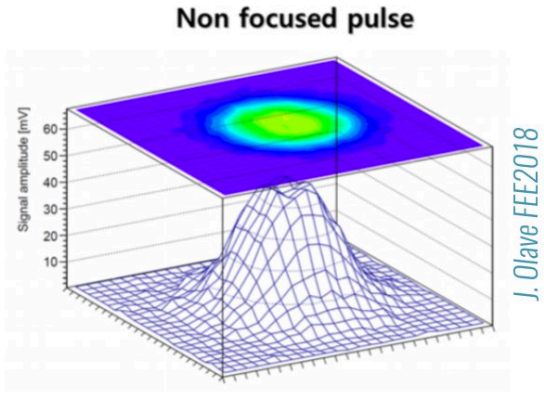
Noise: ~40e- (measured)

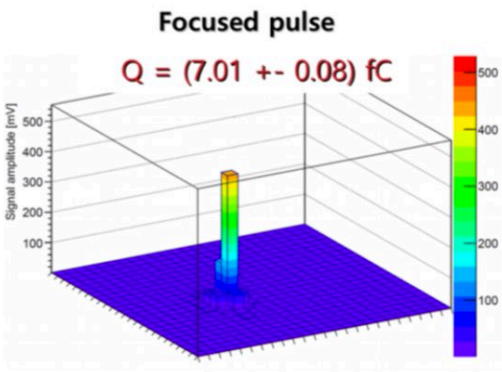
Preliminary results with ^{55}Fe

$$\frac{ADC_1}{ADC_2} \approx \frac{6.5\ keV}{5.9\ keV}$$



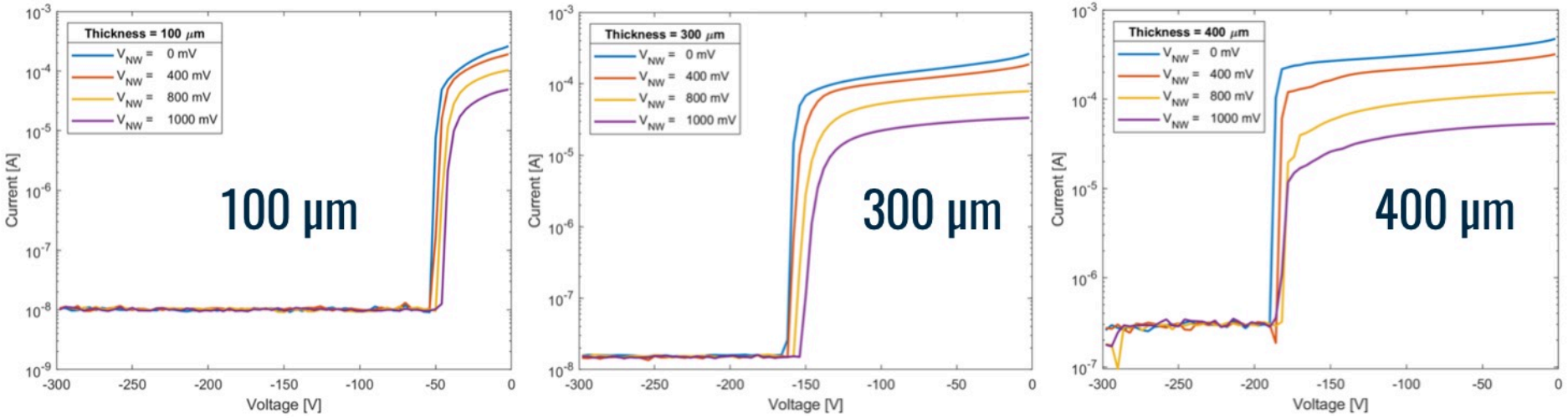
Preliminary results with Lasers

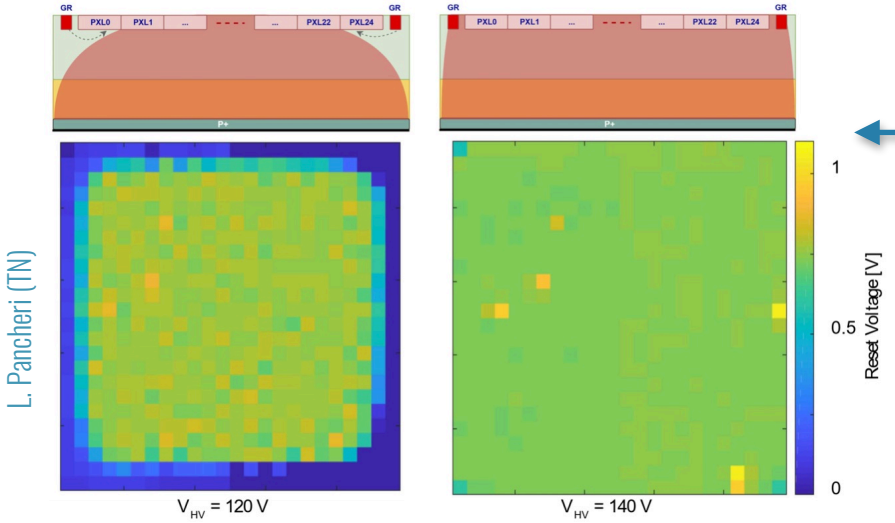




Results in a nutshell: MATISSE

Full depletion studies in 100-300-400 µm prototypes

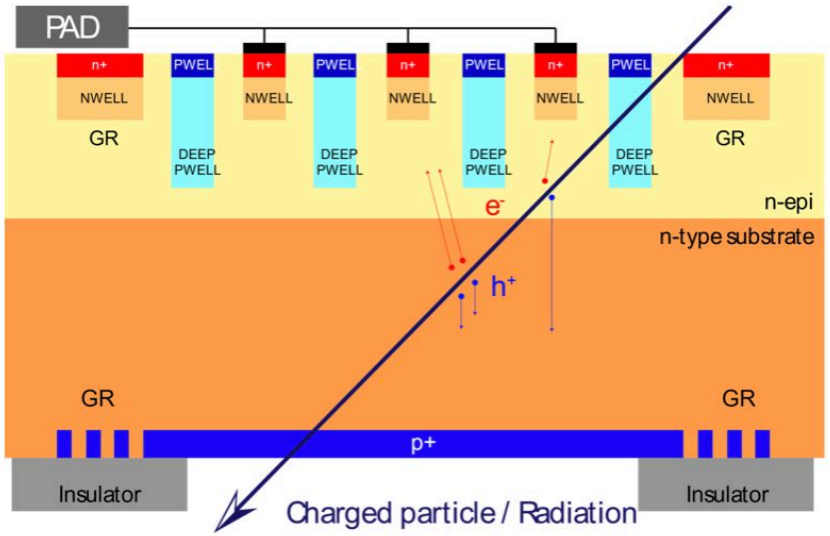


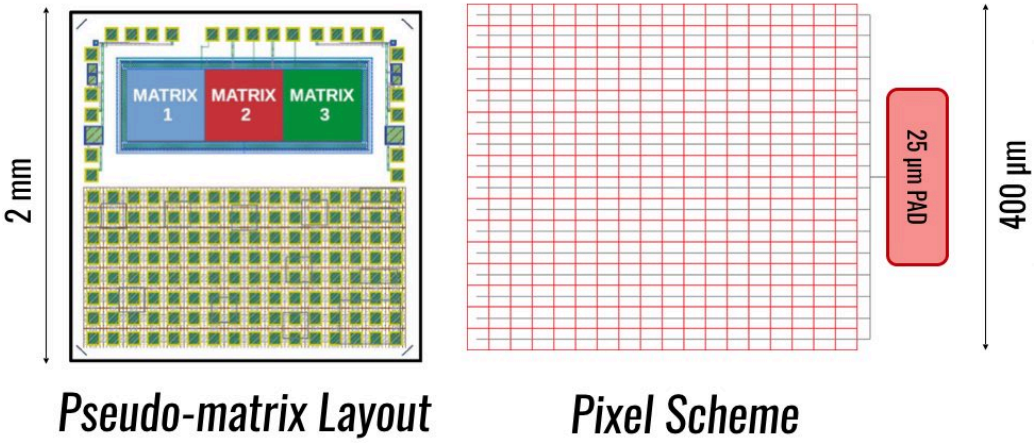


L. Pancheri (TN)

Map of pixel reset voltage (MATISSE 24x24 pixel matrix, 300µm thickness) as a function of the back-side voltage applied to the sensor. Depletion starts from the back-side.

Small-scale demo: Pseudo-Matrices



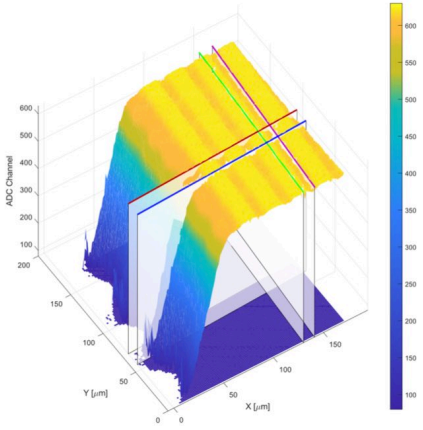


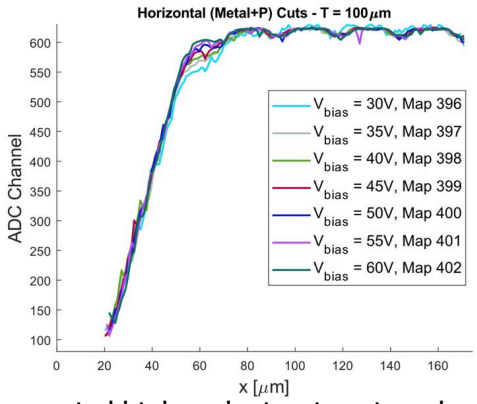
Pseudo-matrix Layout *Pixel Scheme*

- Sensor thicknesses: 100 µm, 300 µm, 400 µm
- Three matrices with different pixel sizes: 10 µm (40 x 45), 25 µm (16 x 18) and 50 µm (8 x 9)
- Front-side deep-pwell, would host the CMOS electronics (no electronics on PMs)
- All the collector nodes of a matrix are shorted and connected to a PAD
- Each pixel is shorted using Al metal lines of increasing width per PM: 6, 8 and 15 µm

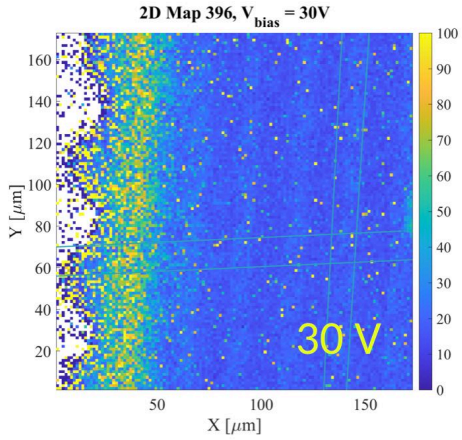
Results in a nutshell: Pseudo-Matrices

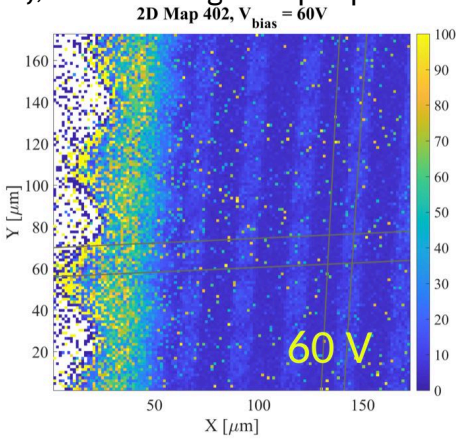
Cuts along the Metal + P and Metal + N lines on the energy map with varying bias voltages show uniform Charge Collection Efficiency above Full Depletion with ~1.7 % loss over metals (100 μm thick)





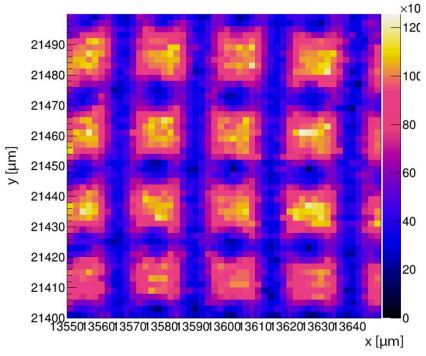
Standard deviation maps show the expected higher electronic noise when the sensor is not depleted (below 30 V), due to the higher top capacitance.

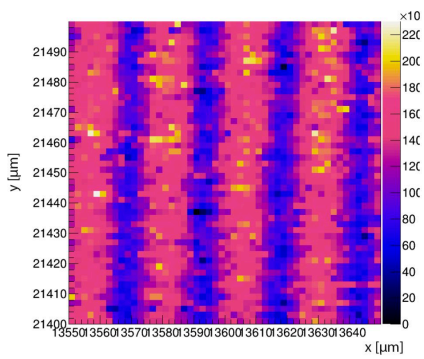




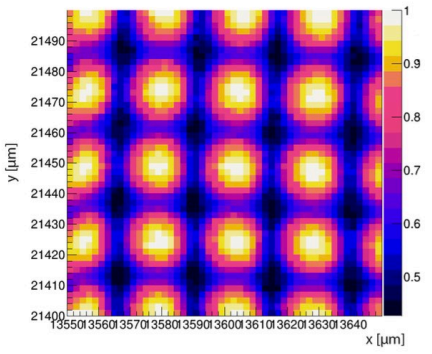
(RUĐER BOŠKOVIĆ INSTITUTE)* Zagreb, Croatia
600 keV to 2 MeV Tandetron
TANDEM 1-6 MeV proton source
LASER TCT laboratory

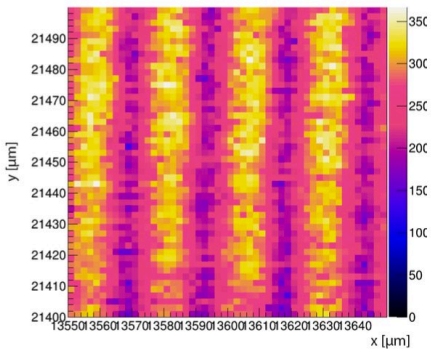
TCT Scan: CCE





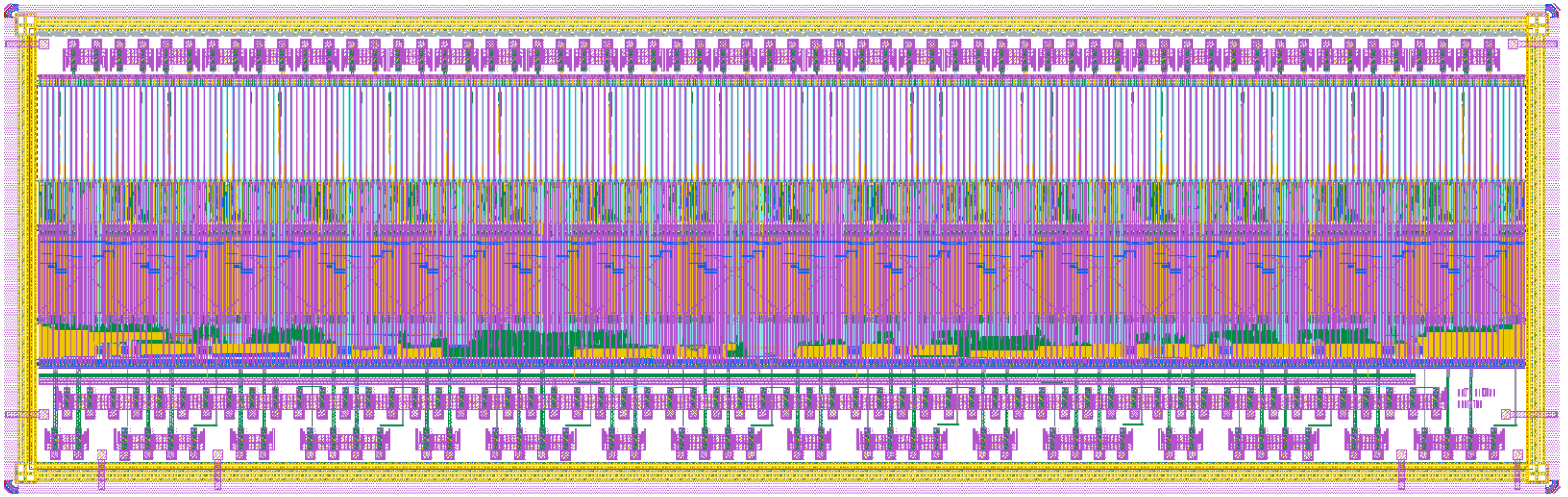
TCT Scan: Amplitude





Chip Architecture

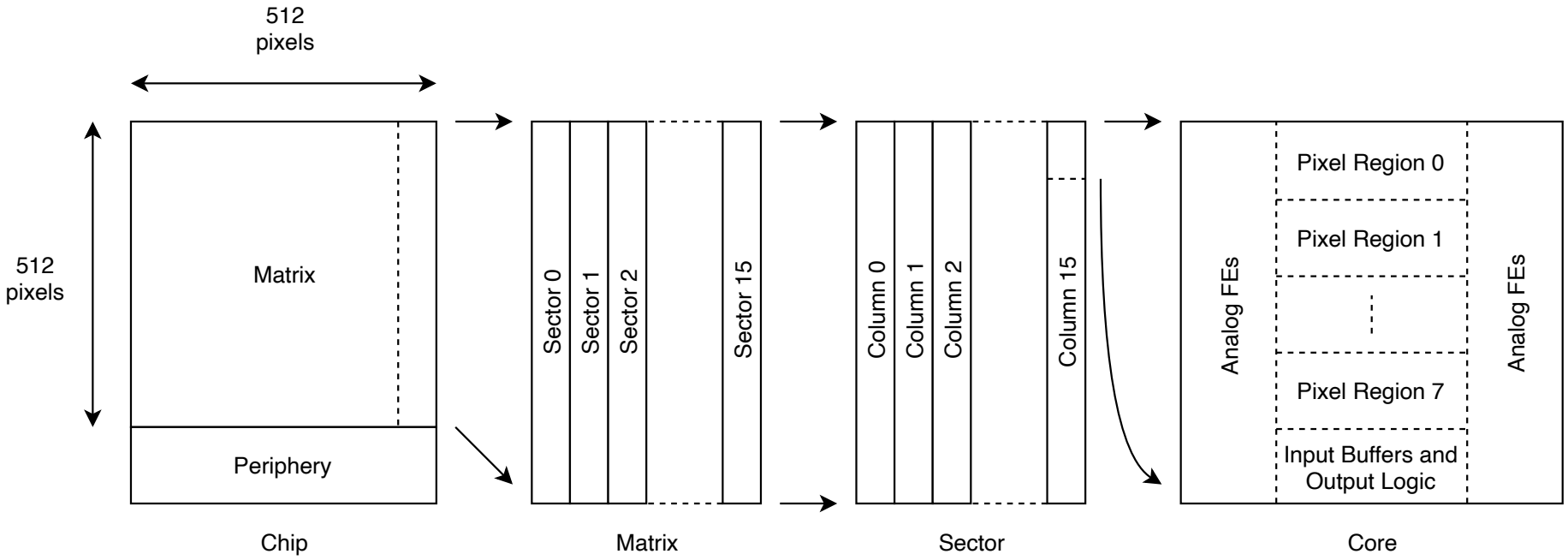
ARCADIA-MD1 - Floorplan



- Pixel size 25 µm x 25 µm: process, back-side pattern and geometry validated in silicon
- Matrix core 512 x 512, "side-abuttable" to accomodate a 512 x 1024 active area (2.56 x 1.28 cm^2).
- Chip architecture and data links scalable to 2048 x 2048 pixels[1]
- Triggerless, binary readout, event rate up to 100 MHz cm^{-2}
- Two flavors: full size (512x512) and mini (32x512 - pictured above)

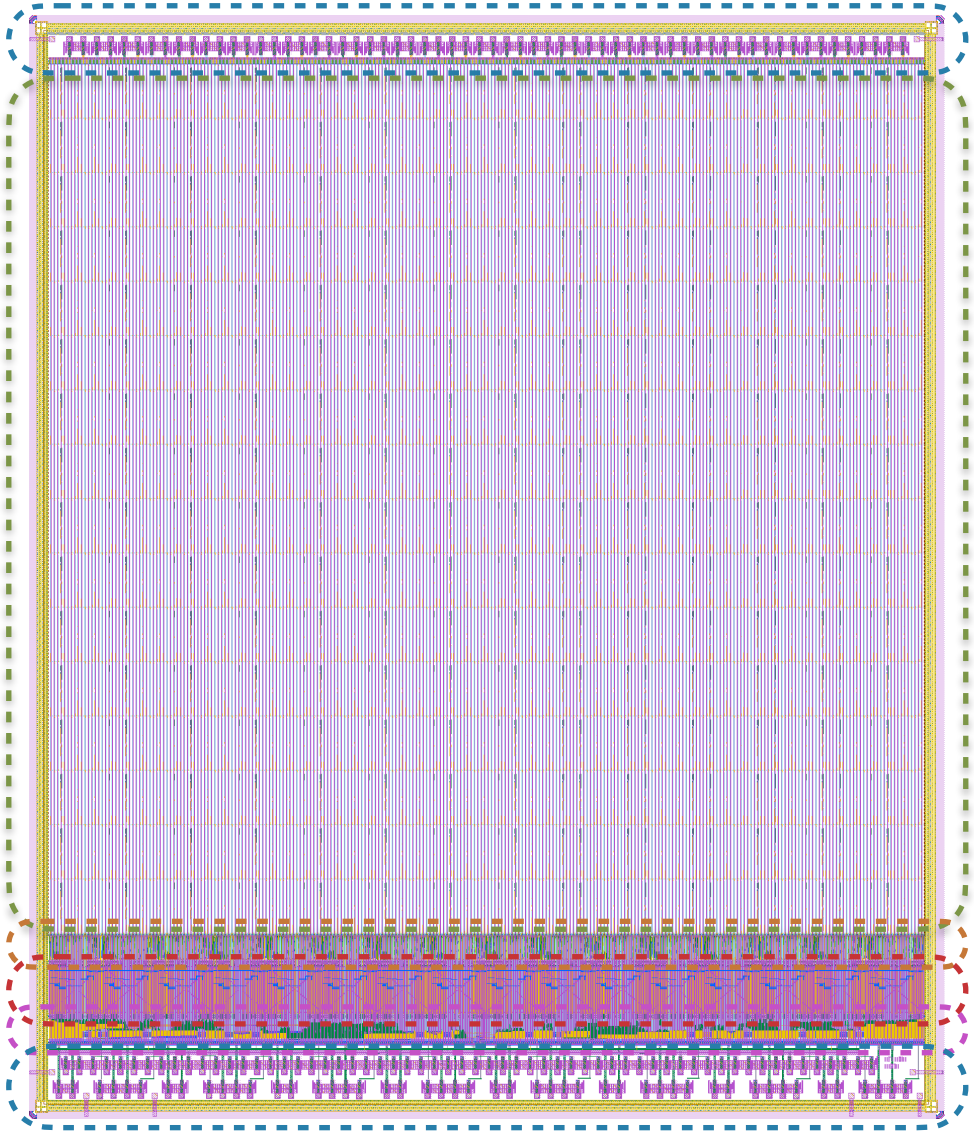
[1] 1D and 2D stitching available at LFoundry

ARCADIA-MD1 - Floorplan scheme



- The Matrix is composed of 16 identical Sectors, each with independent readout and output link
- Sectors (32x512) contain 16 Double Columns, read by a common End Of Sector logic
- Double Columns (2x512) stack 16 Cores, the minimal synthesizable entity in the matrix
- Cores (2x32) bundle together 8 Pixel Regions for optimal PNR and Signal Propagation

ARCADIA-MD1 - Floorplan



Top Padframe

Auxiliary supply, IR Drop Measure

Matrix

512x512 pixels, Double Column arrangement

End of Sector (x16)

Reads and Configures 512x32 pixels

Sector Biasing (x16)

Generates I/V biases for 512x32 pixels

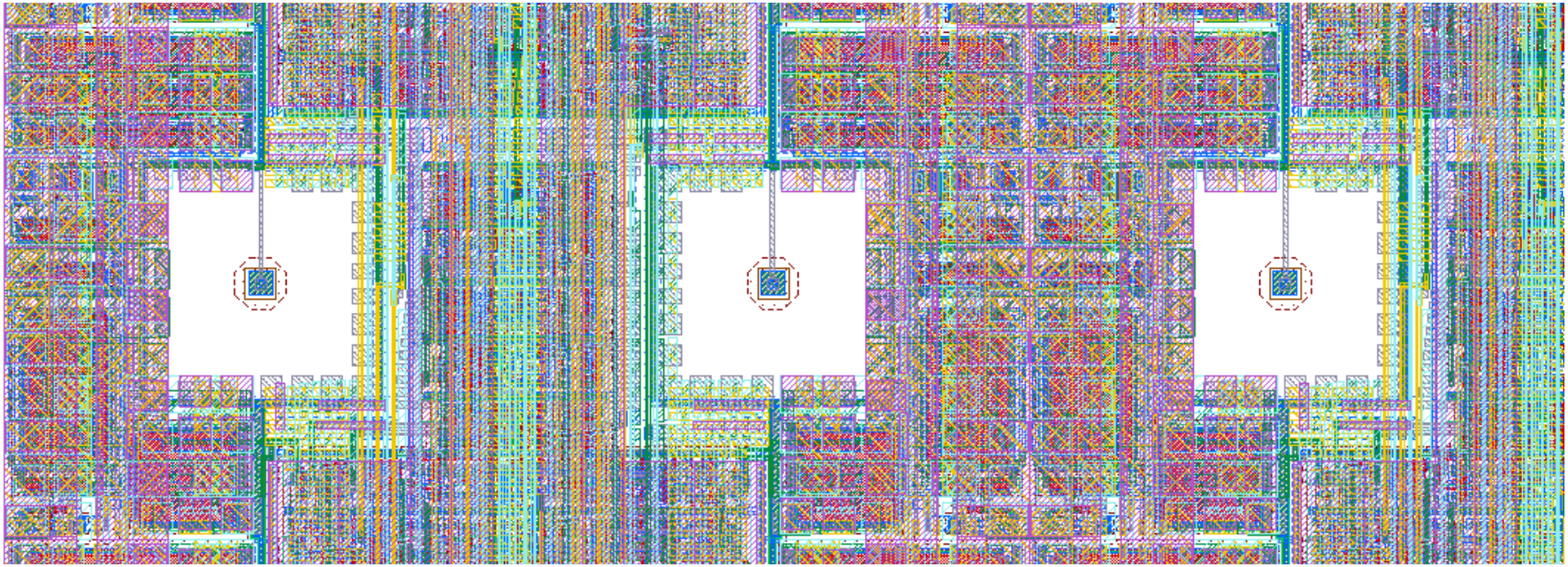
Periphery

SPI, Configuration, 8b10b enc, Serializers

Bottom Padframe

Stacked Power and Signal pads

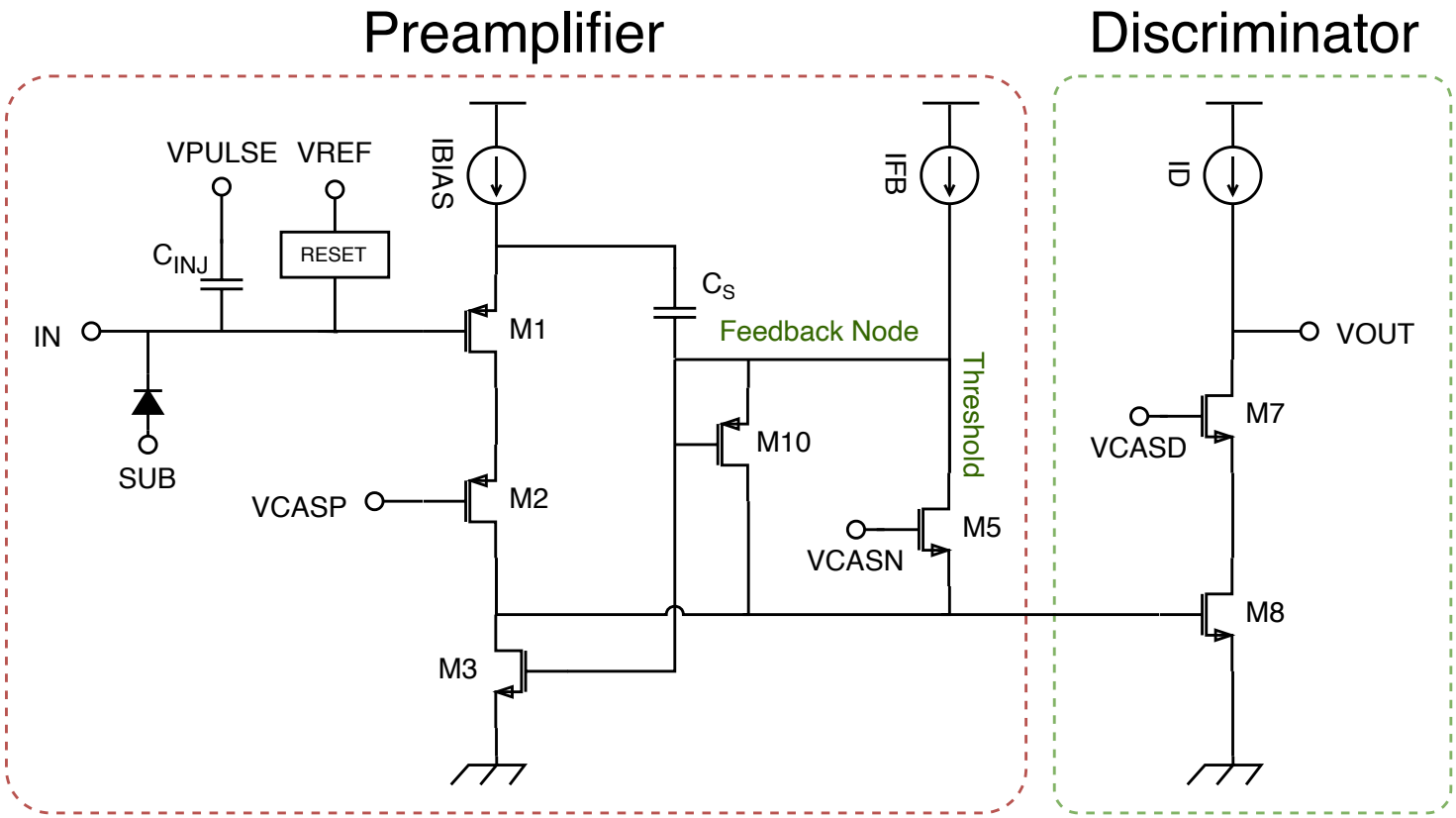
ARCADIA-MD1 - Pixels



- The pixel's area is occupied by the collection diode (16%) and analog and digital circuits (42% both)
- 2-bit pixel configuration for masking and injection enabling
- Digital injection capability for readout chain testing, bypassing FEs
- Custom power distribution scheme to maximize metal occupancy

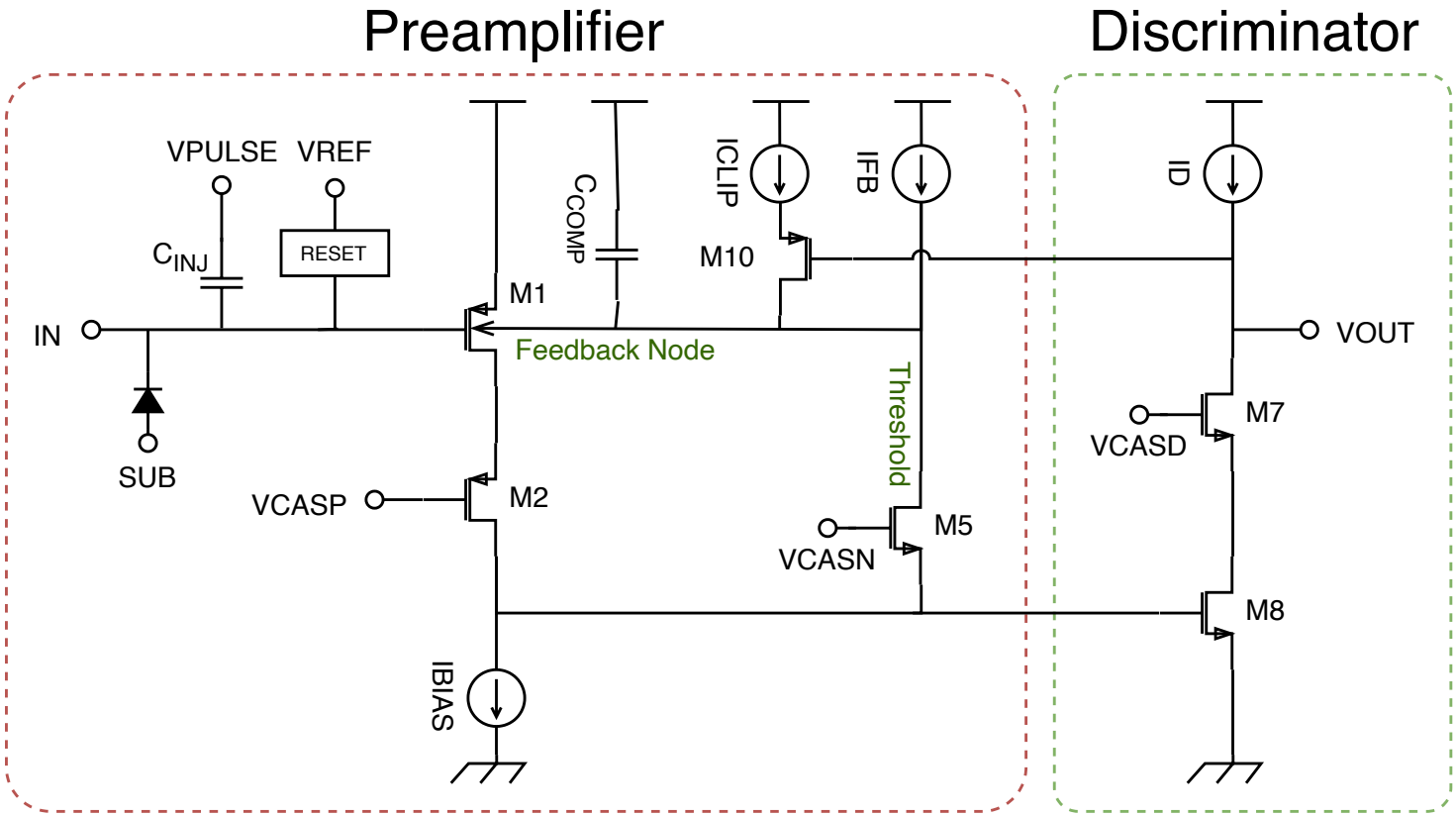
The Analog Front-Ends

FE1 - Inspired by ALPIDE



- Amplification concept based on charge transfer between Cs and Cout, the parasitic capacitance at the preamplifier output
- Small signal gain: Cs/Cout
- M0 resets the input node for big input charges
- M6 clips the signal at the preamplifier output for big input charges

FE2 - Bulk-driven

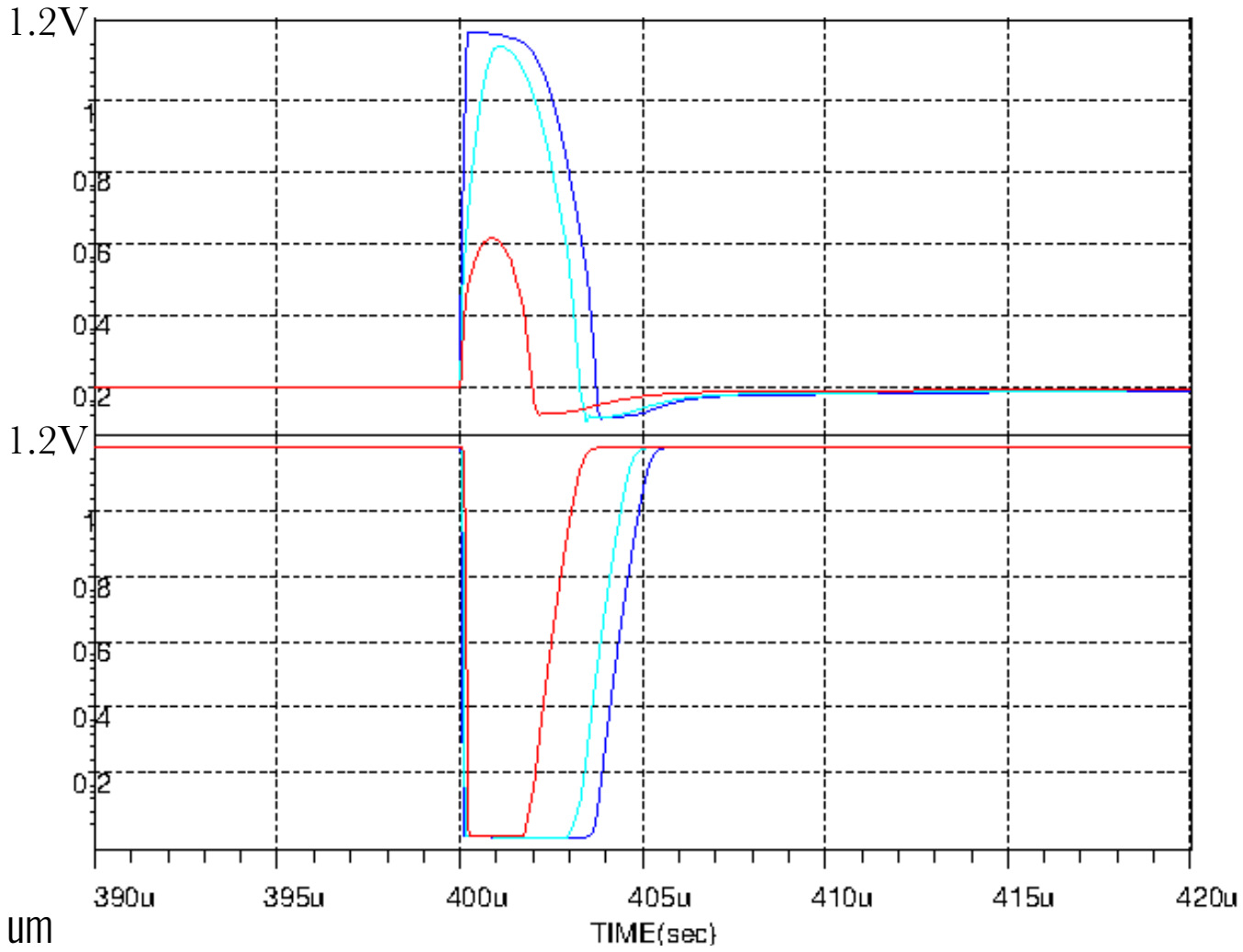


- Small signal gain: gm1/gm5
- Feedback applied to the bulk of input transistor
- Clipping mechanism changed due to different DC voltages in this architecture

FE2 - Post-layout Simulations

Pre-amp
Center
Edge
Corner

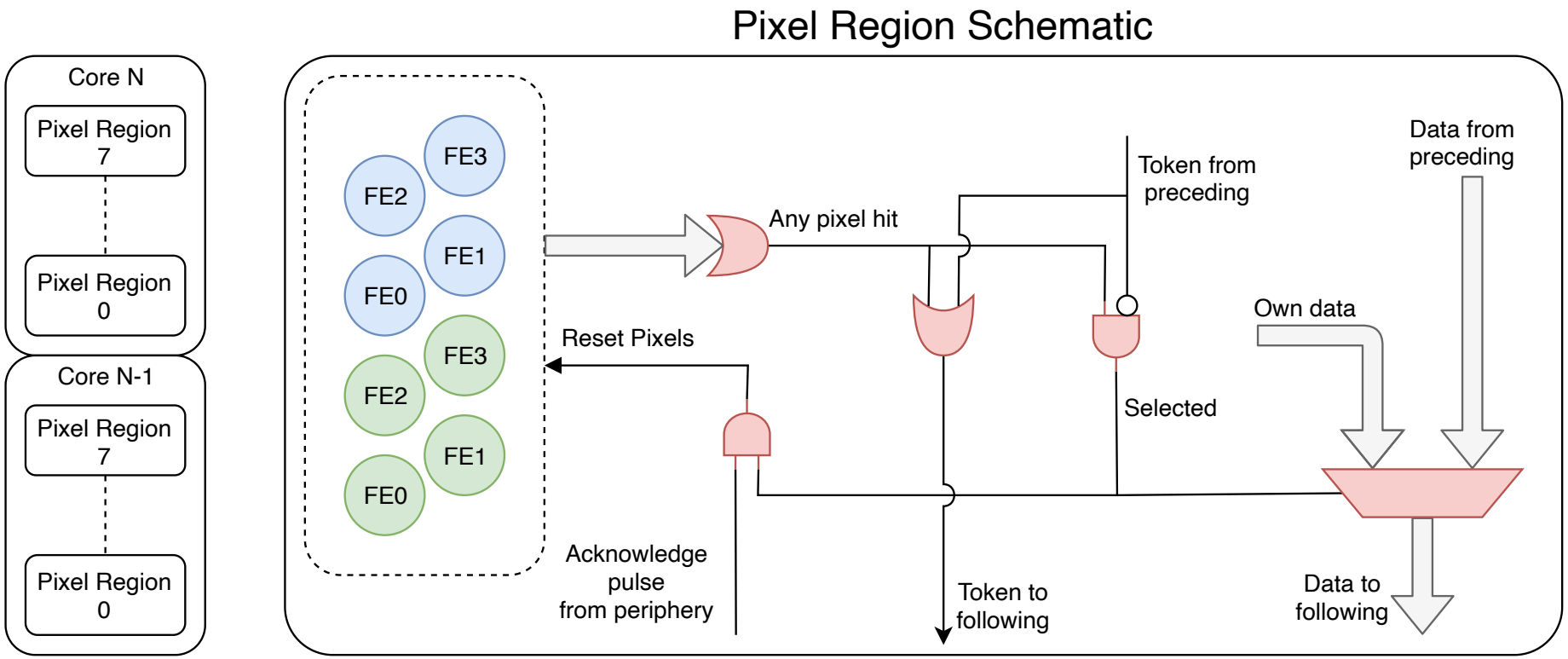
Discr.
Center
Edge
Corner



- 200 MeV muons
- Sensor thickness 100 um

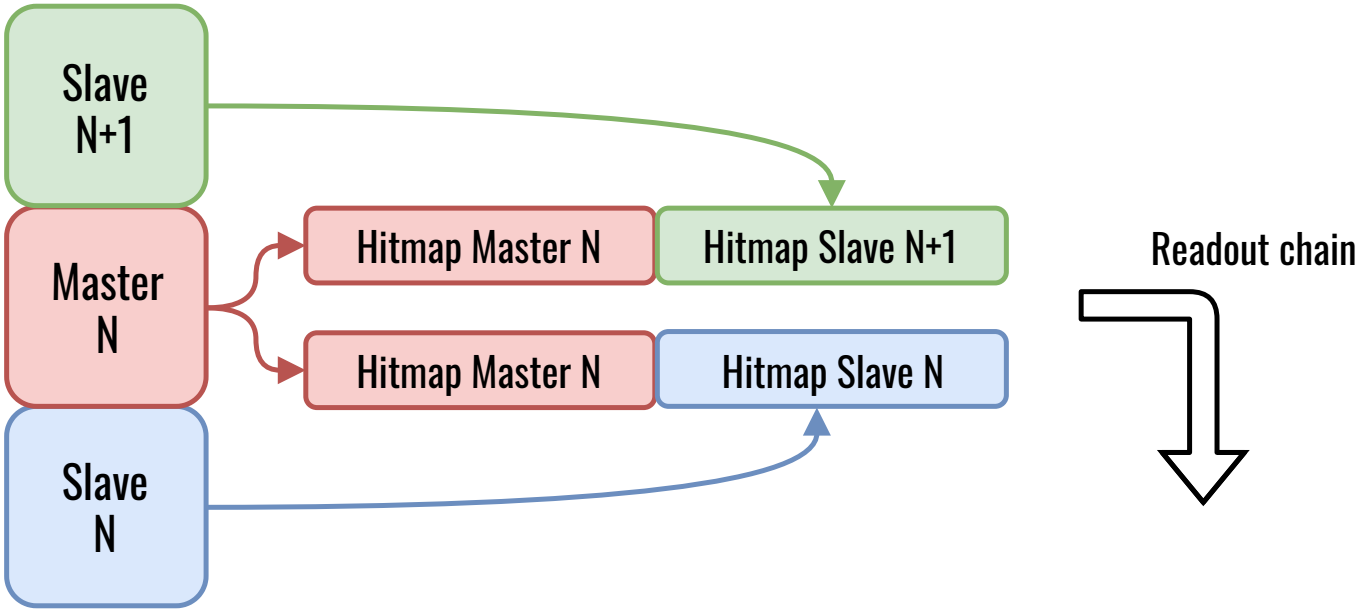
Readout

ARCADIA-MD1 - Readout



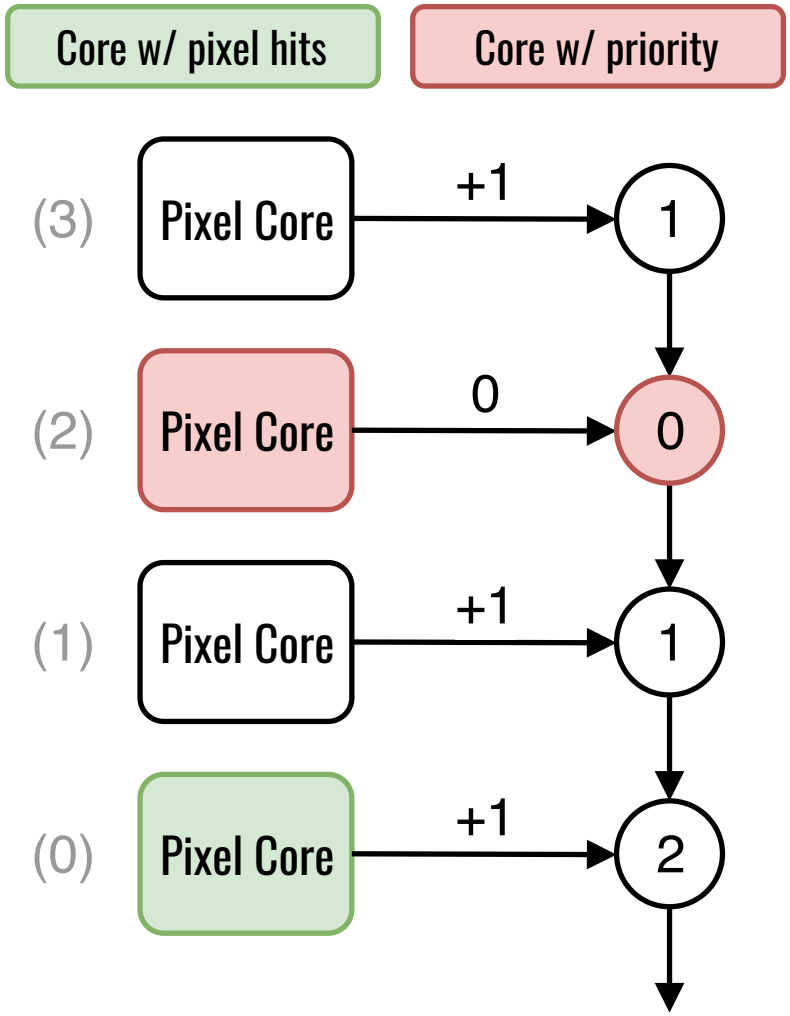
- Pixel Regions use a Token chain to establish Readout Priority
- The data bus propagates: Pixel Region Hitmap and Address + Core Address

ARCADIA-MD1 - Auto-Clustering



- 4 × 2 pixel Regions, logically divided into a Master (2 x 2) and a Slave (2 x 2)
- Master can include the hitmap of either the Top or Bottom Slave in the data packet
- Masters propagate 4 × 2 pixel data packet to the periphery and await Acknowledge pulse
- Aim: Zero suppression, reduction of bus occupancy and readout clock requirement

ARCADIA-MD1 - Indirect Addressing



- Cores are not aware of their own addresses or position in the matrix.
- Core Address is evaluated during readout by a simple adder
- Pixel Region Address is hardcoded (synthesized) in the Core logic
- Pixel configuration must select the cores to configure indirectly
- This strategy allows to save cell area and metal interconnections

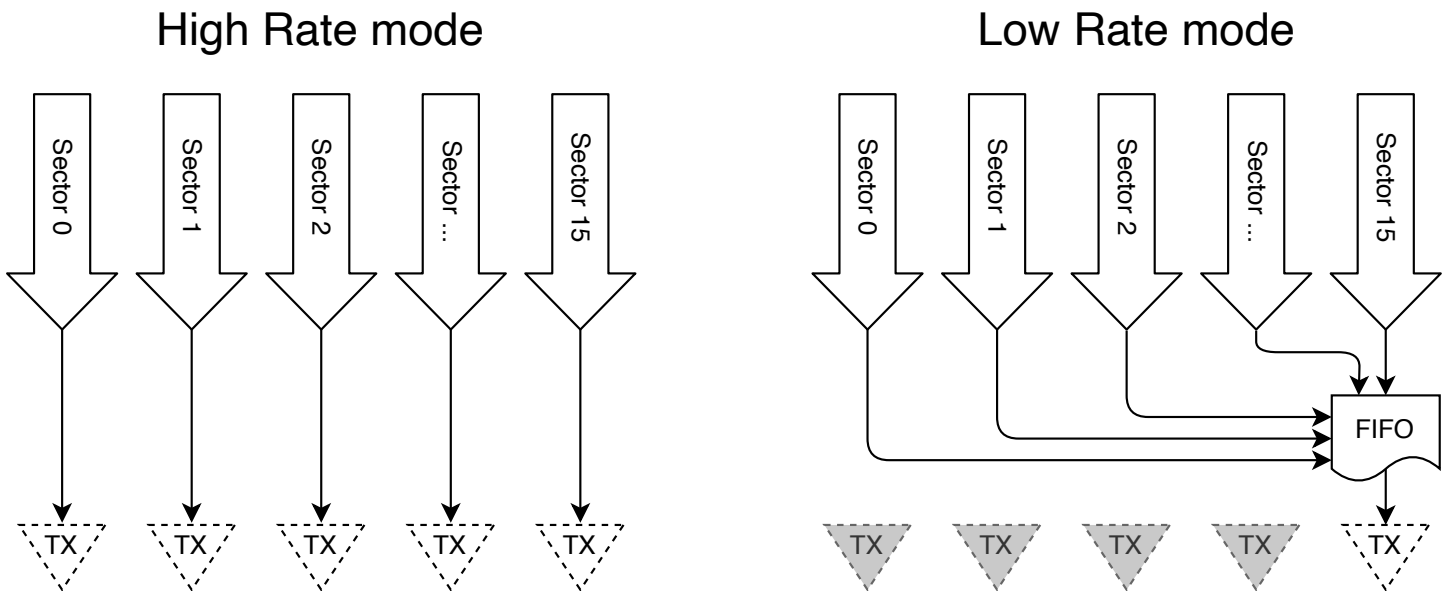
ARCADIA-MD1 - Readout performance

	w/ Auto Clustering	w/o Auto Clustering
Event Rate	100 MHz cm^{-2}	
Matches	99,778%	99,712%
Ghost	0,004%	0,08%
Duplicate	0,11%	0,02%
Column Packet rate	15,7 MPps	19,9 MPps
Column bandwidth	443,11 Mbps	510,18 Mbps

- Randomly generated clusters w/ average pixel occupancy = 4
- Auto-Clustering reduces Column BW of 67Mbps

ARCADIA-MD1 - Peripheral Dataflow

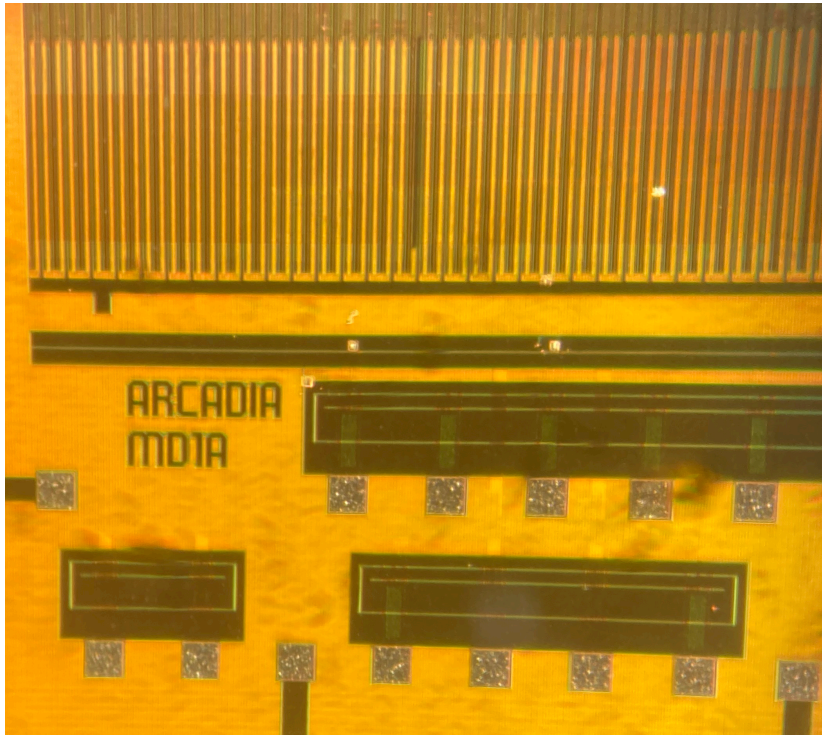
- Each Column (32x512 pixels) has a readout BW of 443Mbps
- Link is DC-balanced via 8b10b encoding, which increase BW requirement to 553Mbps
- Sector data is sent out via dedicated 320MHz DDR Serializers
- In Low Rate Mode, the first serializer processes data from all the sections. The other serializers and LVDS TXs are powered off in order to reduce power consumption.

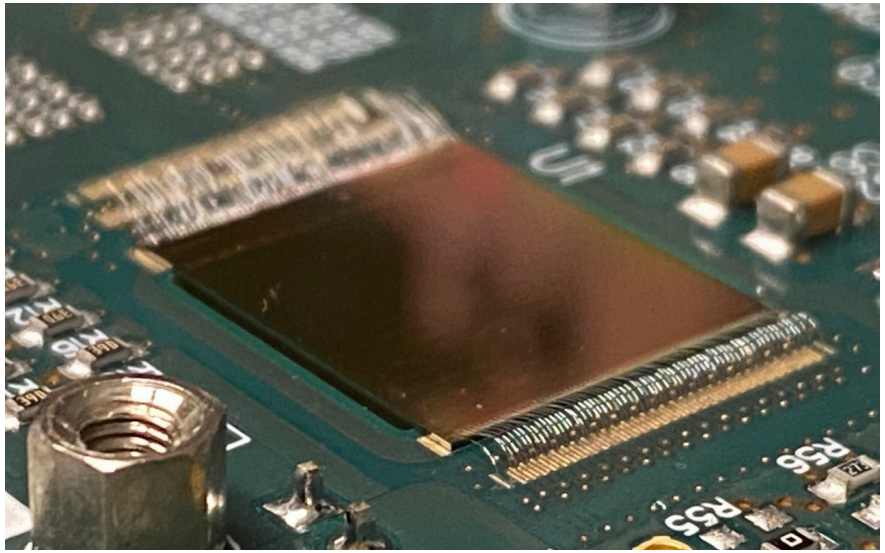


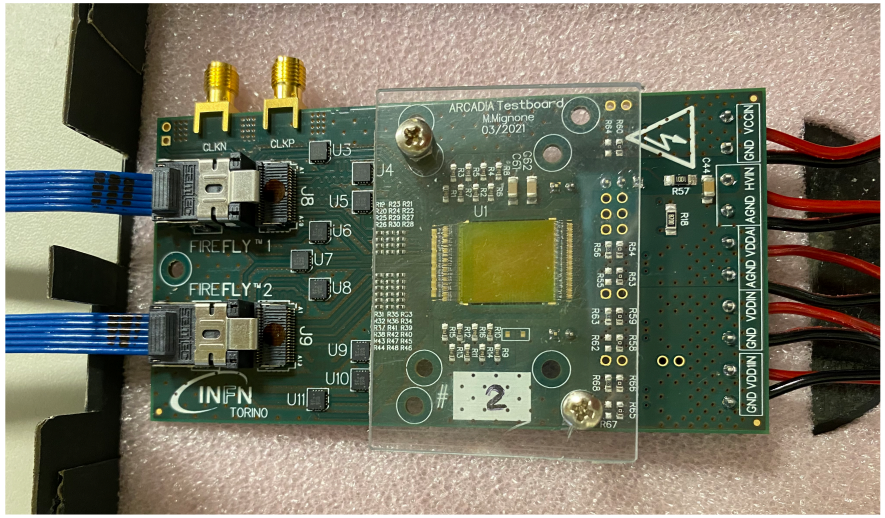
ARCADIA-MD1 Preliminary tests

Submission and Tests

- ARCADIA-MD1 submitted in October 2020
- Dies received in June 2021
- Tests started soon afterwards







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Preliminary tests

- Late-discovery LVDS-TX interface bug has been fixed via Focused Ion Beam
- All of the implemented features have been demonstrated to work as expected
- Tests are now proceeding to fully characterize the performance of the Analog FEs

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Conclusions

ARCADIA-MD2

A second main demonstrator (codename ARCADIA-MD2) has been submitted in June 2021.
Research has focused on power reduction, scalability.

- 16x2 pixel Cores, 8 Cores in the Matrix
- Logic and buffering optimization -> Acknowledge signal propagates 7 times faster!
  - Simulations validated matrices up to 8192 pixels high
- Optional Core addressing failsafe mechanism
- Power optimization in the periphery
- 1 GHz DDR serializer -> 2Gbps bandwidth!
- Now in foundry, expected dies in October

Summary

- The ARCADIA chips target space, medical, and future colliders applications
- Uses a custom LFoundry 110nm CIS process
- Chip architecture focuses on scalability to large areas, low power operation
- Binary readout, high spatial resolution (25um pixel pitch), us timing resolution
- Dies come in 2 flavors, with 2 different Front-Ends
- ARCADIA-MD1 submitted in October 2020, first dies in June 2021
- Tests on all digital and analog features confirmed the expected functionality
- ARCADIA-MD2 submitted in May 2020, dies expected in October 2021
- ARCADIA-MD3 to be submitted mid-2022

ARCADIA: technology platform and system-grade demonstrator architecture

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Thank You for your time !