

Monolithic sensors for the Mu3e experiment

Luigi Vigani, on behalf of the Mu3e collaboration University of Heidelberg Vertex 2021 29/09/2021



Mu3e: Physics Motivation

- Search for $\mu \rightarrow eee$
 - Standard Model: BR ($\mu \rightarrow eee$) < 10⁻⁵⁴
- New physics might enhance BR
- Current limit:
 - BR (μ → eee) < 10⁻¹² (SINDRUM, 1988)
- Aimed single-event sensitivity:
 - BR (μ → eee) < 2 · 10⁻¹⁵ (Phase 1)
 - BR (μ → eee) < 10⁻¹⁶ (Phase 2)
- PSI High Intensity Muon Beamline
- Phase 1 construction starting by beginning of next year



SM

SUSY

 $\tilde{\chi}^0$

 $\tilde{\mu}$

 W^+

 μ^+



2



- Tracking electrons coming from muon decays (~10⁸ Hz in Phase I)
- Magnetic field (1 T)





- Tracking electrons coming from muon decays (~10⁸ Hz in Phase I)
- Magnetic field (1 T)





- Tracking electrons coming from muon decays (~10⁸ Hz in Phase I)
- Magnetic field (1 T)





- Tracking electrons coming from muon decays (~10⁸ Hz in Phase I)
- Magnetic field (1 T)





- Tracking electrons coming from muon decays (~10⁸ Hz in Phase I)
- Magnetic field (1 T)





Momentum resolution crucial for detecting the peak at muon mass...

Material budget is key factor!

1 MeV resolution with 0.1% X/X $_0$ per layer

Invariant mass of signal decay, radiative decay and accidental background (Bhaba+Michel) [Mu3e TDR]





Layer 1/2





Layer 1/2





Layer 1/2



MuPix sensors

Mart

- Monolithic HV-CMOS
 - Super thin with high performance
- 180 nm H18 technology derived from IBM
 - AMS until 2018
 - TSI afterwards
- Long R&D campaign
 - Mupix7 first fully monolithic
 - Mupix8 larger
 - Mupix9 implemented slow control
 - Mupix10 with final size
 - Expected Mupix11 soon



MuPix sensors: MuPix10



- ~2x2 cm² active area
- Chip periphery on bottom



MuPix sensors: MuPix10





- ~2x2 cm2 active area
- Chip periphery on bottom
- Signal collected and amplified by pixels
- Analogue signal driven to periphery
- Each pixel mirrored in periphery
 - \circ $\,$ Analogue signal digitized
- State machine collects hits from double column
- Continuous read-out!
- 4 LVDS link
 - 3 per matrix (inner trackers)
 - 1 mulitplexed (outer layers)



Single pixel read-out: in-cell





Single pixel read-out: periphery



Comparator in digital cell

Records Time-of-Arrival (ToA)

Records time of falling edge

Time-over-Threshold (ToT) computed

2 threshold mode:

- hit flag raised with high threshold
- ToA recorded with low threshold
- Falling edge on high threshold Decreases time-walk



pixel size [µm ²]	80×80
sensor size [mm ²]	20×23
active area $[mm^2]$	20×20
active area [mm ²]	400
sensor thinned to thickness [µm]	50
LVDS links	3 + 1
maximum bandwidth [§] [Gbit/s]	3×1.6
timestamp clock [MHz]	≥ 50
RMS of spatial resolution [µm]	≤ 30
power consumption [mW/cm ²]	≤ 350
time resolution per pixel [ns]	≤ 20
efficiency at $20 \mathrm{Hz/pix}$ noise [%]	≥ 99
noise rate at 99% efficiency Hz/pix	≤ 20

Mag

- 3 LVDS input lines
 - Clock
 - Sync reset
 - Serial input
- Slow control
 - ADC to read internal voltages and temperature
 - Readings sent out via data links
 - Extra temperature diode (analogue output)
- Hit-delay circuit
 - Hit recorded after a fixed delay from ToA
 - Easier time sorting procedure
 - Incidental max value on ToT

- 3 LVDS input lines
 - Clock
 - Sync reset
 - Serial input
- Slow control
 - ADC to read internal voltages and temperature
 - Readings sent out via data links
 - Extra temperature diode (analogue output)
- Hit-delay circuit
 - Hit recorded after a fixed delay from ToA
 - Easier time sorting procedure
 - Incidental max value on ToT





Cross-talk





Multiple metal layers (TSI specific) used to minimize inter-line capacitances. Cross-talk probability < 1.5%

Neighbouring pixels are routed on different lines: cross talk distinguishable from charge sharing

MuPix10: results





110 V breakdown

Efficiency plateau well defined above 30V



MuPix10: results











MuPix10 devices thinned at different thicknesses (by mechanical grinding)



MuPix10: thinning



Severe impact on performance

- 50 µm thin
- 200 Ωcm resistivity
- Only 25 V bias

Efficiency is low

MuPix10: thinning

Severe impact on performance

- 50 µm thin
- 200 Ωcm resistivity
- Only 25 V bias

Efficiency is low

Observation: at same voltage, thicker is still better...

Diffusion? Damage in silicon bulk?

Studies ongoing (new thinning procedure, more complete data to analyze)





DAQ and experimental concept





Prototype of vertex detector

Jun/Jul 2021

50 µm-thin chips mounted on katpon foils

Connected to ladder-boards

Same shape as inner tracker, slightly larger

External connection with commercial cables



DAQ and experimental concept





DAQ and experimental concept





DAQ and experimental concept



DAQ and experimental concept





Worked!

First hitmap ever observed for the Mu3e experiment prototype

Analysis ongoing



Conclusions



- Mu3e is a CLFV experiment which uses pixel sensors to track electrons from muon decays
 - High rates
 - Low energy
- Tight experimental constraints on pixels \rightarrow HV-CMOS!
- MuPix development at the forefront of HV-CMOS R&D
- MuPix10 satisfies most of experimental requirements
- Prototype of vertex detector successful
- MuPix11 underway
- Production of Mu3e starting next year



Backup

Backup: crosstalk





Backup: thinning issue

Atomic force microscopy on backside





Backup: prototype data analysis

Chip-to-chip correlations





Backup: Prototyping



Thermo-mechanical stability



Silicon heater prototype

Reproduction of inner tracker with same materials and connections

Chips are just passive silicon heaters



Backup: Prototyping

Thermo-mechanical stability



Silicon heater prototype

Test stand with Helium cooling system



Backup: Prototyping

Thermo-mechanical stability

- Measurement of temperature-to-power relation
- Temperature difference linearly depending on heat dissipation
- Expected ΔT < 70 K for 400 mW/cm² (conservative limit)
- Cooling concept works
- More detailed studies to come

Silicon heater prototype





