



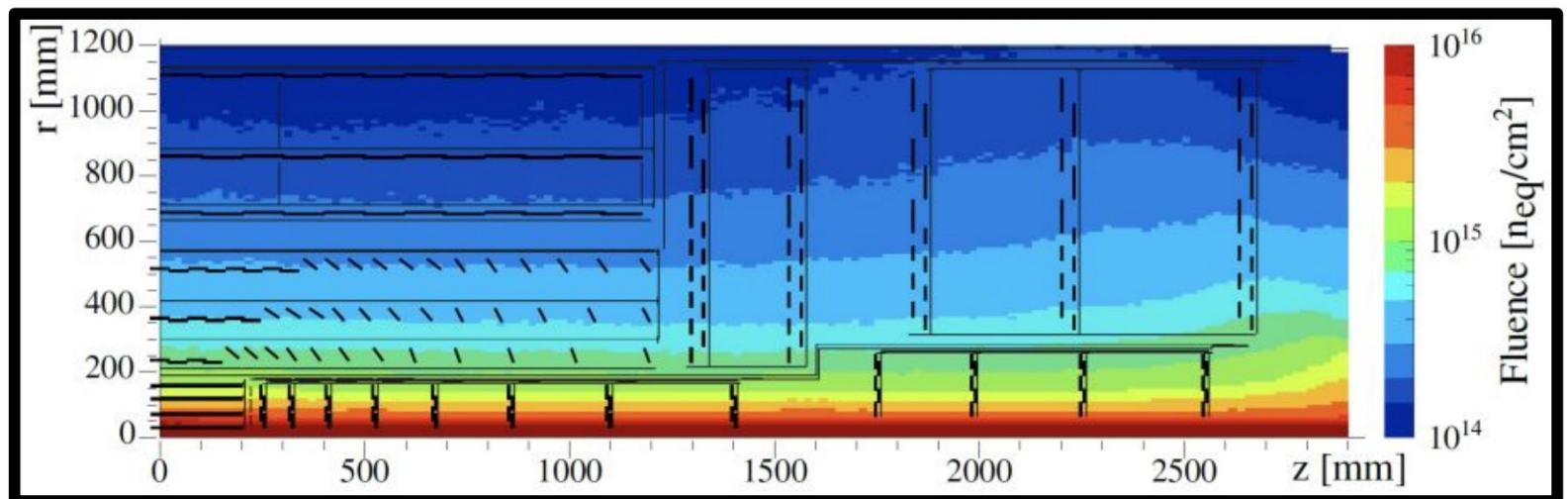
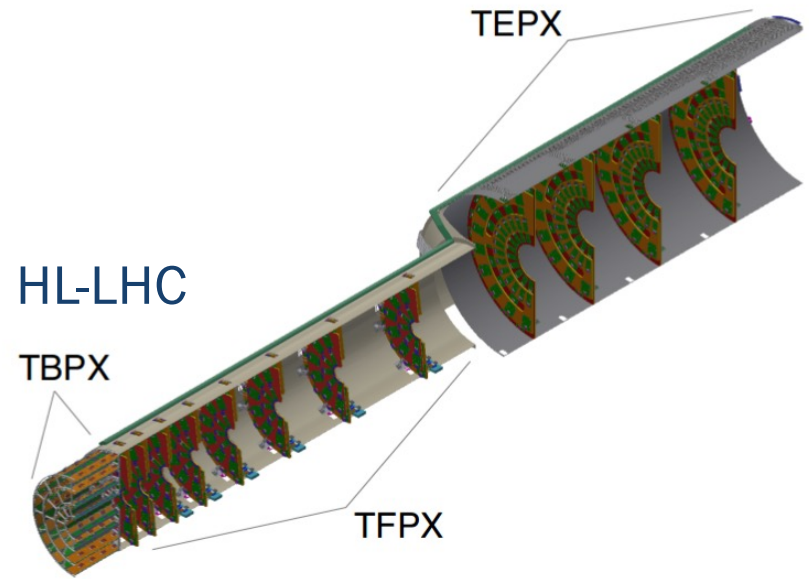
# THE PHASE-2 UPGRADE OF THE CMS INNER TRACKER

Rachel Bartek

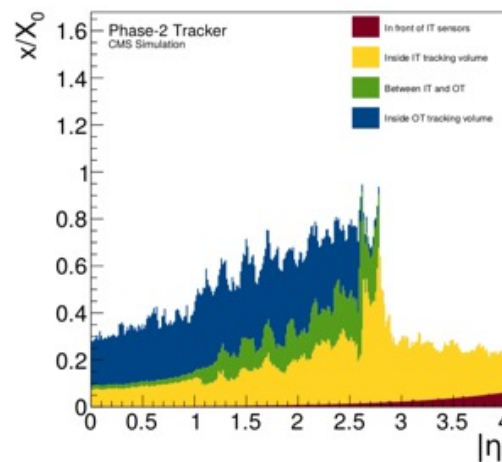
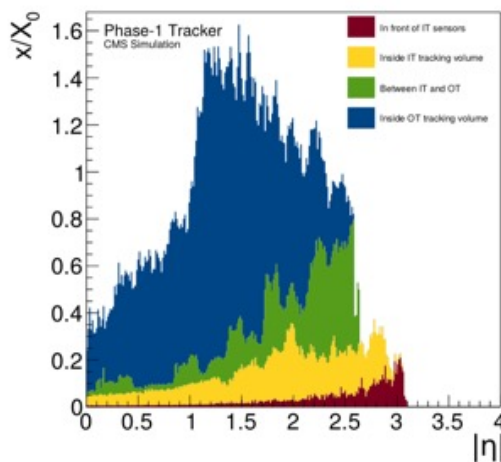
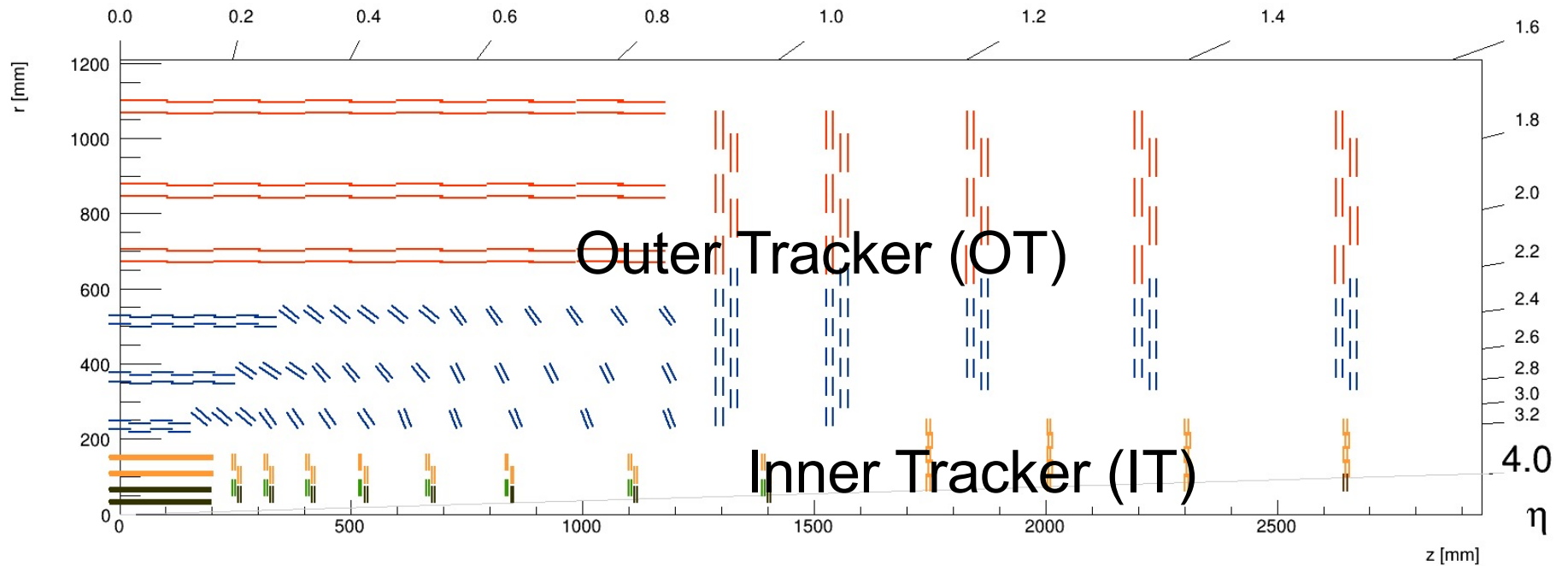
On behalf of the CMS Experiment

# Motivation

- Change in running conditions for LHC to HL-LHC
  - Pileup increasing from 25 to  $\sim 200$
  - Hit rate from 0.58 to 3.2 GHz/cm<sup>2</sup>
  - Radiation from 300 to 3000 fb<sup>-1</sup>
- The above places the following requirements on the inner tracking detector
  - Smaller pixels to reduce occupancy
  - Lower detection threshold to allow two track separation
  - Reduced material budget to improve tracking performance



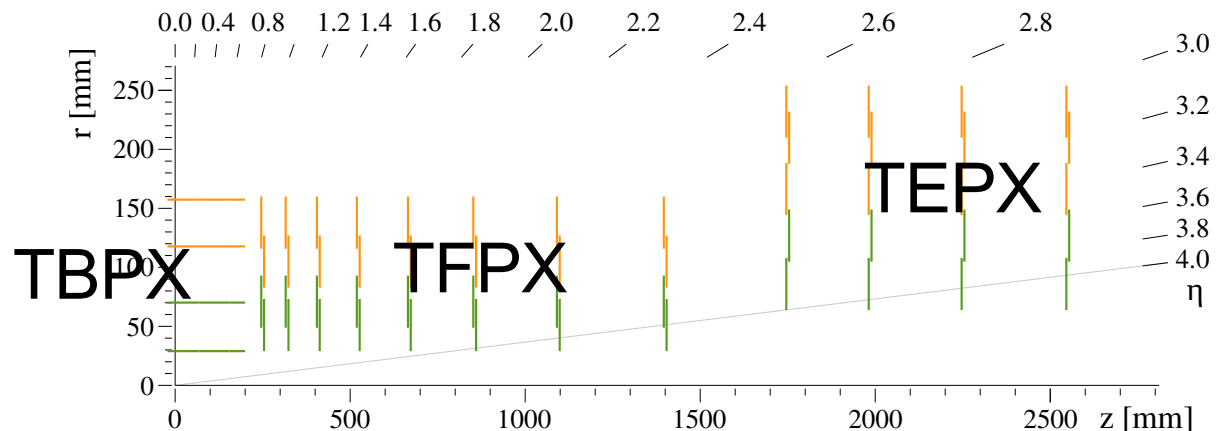
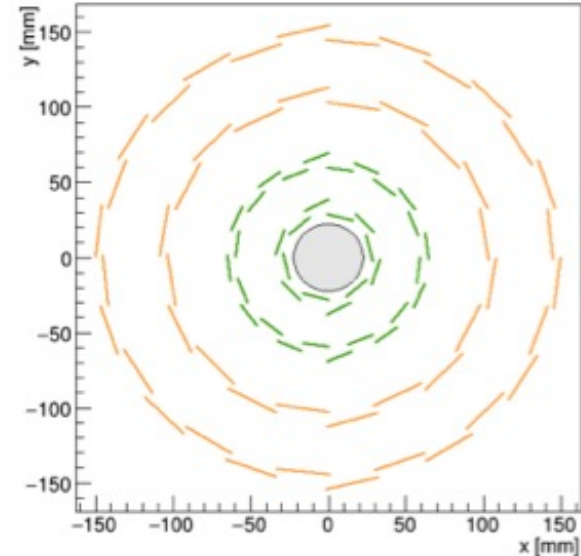
# HL-LHC CMS Tracker



Talk on OT by Kevin Nash  
Next!

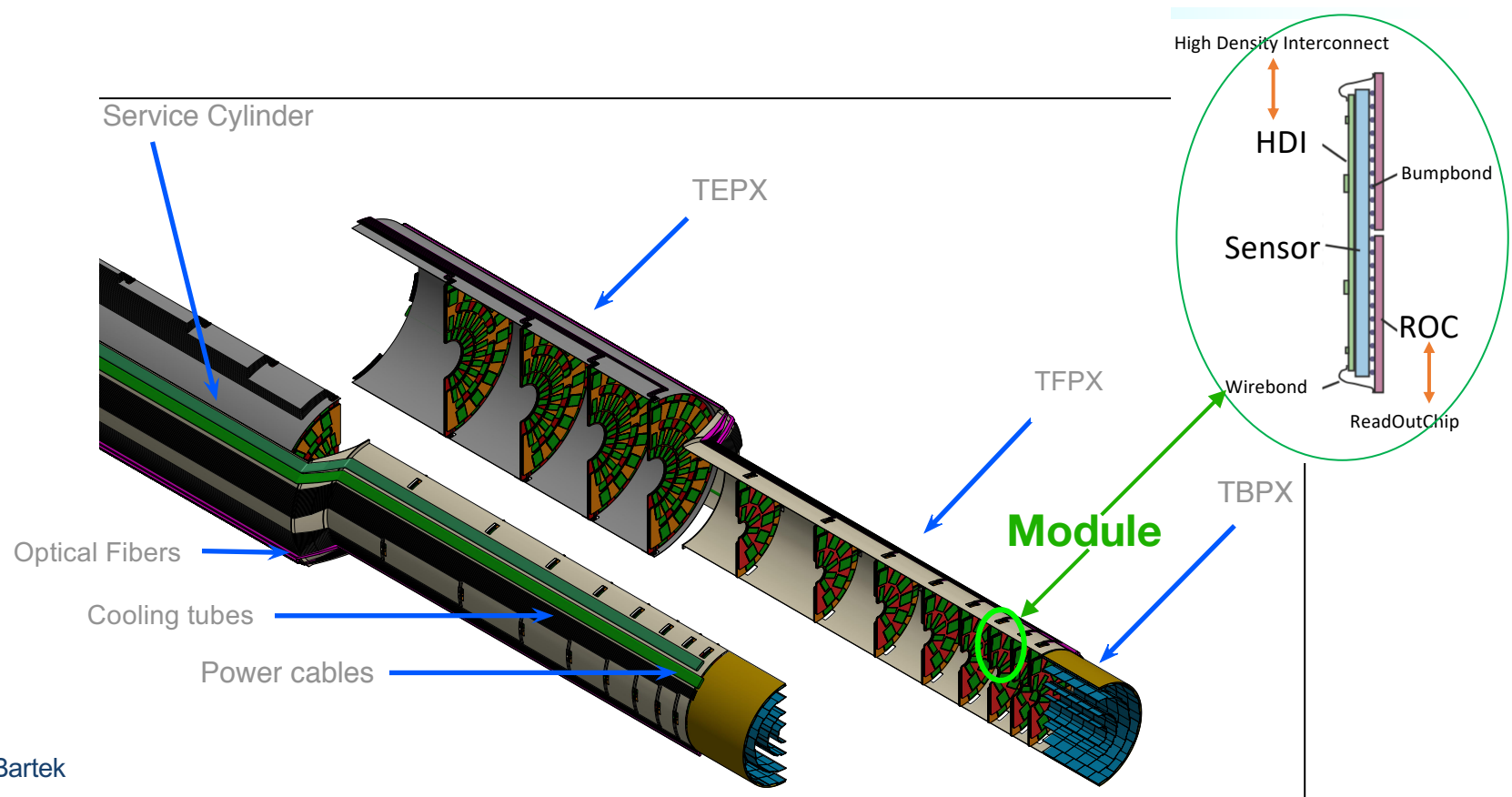
# Detector Layout

- 4 large discs on each side (TEPX)
  - *Each disc made of 4 identical dees*
- 8 small discs on each side (TFPX)
- 4 barrel layers (TBPX)
  - *No crack at  $z=0$*
  - *Two ladders per layer skewed in  $r\phi$  for the insertion of CMS*
- Two types of pixel modules: 1x2 and 2x2 readout chips per module
- Extended coverage up to  $|\eta| = 4$
- Innermost modules located at  $r = 2.75$  cm form the beamline



# Service Cylinders

- Simple installation and removal for quick maintenance without beam pipe removal
- Replacement of innermost layer/ring after long-shutdown 5



# Inner Tracker Sensors

- Decision Q4 2021
- Intense R&D program
- Baseline option:

- n-in-p planar, 150  $\mu\text{m}$  active thickness ( $\sim 1.7\text{kg}$  silicon), 25x100  $\mu\text{m}^2$  cell size

- Bitten implant, no punch-through bias dot
- Hit efficiency  $> 99\%$  after  $\sim 2.0 \times 10^{16} n_{\text{eq}}/\text{cm}^2$

- Alternatives being studied:

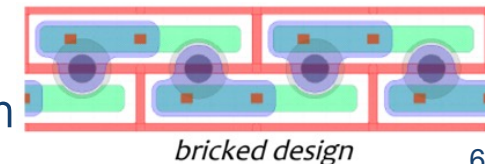
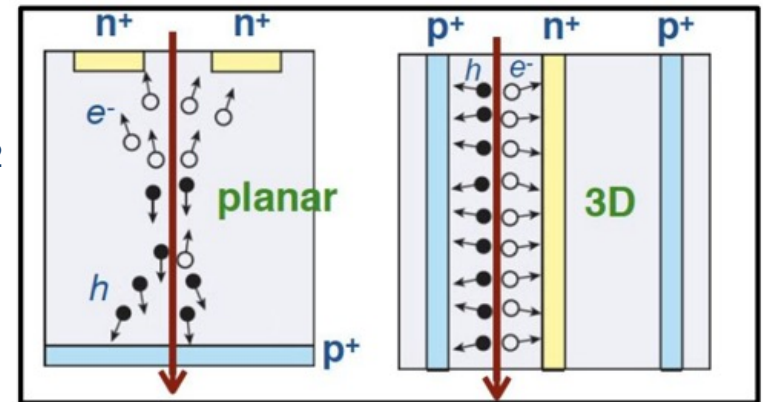
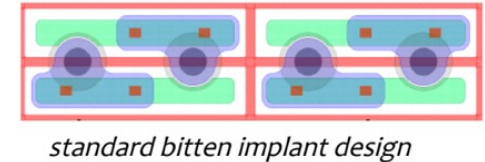
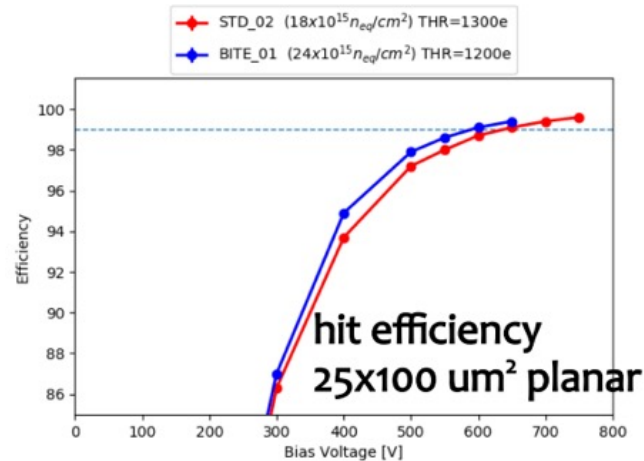
- 3D pixels for TBPX layer 1 and TFPX ring 1

- Better power consumption

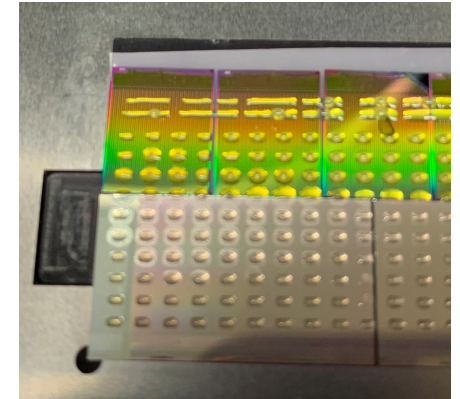
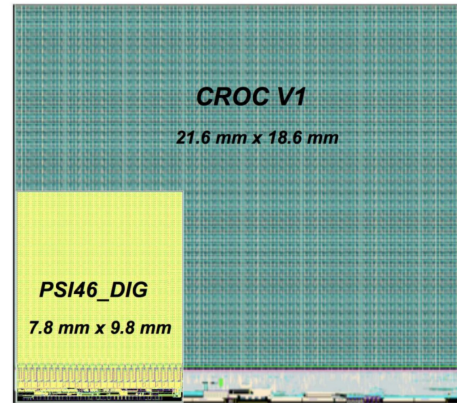
- Negligible degradation in hit resolution after  $1.0 \times 10^{16} n_{\text{eq}}/\text{cm}^2$

- 50x50  $\mu\text{m}^2$  still considered for disks

- Planar sensors with bricked layout in the central  $\eta$  region



# C-ROC

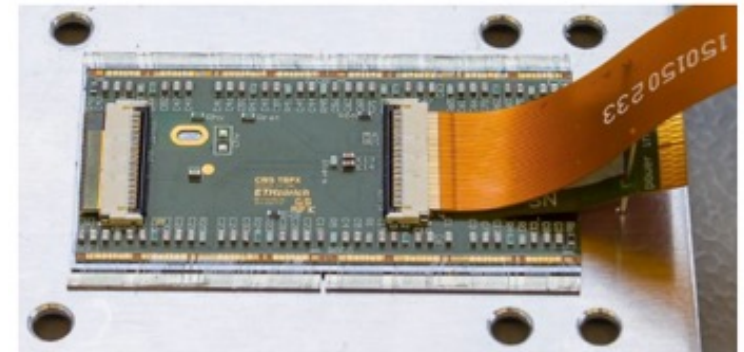
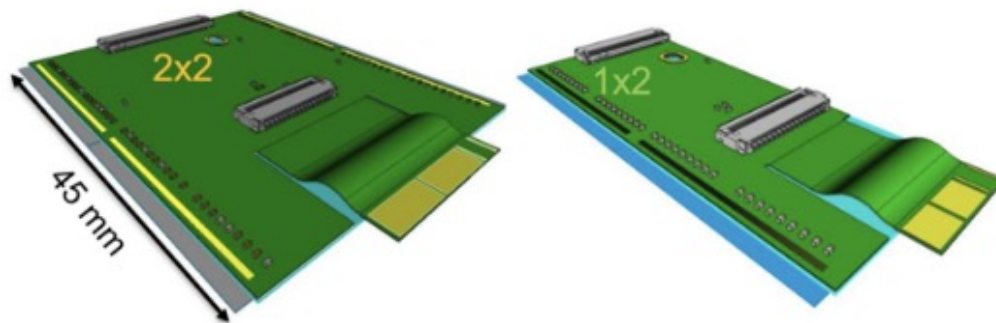
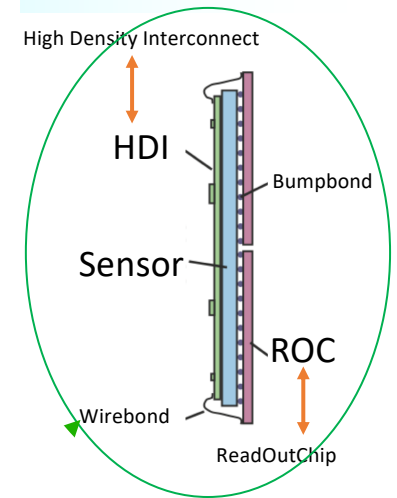


- ASIC is based on CMOS 65nm technology within the CERN RD53 project
  - Radiation tolerant up to 1 Grad (verified at high dose rate)
  - Robust against SEU effects
  - Bonding pad reticles fit both 50x50 and 25x100  $\mu\text{m}^2$  sensor options
  - Low power consumption  $< 1 \text{ W/cm}^2$  at max trigger rate (CMS Level1: 750 kHz)
  - Serial powering via on-chip shunt-LDO regulators (1 for analog, 1 for digital sections) to supply the needed 50 kW with a limited mass of the power cables
- CMS version of RD53 ROC (C-ROC) wafers back at CERN
  - Will be tested and green chips flip chipped
  - Full size ASIC: 432x336 channels
  - Analog FE linear architecture featuring an in-time threshold  $O(1000e)$
  - 4 bit digital readout with selectable 6-to-4-bit dual slope ToT mapping for charge compression (elongated clusters, heavy ionizing particles)



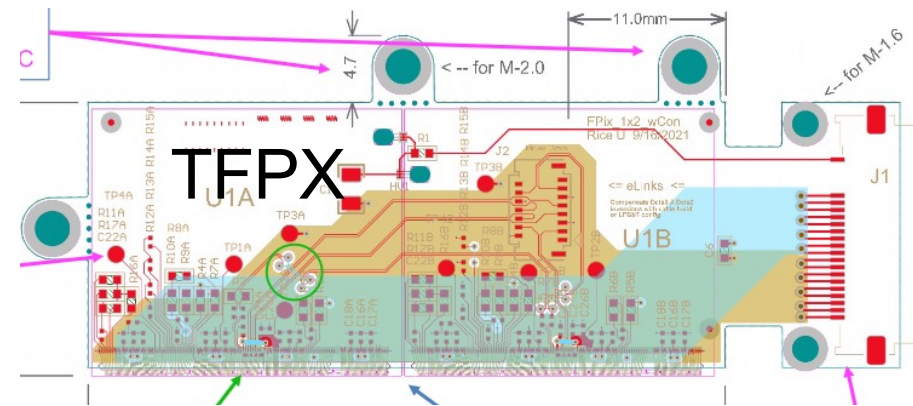
# Modules

- 3892 module plus spares (1156 1x2, 2736 2x2)
  - 2 Billion pixel (124 million in current detector)
- ROC only active electronics on modules
- Cable savers as molex connectors and twisted pair cables fragile
- Geometry constraints:
  - *TBPX*: Both faces of barrel ladders have modules so no service routing on backside with supply and return directly module to module
  - *TFPX* and *TEPX*: service routing on “inactive” surface

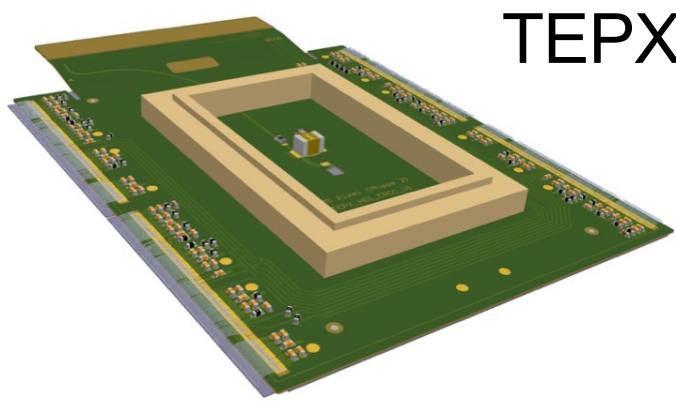




# HDI

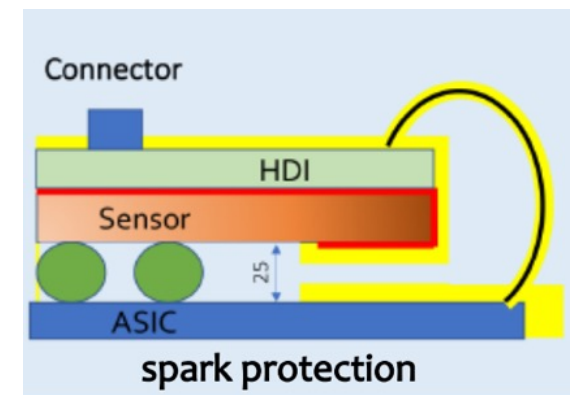
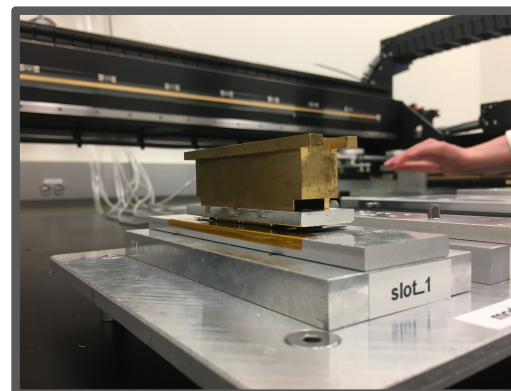
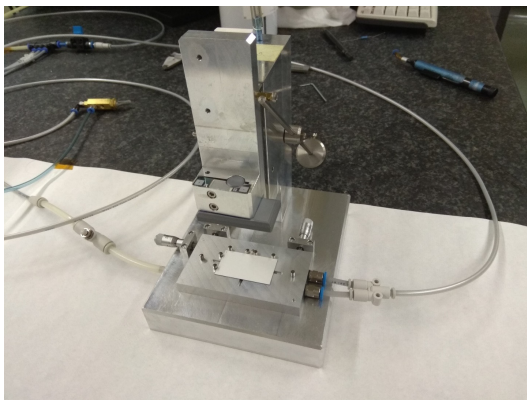
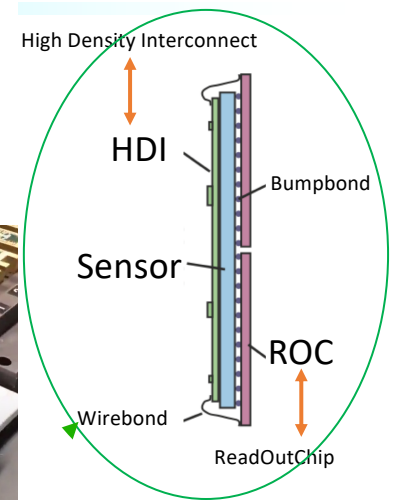
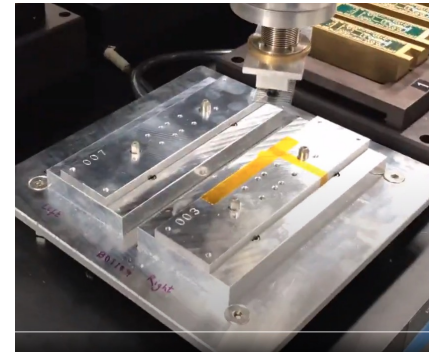


- Flexible PCB containing only passive components
  - *High precision resistors and decoupling capacitors*
- HDI contains return path for supply current
- Careful design for current paths to preserve low material budget
- HV capable of up to 1000 V



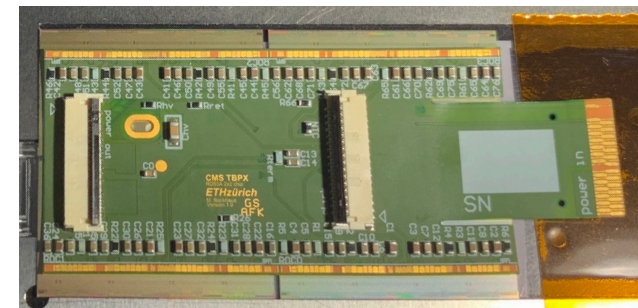
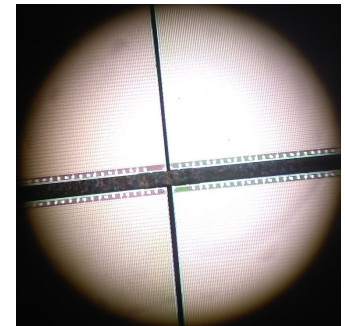
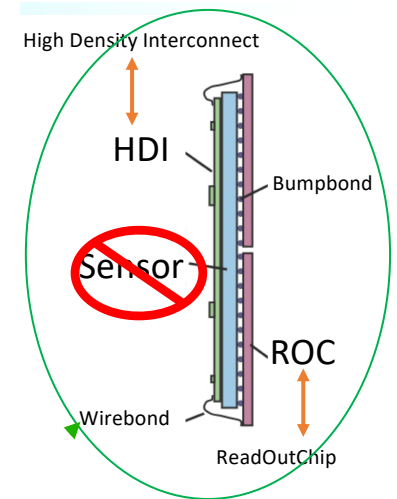
# Module Assembly

- Some modules assembled using jigs
- TFPX modules using robotic gantry
- Glue stamps and stencils used by assembly sites
- After HDI glued to module, aluminum wire bonds connect HDI and readout chip
- Paralyne-N coating for spark protection up to max operation voltage of 800V

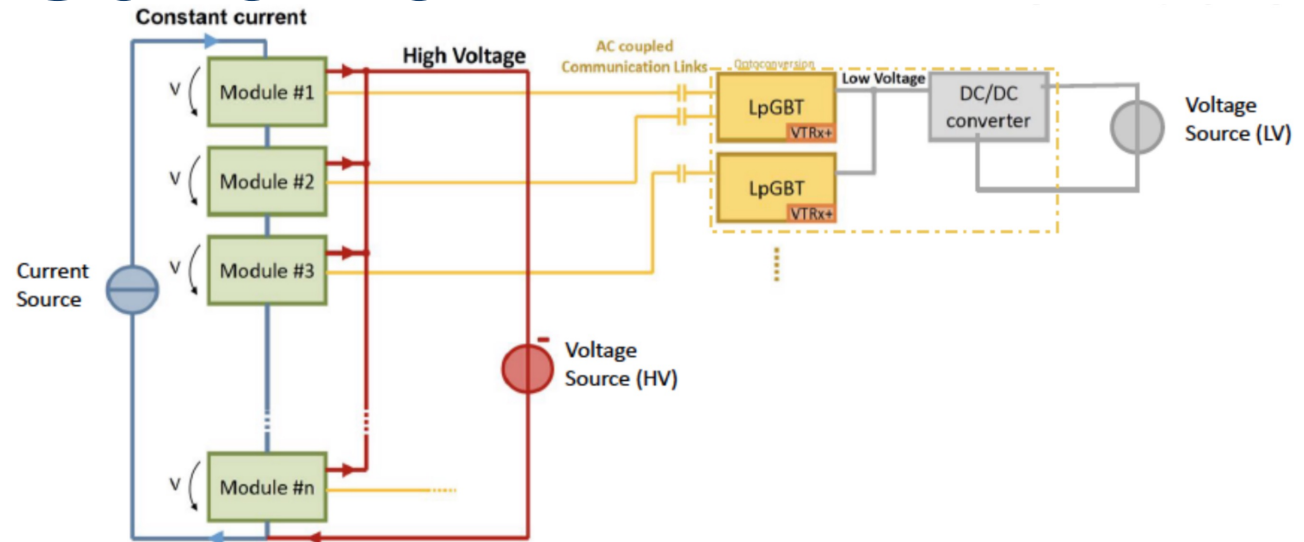
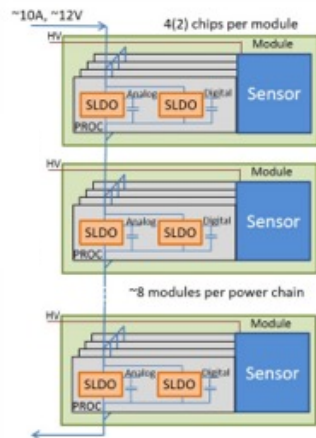


# Digital Modules

- Module with ROC and HDI only
- Useful for testing ROC, developing test stands, and establishing assembly procedures, optimizing bonding parameters
- Have made with RD53A chips
- Plan to make with CROC chips while other modules being flip chipped
- Challenge to leave some space between ROCs but have them positioned similar to bump bonded modules



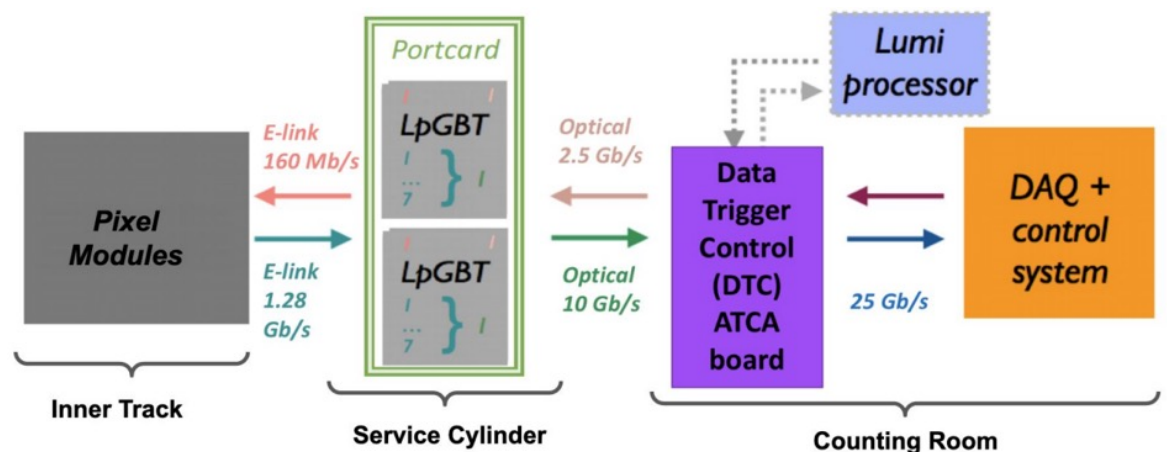
# Powering Scheme



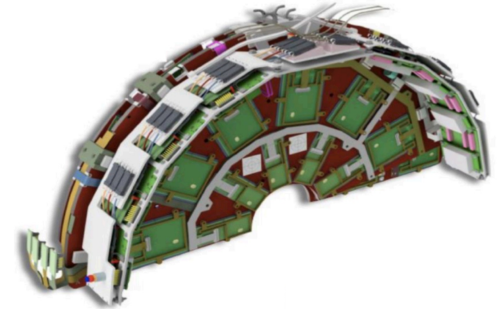
- Serial power
  - Modules grouped in 500 serial power chains, up to 12 modules in a chain
    - Modules powered in series, chips within each module powered in parallel
    - A shunt-LDO (SLDO) on each chip provides voltage regulation for each chip while maintaining a constant current
  - Chips in a module in parallel (4A for 1x2 modules, 8A for 2x2 modules)
  - Sensor bias following the serial power chains with single return line
  - Single power supply module: current source (SP), HV for sensor (0-800V), LV for portcards and pre-heaters required by CO<sub>2</sub> cooling
  - Only copper cladded aluminum wires in the detector volume

# Readout Architecture

- Custom ASICs, LpGBT, VTRX+
- Up to 6 electrical up-links at 1.28 Gb/s per module to LpGBT
  - *Data formatting to reduce data rates by half*
- One electrical down-link at 160 Mb/s per module from LpGBT
  - *Clock, trigger, commands, configuration data to modules*
- 28 Data Trigger Control boards required for inner tracker
- Portcards optoelectronic service card
  - *2x LpGBTs and VTRx+ links, powered via cascaded DC-DC converters*

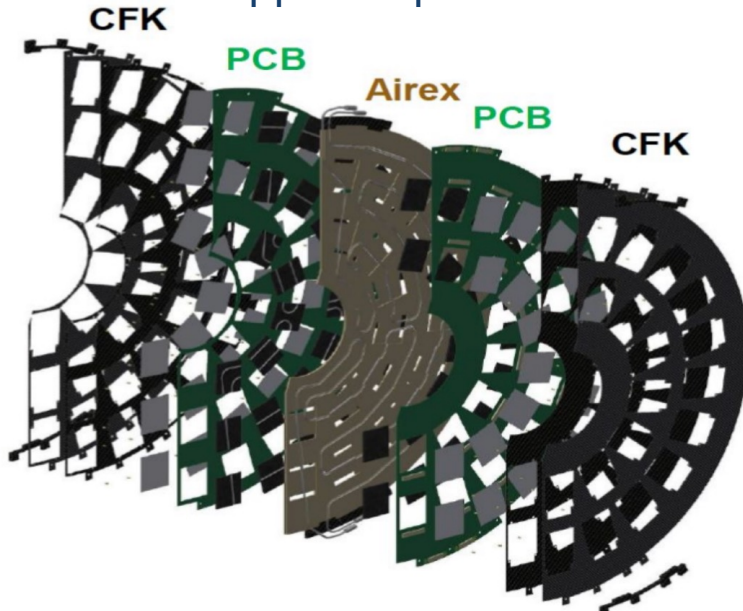


# Mechanical Support



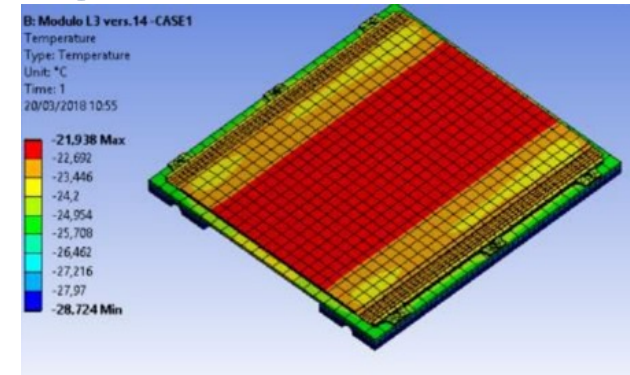
- Light Carbon Fiber structures with embedded cooling pipes
- Disks with flat geometry (unlike turbine in current detector)
- Improved fiber routing which reduces radiation induced attenuation
- Cooling based on evaporative CO<sub>2</sub> (T=-35°C) distributed in 1.8 mm outer diameter stainless steel pipes (168 cooling loops)

TEPX Support exploded view

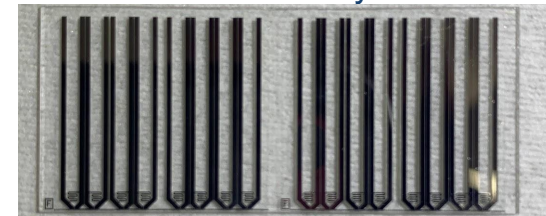


Dee composed of symmetric sandwich:

- Central layer CO<sub>2</sub> pipe and Airex foam
- Thermal Pyrolytic Graphite
- Electrical Isolation: Aluminum Nitride
- Dee-PCB with electrical services
- CFK panel and modules



Glass heaters to mimic module thermal needs to verify simulation



# Summary

- It is extremely challenging to design an inner tracking detector that can fully exploit the high instantaneous and integrated luminosity expected from the HL-LHC
- Prototyping phase is still on-going
  - *Several RD53A modules made to test sensor options*
  - *Digital modules made and being tested*
  - *Sensor technology decision expected soon*
- Construction will not mark the end of R&D efforts for the inner tracker as part will be replaced halfway through HL-LHC run
- The CMS HL-LHC upgrade is ambitious, by necessity, but major progress has been made