Upgrade of the Belle II Vertex Detector

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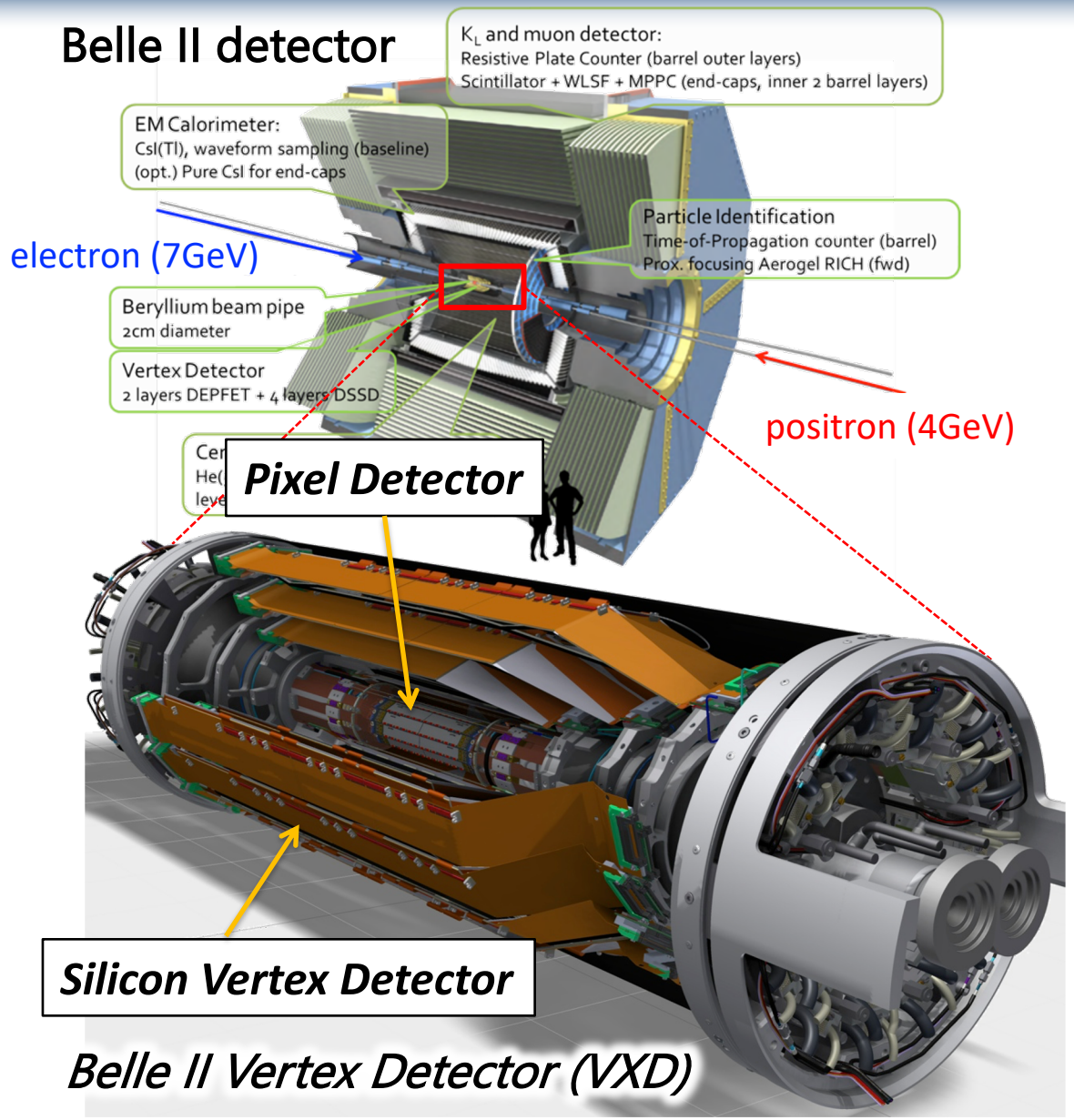
on behalf of the Belle II VXD upgrade collaboration

Sep 28, 2021

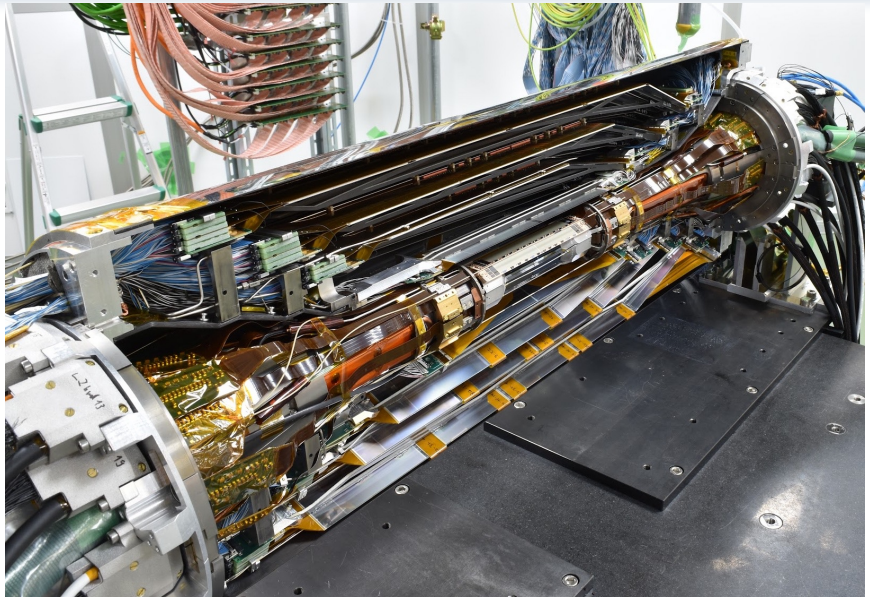
The 30th International Workshop on Vertex Detectors (VERTEX2021)

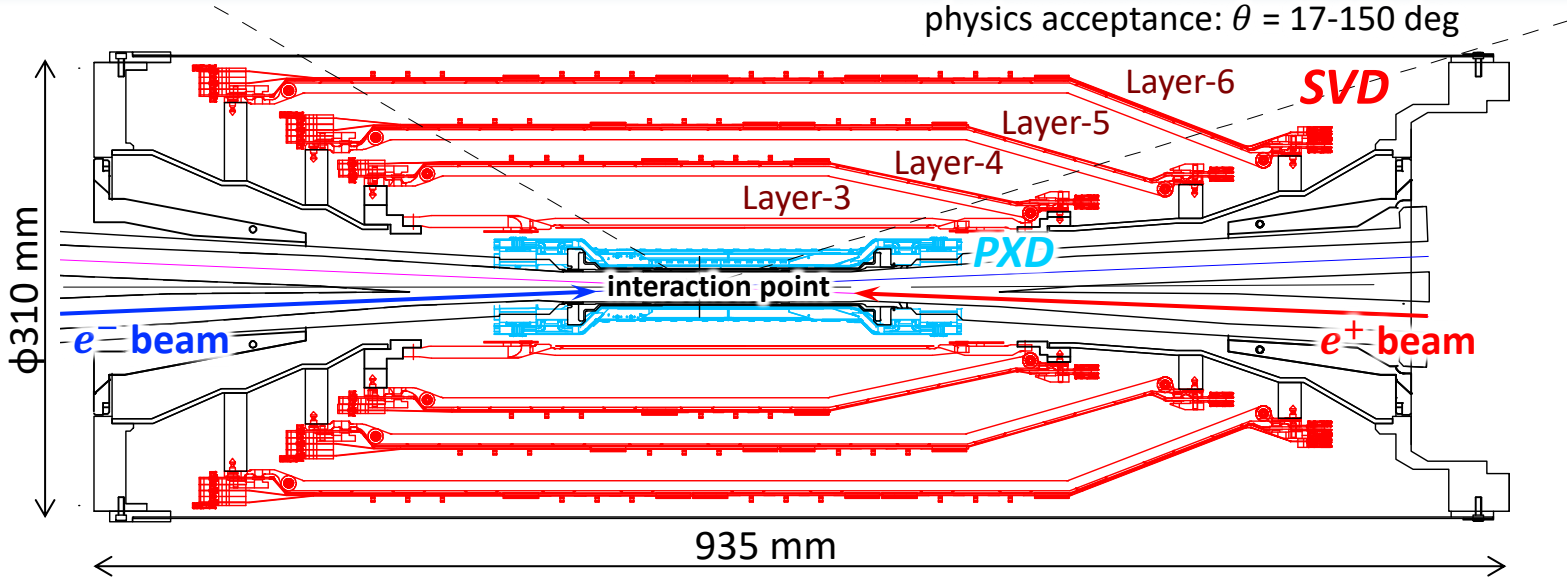
Vertex Detector at Belle II Experiment



- **Belle II experiment at SuperKEKB collider**
  - Luminosity-frontier experiment, exploring new physics beyond the standard model
  - Asymmetric e^+-e^- collisions at $\sqrt{s}$ = 10.58 GeV
  - Target integrated luminosity: 50 ab^{-1}
  - Target instantaneous luminosity: L ~ 6 x 10^{35} $cm^{-2}s^{-1}$
- **Vertex detector (VXD) in Belle II**
  - 2 layers of PiXel Detector (PXD): DEPFET sensor
  - 4 layers of Silicon Vertex Detector (SVD): Double-sided silicon strip (DSSD) sensor
- **Roles of VXD**
  - Determine the vertex position
  - Standalone tracking
  - PID using SVD dE/dx for low p_T tracks
- **Central Drift Chamber (CDC): Outer tracking detector in Belle II**
  - Radial coverage: 168mm<R<1111mm

Current VXD





Pixel Detector (PXD): DEPFET sensor

- **Radius:** 14mm (L1), 22mm (L2)
- **Sensor thickness:** 75μm
- **Material budget:** 0.2%X_0 per layer
- **Pixel size:** 50μm x 55-85μm
- **Long integration time:** 20μs
  - Hit occupancy reduction by Region-of-Interest (RoI) selection using SVD tracks

PXD talk by B. Wang (Sep 27)

Silicon Vertex Detector (SVD): DSSD sensor

- **Radius:** 39mm(L3), 80mm(L4), 115mm(L5), 140mm(L6)
- **Sensor thickness:** 300-320μm
- **Material budget:** 0.7%X_0 per layer
- **Readout strip pitch (P/N):** 50μm/160μm (L3), 50-75μm/240μm(L4-6)
- **Hit time resolution (P/N):** ~2.9ns/2.4ns

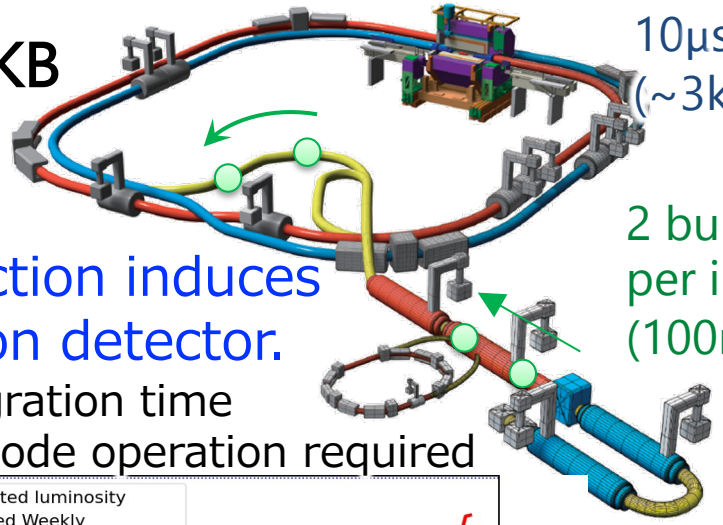
SVD talk by Y. Uematsu (Sep 27)
+ Cluster position resolution by R. Leboucher, Simulation by M. Kaleta (YSF)

VXD Operation in Belle II

Successful VXD operation at present

under continuous beam injections
- to keep constant beam currents
- max.25Hz injection to each beam

SuperKEKB

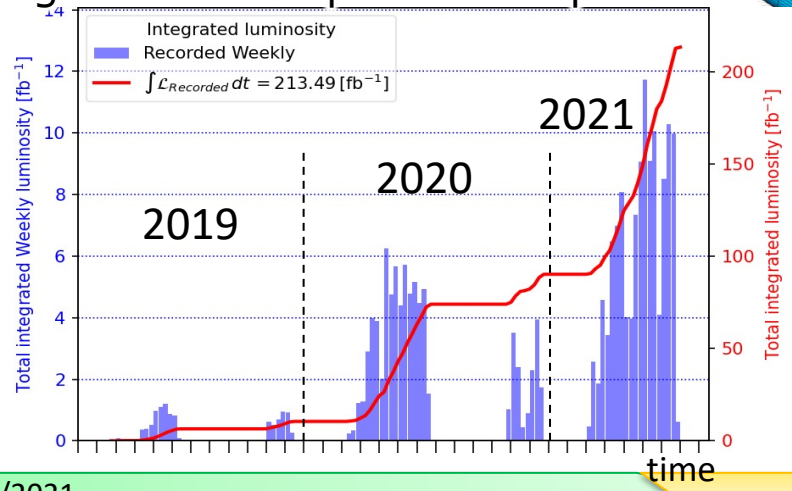


10μs revolution time
(~3km circumference)

2 bunches
per injection
(100ns spacing)

Every injection induces beam BG on detector.

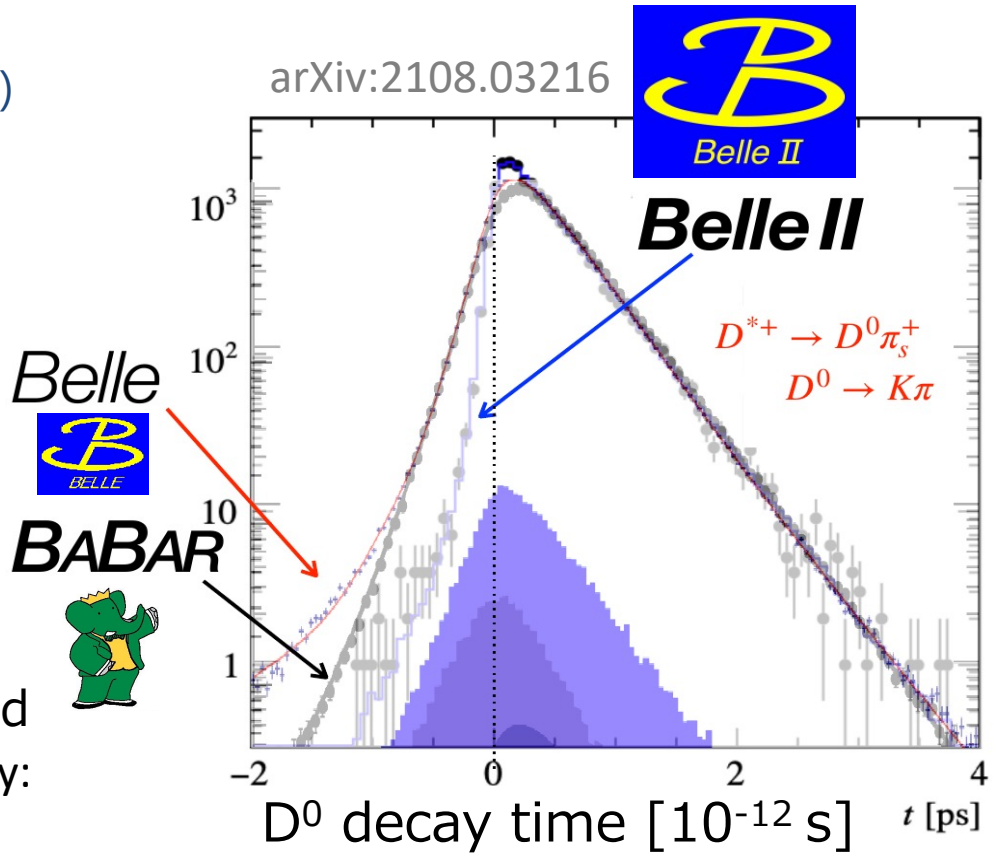
→ short integration time
or gated-mode operation required



So far,
213 fb-1 accumulated
Recorded peak luminosity:
3.12×10^{34} cm^{-2}s^{-1}

Improved vertexing performance

- confirmed by D lifetime measurement
- Resulting time resolution in Belle II is better than Belle/BaBar by factor about 2

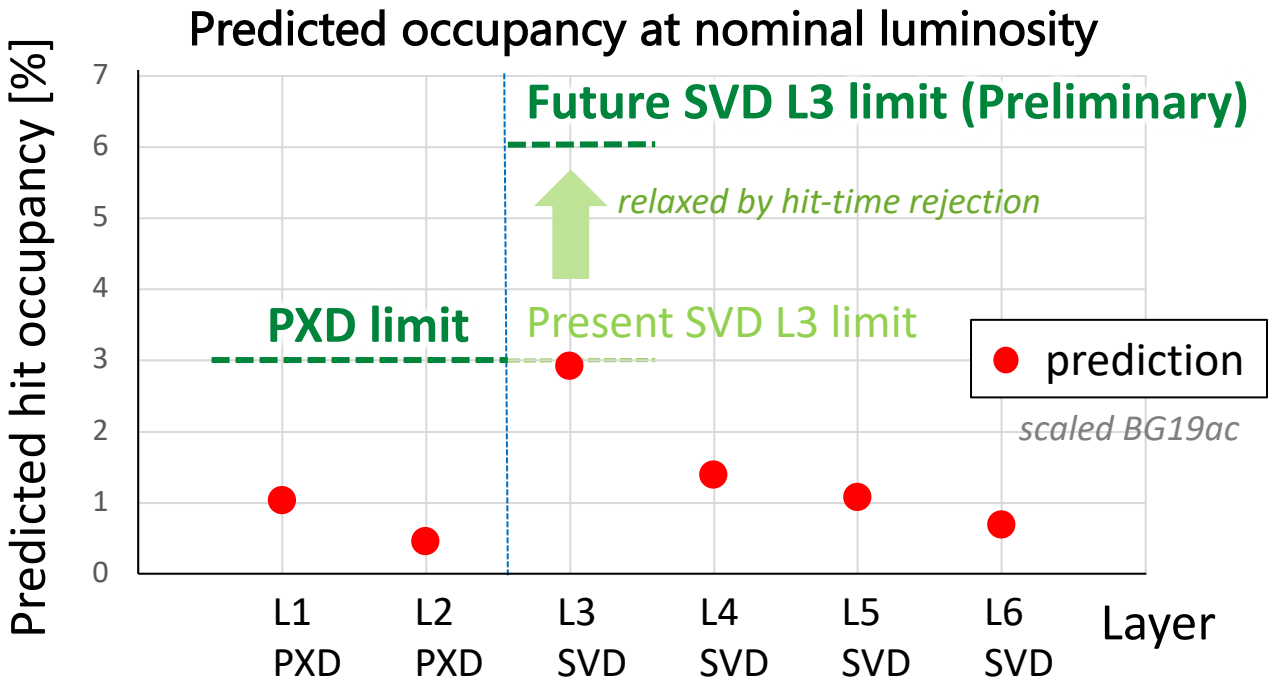


D^0 decay time [10^{-12} s]

World's most precise D lifetime measurements

Limits on current VXD

Tolerance for beam-induced background (BG)



- SVD limit will be relaxed by hit-time BG rejection ☺
- Difficulty of accurate prediction for injection BG and collimator condition at design luminosity ☹
- Drastic change in beam optics for design luminosity → large uncertainty ☹ (β_y^* = 1.0mm → 0.3mm)

No big margin...

Tracking and vertexing performance

- Tracking performance in low-p_t limited by material budget
- Room to improve vertex resolution with better hit position resolution
- Improvement in K_S vertexing desirable

Latency of Level-1 trigger

- Belle II trigger latency is limited to 5.0μs by SVD (depth of APV25 ring-buffer)

So in summary,

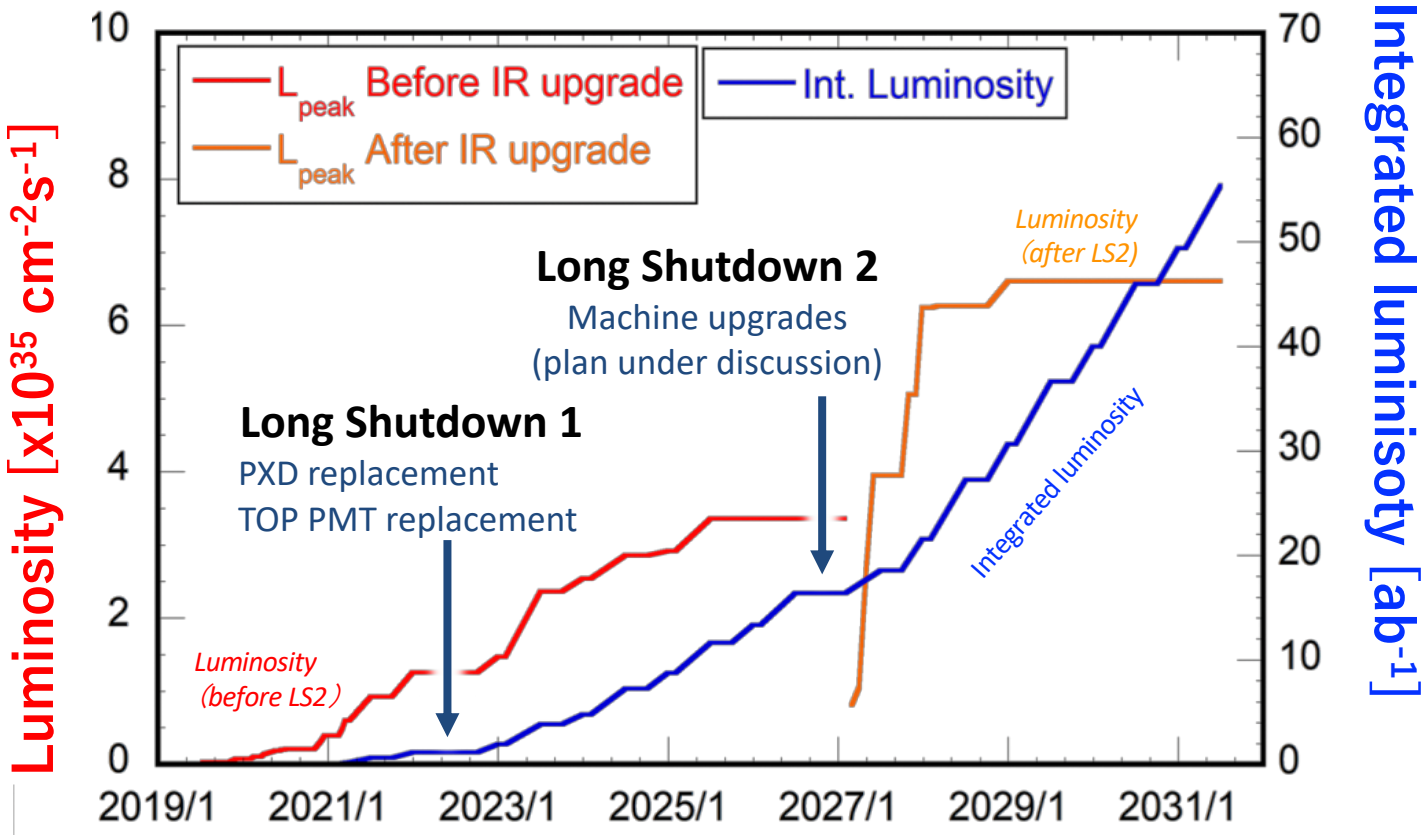
- **Predicted BG within limits, BUT without enough safety margin**
- **Also performance improvement highly desirable**

Timescale of the VXD upgrade project

- **2nd long shutdown for SuperKEKB intermediate upgrade**
  - – Timeframe expected to be 2026-2027, but still with uncertainty
    - Detailed SuperKEKB upgrade plans are under discussion with the international taskforce teams.
  - – Opportunity for large upgrades of Belle II subdetectors
  - – Preparation to be done in several years
    → Currently available technologies preferable

Target of on-going VXD upgrade project

SuperKEKB/Belle II operation projection



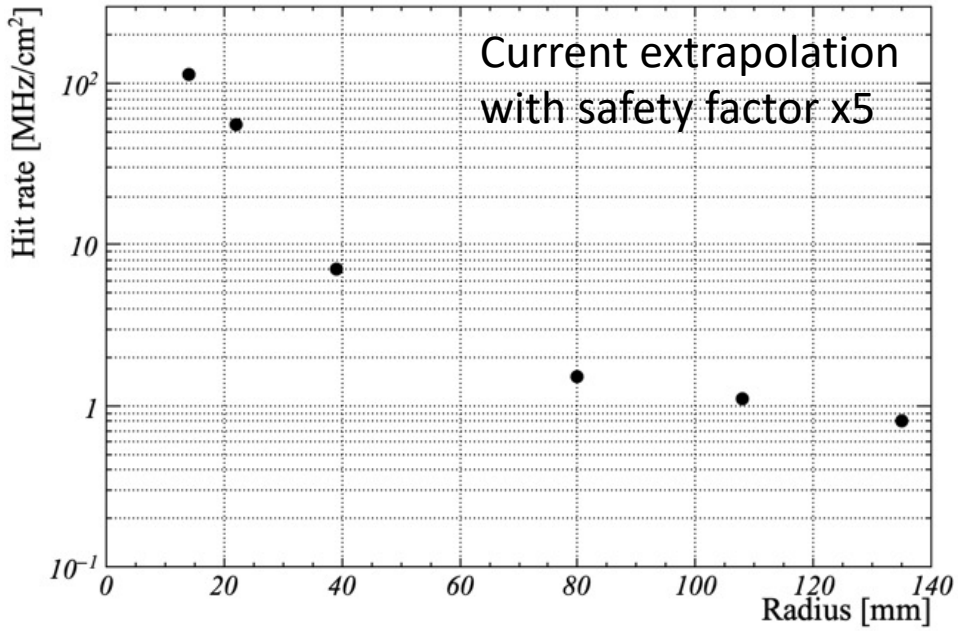
Requirements for the VXD upgrade

Requirements

Radius range: R	14 – 135 mm (**)
Tracking & Vertexing performance at least as good as current VXD	
Single point resolution(*)	< 15 um
Total material budget	< (2x 0.2% + 4x 0.7%) X_0
Robustness against radiation environment current extrapolation with safety factor x5	
Hit rate(*)	~ 120 MHz/cm^2
Total Ionizing Dose(*)	~ 10 Mrad/year
NIEL fluence(*)	~ 5.0 × 10^{13} n_{eq}/cm^2/year

(*) requirement for the innermost layer (R=14mm)
(**) Optionally, we may include also the CDC inner region (135<R<240mm)

Required hit rate tolerance vs. Radius



Possible other improvements by upgrade

- Impact parameter resolution
- Tracking performance for low-p_T tracks
- Longer trigger latency
- Capability of Level-1 trigger creation

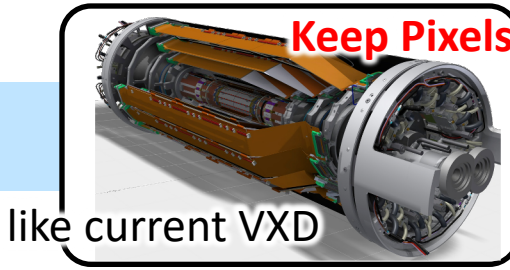
Strategy of upgrade R&D

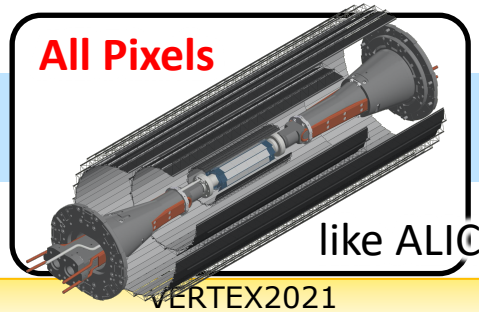
- **Several technology options under investigation by R&D subgroups**
- R&D activities will access the options
  - Which concepts bring best performance?
  - Which technology fit requirements?
  - Which technology fit timeframe of installation?
- CDR to be prepared within ~1 year w/ full-scale prototype test and physics benchmarking
  - and then TDR (w/ full technical description) as well

Several technology R&D subgroups

- Thin DSSD sensor
- DEPFET pixel sensor
- SOI pixel sensor
- CMOS pixel sensor

Detector concept





Performance evaluation

Common analysis framework

w/ different geometries and digitizers

- For systematic performance study of multiple options
- For less development cost and resources

under preparation

R&D subgroup (1): Thin DSSD sensor

Thin/fine-pitch SVD (TFP-SVD) concept

Targets

- Outer layers
- Handle higher hit-rate
  - O(1MHz/cm^2) R>4cm
- Improve tracking/K_S vertexing performance

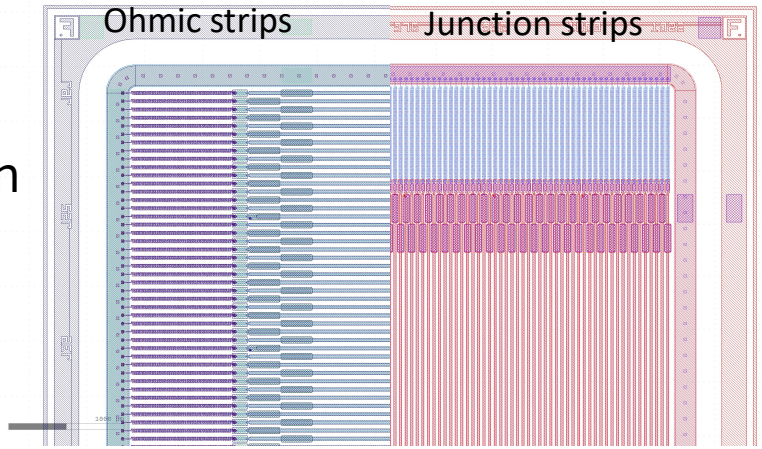
Thin DSSD sensor

Thinner sensor: 140um
- Produced by Micron

Finer N-side strip pitches than SVD: ~85um

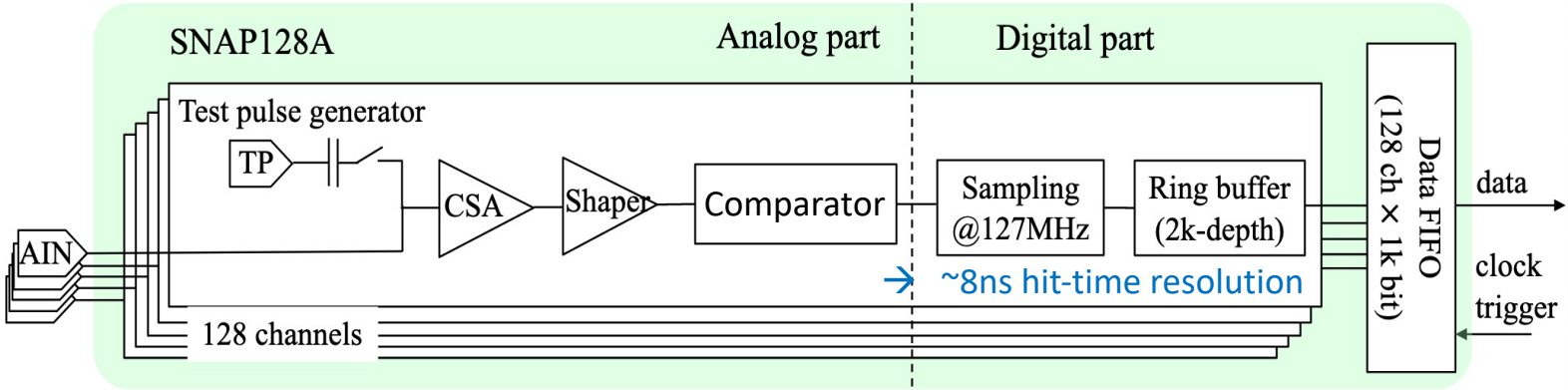
→ **R&D challenges in front-end**
- Noise (smaller signal)
- Heat dissipation (larger # of channels)

TFP-SVD DSSD layout



Dedicated front-end ASIC (SNAP128A)

- 180nm CMOS process by Silterra
- Short signal pulse width: ~55ns (simulation)
- Better noise characteristic and less power consumption than SVD
  - simulated noise: ~640e$^-$ @ C_{det}=12pF
- Binary hit readout
  - to reduce cables



R&D subgroup (1): Thin DSSD sensor

DSSD 1st prototype

- Three protptype sensors delivered

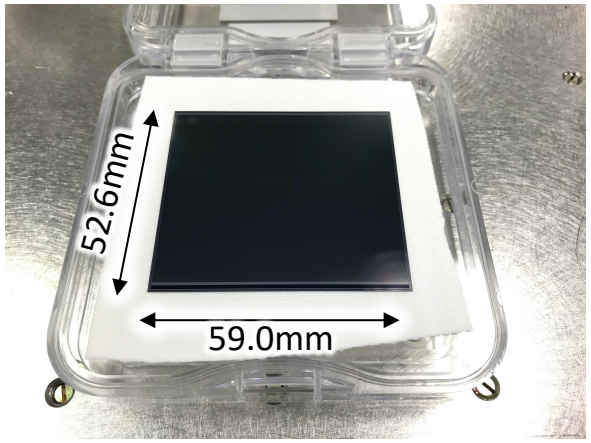
Basic characterization in Micron

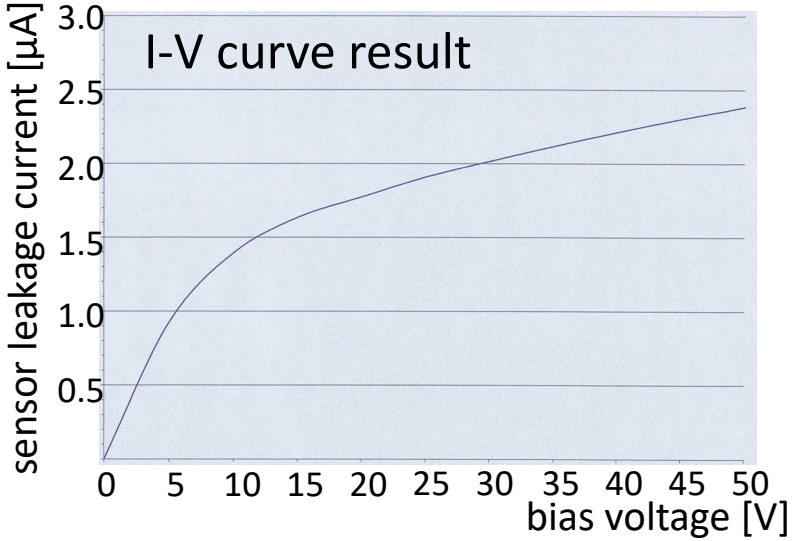
- Reasonable I-V and C-V results
- Thickness: 148±5um
- Full depletion voltage: 14±1 V

Specification of prototype ver.1

Sensor dimension	52.6 mm x 59.0 mm (rectangle)
Active area	51.2 mm x 57.6 mm
Sensor thickness	140 um ± 10um
Junction (P-side) strip	
P-side strip pitch	50 um
P-side strip width	14 um
P-side # of strips	1024
P-side floating string	no floating strip
Ohmic (N-side) strip	
N-side strip pitch	75 um
N-side strip width	14 um
N-side # of strips	768
N-side floating string	no floating strip

DSSD prototype



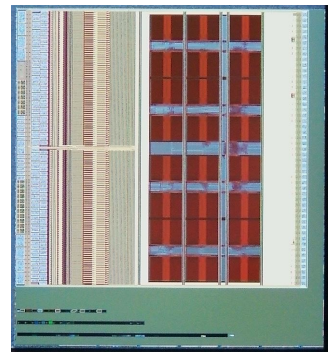


SNAP128A: 1st prototype

- All necessary functions both analog and digital integrated
- Being tested in KEK
  - Amp/shaping part and digital part working
  - Reasonable power consumption: 329mW

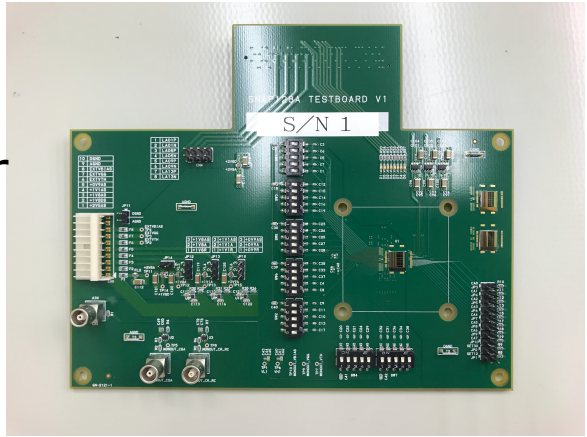
SNAP128A

128ch inputs



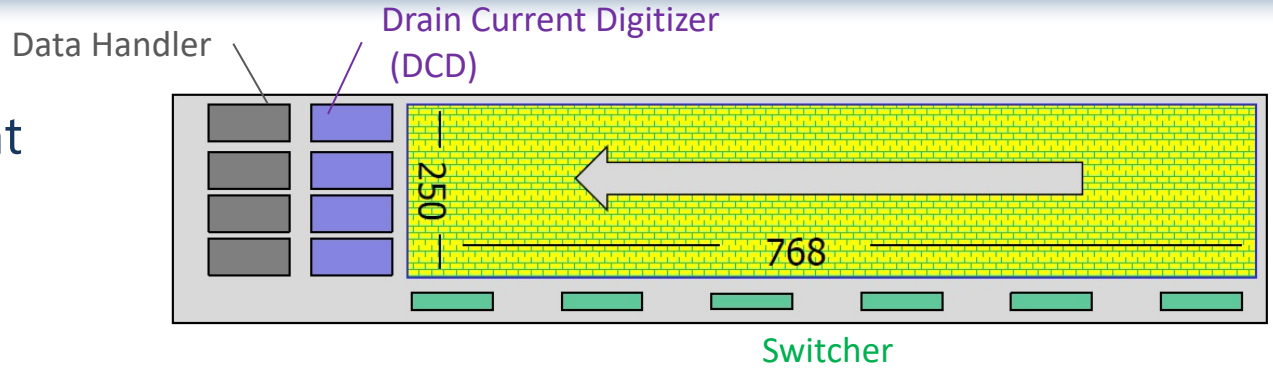
- To be assembled with DSSD to evaluate detector performance in early 2022

SNAP128A test board



R&D subgroup (2): DEPFET pixel sensor

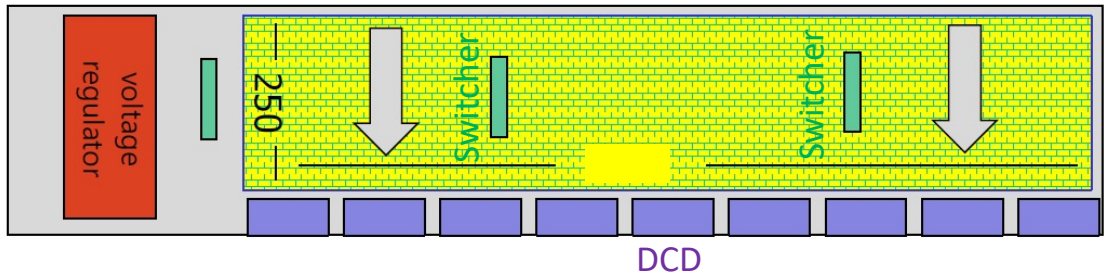
- **Current Belle II PXD**
  - First use of the technology in HEP experiment
  - Current integration time: 20 μs



- **Sensor R&D**
  - Gain increase with shorter FET length L
    - higher amplification in pixel → thinner oxide
      → improved radiation tolerance

$$g = \frac{\mathrm{d}I_{\mathrm{drain}}}{\mathrm{d}Q} \propto \sqrt{\frac{t_{\mathrm{ox}}}{L^3}}$$

  - Extend Cu interconnection layer into pixel array
    - improve the signal integrity of fast signals (e.g. “clear” and “gate”)
- **ASIC R&D**
  - Faster driving and readout circuit
    - Integration speed x2
- **More aggressive option**
  - Rotate readout direction of pixel array by 90°
    - Additional improve on integration speed x3

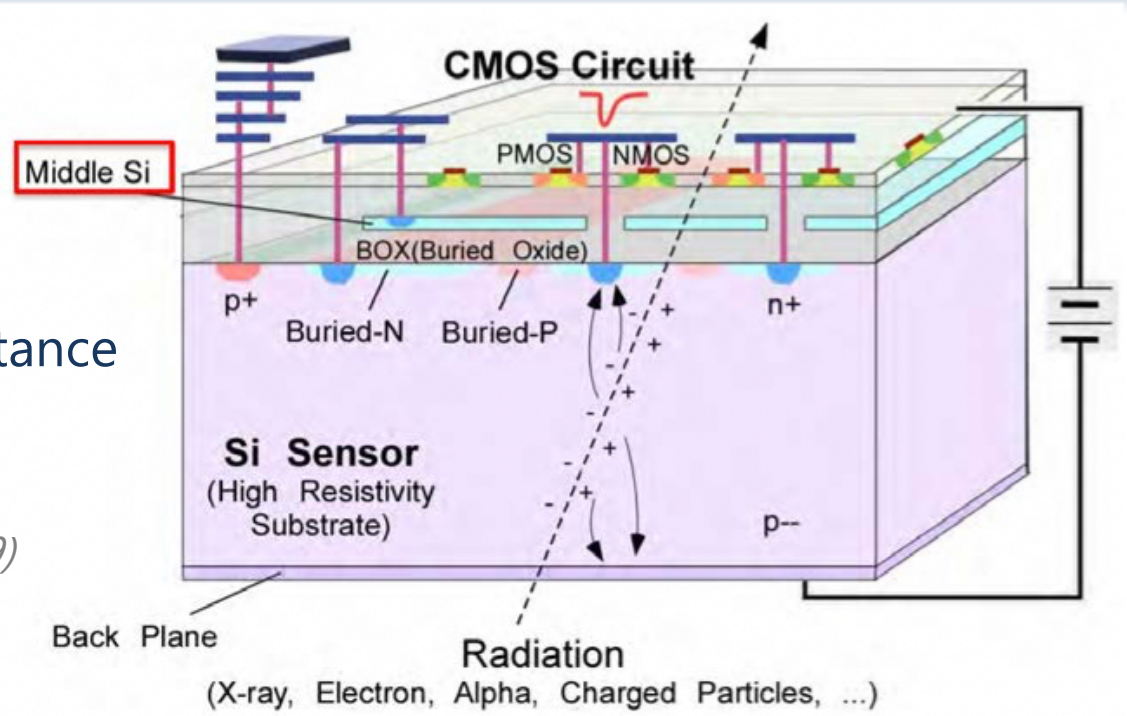


R&D subgroup (3): SOI pixel sensor

Silicon-On-Insulator pixel (SOIPIX)

- CMOS circuit produced on silicon wafer isolated by a buried oxide (BOX) layer
  - Full depleted sensor: Fast signal, good S/N
  - Logics w/o well structure: High density, small capacitance
  - Complex circuit can be implemented in each pixel
- Produced by LAPIS semiconductor

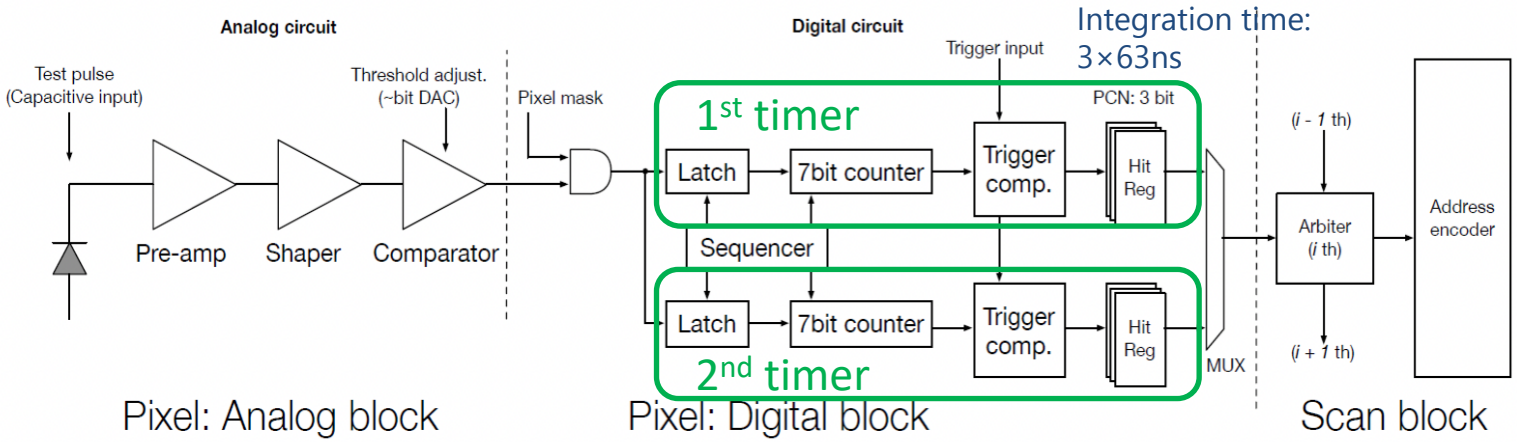
SOI talk by T. Miyoshi (Sep 29)



Dual Timer Pixel (DuTiP) concept

- Alternative operation of two timers allows the next hit before the trigger arrival for the previous hit.
  - Hit loss probability due to pile-up expected to be ~0.03% at 113MHz/cm^2 (assuming 8us trigger latency)

Rough estimation of final power consumption: about 0.1 W/cm^2



R&D subgroup (3): SOI pixel sensor

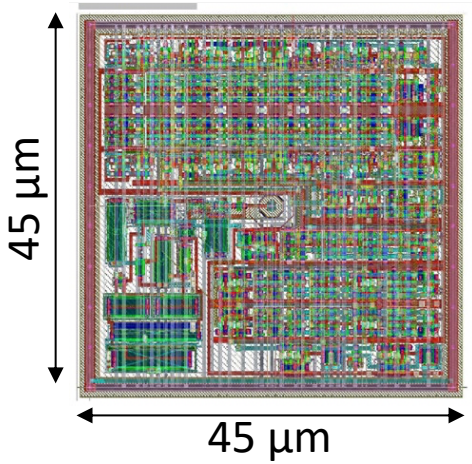
DuTiP 1st prototype

Chip size	6x6 mm^2
Pixel size	45x45 μm^2
Thickness	50 $\mu m^{(*)}$
Clock	15.9 MHz (63ns)
Expected noise	about 86 e^-

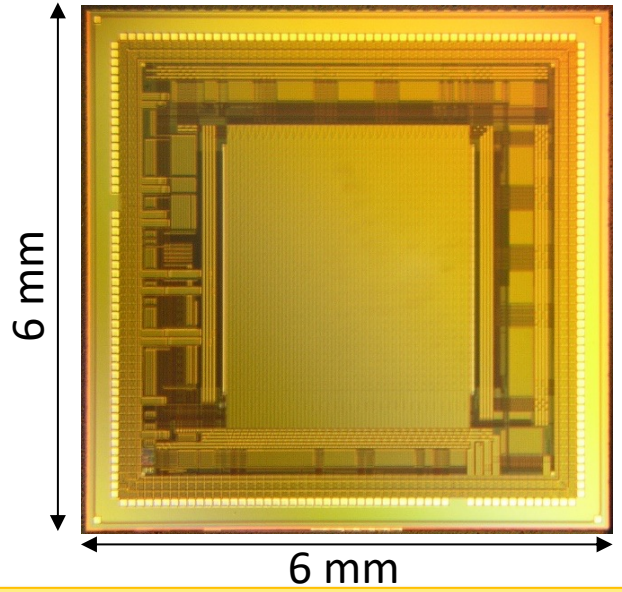
(*) chip to be thinned to 50um in future

- **Circuits already fabricated**
  - Modified ALPIDE (low power) analog circuit
  - Basic in-pixel digital circuit
- **Circuits still to be fabricated**
  - Sophisticated pixel scanning circuit

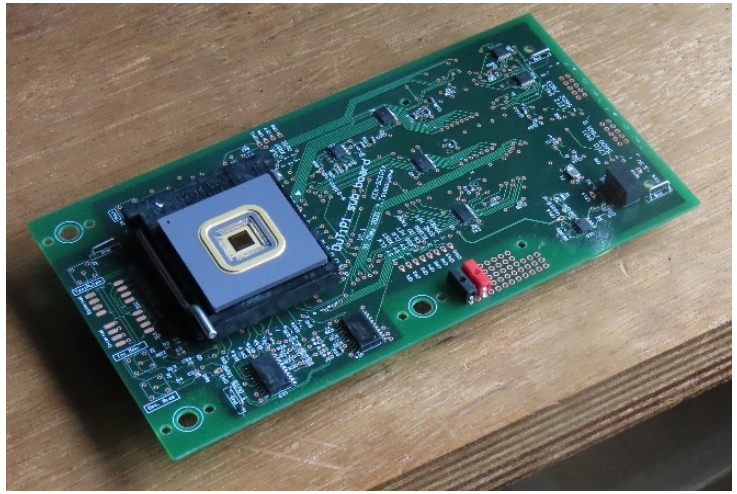
Pixel layout



DuTiP 1st prototype



Sensor evaluation board



Prototype performance evaluation on-going

- digital part working as expected

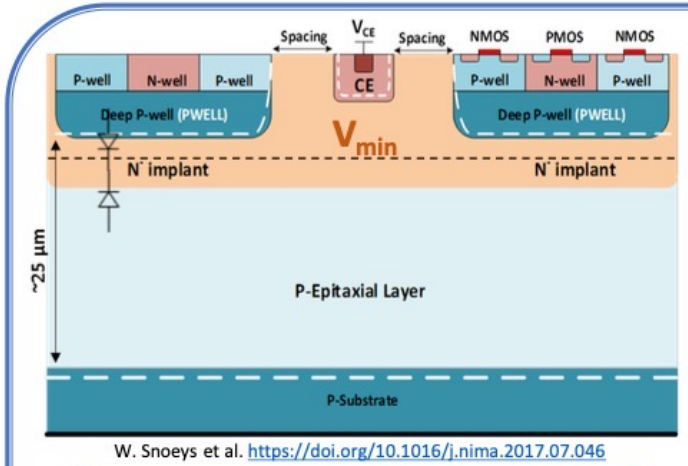
Beam test to be performed

DuTiP 2nd prototype plan

Plan to submit by the end of 2021 (depends on MPW schedule)

- Full functionality
- Semi-final chip size

R&D subgroup (4): CMOS pixel sensors



W. Snoeys et al. https://doi.org/10.1016/j.nima.2017.07.046

DMAPS in TJ 180 nm: Concept

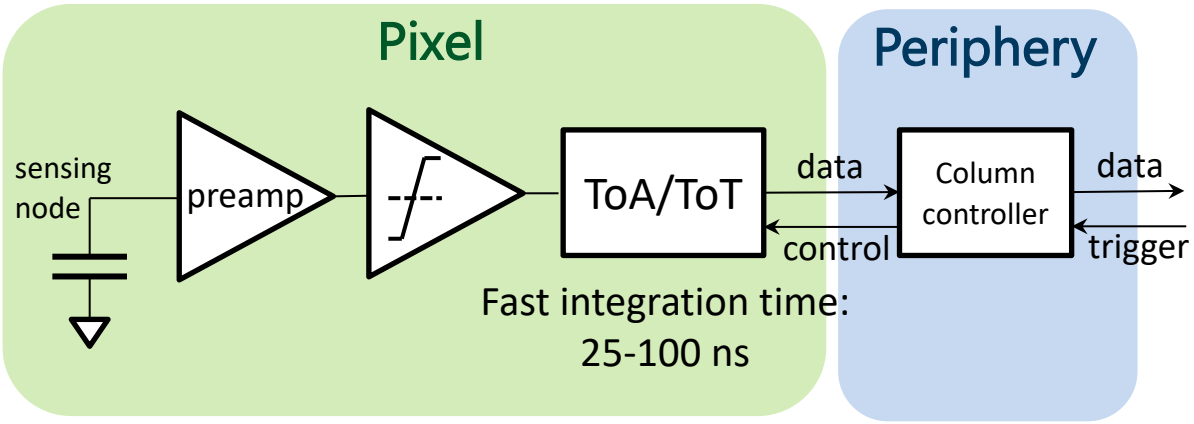
- Small sensor capacitance (Cd)
  - Key for low power/low noise
- Radiation tolerance challenges
  - Modified process
  - Small pixel size
- Design challenges
  - Compact, low power FE
  - Compact, efficient R/O

$C_d \leq 3fF$

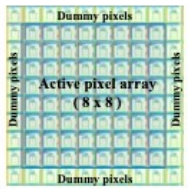
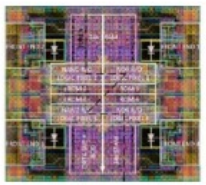
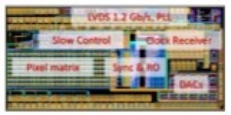
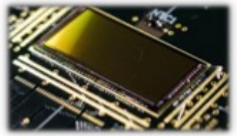
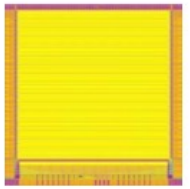
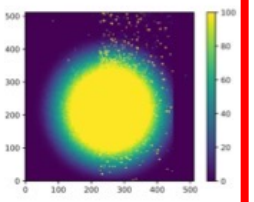
$P \approx \frac{S}{N} \approx \frac{Q}{C_d}$

DMAPS talk by J. Dingfelder (Sep 29)

TJ-Monopix readout scheme



We are here now

TJ-Investigator characterization	TJ-Monopix1 & MALTA Design	TJ-Monopix1 & MALTA Submission	Mini-MALTA sub. with process fixes	TJ-Monopix1 resub. process fixes & Cz	TJ-Monopix2 & MALTA2 Design	TJ-Monopix2 & MALTA2 Submission	TJ-Monopix2 Characterization	"OBELIX" Design
								Full scale System-ready: LDO, CDR, memory etc.
Q2 2016	Q4/2016	Q3/2017	Q3/2018	Q2/2019	Q2/2019	Q3/2020	Present	Future plans

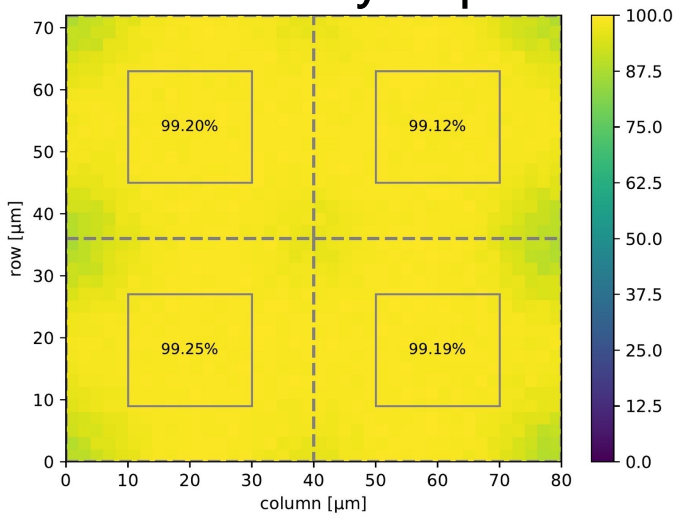
R&D subgroup (4): CMOS pixel sensors

TJ-Monopix1

Characterization started in 2018

- Noise, threshold, gain, hit efficiency, and radiation hardness

Efficiency map



300 µm Cz: 98.6% @ 490 e^-
(with 10^{15} n_{eq}/cm^2 irradiation)

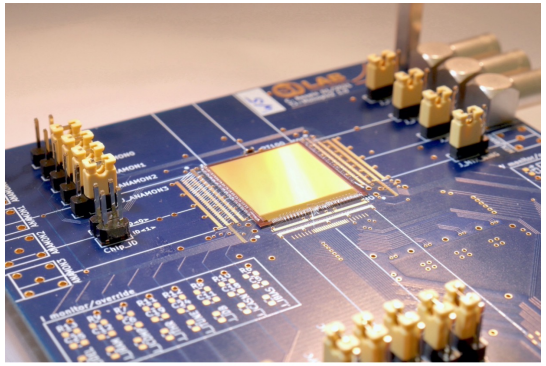
TJ-Monopix2

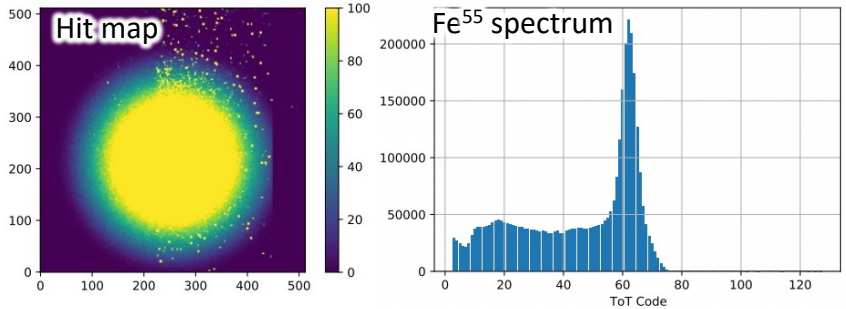
Chip size: 2x2 cm^2

Chip is alive and working

- Synchronization, configuration, DACs
- Analog pixels respond to injection
- Chip detects radiation

Analysis of beam test data on-going





Proof-of-principle prototype

Specification

	TJ-Monopix2
Chip Size	2x2 cm^2 (512x512 pix)
Pixel size	33.04 × 33.04 μm^2
Total matrix power	170 mW/cm^2
Noise	< 8 e^- (improved FE)
LE/TE time stamp	7-bit
Threshold Dispersion	< 10 e^- rms (improved FE + tuning)
Minimum threshold	< 200 e^-
In-time threshold	< 250 - 300 e^-
Efficiency at 10^{15} n_{eq}/cm^2, 30 µm epi	> 97 %
Efficiency at 10^{15} n_{eq}/cm^2, Cz	> 99 %

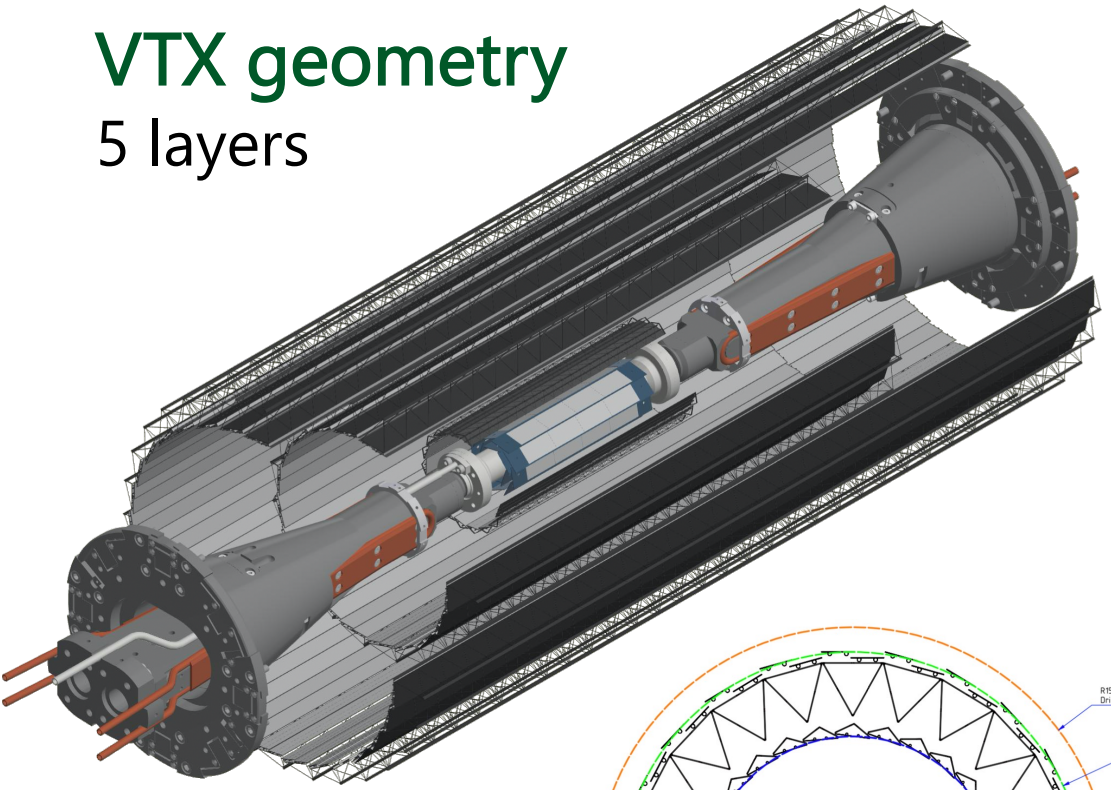
(red) Expectations

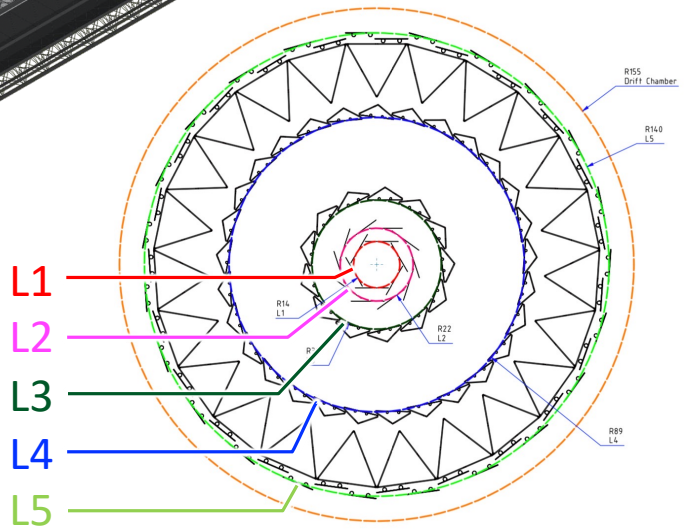
More details about measured performance of TJ-Monopix will be presented in J. Dingfelder's talk (Sep 29).

VTX: An integrated design for fully pixelated option

VTX geometry

5 layers

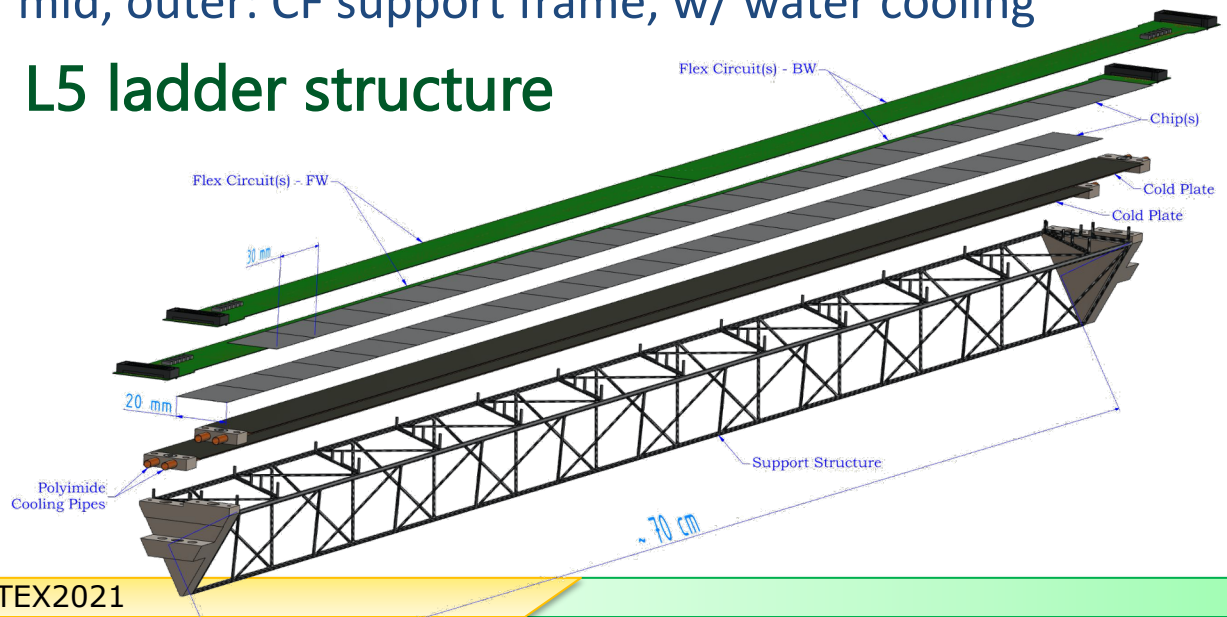




General concept of VTX

- **Fully pixelated detector with CMOS sensors**
  - Chip size: 2x3 cm^2 (same chip in all layers)
- **Low material budget:**
  - sensor thickness ~50 µm
  - 0.1%X_0 (L1-2) / 0.3%X_0 (L3-4) / 0.8% X_0 (L5) per layer
- **Different integration among inner (L1-2), middle (L3-4), and outer (L5) layers**
  - inner: Self supportive silicon ladders, w/ air cooling
  - mid, outer: CF support frame, w/ water cooling

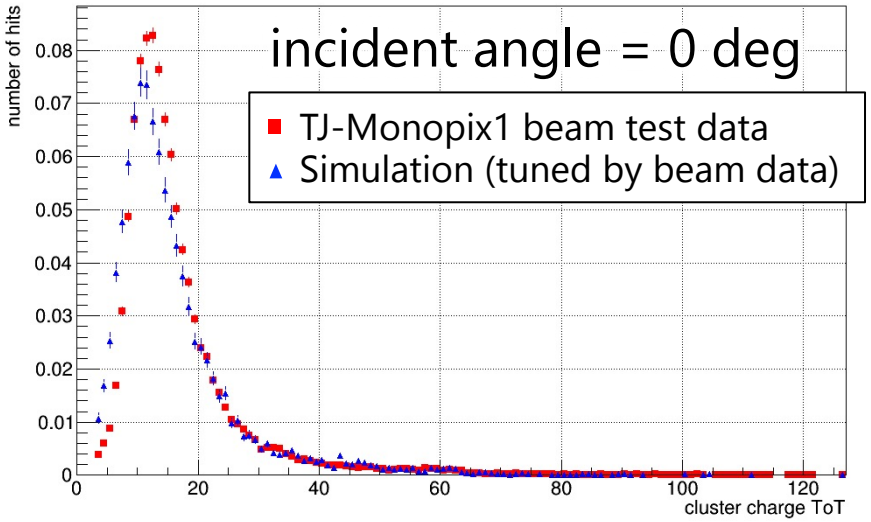
L5 ladder structure



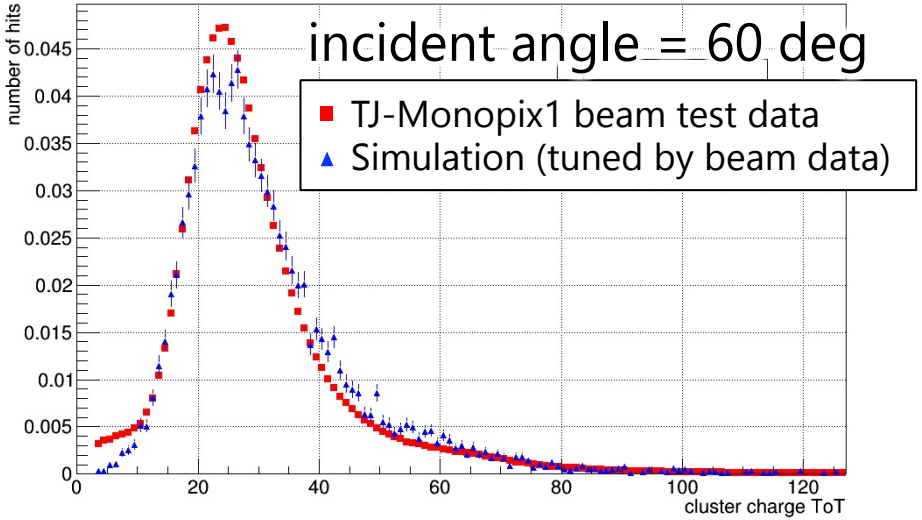
Simulated VTX Performance

- **VTX performance simulation with Belle II analysis framework**
  - Connect to the existing outer-detector tracking
  - Realistic beam backgrounds with accurate Geant4 geometry
- **Realistic pixel sensor model implemented**
  - 30 μm depletion layer
  - 33x33 μm^2 pixels with 7-bit ToT
  - tuned with TJ-Monopix1 beam test data

Cluster charge distribution



Cluster charge distribution



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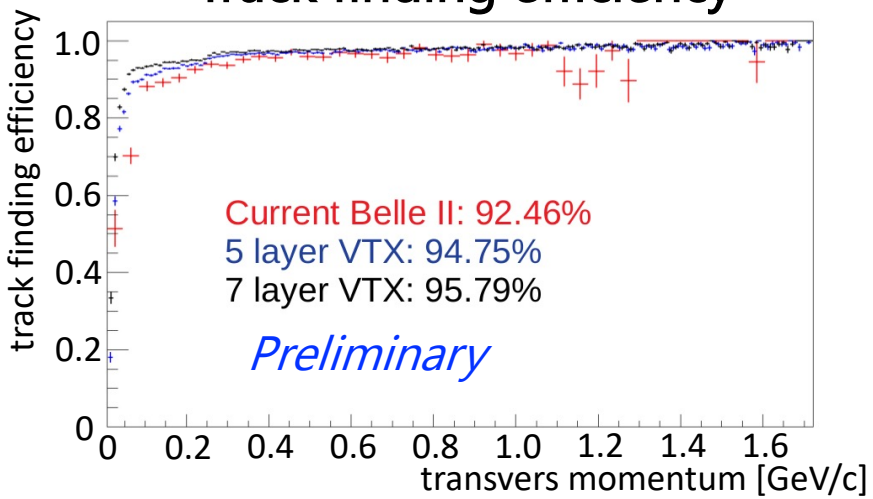
Tracking and vertexing simulation

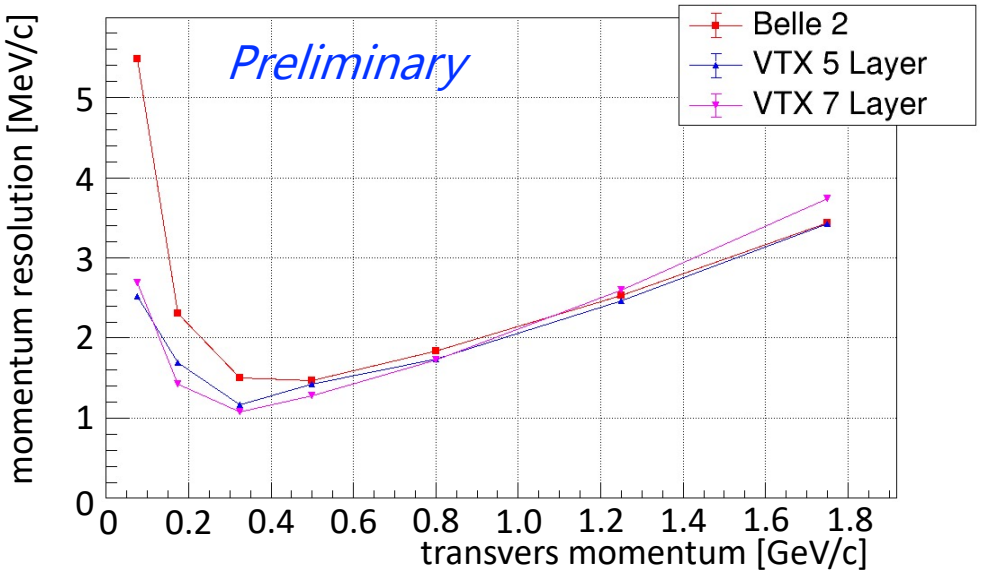
- **Geometry**
  - 5 or 7 barrel layers
  - Simple layer design with realistic material budget
    - 0.1%X0 (inner) + 0.3%X0 (outer) per layer
- **Full tracking chain**
  - VTX-standalone tracking
  - CDC-standalone tracking

  } then combined
- **MC events of Y(4S)→BB generated**

Track finding efficiency



Momentum resolution



Improvements in low p_t thanks to less material budget

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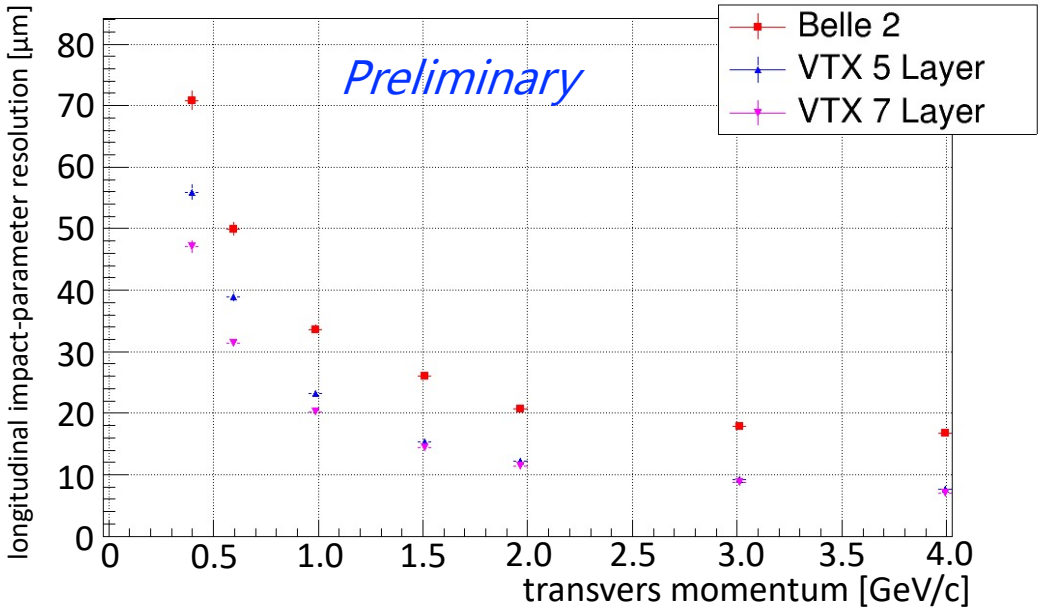
Longitudinal impact-parameter resolution $\sigma(Z_0)$



Improved thanks to better sensor position resolution

Summary and Outlook

- **There is an opportunity for VXD upgrade in Belle II**
  - 2nd long shutdown for SuperKEKB improvement in ~2026-2027
- **Requirements on upgrade**
  - High spatial resolution, small material budget, good hit rate and radiation tolerance

- **Several technology R&D on-going to assess the performance and integration feasibility**
  - Steady process: prototype delivered and performance evaluation started
- **Simulation confirmed excellent performance of VTX fully pixelated option**

Recent technology application in HEP

DSSD	Belle/Belle II SVD, BaBar SVT
DEPFET	Belle II PXD, X-ray astronomy
SOI	X-ray astronomy
CMOS	STAR pixel, CBM MVD, ALICE ITS, ATLAS ITK R&D

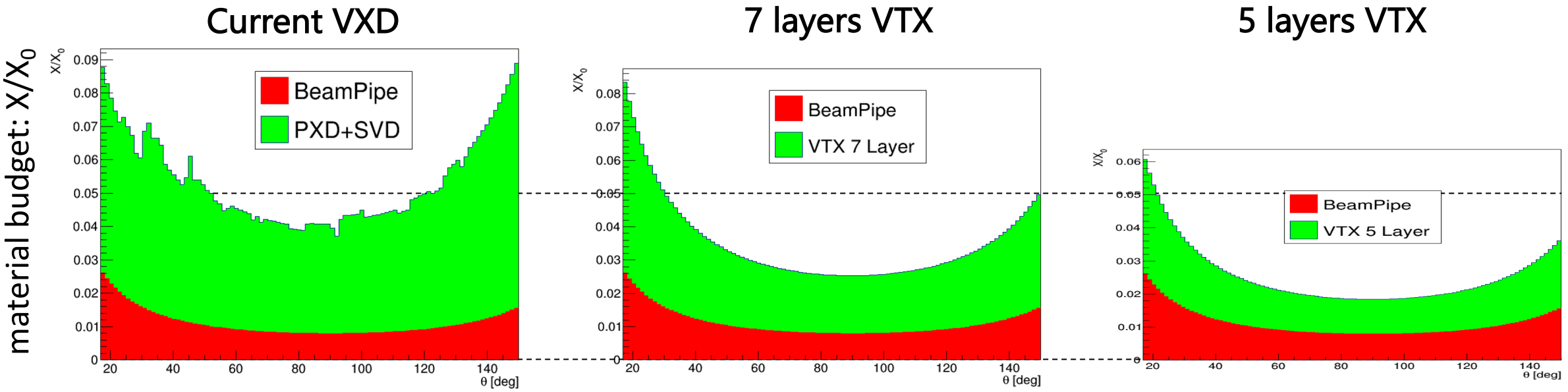
- **CDR to be prepared in 2022: Still a lot to do in a short time**
  - Concept to be proven by beam tests with full-scale prototype
  - Physics benchmarking with full simulation

Technology R&D contributions outside Belle II highly welcome!

Thank you for your attention

backup

Estimated material budget of VTX



- **Very simple detector design, but realistic material budget:**
  - 0.1% X0 (inner layers) + 0.3% X0 (outer layers)
    - 5 layers VTX: L1-2 inner + L3-5 outer, 7 layers VTX: L1-3 inner + L4-7 outer
- **Only barrel layers (no disk sensors in forward)**