Development of the ITS3: a bent silicon vertex detector for ALICE in the LHC Run 4

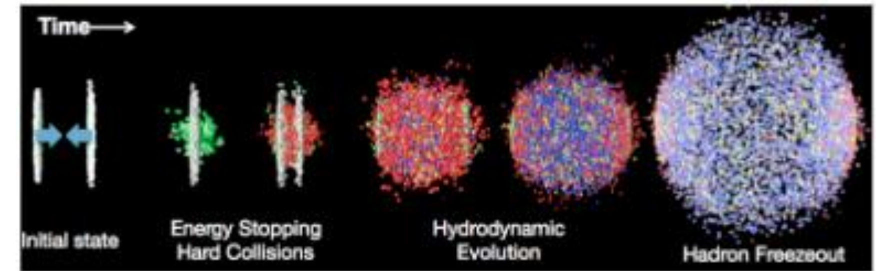
M. Buckland on behalf of the ALICE collaboration

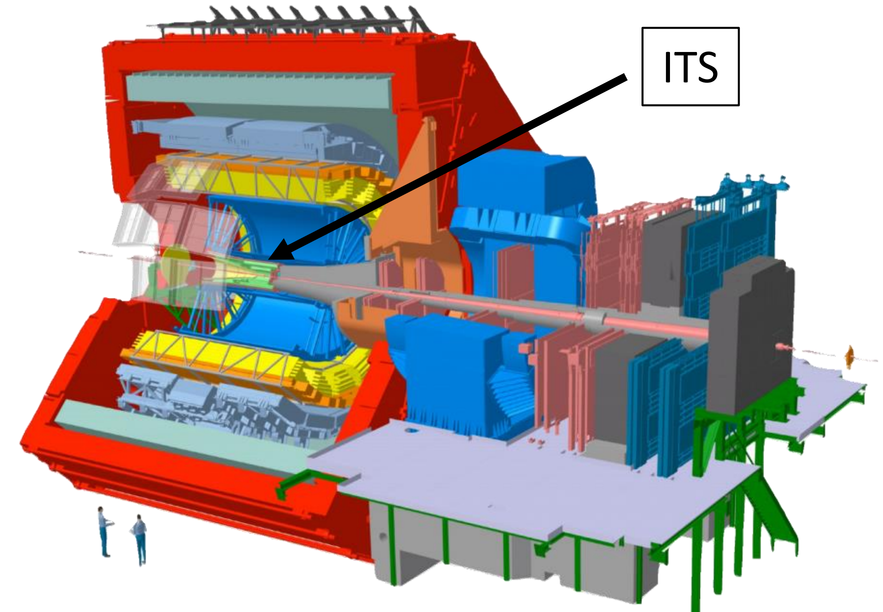
University of Liverpool

Vertex 2021, 27th-30th Sept, Oxford, UK

The ALICE experiment

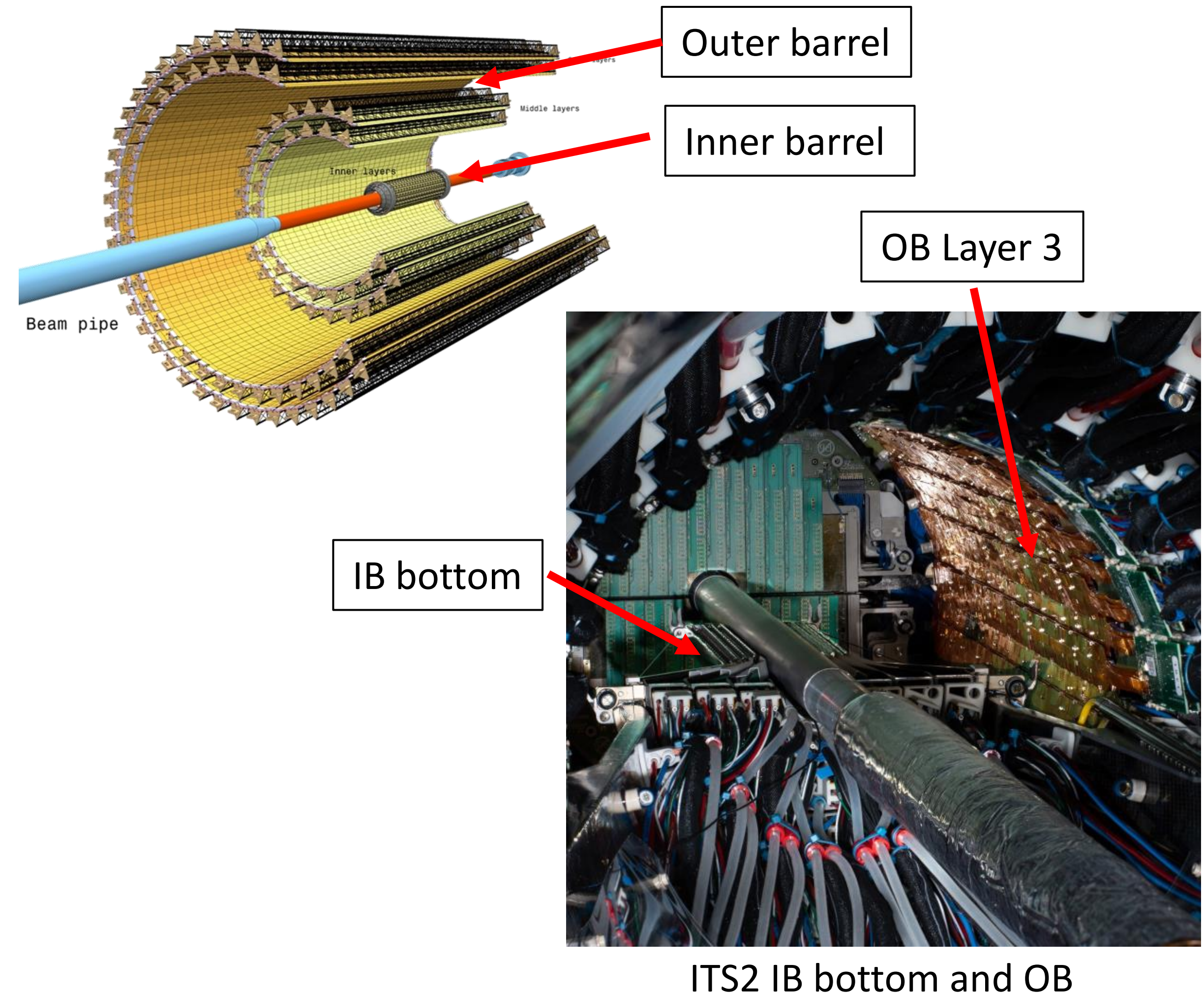
- ALICE is one of 4 experiments based at the Large Hadron Collider (LHC)
- Goal: study and characterise the Quark Gluon Plasma state of matter and new phenomena in QCD
- Performs measurements of ultra-relativistic pp, p-Pb and Pb-Pb collisions
- Designed for heavy-ion physics
- Particle identification through several techniques and multiple detector technologies
- One such detector is the Inner Tracking System (ITS) that has recently undergone an upgrade





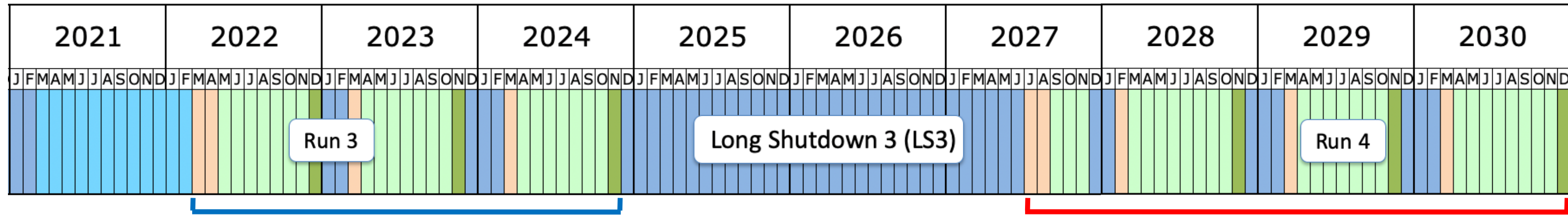
Inner Tracking System Upgrade

- New ITS is entirely based on Monolithic Active Pixel Sensors (MAPS), ITS2
- Consists of 7 concentric layers (3 inner barrel and 4 outer barrel) -> 12.5G pixels (~ 10 m^2 area)
- Uses custom designed ALPIDE chips
- Provides exceptional performance:
  - Fake hit rate < 10^{-6} per pixel per event
  - > 90% tracking efficiency for p_T > 200 MeV/c
  - 15 µm pointing resolution at p_T 1 GeV/c
- Fast removal/insertion of inner barrel for yearly maintenance
- Installed in 2021 and under commissioning ready for Run 3



ITS2 IB bottom and OB

Improvement for Run 4

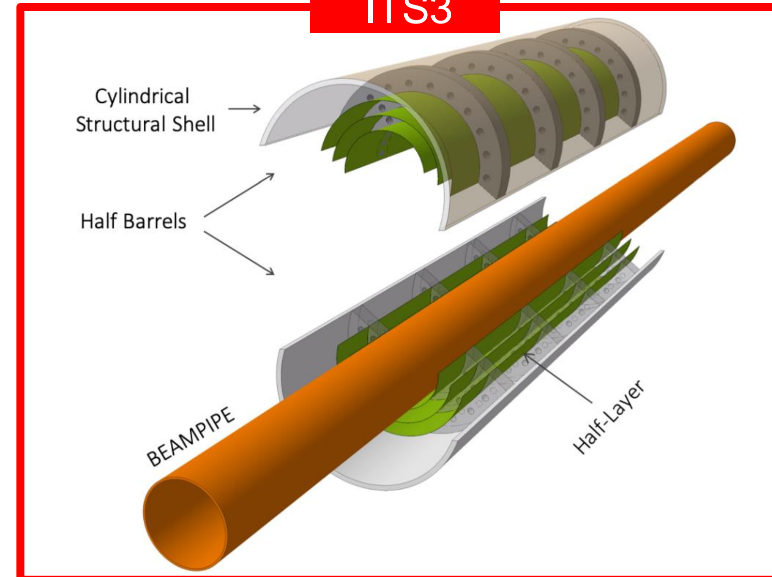


ALICE 2 (Run 3)

ALICE 2.1 (Run4)

ITS2 Inner Barrel

ITS3

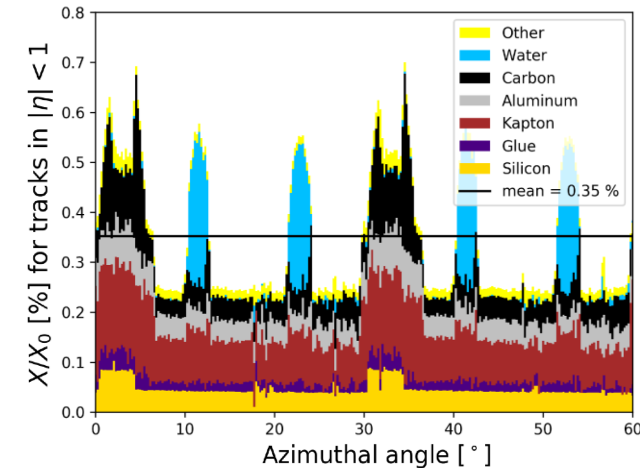


By replacing the inner barrel: can we get closer to the IP? Can we further reduce the material?

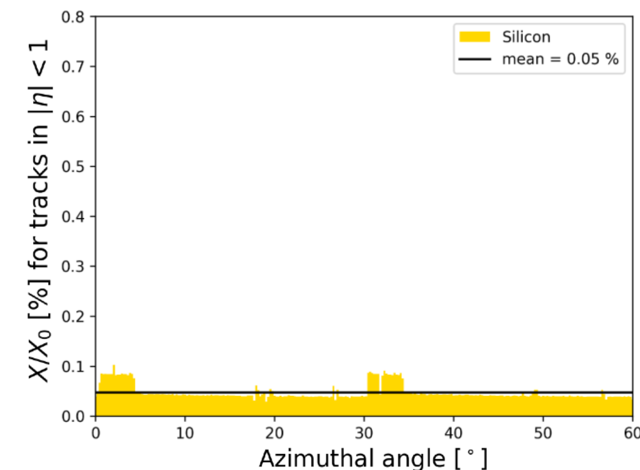
Motivation for ITS3

ALICE

- Current ITS2:
  - Only 1/7th of the total material is silicon
  - Fluctuations due to support/cooling and overlap
- Can we further reduce the amount of material?
- Removal of water cooling
  - Possible with low chip power consumption, ≈ 20 mW/cm²
- Removal of circuit board (power and cooling)
  - Possible if integrated on chip
- Removal of mechanical support
  - Benefit from increased stiffness of rolling Si wafers
- Possible to reach 0.05% X_0?



Removal of material



Project start-up

Expression of Interest

ALICE-PUBLIC-2018-013

Expression of Interest
for an
ALICE ITS Upgrade in LS3

ALICE Collaboration, CERN, Geneva, Switzerland

Abstract

Geneva, Switzerland

[ALICE-PUBLIC-2018-013]
https://cds.cern.ch/record/2644611

Letter of Intent

Letter of Intent
for an
ALICE ITS Upgrade in LS3

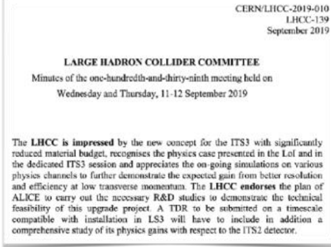
ALICE Collaboration, CERN, Geneva, Switzerland

Abstract

Geneva, Switzerland

[CERN-LHCC-2019-018 ; LHCC-I-034]
https://cds.cern.ch/record/2703140/

LHCC 139 (Sep 2019)



CERN/LHCC-2019-010
LHCC-139
September 2019

LARGE HADRON COLLIDER COMMITTEE

Minutes of the one-hundredth-and-thirty-ninth meeting held on
Wednesday and Thursday, 11-12 September 2019

The **LHCC is impressed** by the new concept for the ITS3 with significantly reduced material budget, recognises the physics case presented in the LoI and in the dedicated ITS3 session and appreciates the on-going simulations on various physics channels to further demonstrate the expected gain from better resolution and efficiency at low transverse momentum. The **LHCC endorses** the plan of ALICE to carry out the necessary R&D studies to demonstrate the technical feasibility of this upgrade project. A TDR to be submitted on a timescale compatible with installation in LS3 will have to include in addition a comprehensive study of its physics gains with respect to the ITS2 detector.

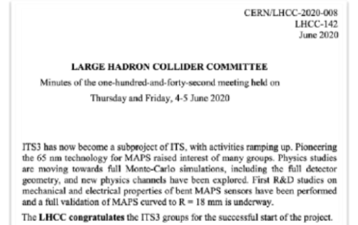
"The LHCC is **impressed** by the new concept for the ITS3…"

R&D kick-off (Dec 2019)

Project setup (spring 2020)

- Project leaders
- Work packages conveners
- Institutes joining

LHCC 142 (Jun 2020)



CERN/LHCC-2020-008
LHCC-142
June 2020

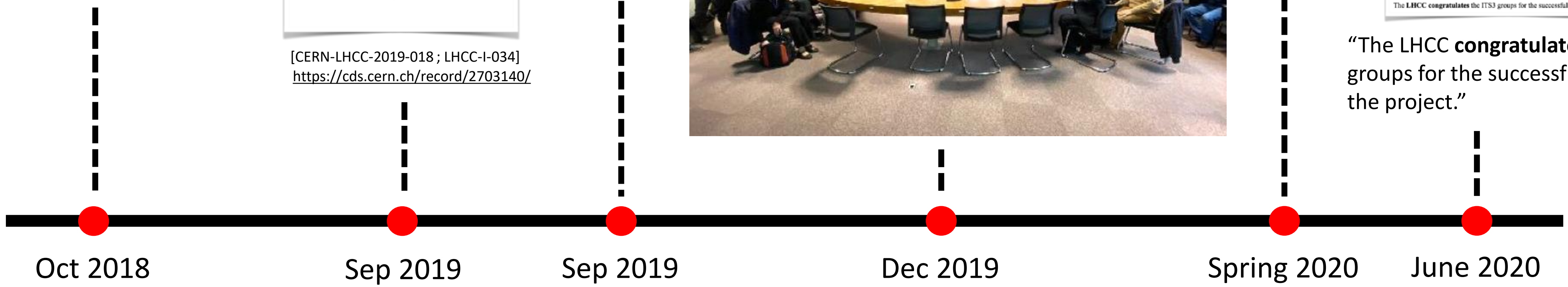
LARGE HADRON COLLIDER COMMITTEE

Minutes of the one-hundred-and-forty-second meeting held on
Thursday and Friday, 4-5 June 2020

ITS3 has now become a subproject of ITS, with activities ramping up. Pioneering the 65 nm technology for MAPS raised interest of many groups. Physics studies are moving towards full Monte-Carlo simulations, including the full detector geometry, and new physics channels have been explored. First R&D studies on mechanical and electrical properties of bent MAPS sensors have been performed and a full validation of MAPS curved to R = 18 mm is underway.

The **LHCC congratulates** the ITS3 groups for the successful start of the project.

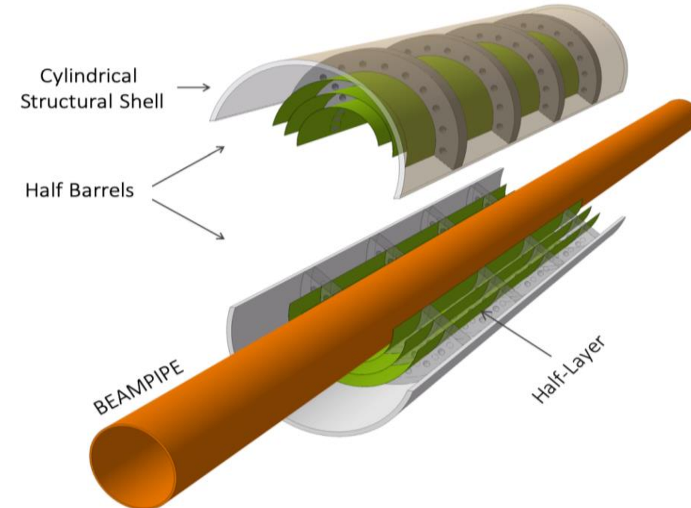
"The LHCC **congratulates** the ITS3 groups for the successful start of the project."



ITS3 layout and design

ALICE

- Main elements:
  - Use stitching to create wafer-scale chips, 280 mm
  - Thinned sensors (20-40 µm), become flexible, bent to the radii of the half layers
  - Held in place with carbon foam
  - New beryllium beampipe, thinner (500 µm) and closer to interaction point (16 mm)
- Main benefits:
  - Very low material budget 0.02-0.04% X_0
  - Homogeneous material distribution resulting in negligible systematic error from material distribution

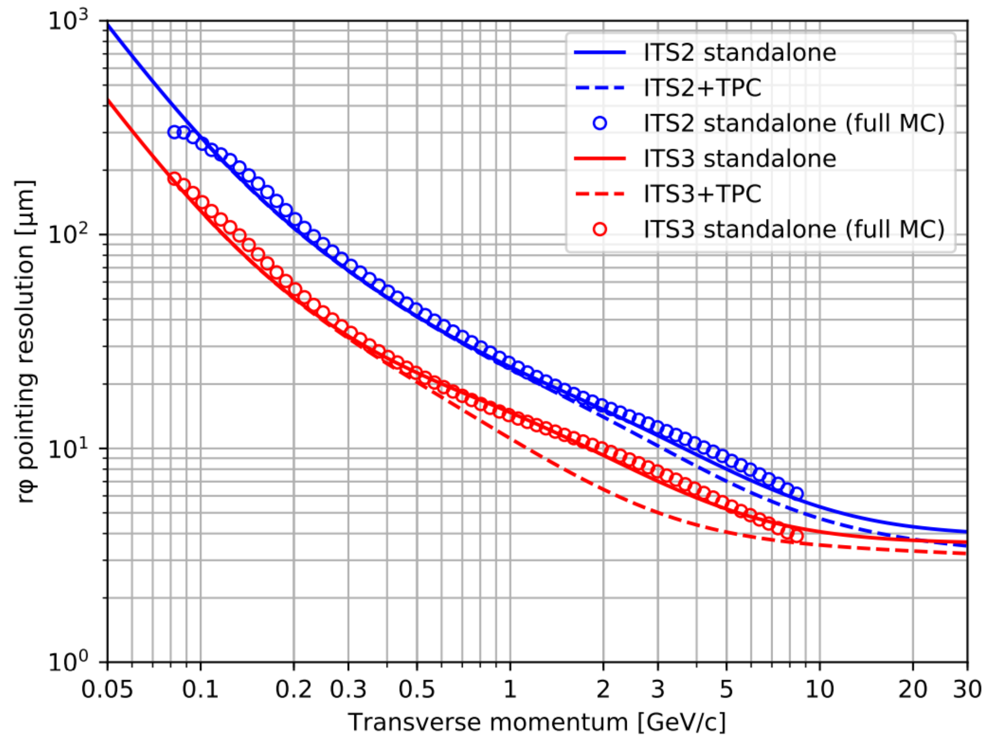


Beampipe inner/outer radius (mm)	16.0/16.5		
Layer parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	270		
Pixel sensors dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of pixel sensors	2		
Pixel size (μm^2)	O(15 x 15)		

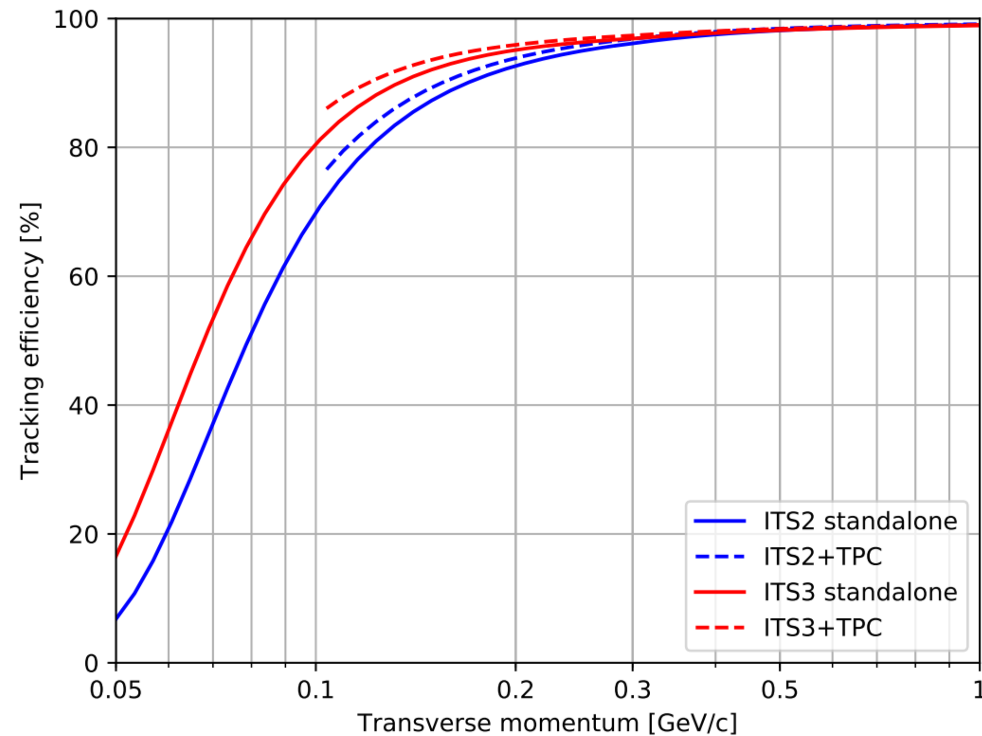
ITS3 performance

ALICE

- Compare ITS2 to ITS3



Pointing resolution: factor 2 improvement over all momenta

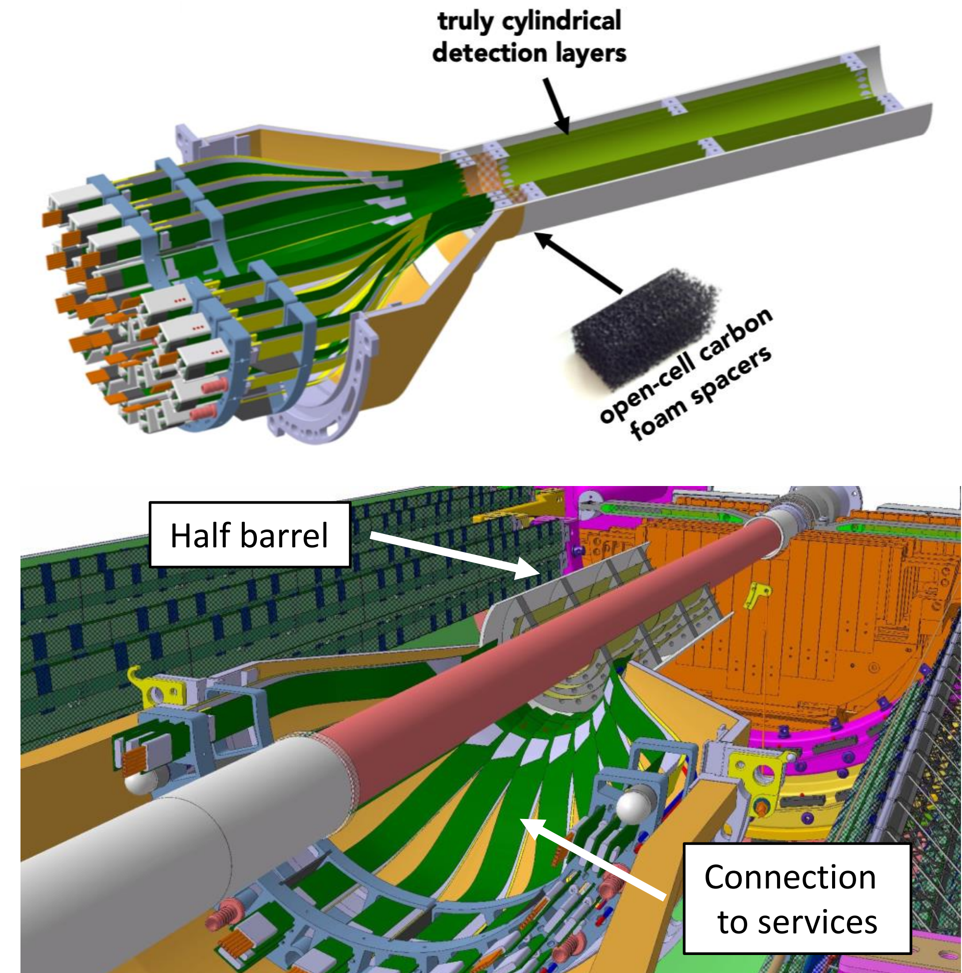


Tracking efficiency: large improvement at low p_T

Mechanics and integration

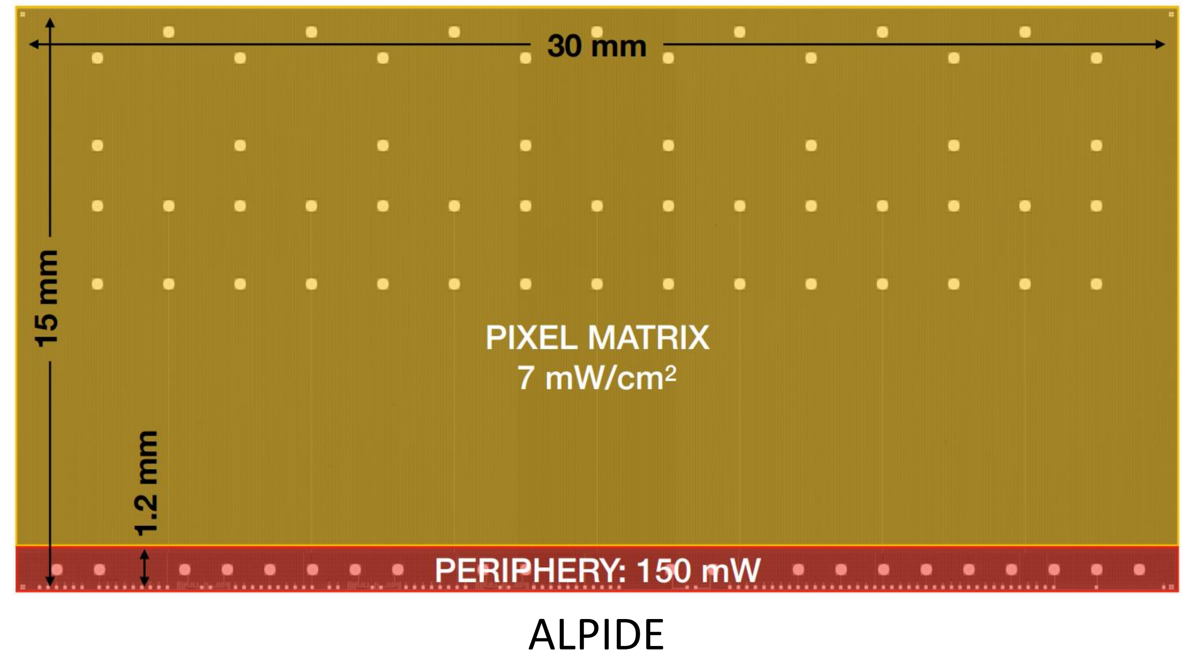
- Mechanics:
  - Layout based on air cooling
  - Layers separated and held in place by low density carbon foam

- Integration:
  - Replaces ITS2 inner barrel
  - Uses existing services (power, readout, cooling)
  - Surrounding and end support structures fix it in place
  - Water cooling at the extremities for the chip peripheries



Cooling

- Inside the active area, air cooling is possible if chip power consumption is ≈ 20 mW/cm^2
- The average over the whole ALPIDE is already close at ≈ 40 mW/cm^2
- If the chip is separated into pixel matrix and periphery, power consumption drops
- The chip becomes largely sufficient if periphery is outside the fiducial volume

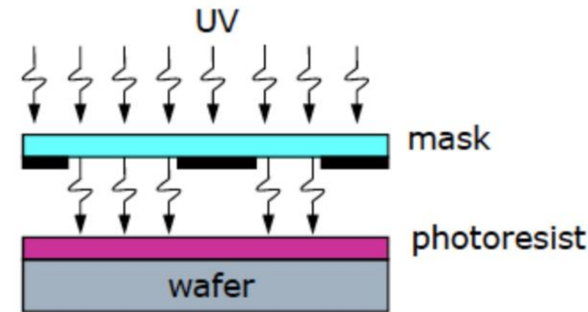


ALPIDE

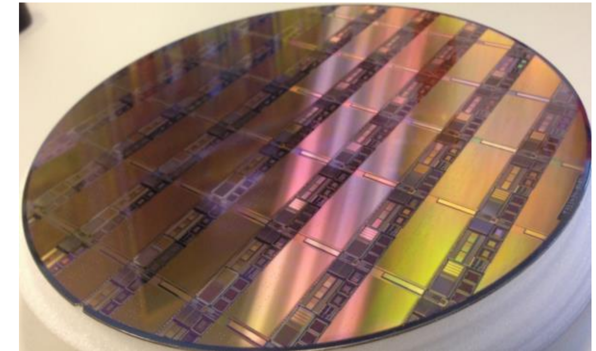
Wafer-scale chip

ALICE

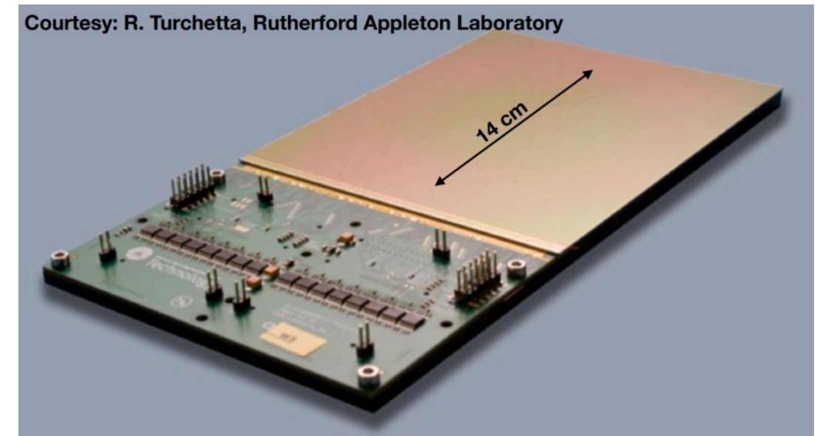
- Another main element of the ITS3 design is the use of wafer-scale chips
- Traditionally chip size is restricted by CMOS manufacturing (reticle size)
  - Typically a few cm^2
  - Modules are tiled with chips connected to a flexible printed circuit board
- Possible to create a wafer-scale chip with stitching, i.e. aligned exposure of the reticle to create larger circuits
  - Used in industry
  - 300 mm wafer can house a chip long enough for a full ITS3 half layer
  - Requires dedicated chip design



Principle of photolithpgraphy

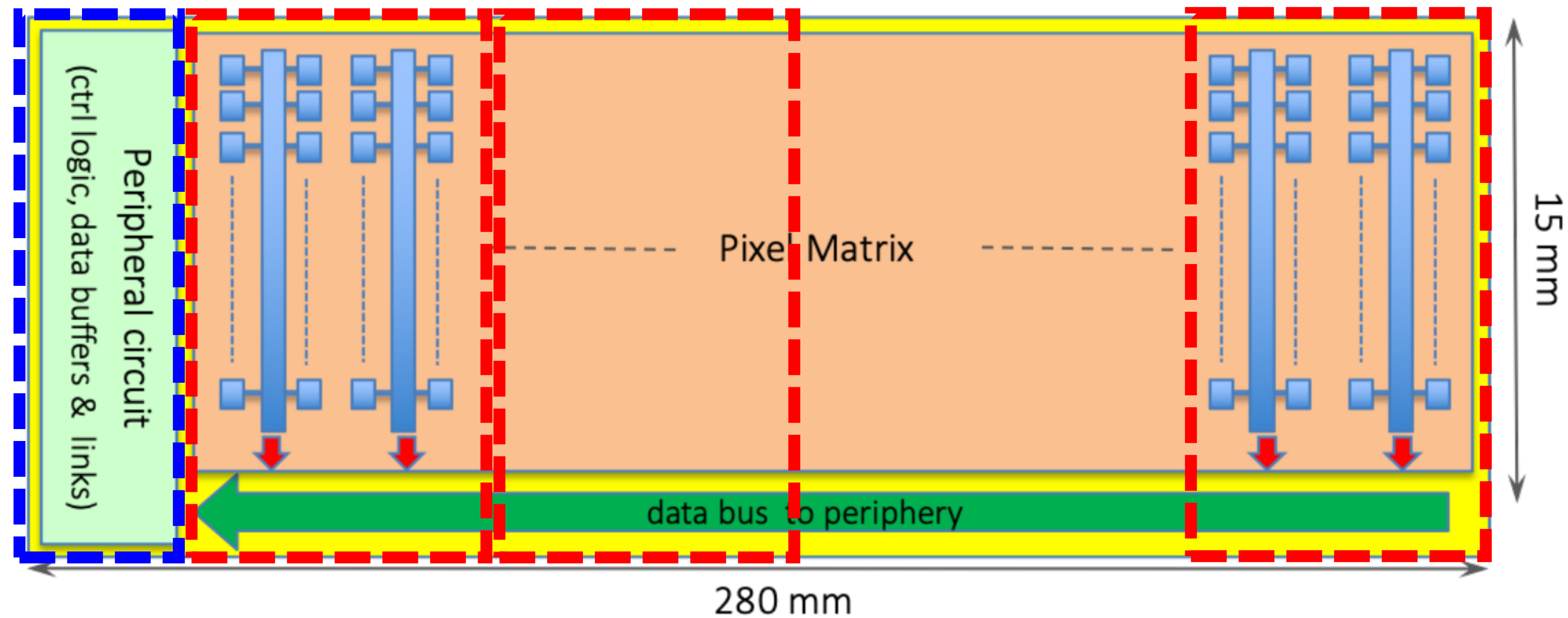


200 mm ALPDIE prototype wafer



Wafer-scale sensor

Wafer-scale chip – architecture

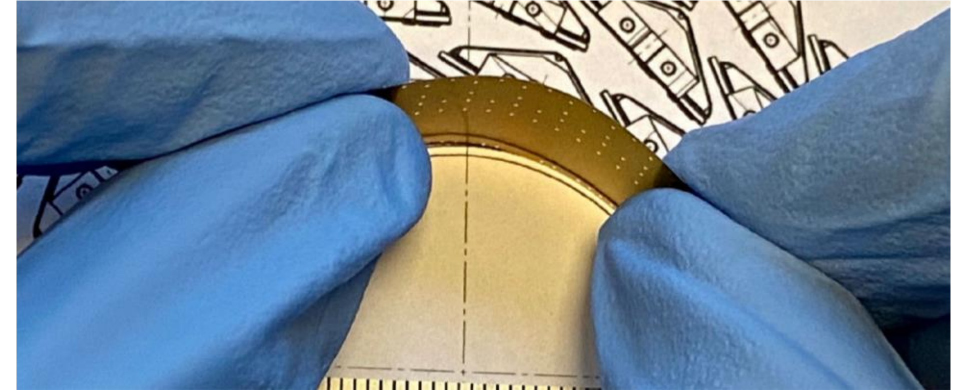


- Uses ALPIDE as a baseline architecture, double column priority encoders
- One thing to take into account is that stitching requires a regular, periodic structure
- Chip is split into 2 sections:
  - Periphery – housing data, logic and electrical interfaces
  - Pixel matrix – housing pixels and data bus to the periphery and repeated N times

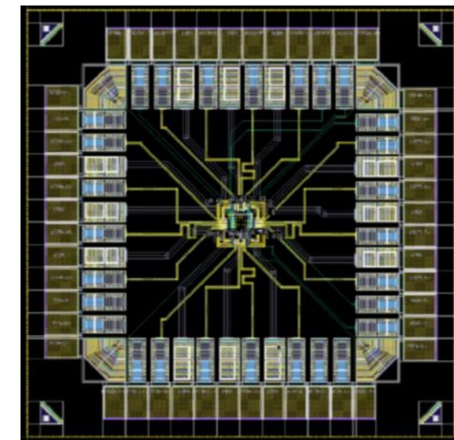
Moving to 65 nm

ALICE

- With the success of ALPIDE (180 nm) for the ITS2, this chip is a good starting point for ITS3
- Using a smaller technology, 65 nm, will open up more possibilities:
  - Lower power consumption when moving to deeper sub-micron
  - Produced on 300 mm wafers, allows for complete z-coverage in detector
  - Possibility to use stitching to reach wafer scale sensors
- Challenges:
  - Optimise sensor design for yield
  - Radiation hardness needs testing (moderate levels foreseen)
  - Charge collection to be optimised



Bent 50 µm thick ALPIDE

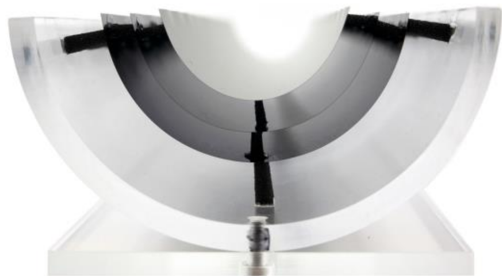


65 nm pixel test structure

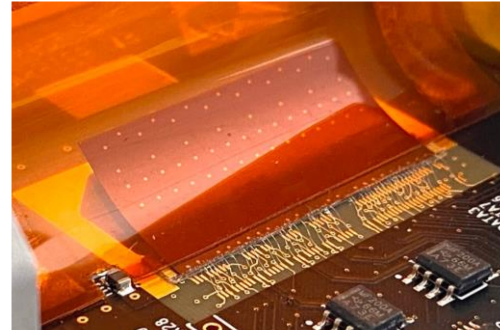
ITS3 R&D branches

ALICE

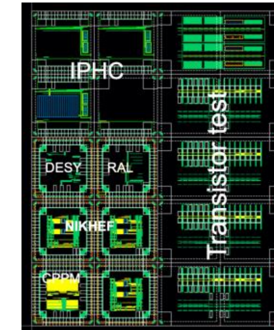
Mechanics and integration
Prototyping and testing of bending, mechanics and integration in the detector



Sensor performance
Testing and performance assessment of bent ALPIDEs

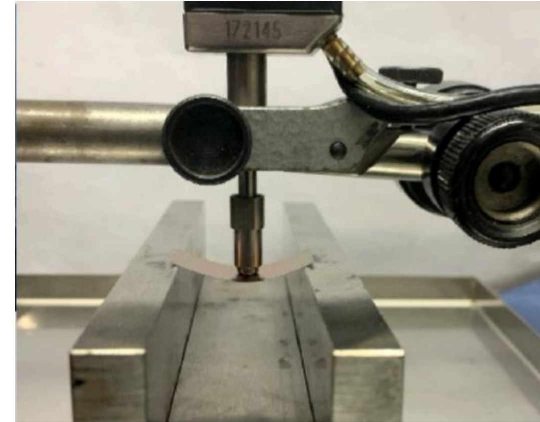


Chip design
Design of test structures in 65 nm ready for wafer-scale chips

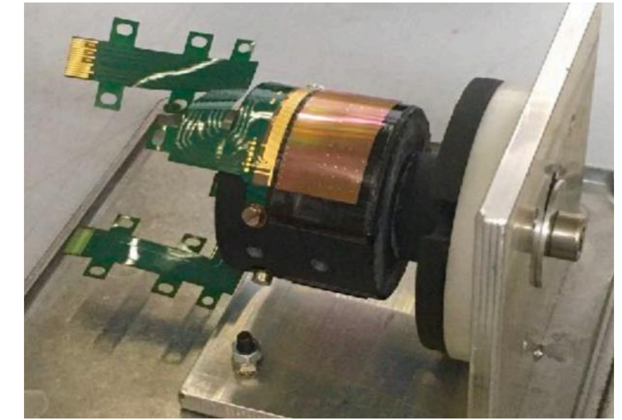


ALPIDE bending

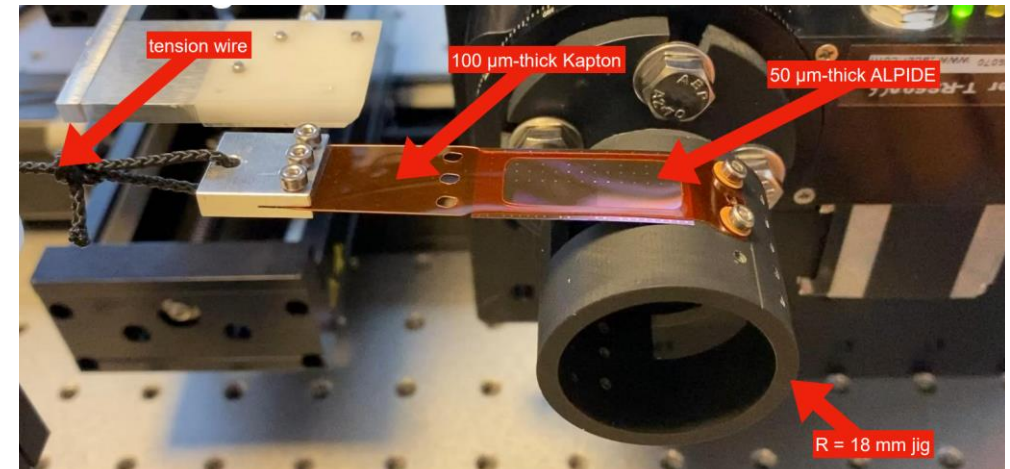
- Seen with ALPIDE that at 50 µm the chips become flexible
- Benefit of going thinner is that the bending force scales with thickness to the third power
- Different methods for bending explored and measured:
  - Long edge or short edge
  - 3 point or 4 point bending to measure the force
  - Different radii
  - Bonding before and after bending
  - Using cylindrical objects to produce a bend



3 point bending



Bent along long-edge, r = 18 mm

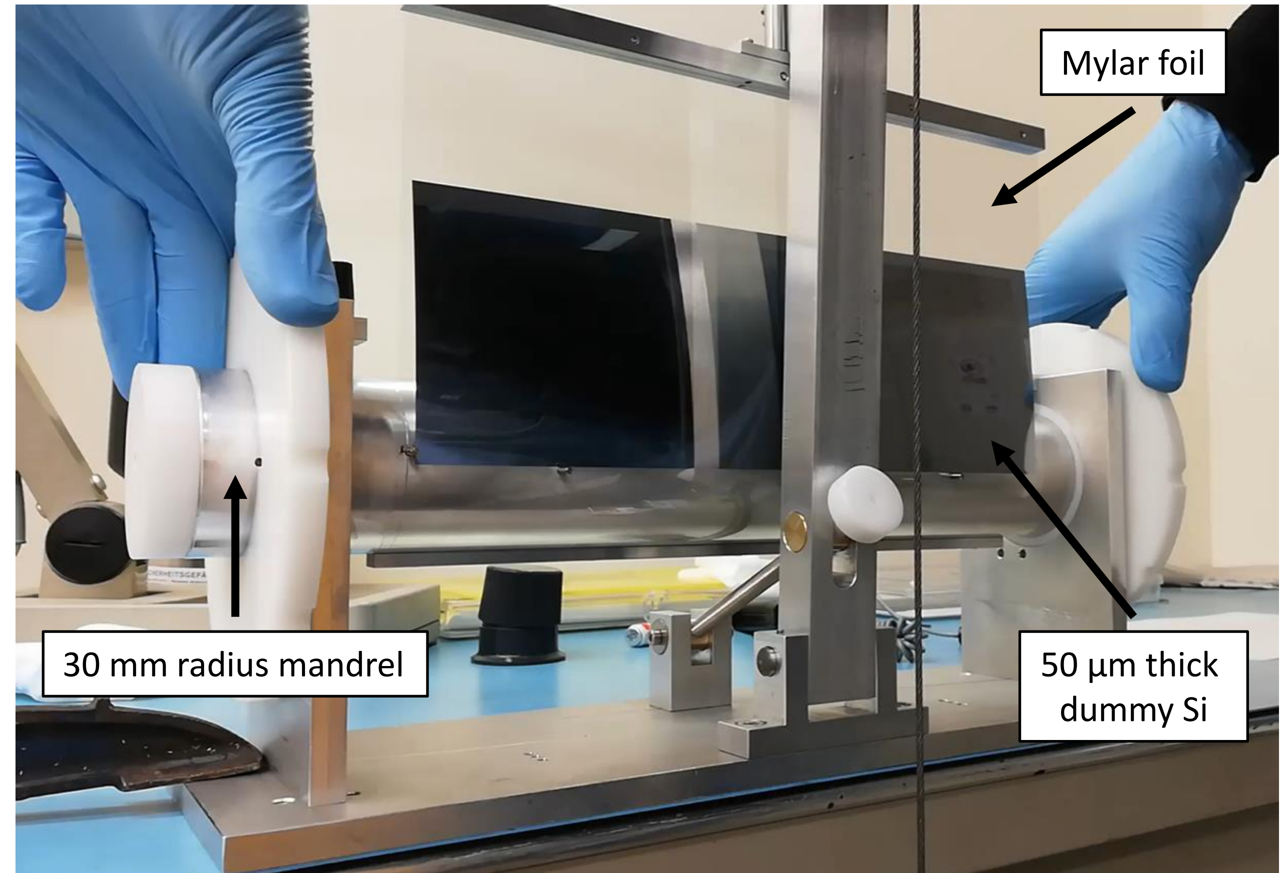


Automated bending tool

Wafer-scale bending

ALICE

- Tests have been carried out on bending 50 µm thick dummy wafers
- The technique has been developed and can now be done in a reliable and repeatable way
- Uses tensioned mylar foil to hold the wafer
- It is then attached to a mandrel of the desired radius and turned to produce a bend
- Bent wafers can then be used in a mechanical mock-up

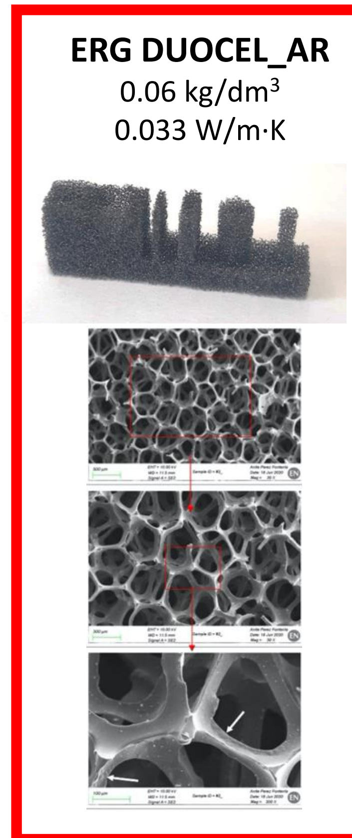


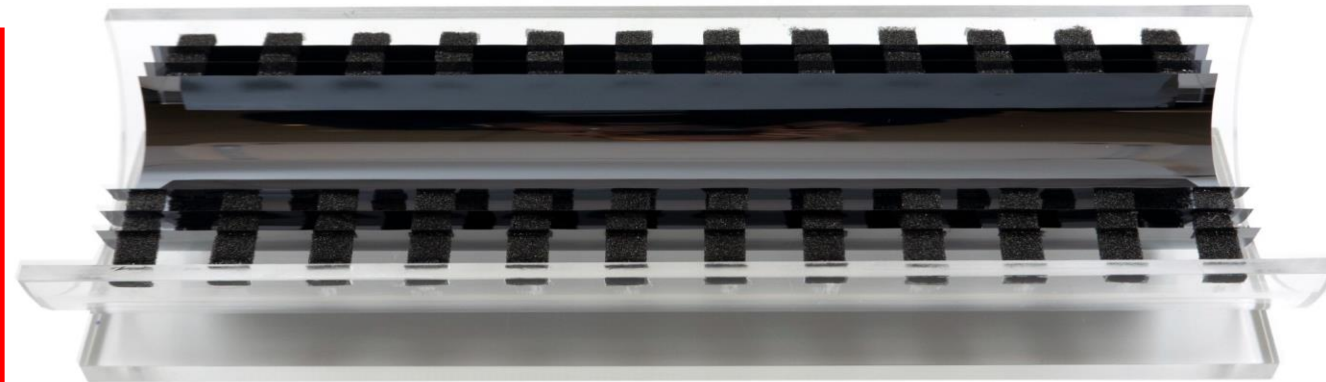
Wafer-scale bending tool

ITS3 mechanical demonstrator

ALICE

- Full size mechanical mock-up of ITS3 half barrel with 3 layers
- Choice of carbon foam based on machinability and thermal properties
- Already see that minimal material is needed to hold the Si in place
- Work in progress to determine the best assembly procedure
- Study of mechanical and thermal properties ongoing

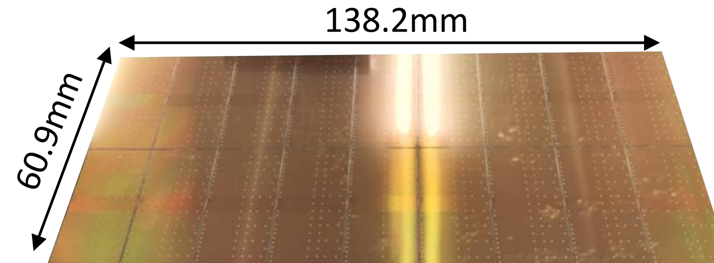




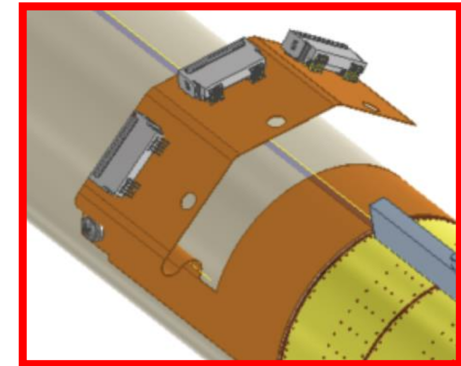
Full size mock-up with 3 layers

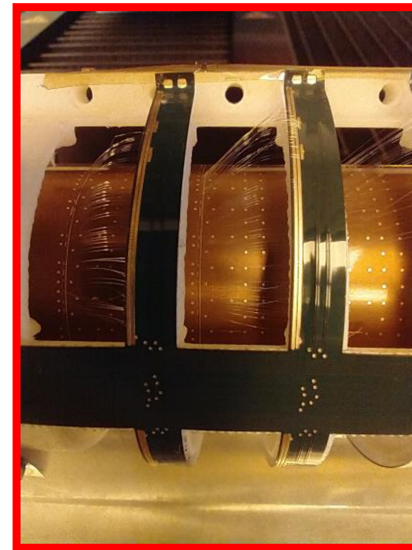
Super-ALPIDE

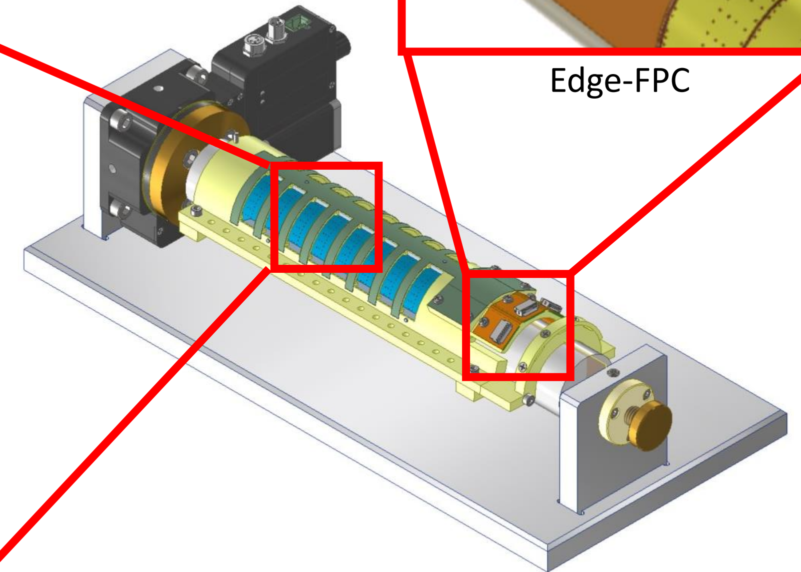
- Possible to create a large bent operational sensor with existing ALPIDEs?
- Super-ALPIDE:
  - 18 (9x2) not diced ALPIDEs
  - Close to ITS3 half-layer 0 dimensions
  - Supported by an exo-skeleton
  - Needs individual interconnections to FPC
- R&D on:
  - Handling and bending large area chips
  - Gluing procedure of FPC on exo-skeleton
  - Wire-bonding in complex and curved geometry
  - Mechanical support and alignment tools
  - First bent flex prototype (for powering and data streaming), edge-FPC



Super-ALPIDE, 18 not diced chips

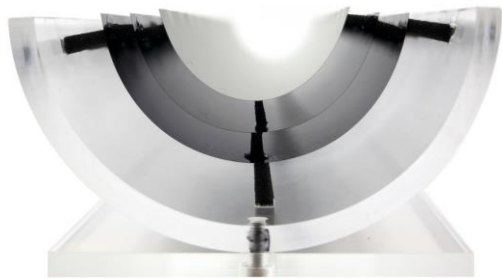

Edge-FPC


Exo skeleton + FPC + wire bonds


Super-ALPIDE design

ITS3 R&D branches

Mechanics and integration
Prototyping and testing of bending, mechanics and integration in the detector



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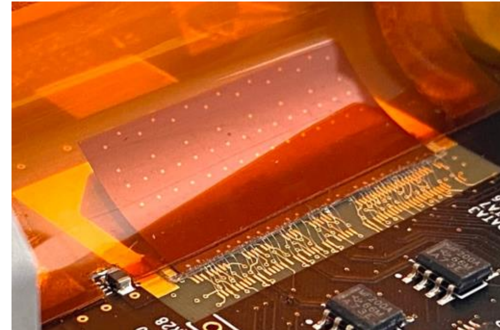
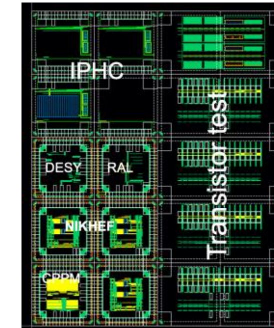
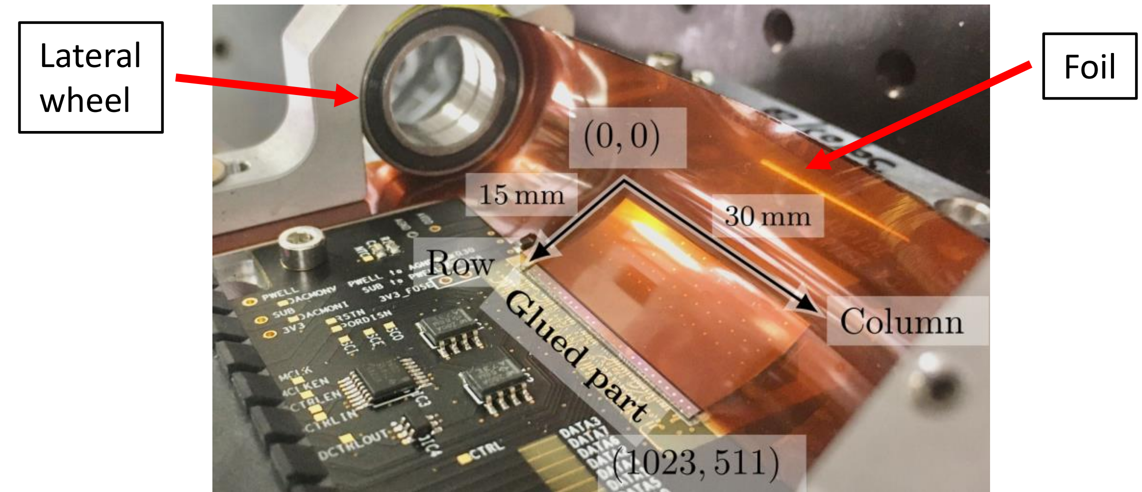


Chip design
Design of test structures in 65 nm ready for wafer-scale chips

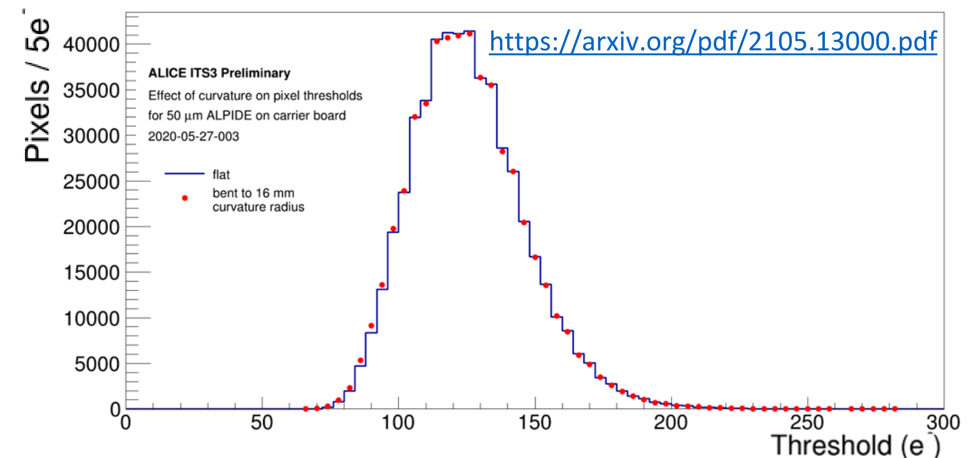


Bent ALPIDE testing

- 50 µm ALPIDE bent along the short edge, r = 16 mm
- Sensor is glued to the carrier on the periphery then bonded
- The remaining unattached part of the chip is placed between 2 layers of polyimide foil
- Two lateral wheels are controlled with micrometre precision to bend the chip
- Lab measurements have shown minimal effect of the bending on electrical performance:
  - Slight change in currents
  - Threshold and noise are the same
  - No variation in the number of dead pixels

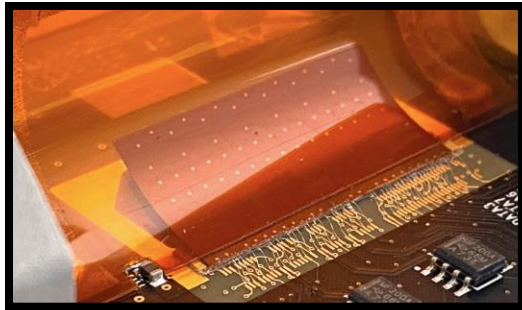


Bent along short-edge, r = 16 mm

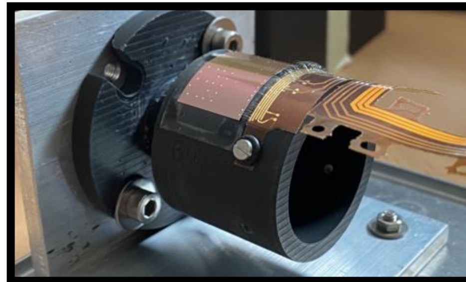


Bent ALPIDE testing – test beams

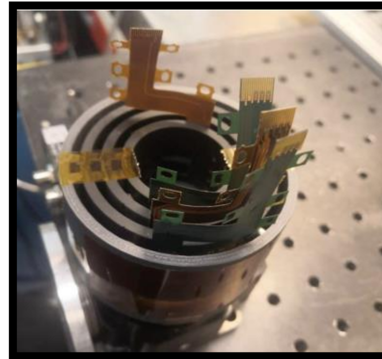
- Extensive test beam campaign with different DUTs in different configurations and a carbon foam study



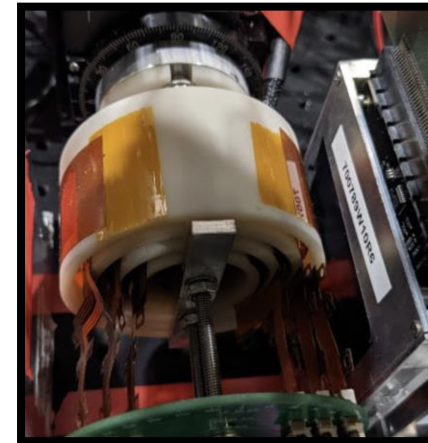
First bent ALPIDE on "standard carrier"



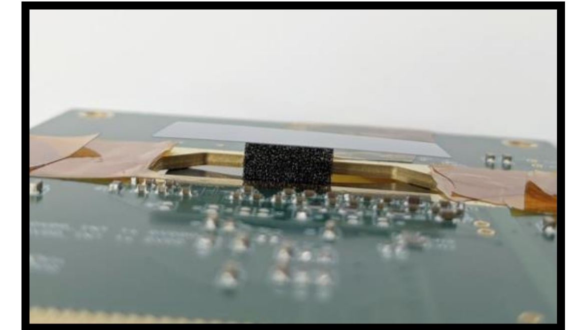
Bent ALPIDE on cylindrical mount



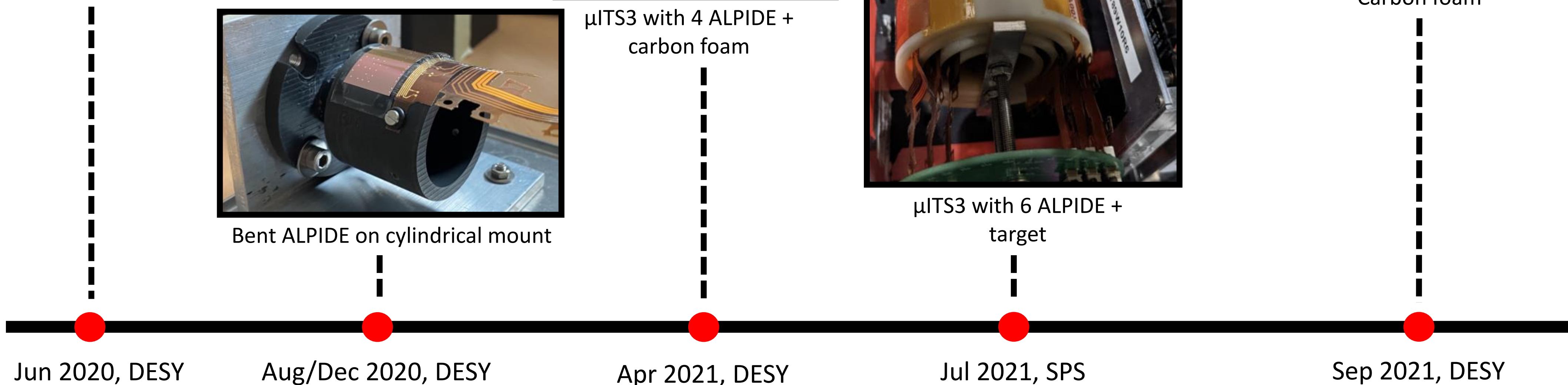
µITS3 with 4 ALPIDE + carbon foam



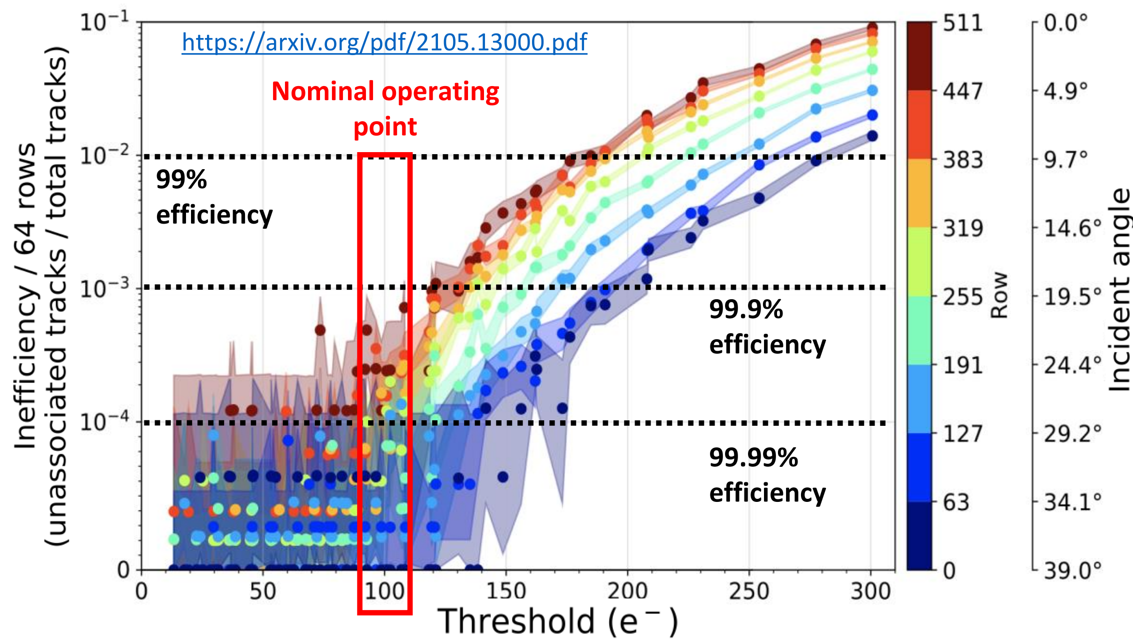
µITS3 with 6 ALPIDE + target

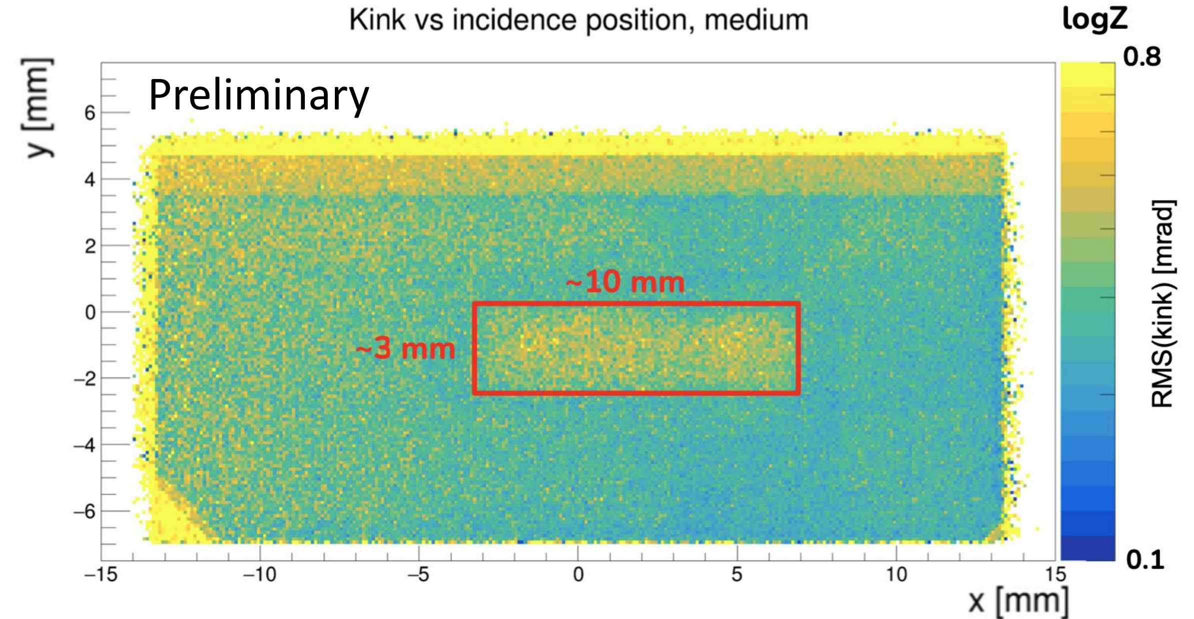


Carbon foam



Test beam results

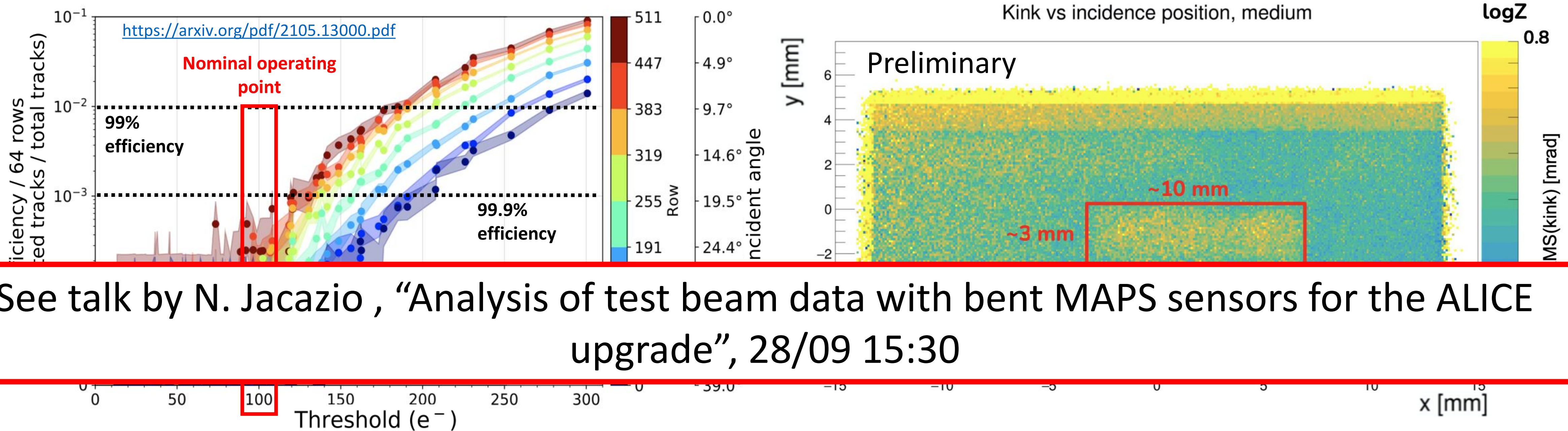




- Inefficiency of bent short-edge ALPIDE
- > 99.9% efficiency at threshold of 100 e⁻ (nominal operating point of ALPIDE)
- See an increase in efficiency for larger beam incident angles (decreasing row number)

- The kink angle distribution in the carbon foam setup
- Gives the width of the scattering angle distribution and the amount of scattering the carbon foam produces

Test beam results

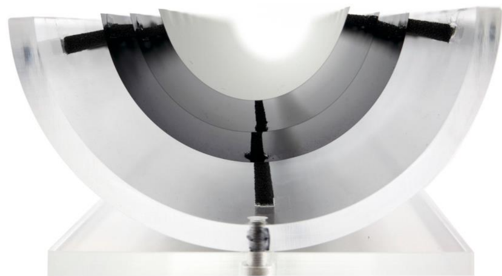


- Inefficiency of bent short-edge ALPIDE
- > 99.9% efficiency at threshold of 100 e⁻ (nominal operating point of ALPIDE)
- See an increase in efficiency for larger beam incident angles (decreasing row number)

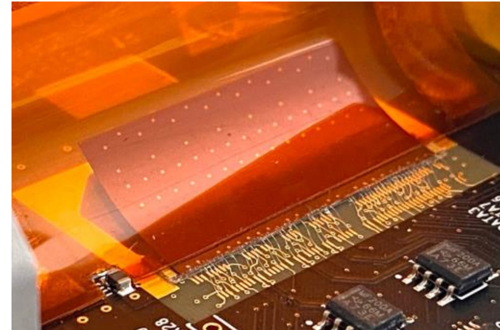
- The kink angle distribution in the carbon foam setup
- Gives the width of the scattering angle distribution and the amount of scattering the carbon foam produces

ITS3 R&D branches

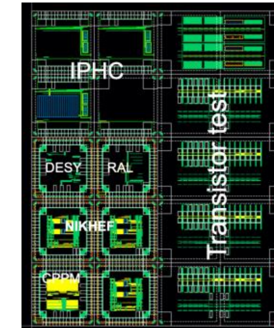
Mechanics and integration
Prototyping and testing of bending, mechanics and integration in the detector



Sensor performance
Testing and performance assessment of bent ALPIDEs

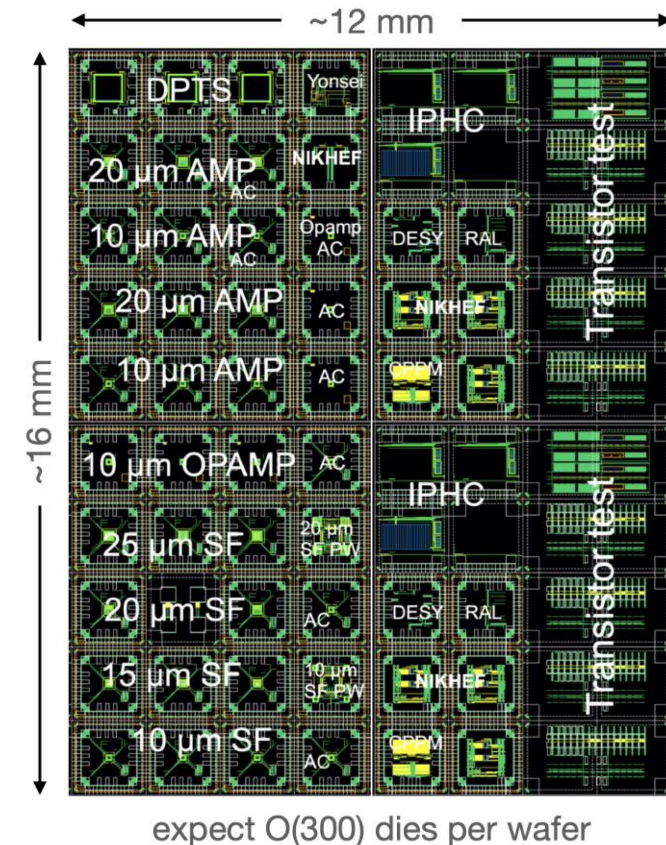


Chip design
Design of test structures in 65 nm ready for wafer-scale chips



First 65nm submission – MLR1

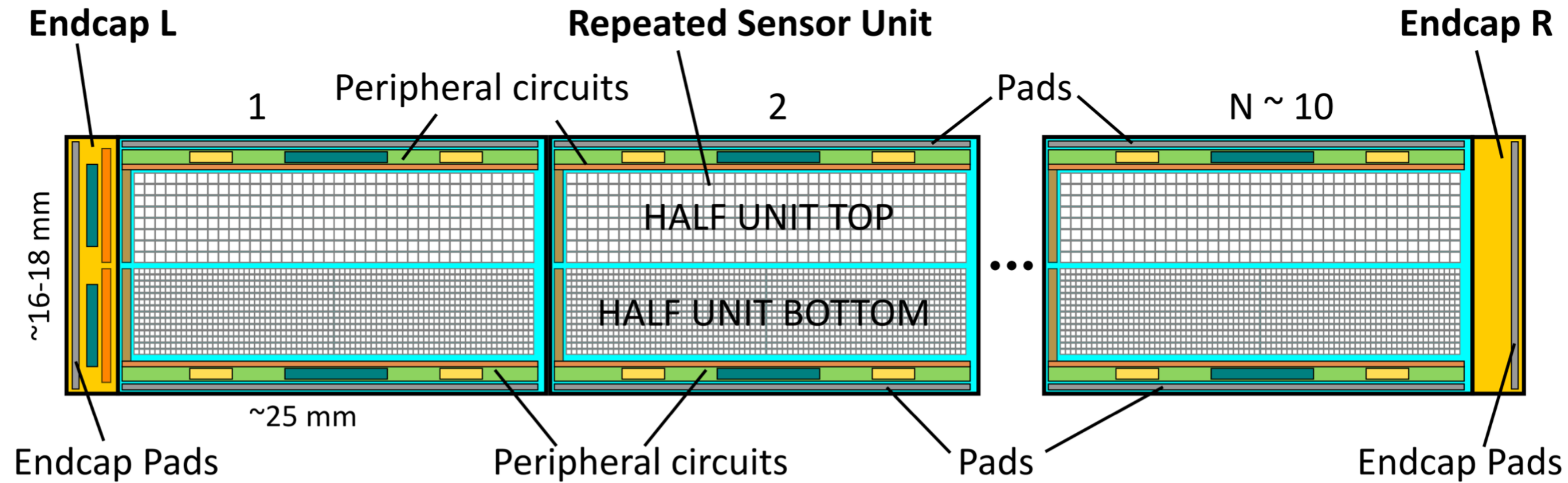
- First submission in 65 nm technology was in late 2020 – MLR1
- ITS3 plays a leading role in the evaluation
- Comprised of many first test structures:
  - Transistor test structures for radiation hardness
  - Various diode matrices for charge collection
  - Analog building blocks
  - Digital test matrices
- First wafers have been received
  - Laboratory characterisation started and ongoing
  - Test-beam campaign in near future, Oct + Dec 2021
- Wafer-scale blocks to be diced to study mechanical properties



expect O(300) dies per wafer

ER1 – stitched sensor prototype

ALICE



- First attempt will adjoin identical but functionally separate sub-units
- This will be repeated N times until the two side edges where endcaps will be placed
- Stitching is used to connect metal traces for power distribution and long range on-chip interconnect busses
- Ongoing development with a mock submission by end of 2021

Summary

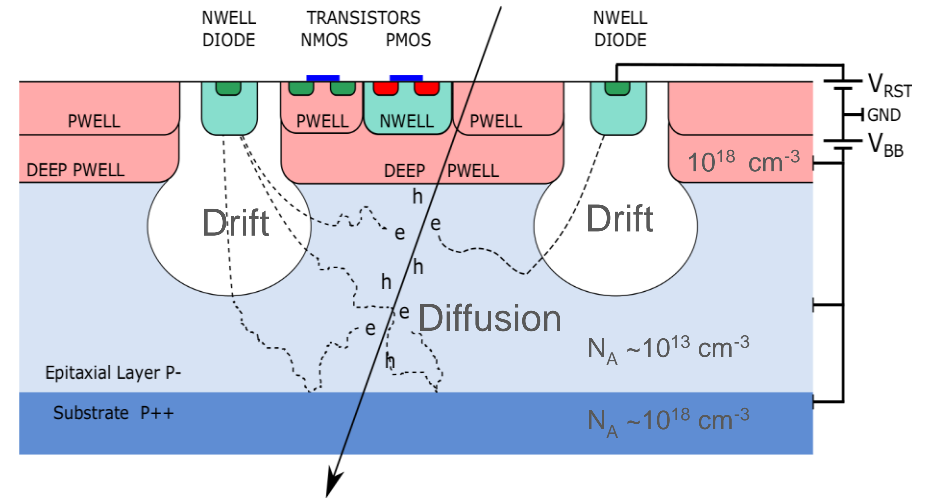
ALICE

- **ITS3** is a planned upgrade of the current ALICE inner barrel during LS3 ready for **Run 4**
- Consists of a fully cylindrical, bent silicon tracker utilising ultra-thin (**20-40 μm**), wafer scale (**300 mm**) MAPS in **65 nm** technology
- R&D is underway and progressing rapidly:
  - **Successful** bending and verification, in both lab and test beams, of ALPIDE sensors
  - **Full-size** mockup of ITS3 half-barrel
  - Super-ALPIDE for development of mechanical, inter-connections and bending techniques on a **large-scale operational** sensor
  - First submission in 65 nm technology with chips now **available** for testing

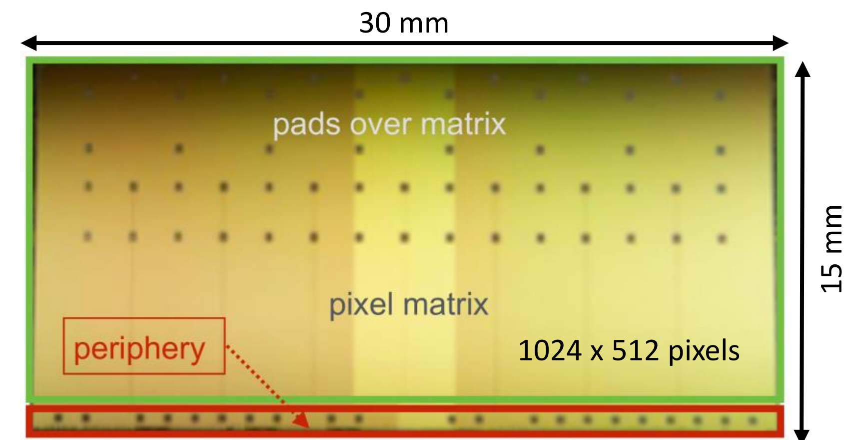
Backup

Backup - ALPIDE chip

- Monolithic chip produced by Tower Jazz in 180 nm CMOS imaging process technology
- Full CMOS circuitry implemented in each pixel exploiting the deep technology feature
- High resistivity (>1 kΩcm) p-type epitaxial layer (25 µm thick) on p-type substrate
- Small reverse bias possible (< -6 V), increase depletion region



- Features:
  - In-pixel amplification, discrimination and multi-event buffer
  - Low power consumption, 40 $mWcm^{-2}$
  - Small periphery for control and readout functions
  - Hits readout using priority encoder
  - Event time resolution < 20 µs
  - High speed readout of up to 1.2 Gbit/s



ITS3 timeline