Radiation tolerance of ITkPixV1

Maria Mironova on behalf of the RD53 collaboration

The 30th International Workshop on Vertex Detectors

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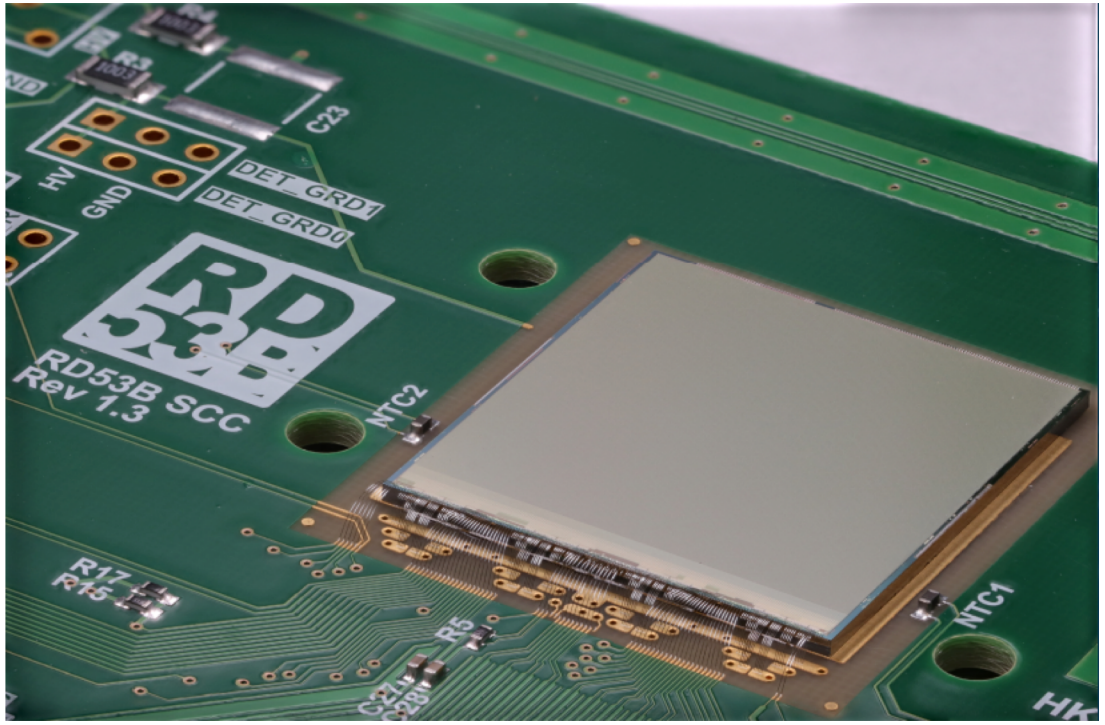
Introduction

- Readout chips designed by RD53 collaboration @ CERN
- First joint ATLAS and CMS prototype: **RD53A**
- Based on this, development of improved **RD53B** chip
- Common design produced in two versions:
  - ATLAS ITkPixV1
  - CMS CROC
- Main difference between ATLAS and CMS chip in size and type of analog front-end used (differential for ATLAS, linear for CMS)
- ATLAS ITk pixel detector is expected to receive doses of up to **1 Grad** during the lifetime of HL-LHC
- Need to understand the impact of TID damage on the readout chips



→ **Irradiate chip prototypes using X-ray systems**

Ring oscillators in ITkPixV1

- ITkPixV1 includes ring oscillators for radiation testing (located at the chip bottom)
- 42 ring oscillators made with different logic cells and different transistor sizes (strength 0, 1 and 4)
- Oscillator drives a 12-bit counter, enabled for a given period of time

→ **Calculate frequency f or delay $T_D = 1/(N \cdot f)$**

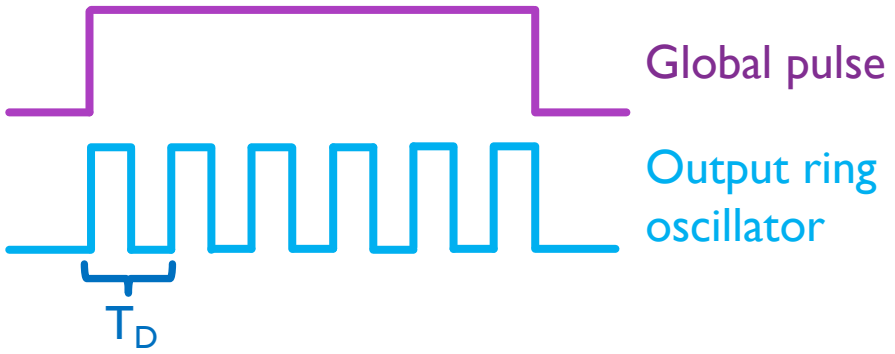
- During irradiation ring oscillator frequency decreases

→ Characterise radiation damage on the different kinds of logic cells

→ **Proxy to understand gate delay**

→ too large delay will cause digital logic to fail

→ > 200% increase in delay shows issues in simulation

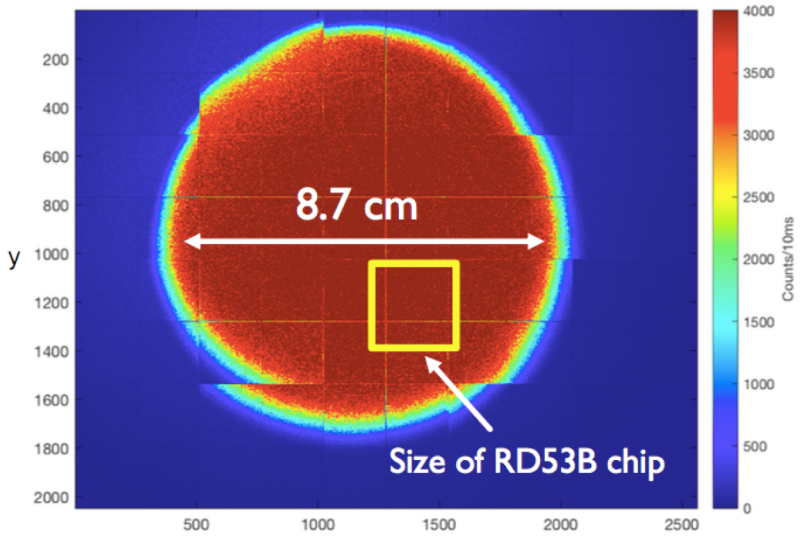


Group	Types	#
A B left B right	CLK, Inv, NAND, NOR Driving strength 0 and 4 w/ different lengths	3 x 8
B FF	Scan/standard/neg-edge D-flip-flop	6
B LVT	LVT inverter & 4-input NAND Strengths 0 and 4	4
B CAPA	Injection-capacitor loaded 4-input NAND	8

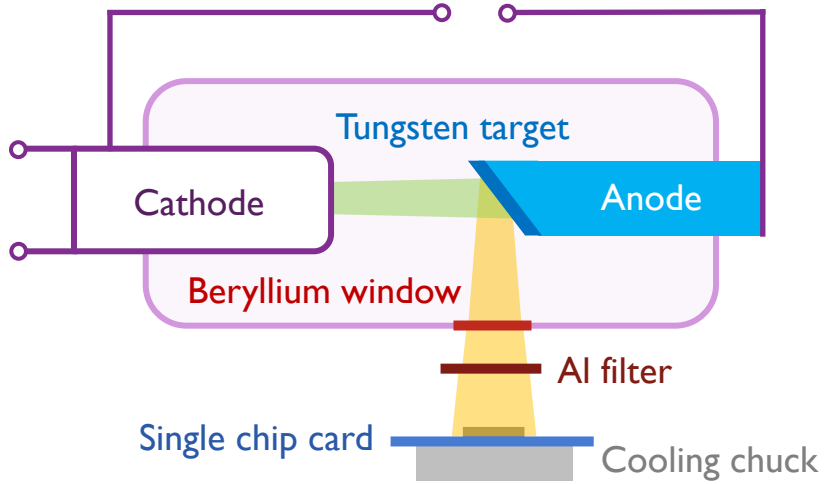
Irradiation setup

- Irradiation setup at Oxford:
  - X-ray tube with a tungsten target
  - Peak X-ray flux at 50kV, 60 mA (3kW)
  - Dose rate calibration using calibrated diodes → consistent with different sites
- Common irradiation procedure:
  - Characterise chip before irradiation (ring oscillators, threshold distributions)
  - During irradiation, read the ring oscillator frequency (at least every 0.1 Mrad)
  - Otherwise, keep the chip busy by running digital scans
  - Keep the chip cold (-10 ± 1 C)
  - Monitor (at least) the digital voltage (VDDD) and temperature

Beam spot 10 cm from the source



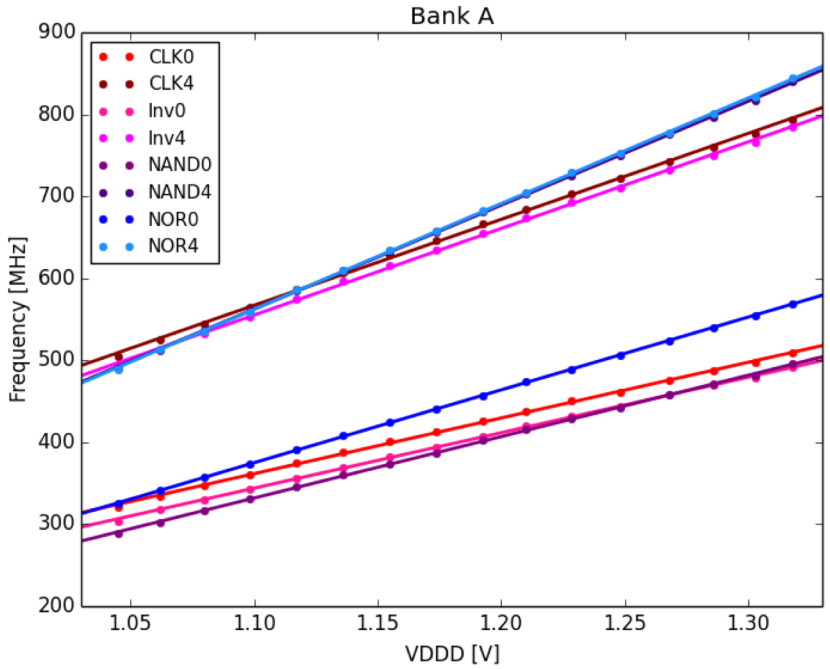
Sketch of X-ray setup

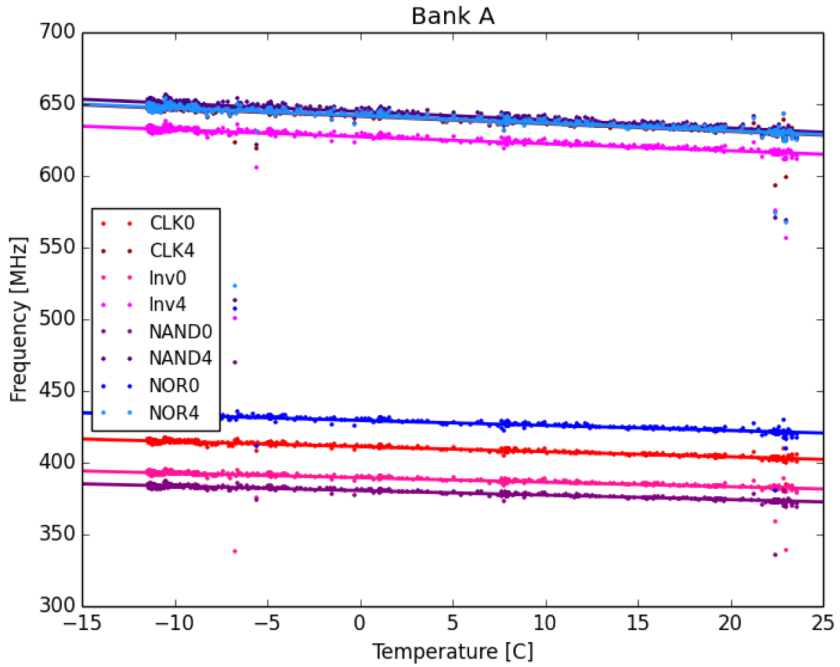


Ring oscillators in ITkPixV1

- Ring oscillators frequency depends on digital voltage (VDDD) and temperature
- Measurements before irradiation:
  - Frequency vs VDDD: change by up to 200 MHz between 1.0 and 1.3 V → used to account for VDDD changes during irradiations
  - Frequency vs temperature: change by up to 20 MHz

Frequency vs VDDD

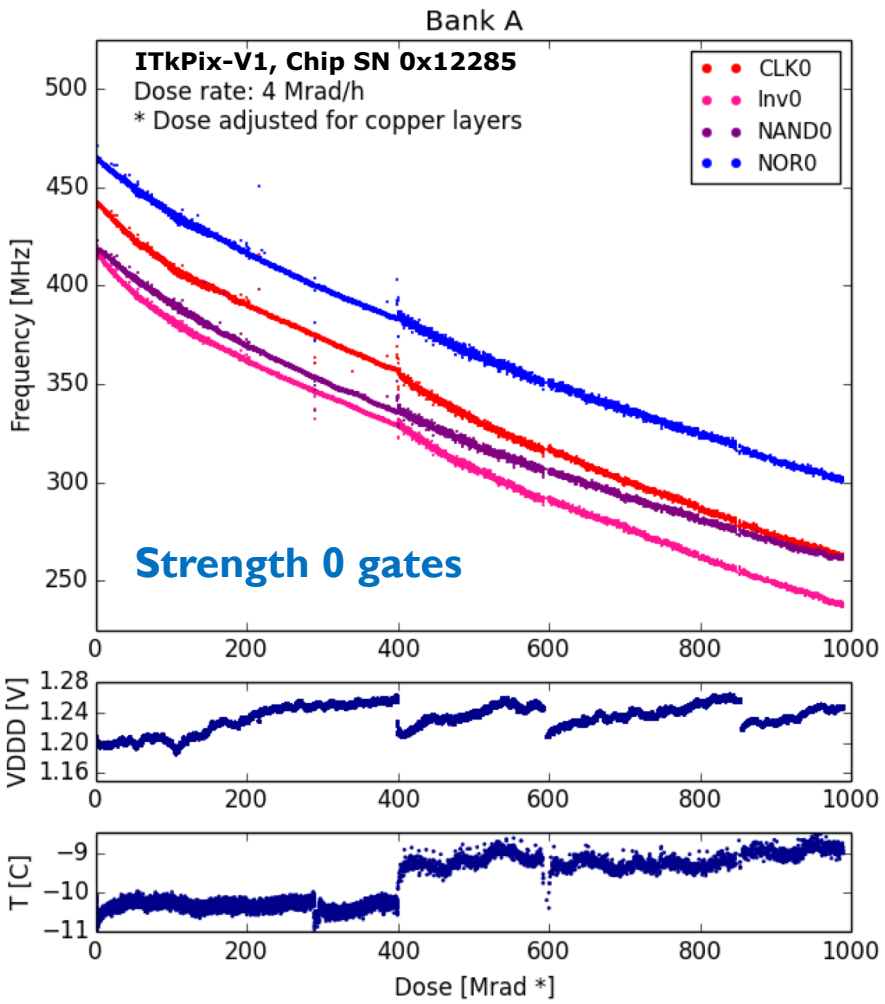


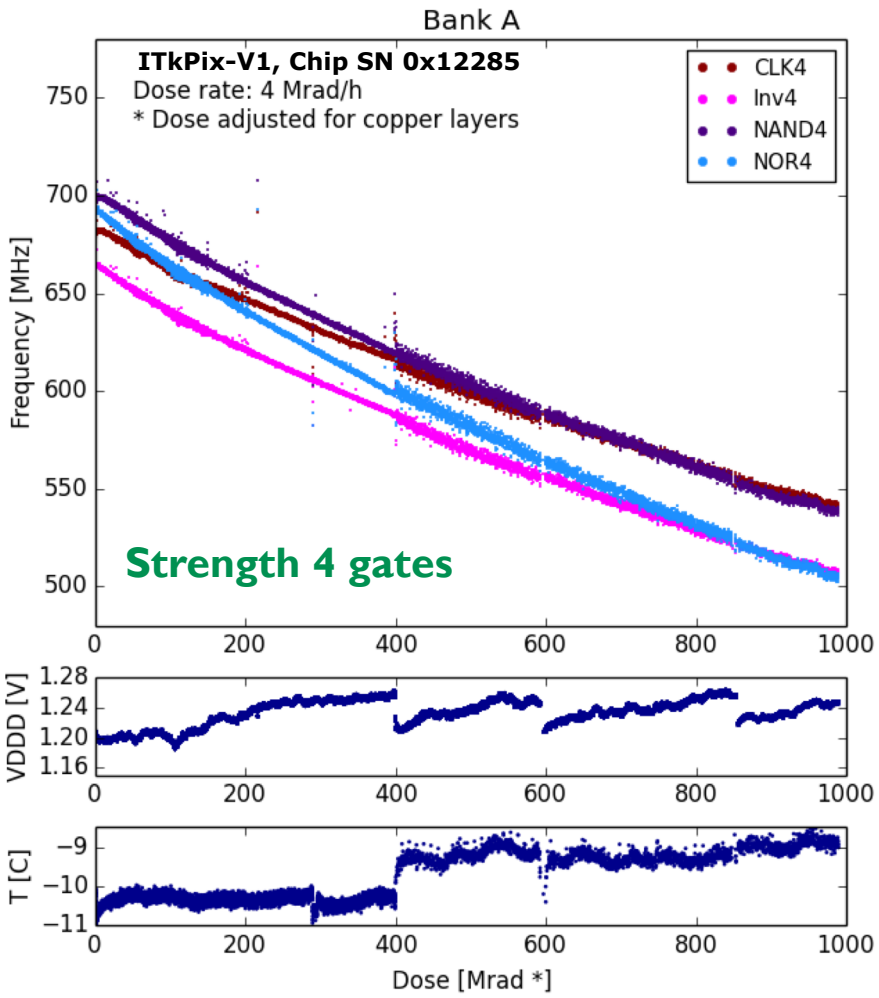


Frequency vs temperature

High dose rate irradiations

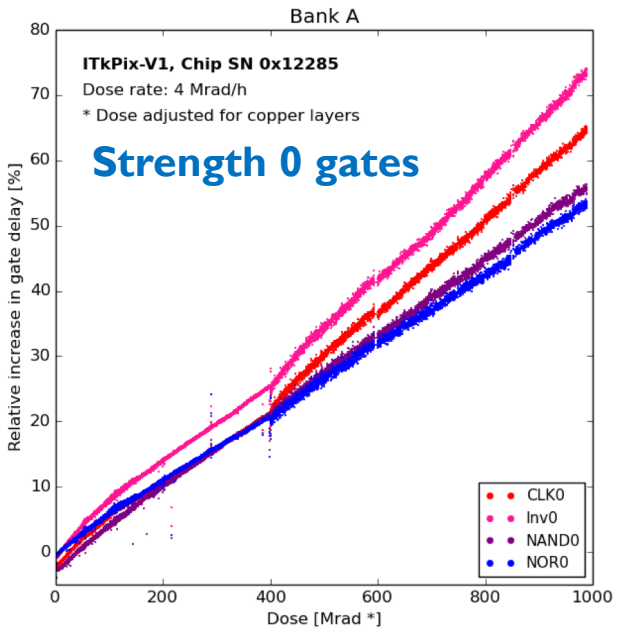
- Several high dose rate irradiation campaigns performed
- E.g. with 4 Mrad/h @ Oxford
- Monitoring of VDDD and temperature
- **No operational issues up to 1 Grad**
- Expected decrease in ring oscillator frequencies

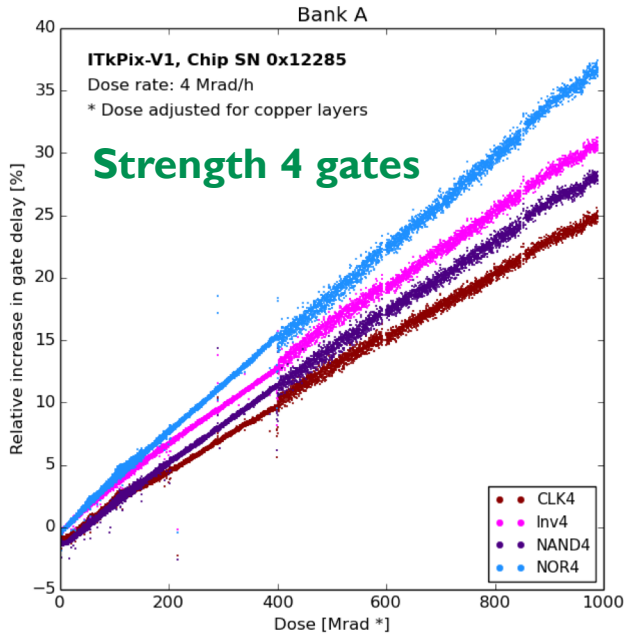


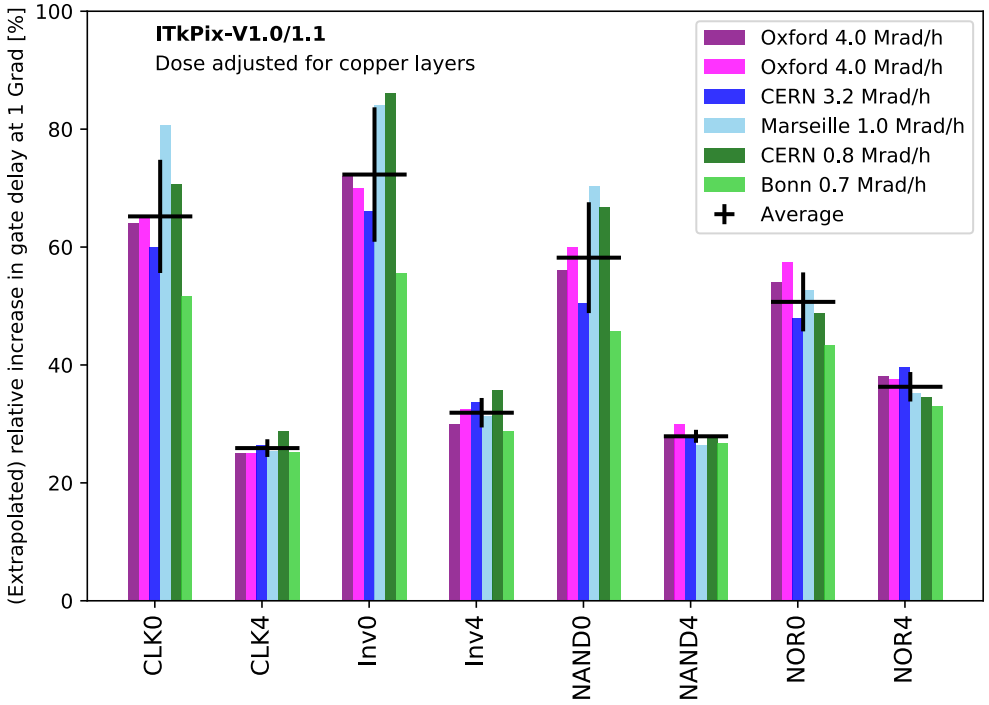


High dose rate irradiations

- Calculate relative increase in gate delay for each ring oscillator as $T_D = 1/(N \cdot f)$
- At high dose rate:
  - Increase for strength 0 gates up to 80% (→ not used in the chip)
  - **Increase for strength 4 gates up to 40%**







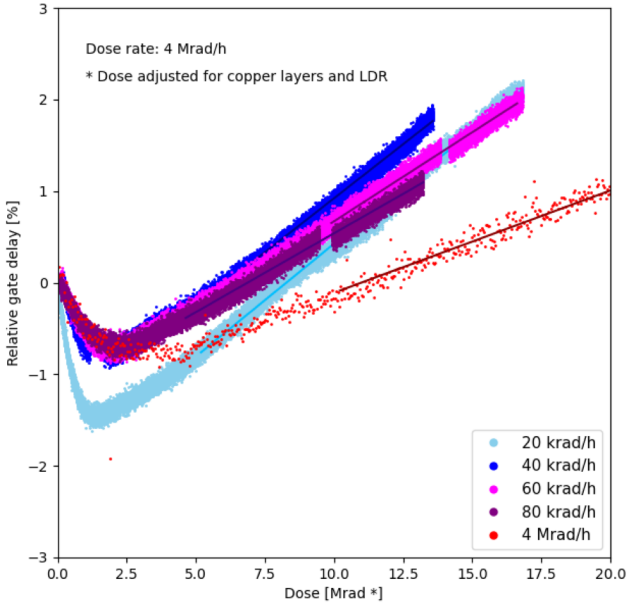
- Comparison of high dose rate irradiations at different sites

→ **Good agreement, especially for strength 4 gates**

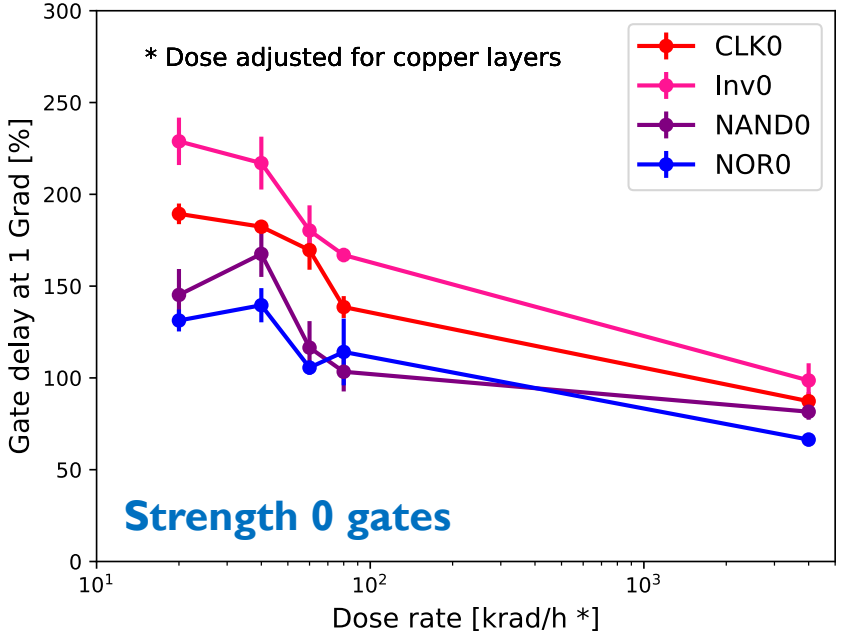
Low dose rate effects

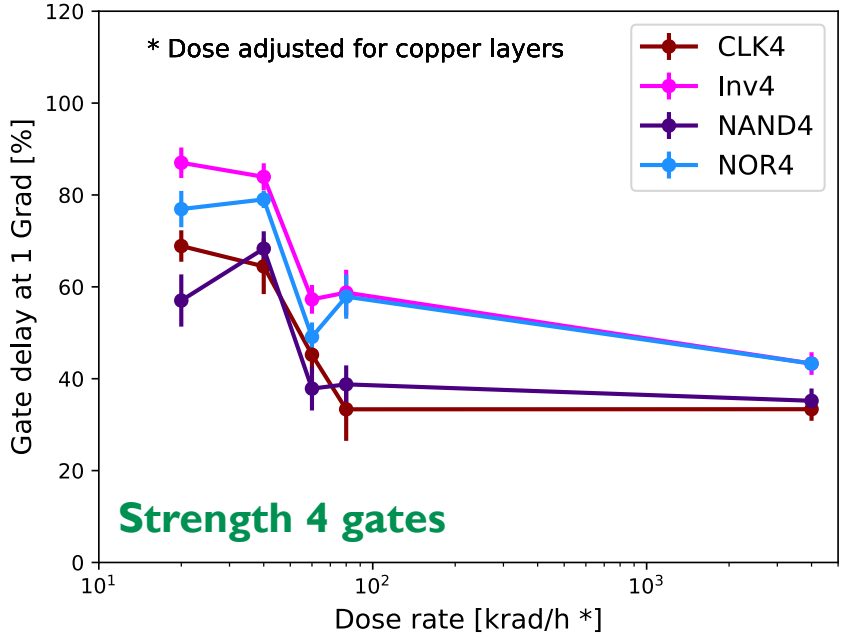
- Impact of low dose rate (<100 krad/h) effects studied for low total doses in X-ray setups
- **Damage increases for low dose rate by approximately factor 2 (assuming optimistic linear extrapolation)** → effect stronger for strength 0 gates
- Trend flattens out at both low and high dose rates

Delay for different dose rates



Increase in gate delay as a function of dose rate





Low dose rate delay degradation

- Measurements with SLIPPER (**SL**ow **I**rradiation of **P**hase-2 **P**ix**E**l **R**eadout)
- Low dose rate irradiation of RD53A chip with Kr-85 at 25 krad/h

→ collected 550 Mrad of total dose over 3 years

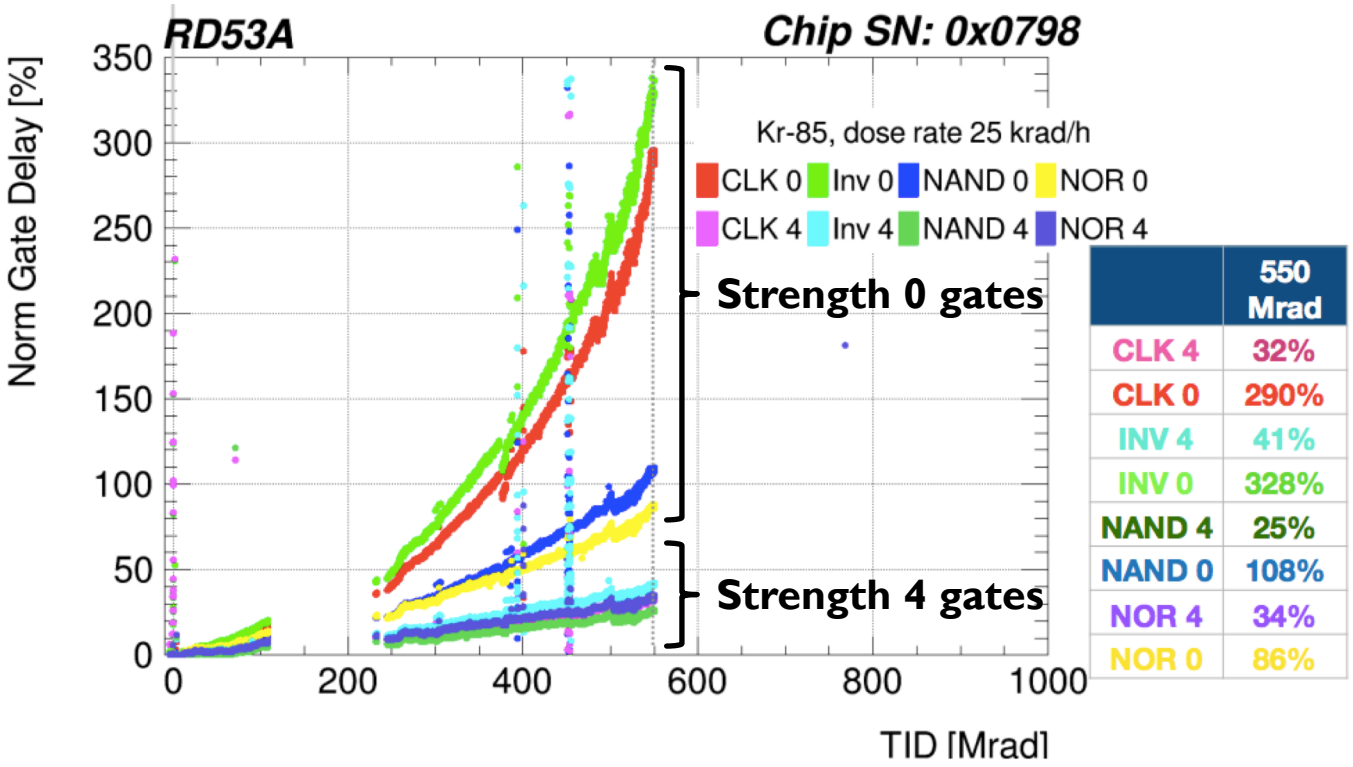
- Delay degradation seen to be non-linear with for strength 0 gates

→ **Linear scaling of HDR results seems to not be appropriate**

→ Further study needed

→ Additional SLIPPER setups planned with RD53B

- Note: Strength 0 gates not used in RD53B logic



	550 Mrad
CLK 4	32%
CLK 0	290%
INV 4	41%
INV 0	328%
NAND 4	25%
NAND 0	108%
NOR 4	34%
NOR 0	86%

Results from Aleksandra Dimitrevska

Analog performance

- Analog performance of ITkPixV1 after irradiation to 1 Grad
- Performed threshold scans after irradiation for a large range of parameters → to compare with measurements before irradiation
- Number of failed pixels <5% for most parameter settings

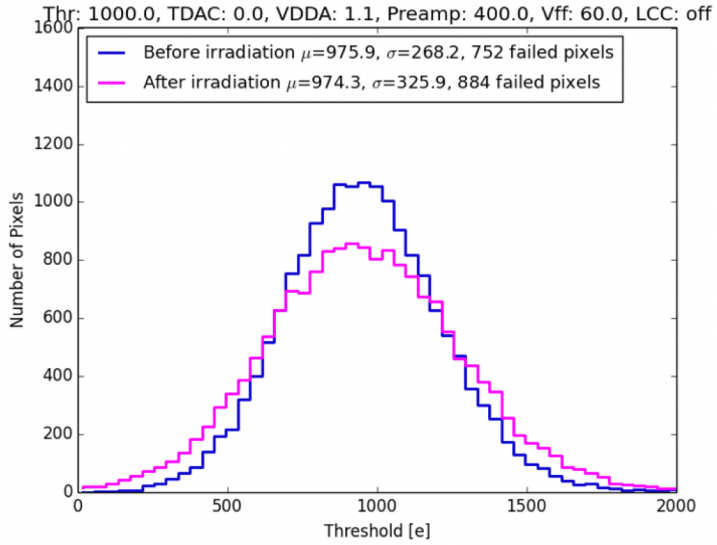
→Increase in width of threshold distributions

→**Chip operational for most settings after irradiation to 1 Grad**

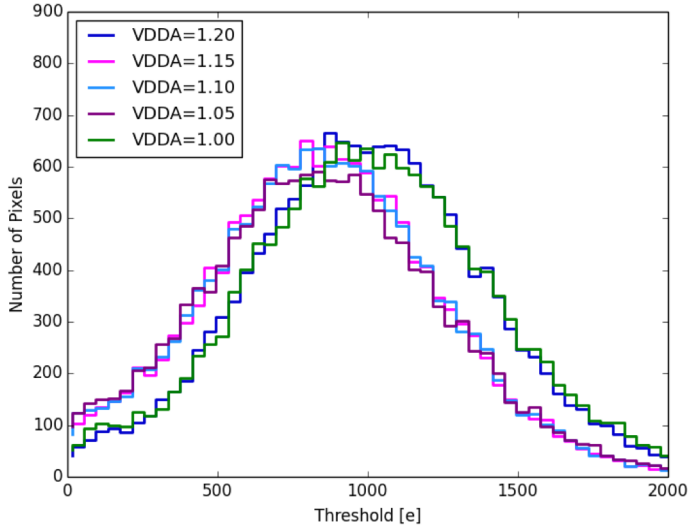
- At chip settings given by simulations, decrease analog voltage (VDDA)
- RD53A stopped working at VDDA < 1.1 V

→ **Even after irradiation ITkPixV1 is operational down to 1.0 V**

Threshold scan before and after irradiation



VDDA study after irradiation



Conclusions

- **Presented irradiation results on the latest ATLAS readout chip prototype**
- **High dose rate irradiation results**

→ Several HDR irradiations performed up to 1 Grad, gate delay increase of up to 40% observed for strength 4 gates

- **Low dose rate irradiation results**

→ Several LDR irradiations performed at different dose rates, increase in damage at low dose rate observed

→ Non-linear behaviour of delay degradation at high total dose rates

- **Analog FE performance during and after irradiation**

→ No significant issues with AFE after 1 Grad

→ Most aspects of the ITkPixV1 chip tested and performing well up to total doses of 1 Grad

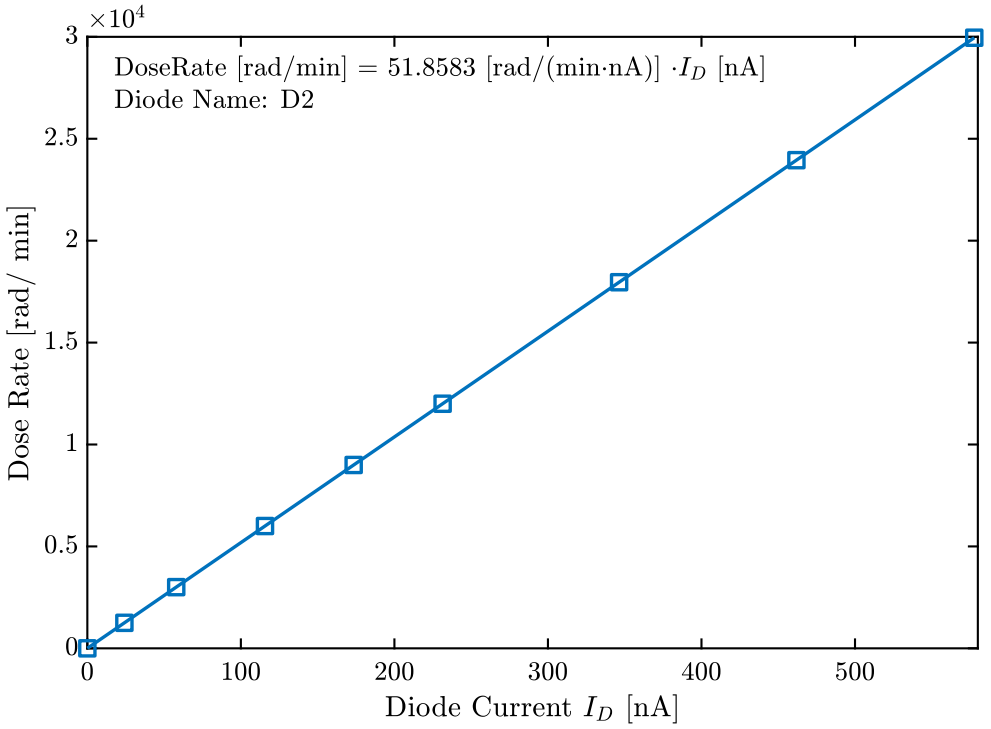
Thank you!

Any questions?

Backup

Calibration setup

- X-ray tube with tungsten target, operated at 40kV
- 150 µm Al filter for to remove low-energy components
- Dose rate calibration using AXUVHS5 calibrated pin diodes
- Properties:
  - Sensitive depth: 50 µm
  - Sensitive area: 1 mm^2
  - Biasing voltage: 50 V
- Measures current which can be used to convert into SiO_2 equivalent dose



Example calibration curve for AXUVHS5 diode

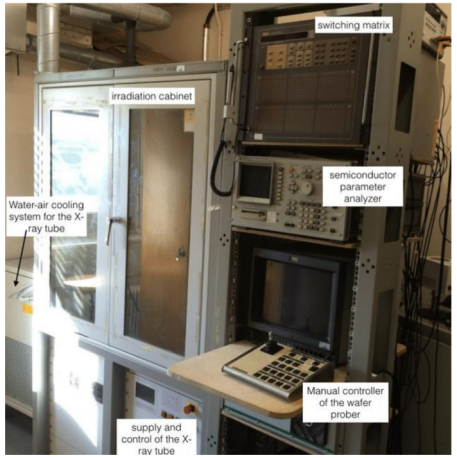
Irradiation sites

CERN ATLAS

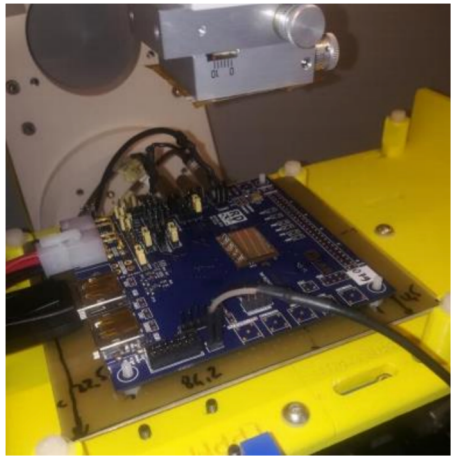
Bonn

Oxford

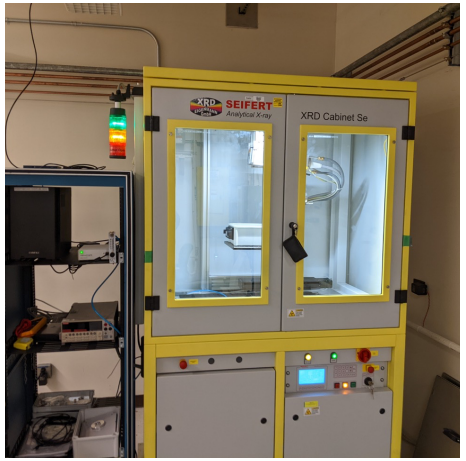
CERN EP/ESE



Marseille



LBL



- **Irradiations of RD53B chips performed at five different sites**

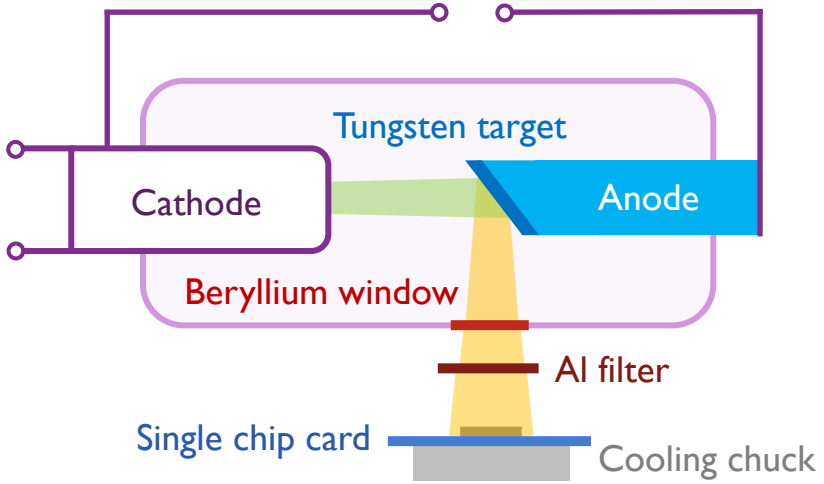
→ LBL setup preparing for irradiations soon

Common irradiation procedures

- Decided on common configuration for X-ray setups involved in irradiations of ITkPixV1 (40 kV, 150µm Aluminium filter)
- Dose rate calibration using calibrated diodes (provided by CERN - F. Faccio et al.)
- Common calibration procedure described in document here
- Add additional 20% correction factor to delivered dose due to absorption in the copper layers in the chip (backup)
- Common irradiation procedure:
  - Perform pre-irradiation measurements of ring oscillators and analog front-end
  - During irradiation, read the ring oscillator frequency (at least every 0.1 Mrad)
  - Otherwise, keep the chip busy by running digital scans
  - Keep the chip cold (-10 ± 1 C)
  - Monitor (at least) the VDDD voltage and temperature

Calibration diode

Sketch of X-ray setup

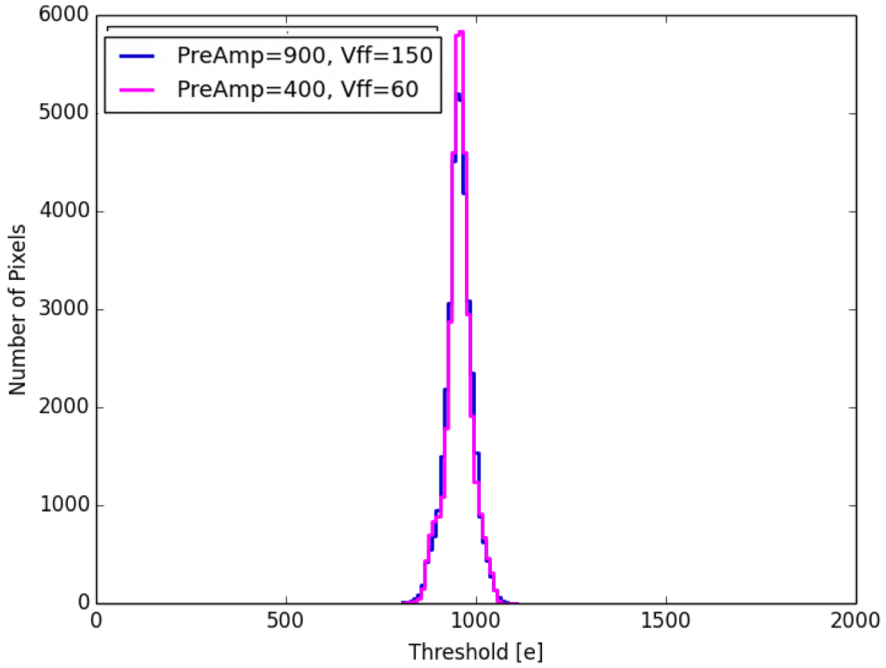


Analog FE after irradiation - Tuning

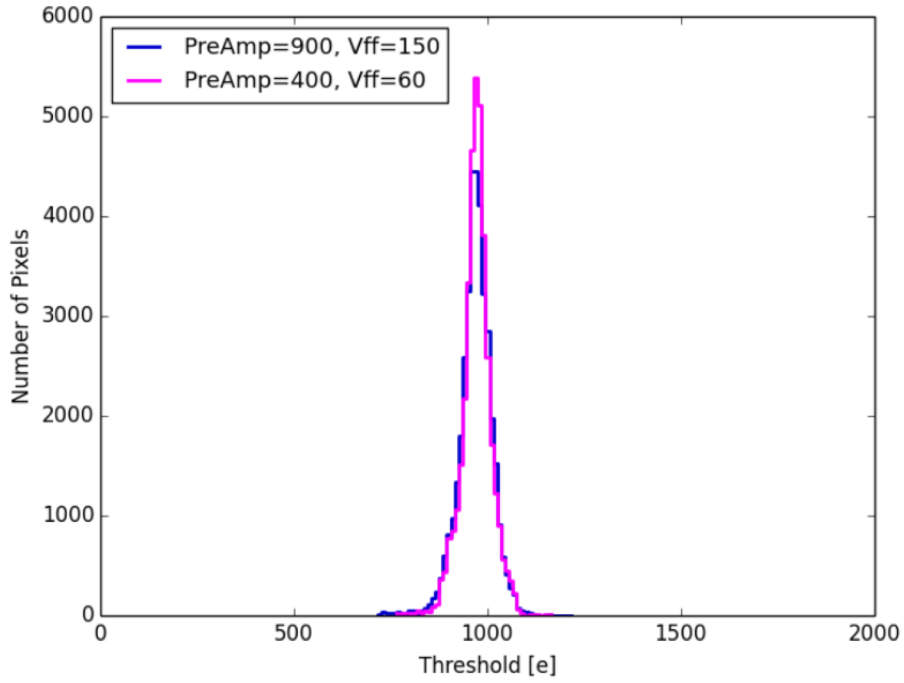
- Tune and measure threshold at two points with target threshold 1000:
  - Preamp=900 + Vff=150 and Preamp=400 + Vff=60
  - Other parameters: VDDA= 1.2, LCC off

→ Chip still well tuneable after irradiation to 1 Grad

Before Irradiation



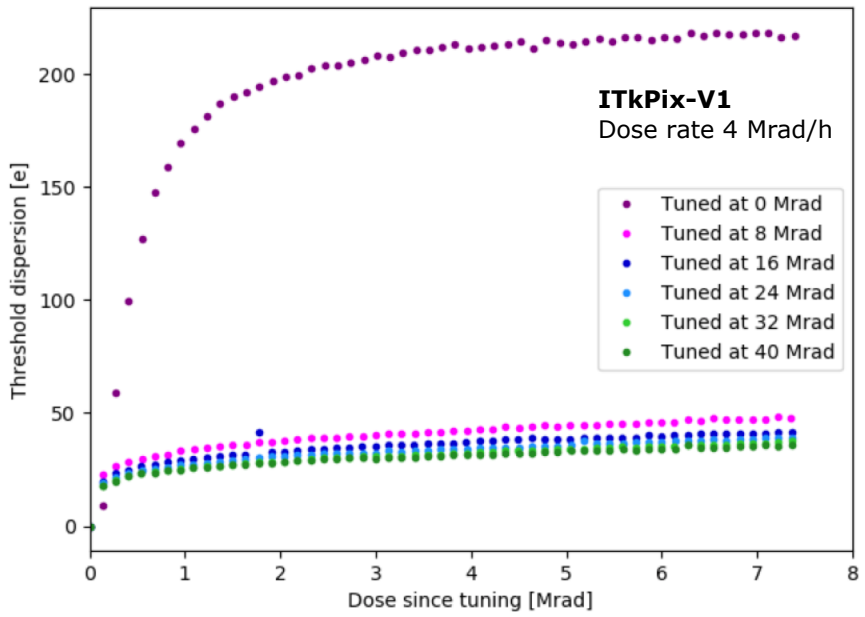
After Irradiation



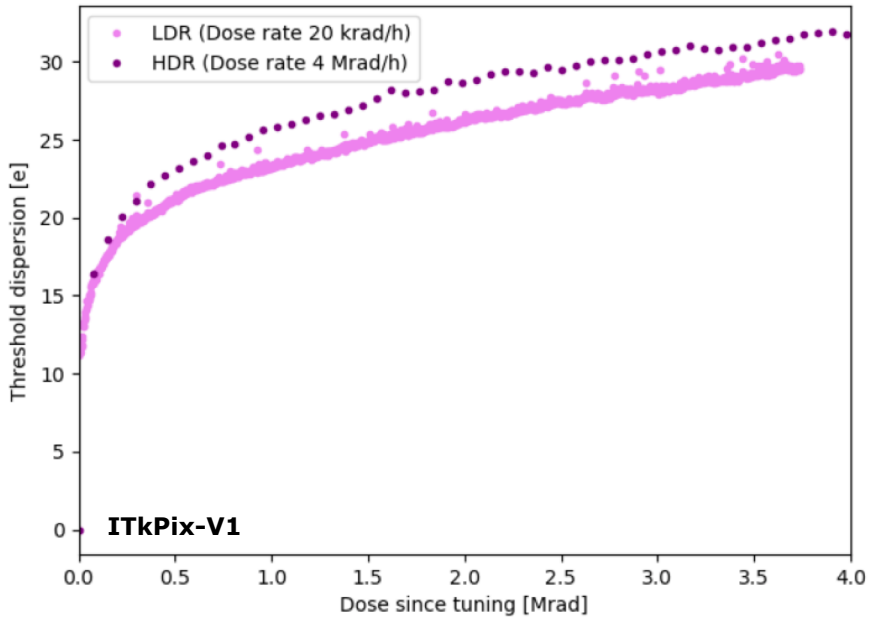
Analog front-end during irradiation

- Characterise damage to analog front-end (AFE) during irradiation
- Calculate how quickly a tuned threshold distribution disperses with irradiation
  → very quick dispersion at the beginning of the irradiation, afterwards thresholds disperse much slower
  → **most damage to the AFE in the first few Mrad**
- No significant difference between low and high dose rate → expected due to larger transistor size

Threshold detuning at different total doses



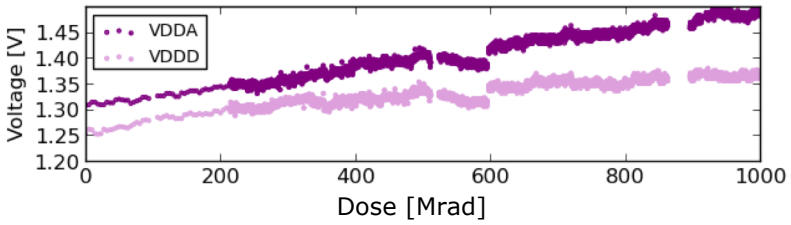
Threshold detuning at different dose rates



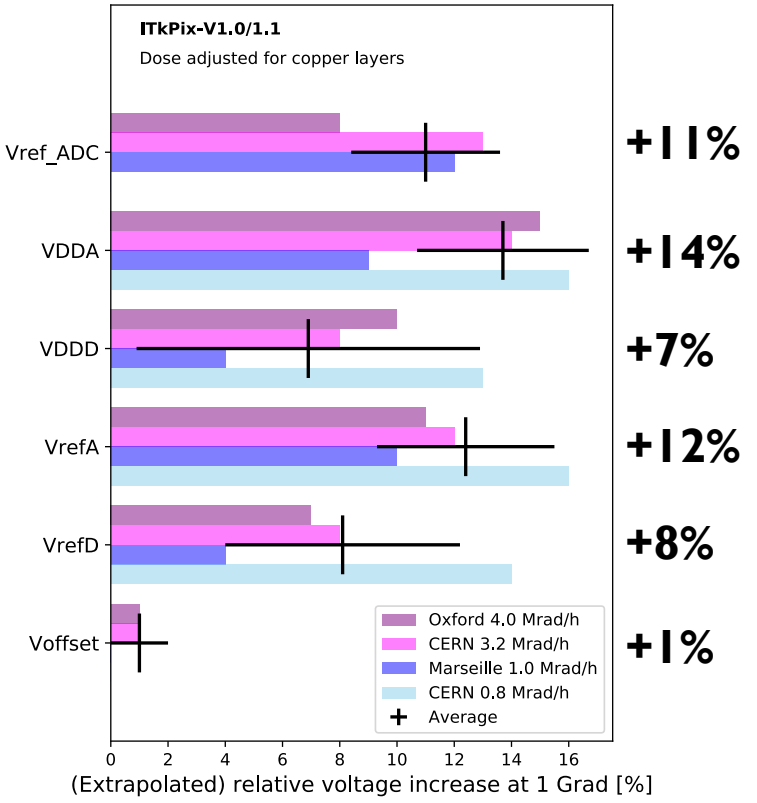
SLDO irradiation

- Drift of different chip reference voltages observed with irradiation (up to +15%)
- Irradiation campaigns focusing on SLDO behavior performed
- No start-up issues observed after irradiation to 1 Grad
- Later start-up due to shift in untrimmed VDDA value

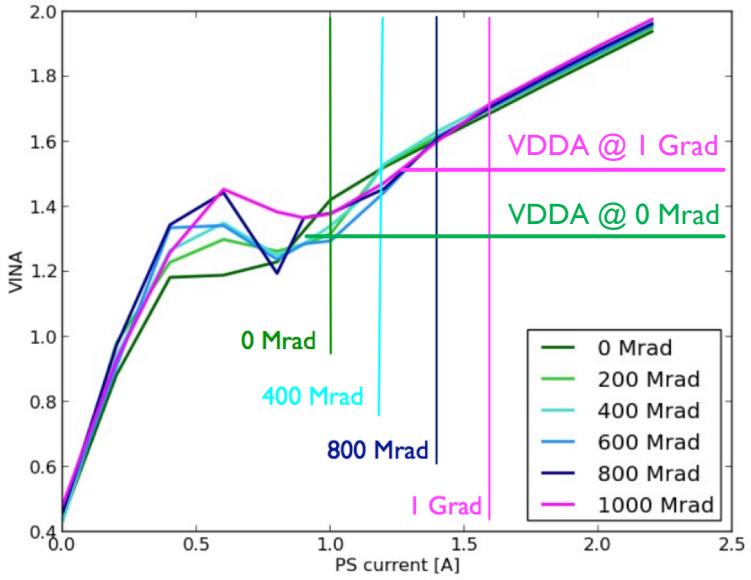
VDDA/VDDD with irradiation



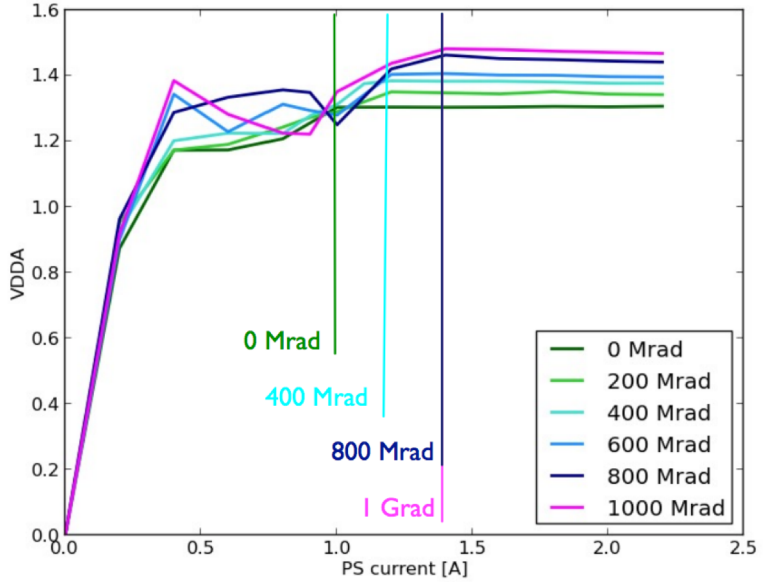
Increase of voltages after 1 Grad



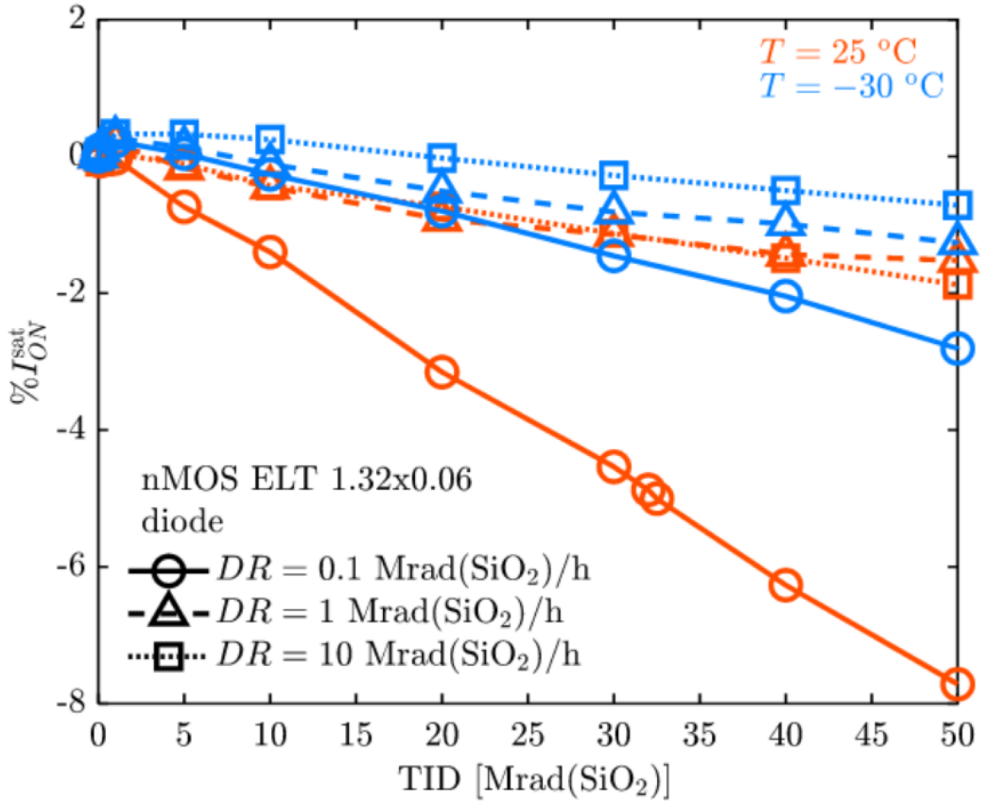
VinA

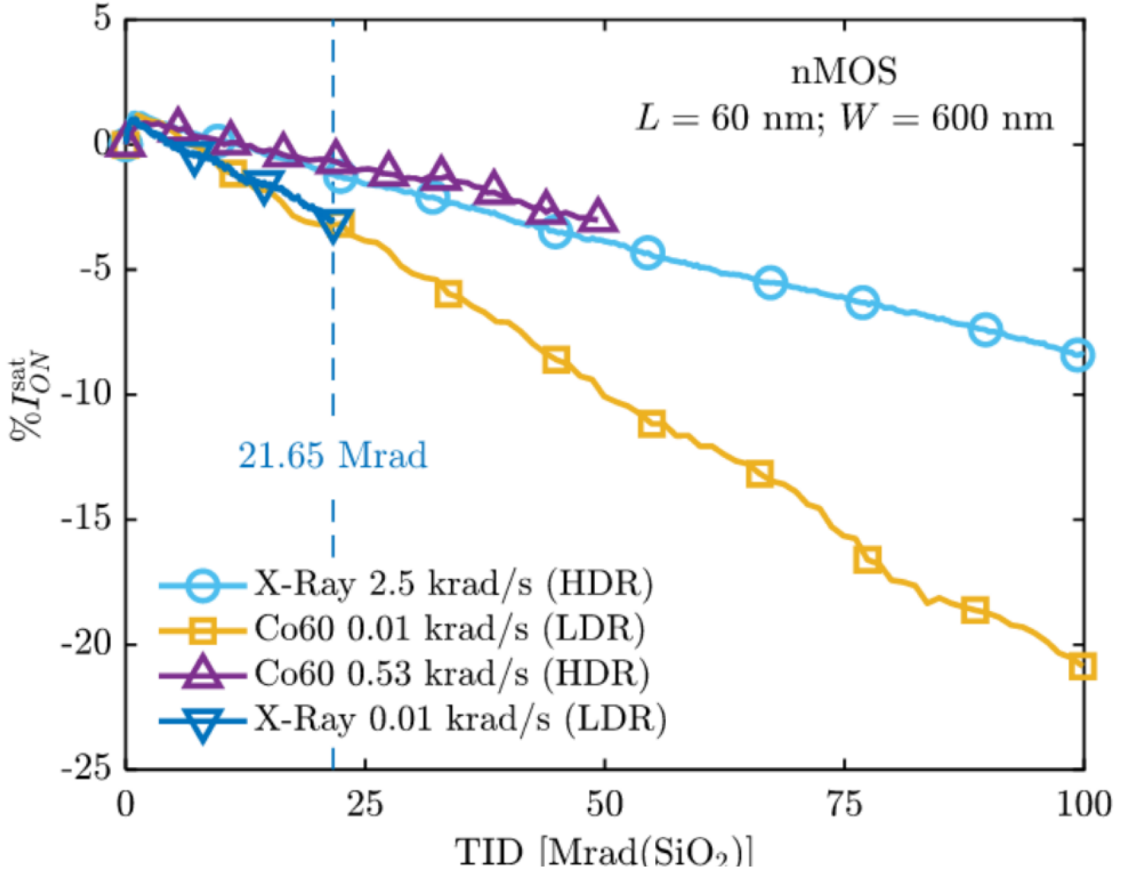


VDDA



Low dose rate expectations





F. Faccio and G. Borghello

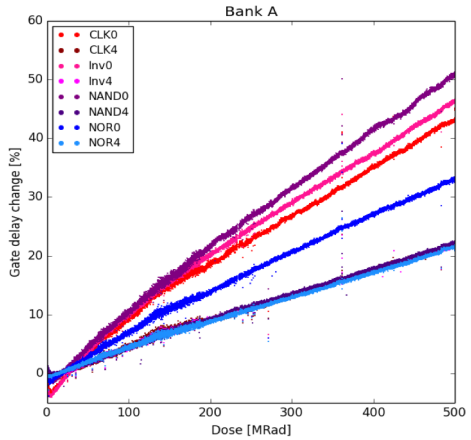
Extrapolation of gate delay at LDR

- Use the ratios calculated previously and HDR results

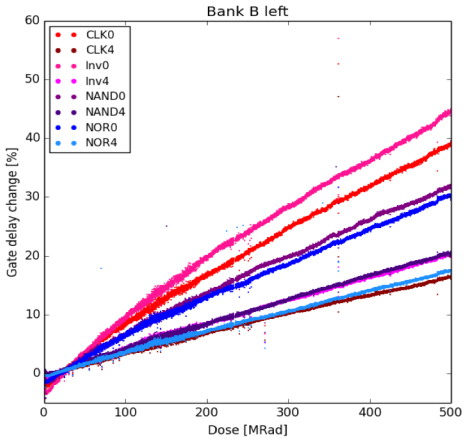
→ calculate expected ring oscillator delay degradation at 500 Mrad of LDR

- Largest for NAND 0 (50%) (but just for Bank A)
- Inv 0 (~45%) and CLK 0 (~40%) consistent between Bank A and Bank B

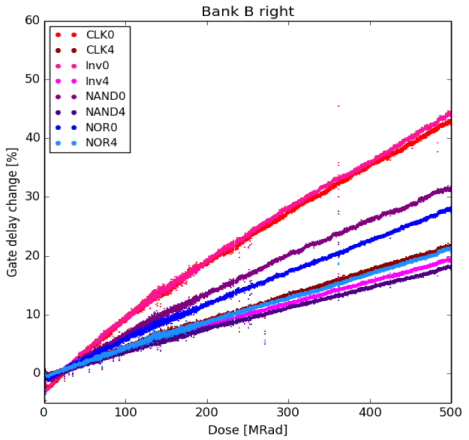
Bank A



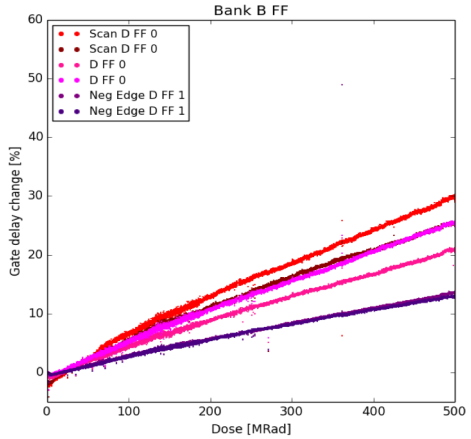
Bank B left



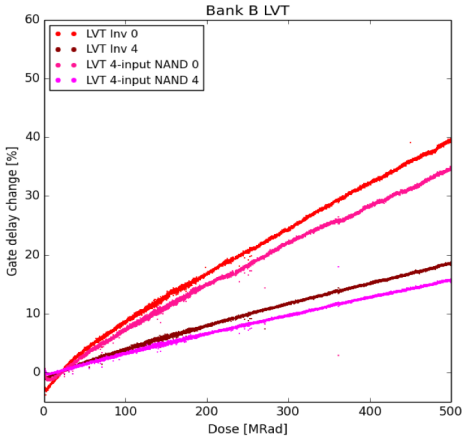
Bank B right



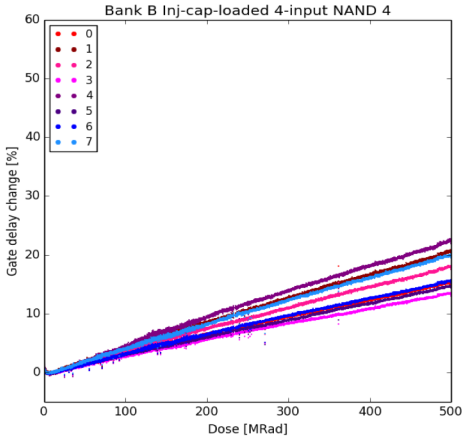
Bank B FF



Bank B LVT

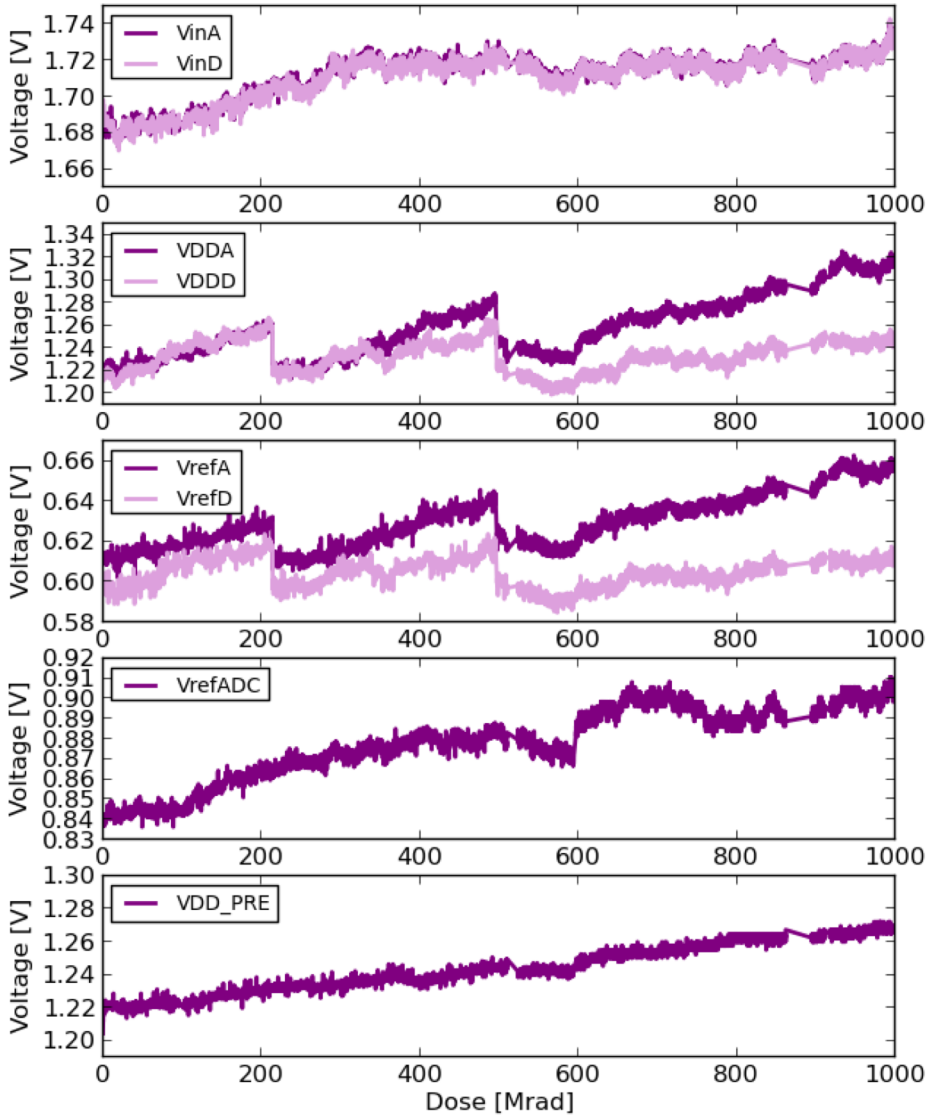


Bank B inj-cap



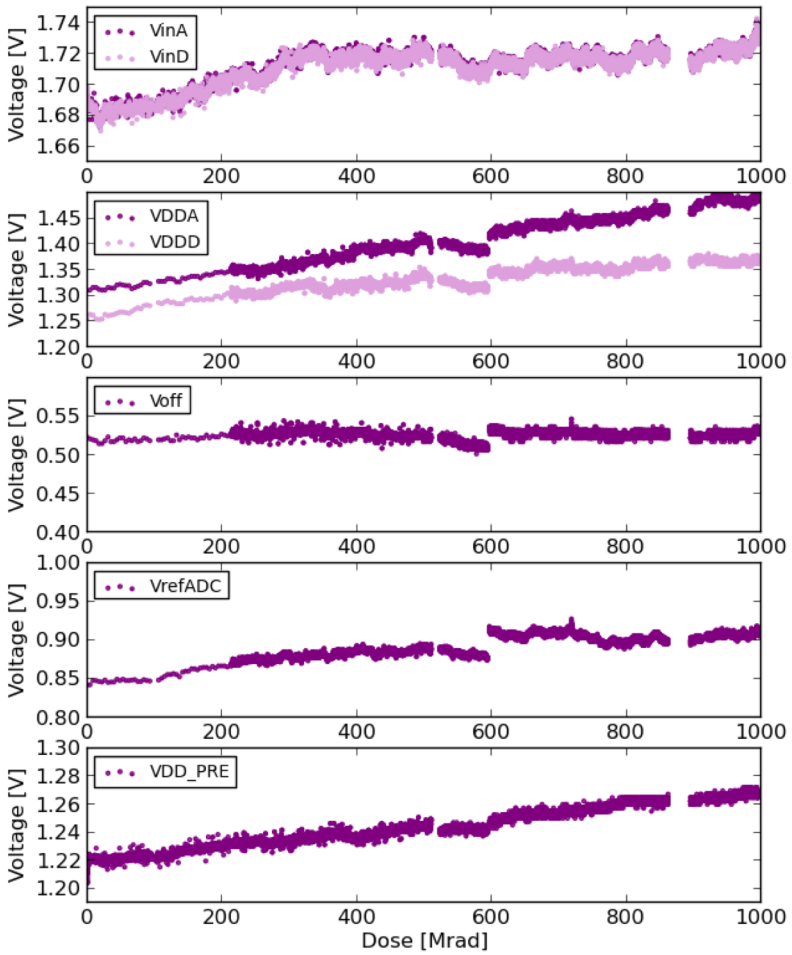
Monitored voltages

- Main focus of campaign on voltages and currents relevant to chip operation
- Chip voltages measured from the SCC pins using the AnaMon card
- VDDA and VDDD were regularly trimmed to be around 1.2 V
- For both Vref and VDD the analog voltage seems to increase faster → consistent with what was observed in measurements at other sites
- In comparison, VDD_PRE stays fairly constant

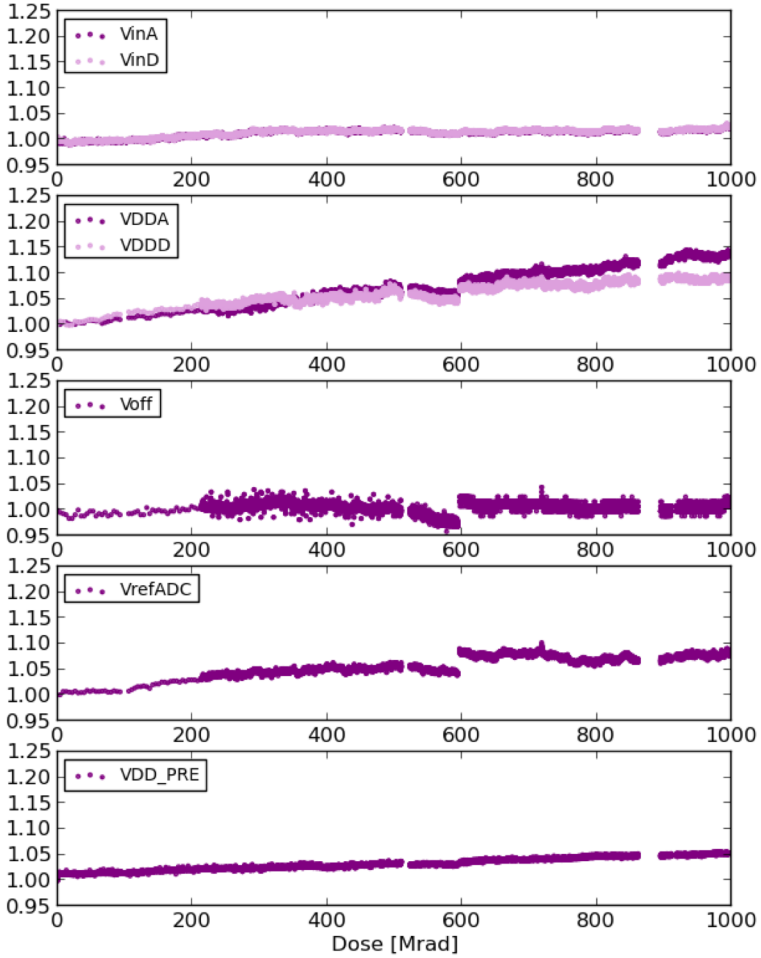


Monitored voltages

Absolute values



Relative change

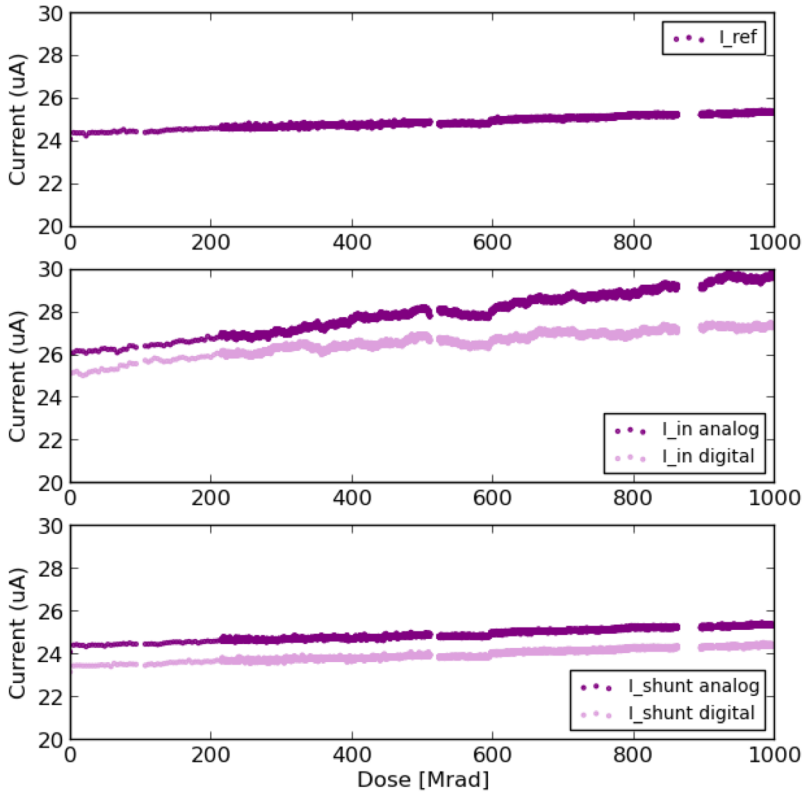


- Check voltages without change in trimbit settings
- VDDA increases more than VDDD
- Vofs stays very constant
- Relative increases over 1 Grad:

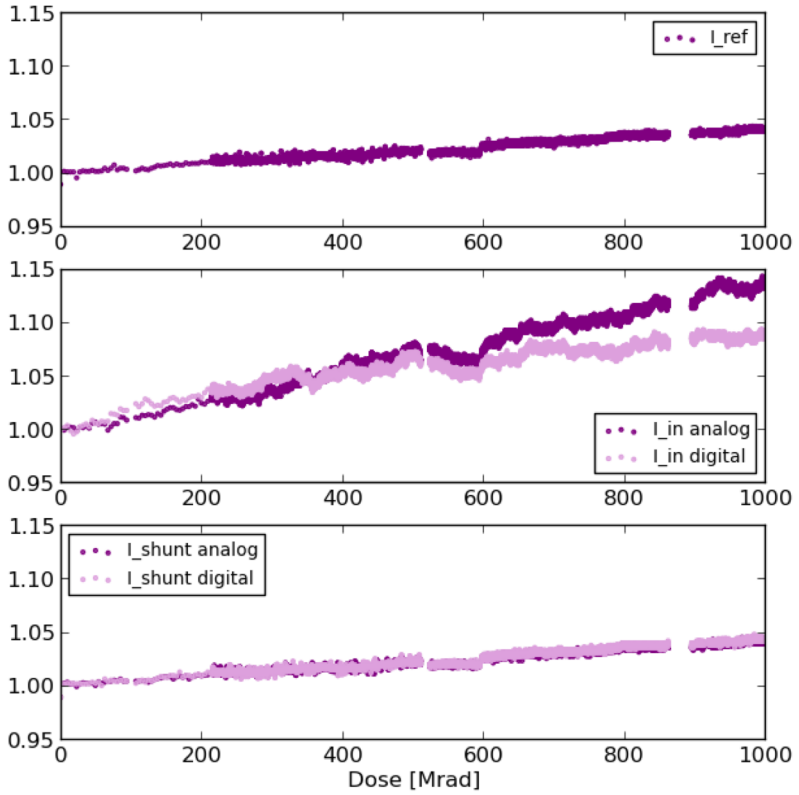
Voltage	Increase
VinA/D	+ 2 %
VDDA	+ 15 %
VDDD	+ 10 %
V_ofs	< 1%
Vref_ADC	+ 8%
VDD_PRE	+ 5%

Monitored currents

Absolute values



Relative change



- Monitored currents from the IMUX
- Relative changes over 1 Grad:

Current	Increase
Iref	+ 4 %
I_{in} analog	+ 14 %
I_{in} digital	+ 9 %
I_{shunt} A/D	+ 5%