# LGAD Development for the LHC's High--Luminosity Upgrade at Teledyne e2v

30th International Workshop on Vertex Detectors, 30 September 2021

<u>M. Gazi</u>, P. Allport, D. Bortoletto, L. Gonella, D. Hynds, D. Jordan, I. Kopsalis, S. McMahon, J. Mulvey, R. Plackett, K. Stefanov, E. G. Villani



## Outline

- Introduction: Ultra Fast Silicon Detectors
- Project overview: LGADs manufactured by Teledyne e2v
- Wafer characterization
- Dicing and post-dicing treatment
- Charge gain measurement
- Preliminary jitter measurements
- Future plans and Summary

### The need for Ultra Fast Silicon Detectors



- Pile-up is one of the major challenges for tracking at the HL-LHC
- Timing information used to disentangle overlapping events
- ATLAS High-Granularity Timing Detector placed outside the ITk

### Teledyne e2v LGAD project

- LGAD: Low Gain Avalanche Detector
- Targeting track timing resolution of approx. 30-50 ps over detector lifetime
  - Time resolution benefits from high slew rate -> increased by introducing internal gain
  - Impact ionization in gain layer -> boron implantation (p<sup>+</sup>)
- Pre-manufacture simulation done in TCAD
- University of Oxford, University of Birmingham, Open University, Rutherford Appleton Laboratory





## Teledyne e2v LGAD project

- Epitaxial layer: 50 um thick, high resistivity
- 8 different combinations of manufacturing parameters (only 3 shown below)
- Each field contains LGADs and PiN diodes of the same layout (4 mm, 2 mm, 1 mm)



Wafer code	Implant dose (normalised*)	Implant energy (normalised*)
А	1.07	1.11
В	1.07	1.05
G	1.00	1.05

\*values normalised to a reference wafer which is not included in the table

#### Characterization of wafers

#### *T* = 21°C, *f* = 100kHz

#### 4 mm devices



#### Characterization of wafers

#### *T* = 21°C, *f* = 100kHz

#### <u>1 mm devices</u>



### Laser dicing of wafers

- Laser dicing
  - Laser wavelength  $\lambda$  = 1028 nm
  - Power: 10 W
  - Beam size: 25 x 25 um<sup>2</sup>
- Measurable effects of dicing on the leakage current
  - Further investigation needed to see if saw dicing produces the same effect



Custom-made 3D printed frame to keep sensors in place and allow for direct comparison pre- and post-dicing



### Post-dicing treatment - thermal annealing

- Suspected surface states formed after wafer dicing
  - Detrimental effects of laser dicing: lower breakdown voltage, soft-breakdown behaviour (gradual breakdown over a longer voltage range, often starting relatively soon)
- Thermal annealing at 150°C applied for 2 hours



#### Charge gain measurement laser setup



30/09/2021

### Charge gain measurement – laser and amplification

- First stage amplifier: Santa Cruz Readout v1.1
- Second stage amplifier: RF amplifier FEMTO HSA-X-2-40, 40 dB – 2GHz
- Impedance matched to 50 Ohm
- The combined effect of the chain of amplifiers simulated in SPICE
  - Estimate the gain of the chain
- Laser wavelength: 1064 nm
  - average energy: 77.9 fJ
  - pulse width 69.5 ps



# Charge collected and gain - LGAD vs PiN (1mm)

- Conversion from the amplifier output to collected charge is achieved by estimating the gain of the chain of amplifiers from a SPICE simulation (92.5 dB or 42,170 for C<sub>in</sub> of 2 pF)
- The gain is estimated as the ratio of the charge collected by LGAD and PiN
- Small additional correction (approx. 2.2%) due to the bandwidth limitation of the amplifier chain not included yet



## 1mm LGAD jitter measurement – preliminary results

- Jitter the spread (standard deviation) of time delay between 50 % of trigger signal amplitude and 50 % of LGAD signal amplitude
- Average energy of the laser pulse lowered below 79 fJ
- Low pass filter applied at 1 GHz noise issues
- Unirradiated device; No subtraction of other contributions



*T* = 21°C

### Summary and Future Plans

- First batch of LGAD devices manufactured by Teledyne e2v, currently being tested at Oxford, Birmingham, Open University and Rutherford Appleton Laboratory
- Post-dicing treatment required (thermal annealing) laser dicing
- Wafer A 1mm: gain of around 25 at voltage of 225 V, preliminary measurement of jitter <20 ps for bias voltages above 200 V</li>
- Test wafers with other manufacturing parameters
- Quantify saw dicing effects on wafers (currently using laser dicing)
- Further timing measurements with fast laser
- Prepare for second wafer batch from Teledyne e2v
  - Larger arrays produced, possibility for individually diced devices
  - Implementation of observations from the first batch

#### 30/09/2021

#### Backup – Timing Measurement setup



30/09/2021

#### Backup – Timing Measurement uncertainties



### Backup – LGAD 1mm, 200 V



#### 30/09/2021

## Backup – LGAD 1mm, 200 V, FFT

30/09/2021



### Backup – LGAD 1mm, 240 V, histogram



30/09/2021

### Backup - LGAD Simulation I

• Fabrication steps of the devices simulated using TCAD tool from Synopsis



#### **PROCESS flowchart**

### Backup - LGAD Simulation II

• Electrical simulation setup, common to PiN and LGAD, with RC network



 Bulk radiation damage not included in this iteration, but effects of Si-SiO<sub>2</sub> surface states have been modelled

### Backup – Simulated cross-section



#### • <u>2 implantation models implemented:</u>

- MC (1e5 runs) using BCT with modified parameters
- Pearson IV (analytical)

$$\frac{\Delta E_{\rm n}}{E_0} = \frac{4M_1M_2}{(M_1 + M_2)^2} \cos^2(bI) \quad X\alpha$$

E lost by BC by Nucl. Scattering custom factor  $\alpha$  (=1 default)



Multi-body collisions for crystal [0.25,1] lattice constant assume d=1

