MAPS for Upstream Tracker in LHCb Upgrade II

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On behalf of the LHCb UII UT collaborators

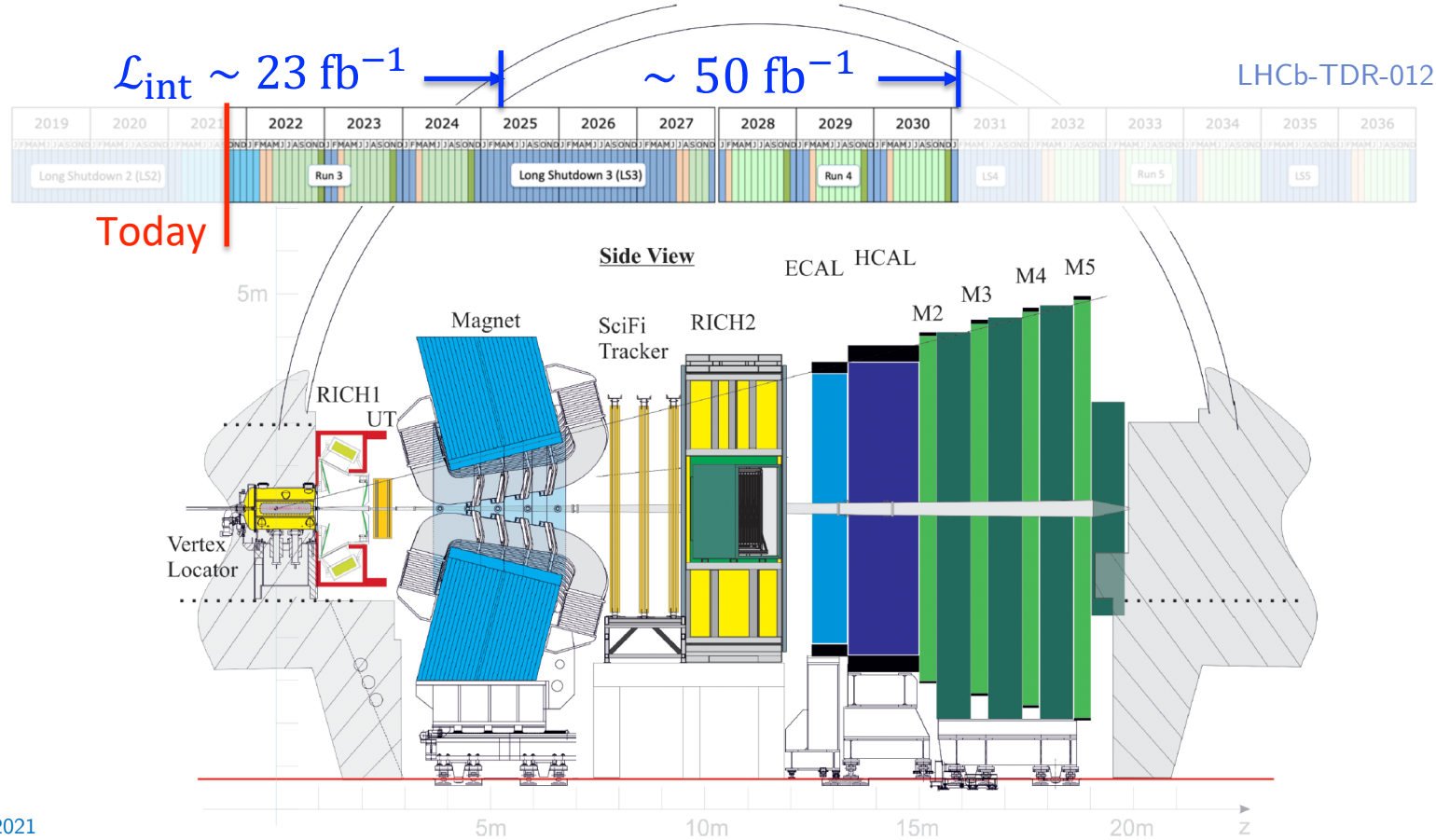
VERTEX 2021

Content

- Upstream Tracker in LHCb Upgrade I
- Upgrade II challenges
- MAPS for UT in Upgrade II

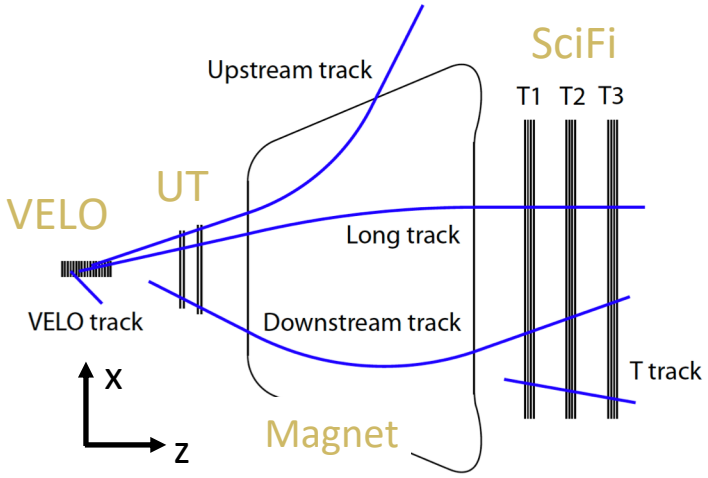
LHCb Upgrade I

- Instantaneous luminosity $\times 5 \rightarrow 2\times10^{33}\mathrm{cm}^{-2}\mathrm{s}^{-1}$
- Hardware trigger (40 MHz →1 MHz) completely removed
- New subsystems installed including the full tracking system

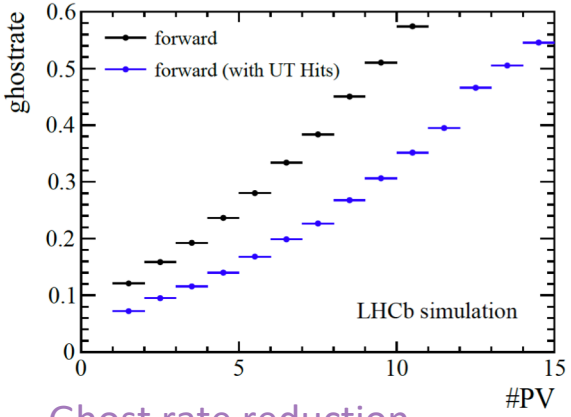


Role of Upstream Tracker (UT)

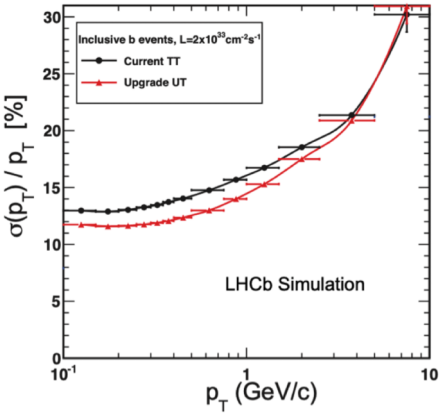
- Essential for full-software trigger
  - Speed up matching between VELO and SciFi segments
- Reduction of the ghost rate
- Improvement of resolution at low p_T
- Efficient reconstruction for long-lived particles ($K_S^0 \to \pi^+\pi^-$, $\Lambda \to p\pi^-$)



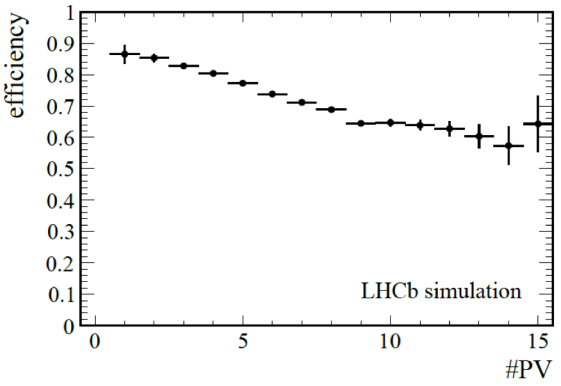
LHCb-TDR-015



Ghost rate reduction when requiring UT hits



Momentum resolution



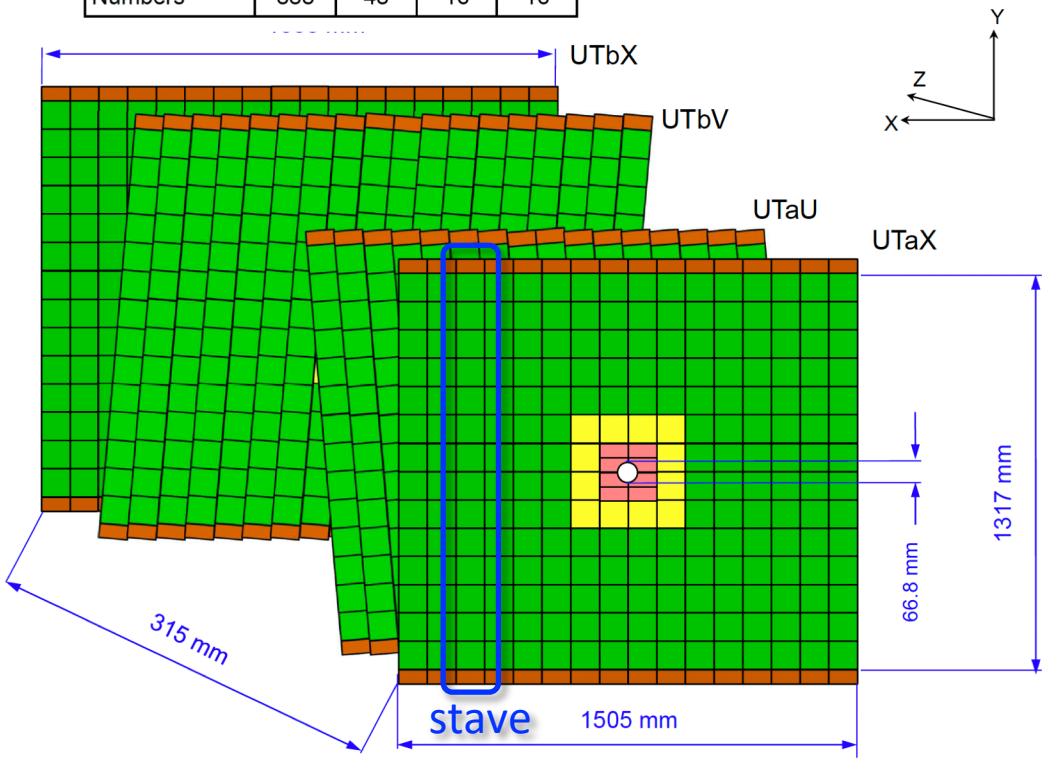
Reconstruction efficiency for downstream tracks

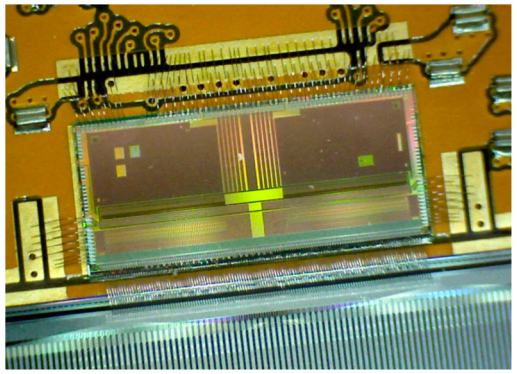
UT detector in Upgrade I

Igor Kostiuk "Tracking for LHCb Run3 - VELO detector construction and the Silicon Upstream Tracker"

Sensor	A	B	C	D
Type	p-in-n	n-in-p	n-in-p	n-in-p
Thickness(μm)	320	250	250	250
Pitch (μm)	187.5	93.5	93.5	93.5
Length (mm)	~100	~100	~50	~50
Strips/sensor	512	1024	1024	1024
SALTs/sensor	4	8	8	8
Numbers	888	48	16	16

- Four planes of silicon strip detectors
  - Strips along y-axis (or $\pm 5°$)
- Higher segmentation near the center
- Innermost $\Phi_{max} \sim 5 \times 10^{14}\ n_{eq}/cm^2$
- Readout ASICs "SALT" at sensor proximity

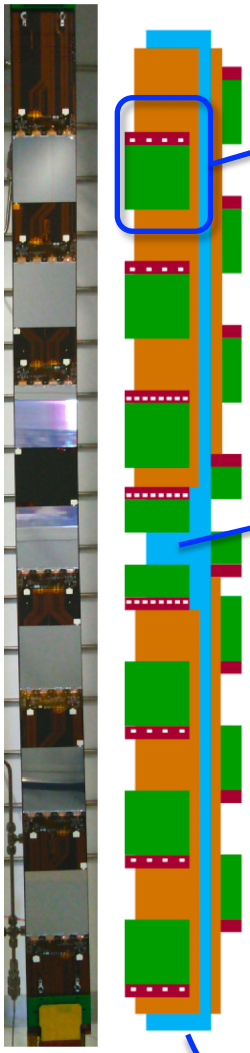


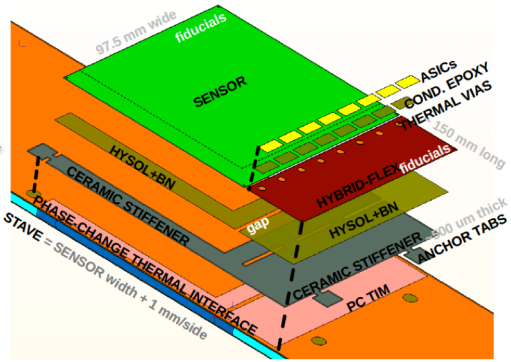


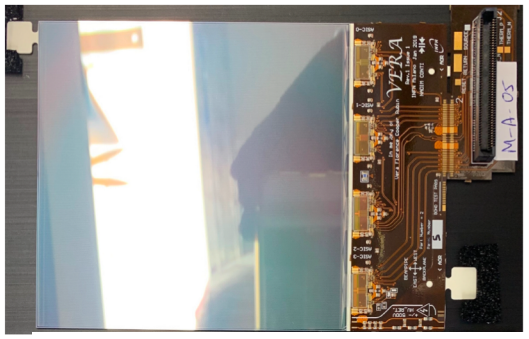
Silicon ASIC for LHCb Tracking

- 40MHz readout
- 128 channels, 6-bit ADC
- Common mode noise correction & zero suppression
- Radiation tolerance of 30 MRad

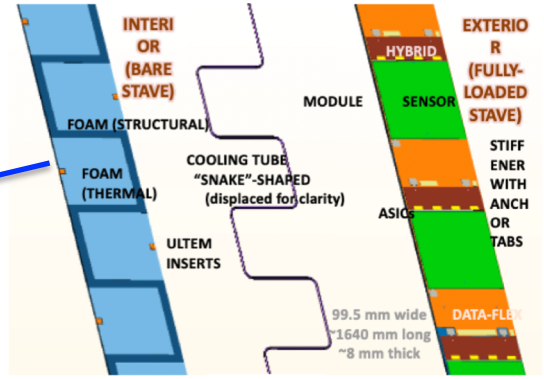
UT detector in Upgrade I



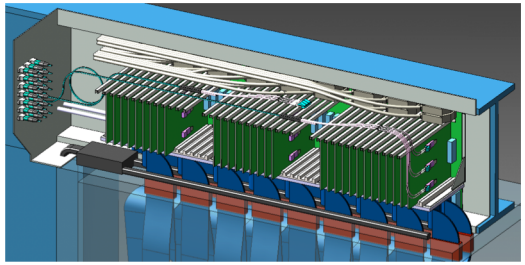




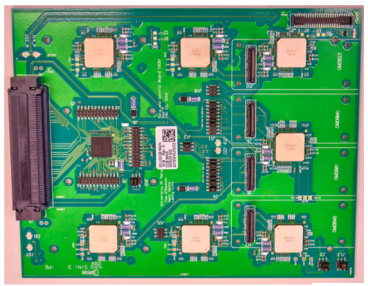
Module with 4 SALT chips



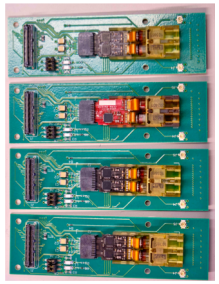
- Modules mounted on both sides of staves to allow overlapping
- Stave: Cooling tube (CO_2) embedded in foam core + CFRP face sheets
- Stave readout at both ends:
  - data formatting, timing distribution, control and optical conversion



Peripheral Electronics Processing Interface



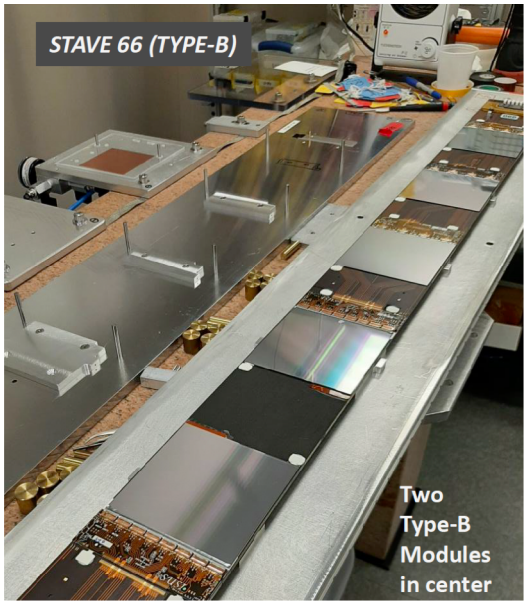
Data Control Board with GBT chipset

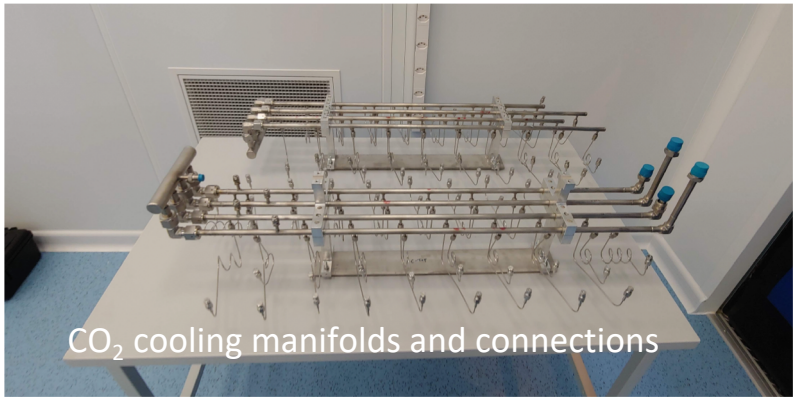


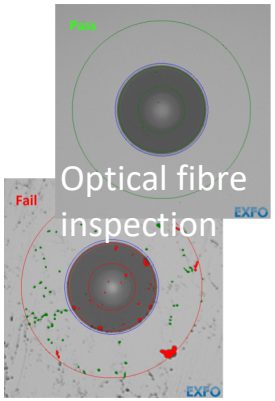
Versatile link optical tranceiver

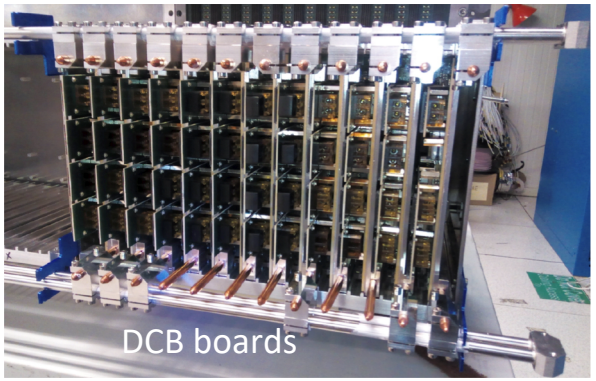
UT installation

- Module production complete for core
- Stave production progressing well
  - Type A/B for C-side completed
- Preparation work in parallel:
  - PEPI/LV/HV/cooling/mechanics…
- First stave installation expected in mid-October
- Assembly of C-side in November, A-side by Feb 2022 before cavern closure





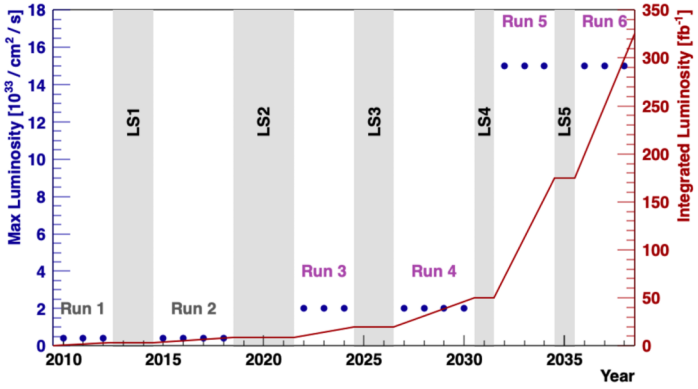




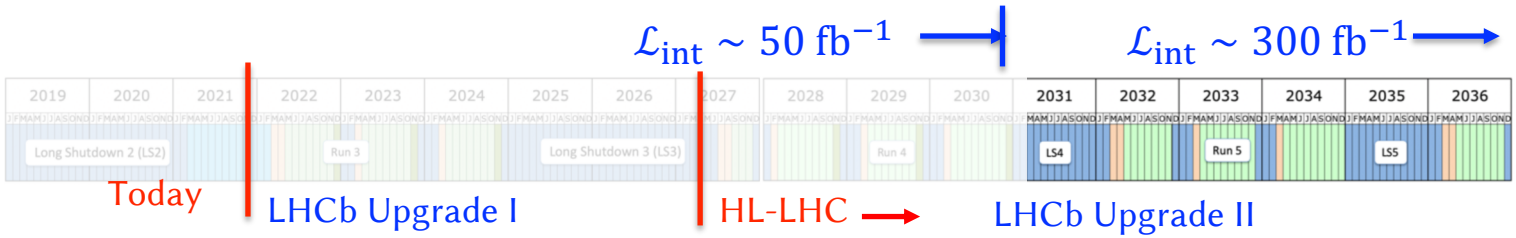
Upgrade II

- Upgrade II planned at LS4 to fully exploit the HL-LHC potential in flavor physics & beyond
- Aim for an luminosity of $1.5 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$ and $\mathcal{L}_{\mathrm{int}} \sim 300\ \mathrm{fb}^{-1}$ in the lifetime of LHC

- High-lumi operation challenges:
  - Large pile-up: $\mu \sim 1 \rightarrow 5$ (UI) $\rightarrow 40$ (UII)
  - High multiplicity
  - Severe radiation damage
  - ...



CERN-LHCC-2017-003
arXiv: 1808.08865

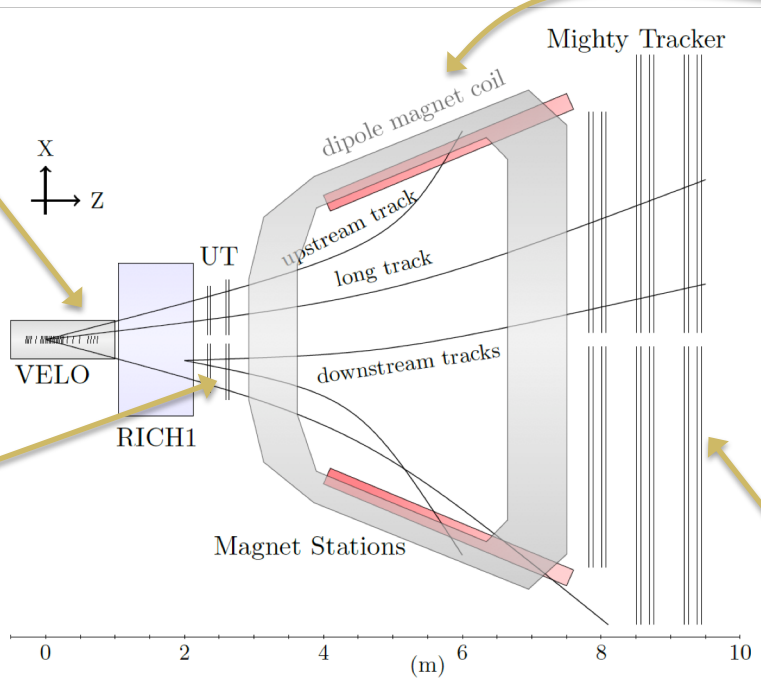


Tracking system at Upgrade II

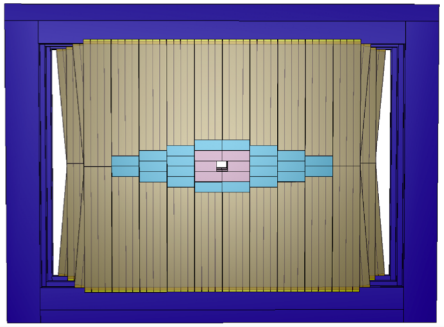
- Efficient track reconstruction is key in real-time software trigger
- Physics benchmark channels requires
  - Momentum resolution ~ 0.5-1%; IP resolution ~ 25 um
  - Long tracks with >95% efficiency and <10% ghost rate
  - Without reducing current acceptance or adding more material budget

New technology
Adding timing info

Nathan Jurik "A pixel detector with Timing for LHCb Upgrade 2"



New detector inside magnet to improve low momentum tracking



Will the current UT work under UII condition?

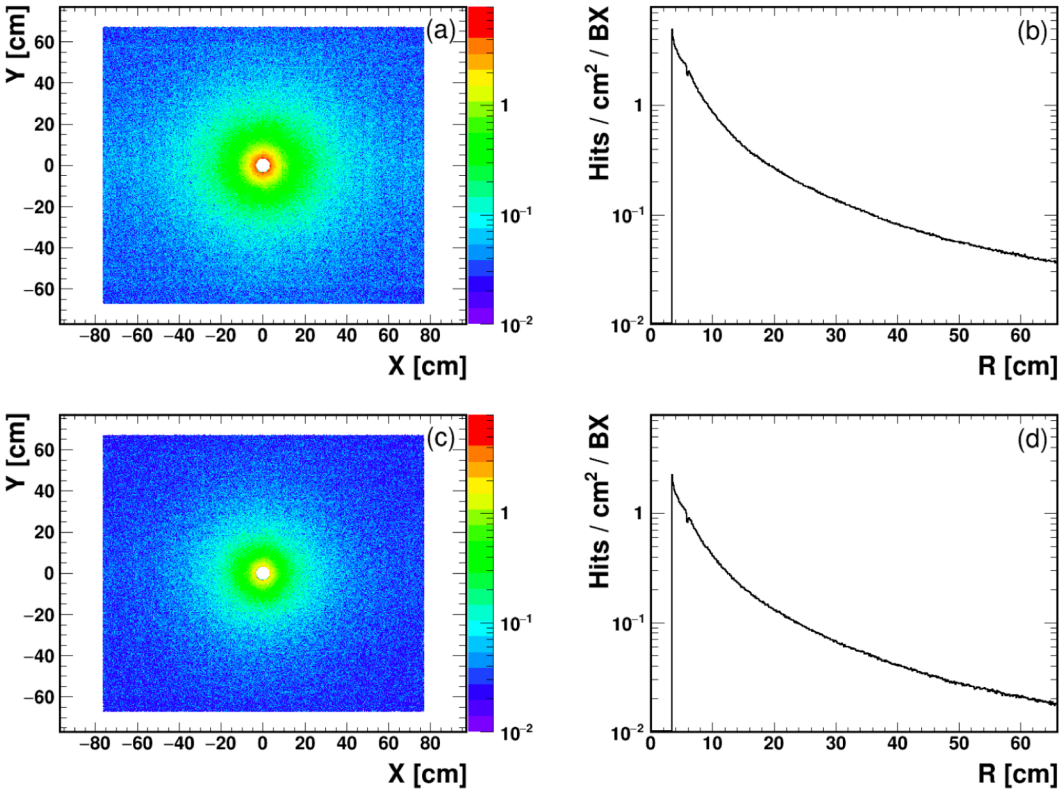
Inner part of SciFi replaced with "Mighty Tracker" using CMOS

Upgrade II challenges for UT

- The max hit density ~ 6 hits/cm^2/BX for beam-beam crossings at UII
  - Or 4 hits/cm^2/BX averaged over all bunch crossings (2400 bb/3564)
- For Pb-Pb it is ~ 3 hits/cm^2/BX, while <50% bunches has beam-beam crossing, hence less problem with data rate

$p\ p$

Pb Pb

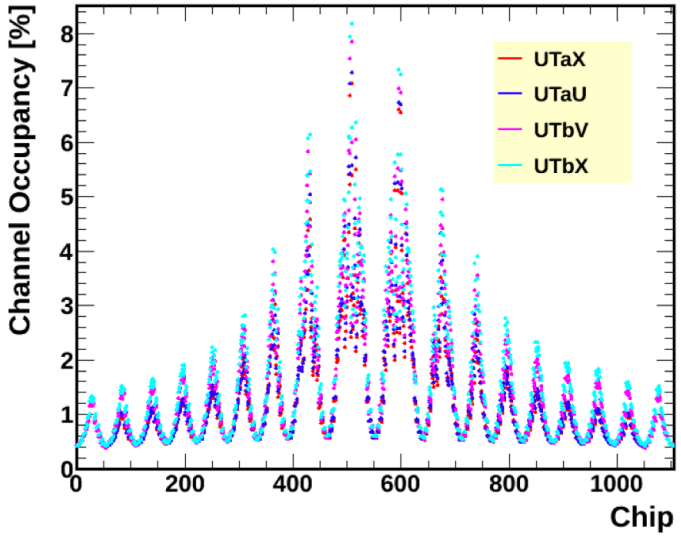


A new UT is mandatory!

- UT optimized for $2 \times 10^{33}\ \mathrm{cm^{-2}s^{-1}}$, can handle date rate of $\times 1.5$ higher
- Upgrade II luminosity $1.5 \times 10^{34}\ \mathrm{cm^{-2}s^{-1}} \rightarrow \times 7.5$ increase is too much
  - The occupancy (max ~10%) will compromise the performance

Channel occupancy [%]

0.42	0.45	0.47	0.49	0.52	0.54	0.57	0.60	0.60
0.46	0.49	0.52	0.56	0.59	0.63	0.68	0.74	0.77
0.53	0.58	0.62	0.68	0.73	0.83	0.89	1.00	1.06
0.64	0.70	0.77	0.86	0.96	1.10	1.26	1.48	1.63
0.78	0.88	0.97	1.13	1.27	1.54	1.81	2.34	2.72
0.96	1.10	1.23	1.45	1.68	2.05	2.63	2.84	3.87
1.28	1.45	1.54	1.81	2.04	2.57	3.42	4.48	3.95 / 5.13



A new UT is mandatory!

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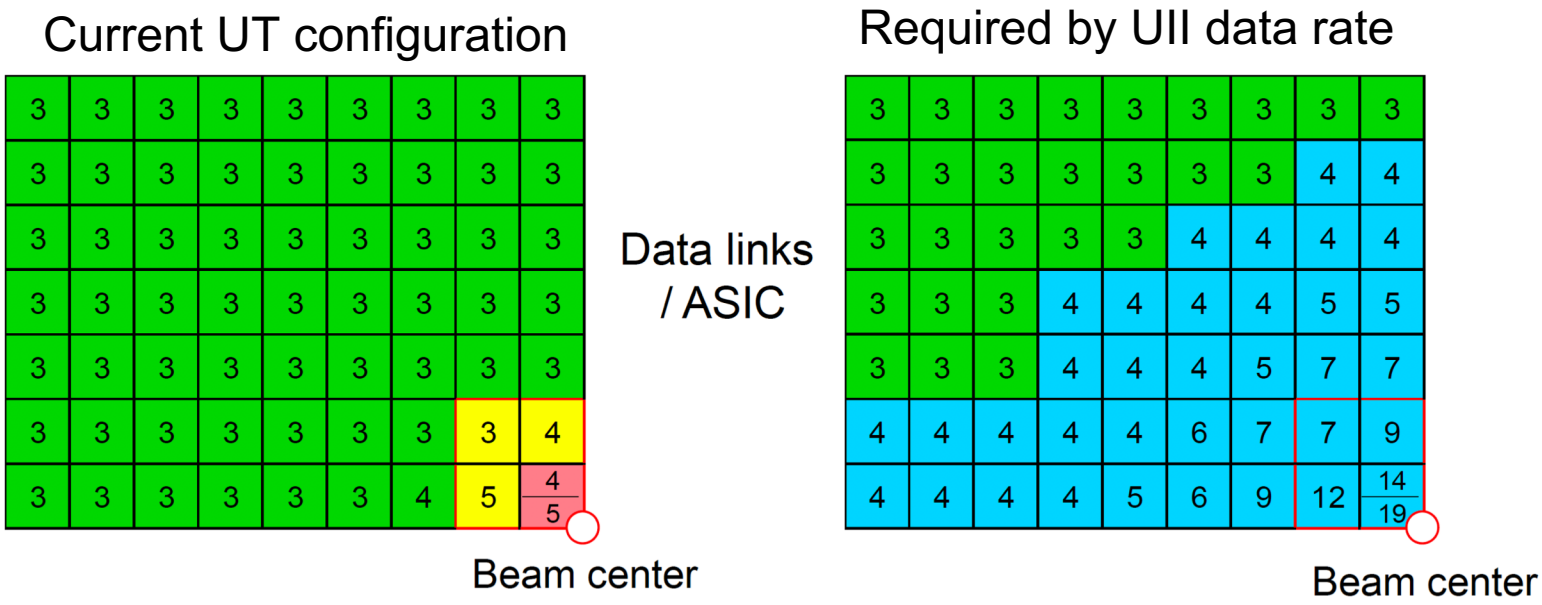
- Upgrade II luminosity $1.5 \times 10^{34}\ \mathrm{cm^{-2}s^{-1}} \rightarrow \times 7.5$ increase is too much
  - The occupancy (max ~10%) will compromise the performance
  - The data rate would be too high
  - Max dose $\sim 3 \times 10^{15}\ n_{\mathrm{eq}}/\mathrm{cm}^2$ may be too high for current sensor



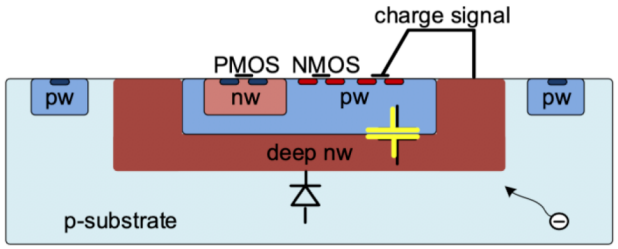
Possible solutions: CMOS MAPS

- Advantages
  - Excellent space resolution
  - Low material budget
  - High integration in monolithic technology

- Challenges
  - Readout architecture for high hit rate
  - High radiation tolerance
  - Sub-ns time resolution
  - Low power consumption

Two main options

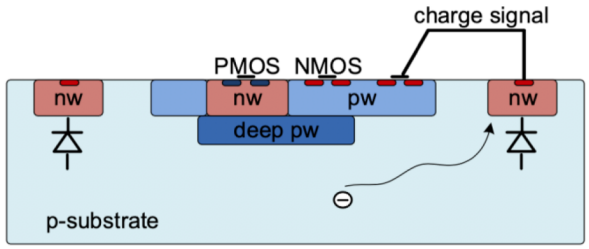
HV-CMOS



Large collection electrode

- Typical pixel size: $50 \times 150\ \mu m^2$
- Circuitry inside collection well
- High radiation hardness
- Higher noise
- Higher power consumption
- Possible crosstalk
- Presently developed under AMS-180 (MuPix, ATLASPix) and LF-150 technologies (Monopix2)

LV-CMOS

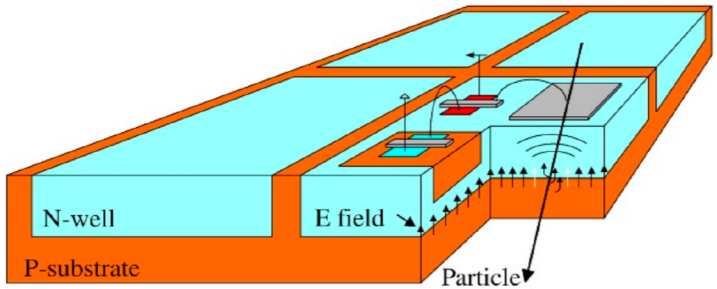


Small collection electrode

- Typical pixel size: $30 \times 30\ \mu m^2$
- Circuitry outside collection well
- Radiation hardness with process modification
- Lower noise
- Lower power consumption
- Less sensitive to crosstalk
- Presently developed under TJ-180 (Monopix2, MALTA2)

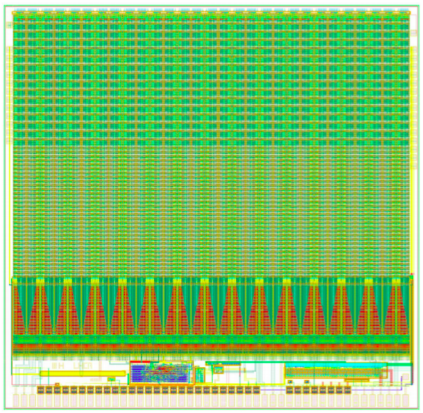
HV-CMOS for UT and Mighty Tracker

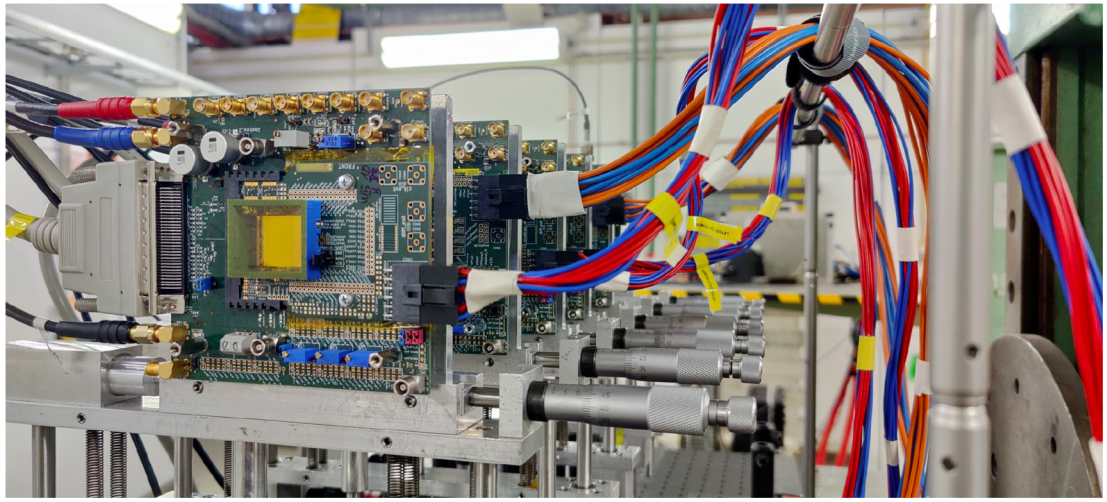
- HV-CMOS is a promising technology for both UT and MT
- Development for Mu3e and ATLAS
  - 180nm process with good intrinsic radiation hardness
  - $50 \times 150\ \mu m^2$
  - Time resolution of 5ns
  - 160 mW/cm^2 power consumption
- R&D target:
  - Time resolution better than 3-4 ns to tag the 25 ns LHC bunch
  - Material budget < 1% X_0/layer
  - Sustain $3 \times 10^{15}\ n_{eq}/cm^2$

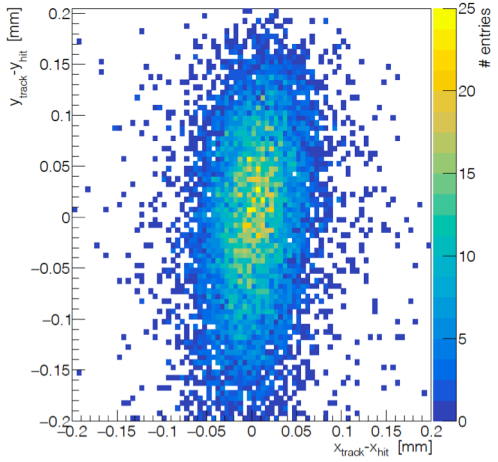


MightyPix prototype

- A first MightPix prototype produced in 2020
  - $100 \times 165\ \mu m^2$, $50 \times 165\ \mu m^2$
  - Tested at DESY beam
  - Irradiation performed to fluences between 10^{14} and $9 \times 10^{15}\ n_{eq}/cm^2$
- Second prototype to submit in later 2021



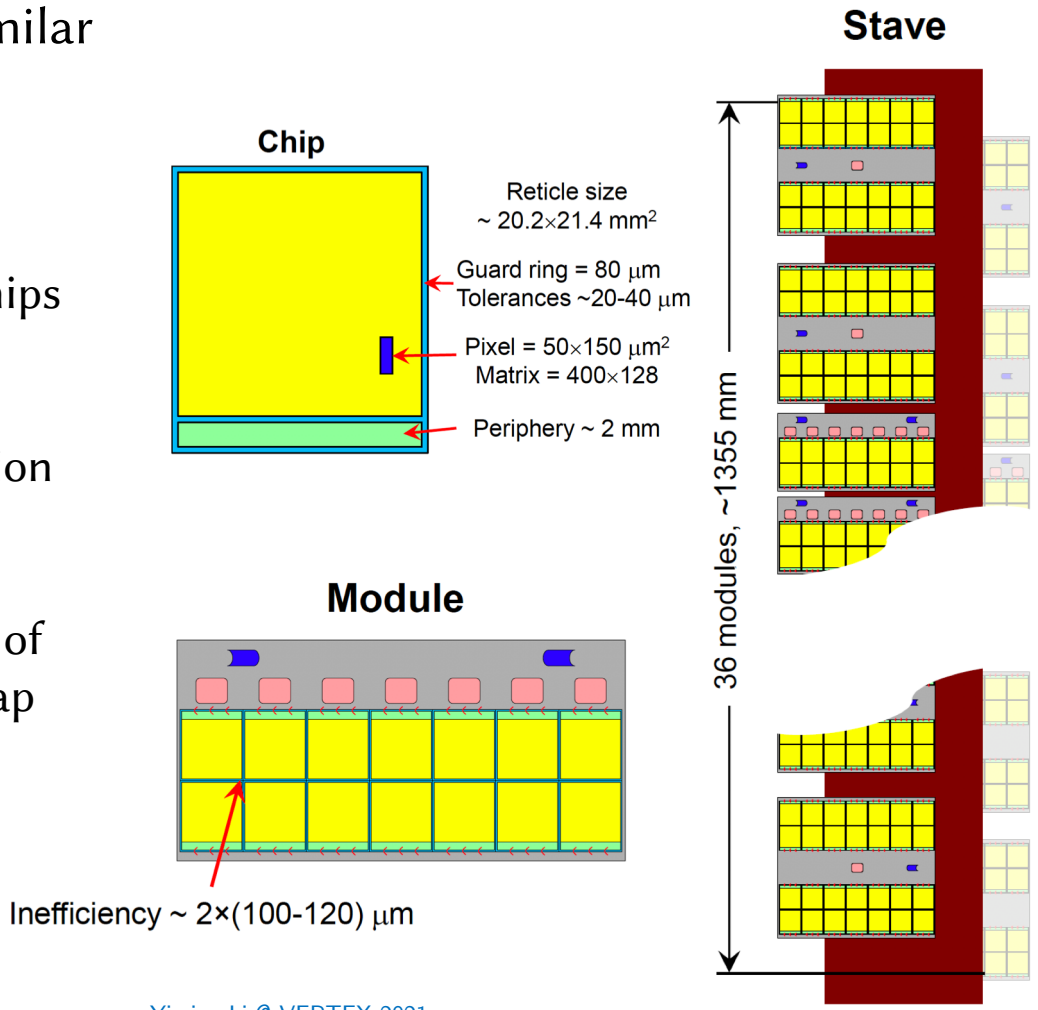




System design

- A proposed system design using MightyPix-like HV-CMOS
- LV-CMOS would be similar

- Module contains 7 × 2 chips for efficient use of lpGBT
- Dual module at outer region with reduced lgGBT links
- 36 modules on both sides of stave to allow 1mm overlap



System design

- As current UT: 4 detector planes, each with 12 staves
  - Further study needed to study impact of reducing to 3 layers
- Beam hole ± 39 mm $\times \pm 37$ mm (4×4 chips)
- Power consumption estimated 16 – 40 kW

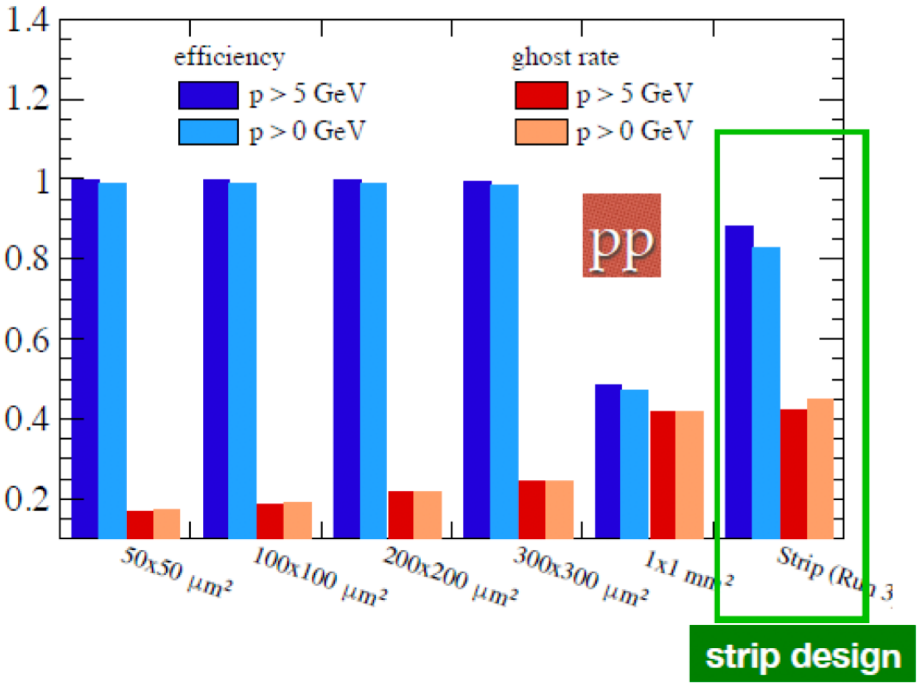
A box corresponds a 7×2-Chip module

Ring	5	4	3	2	1	All
e-links / chip	1	1	1	1-3	2-7	
Gbps / e-link	0.32	0.64	1.28	1.28	1.28	
lpGBT / module	0.5	1	2	7	14/10	
Num of modules	1312	240	80	64	32	1728
Num of data lpGBTs	656	240	160	448	384	1888
Num of ctrl lpGBTs	656	240	80	192	144	1312

Dual-module

Performance of standalone UT reconstruction

- A flexible reconstruction algorithm to allow UT optimization on:
  - Pixel size
  - # or position of layers
  - Timing info
- Preliminary results:
  - for 4 layers of pixels below $300 \times 300\ \mu m^2$
  - Efficiency > 98%
  - Ghost rate < 25%
- More optimization to perform



R&D plans

- Detailed studies will be carried out to define / optimize the UT design
  - *Impact on tracking performance of VELO-UT(-MS)*
  - *Detector acceptance optimization associated with magnet station*
  - *Optimisation on number and layout of layers (3 vs. 4)*
  - *Estimation of material budget and cooling options*
  - *Effect of a possible additional timing layer with different technology*
  - ...

Summary

- A new Upstream Tracker is being built for the imminent Run 3
- However it will not be able to operate under Upgrade II condition
- CMOS is the most promising technology for UT at UII
  - Common development on the sensor for UT and Mighty Tracker
  - Initial system design exists, a lot of R&D and studies ahead