The 30th International Workshop on Vertex Detectors

VIRTUAL (Oxford) 27-30 September 2021

Status of the TimeSPOT project

results on silicon sensors and electronics

30/9/2021

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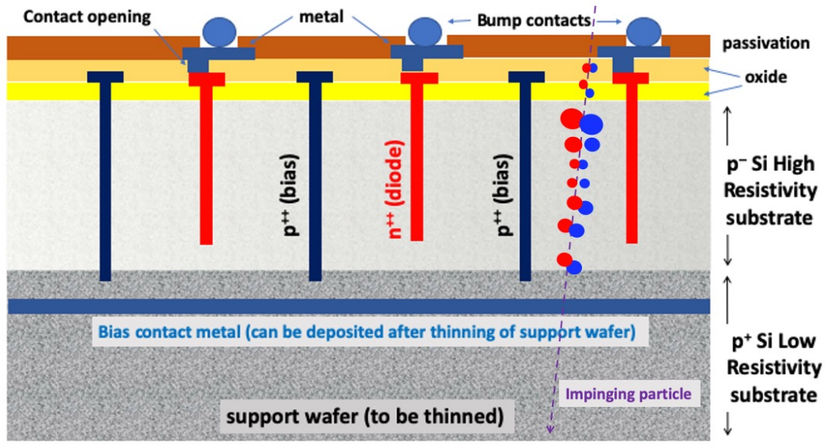
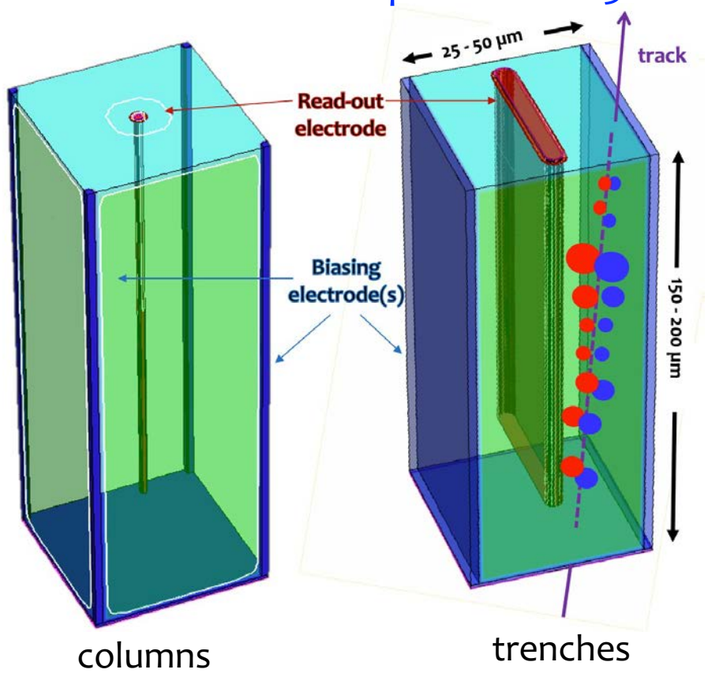
TIME and SPace real-time Operating Tracker

3D silicon sensors: a geometric approach



Deep Reactive Ion Etching

Column or trench aspect ratio ≈ 30:1



Concept

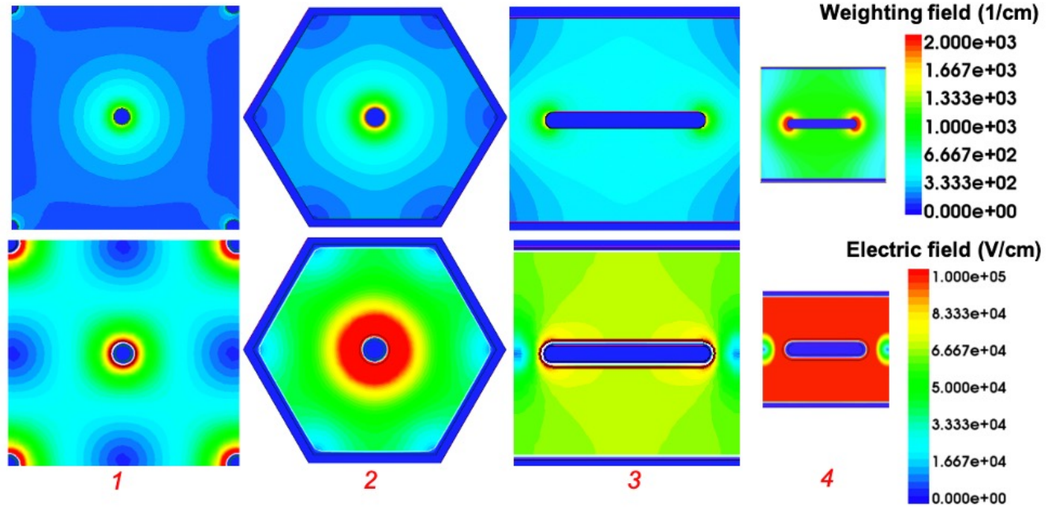
(S. Parker et al., 1997):
Perpendicular electrodes

↓

Inter-electrode distance d independent of sensor thickness z

↓

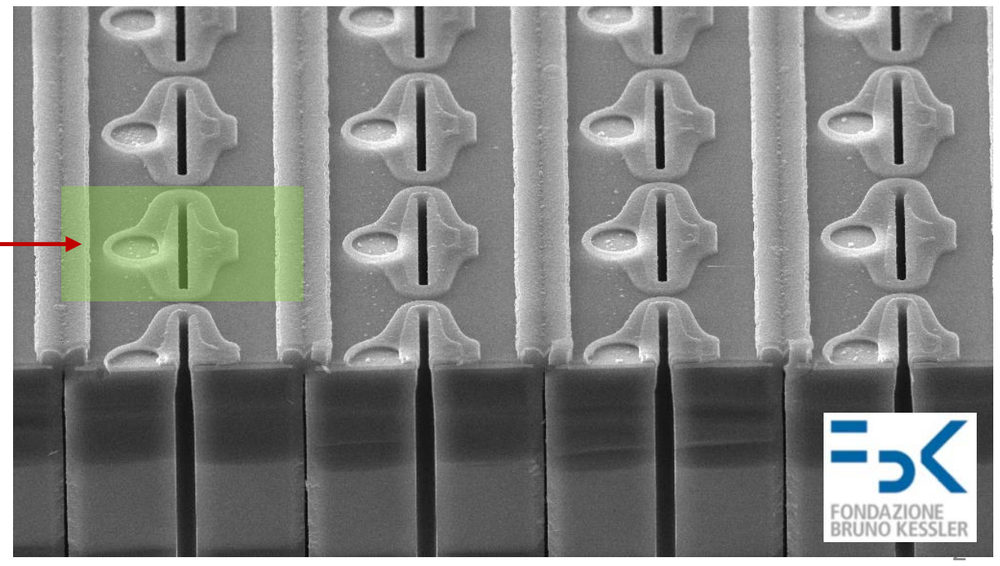
Sensitive volume and electrode shapes can be designed for maximum performance



$$i = qE_w \cdot v$$

High and uniform E field

TimeSPOT pixel
(size 55x55x150 µm³)
~2 fC MPV

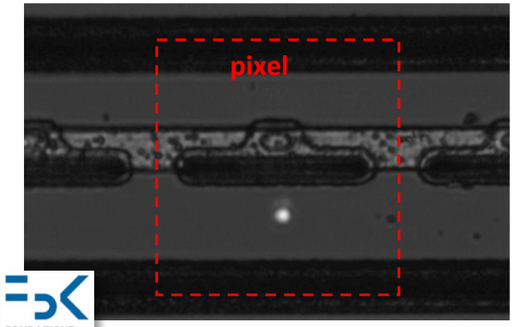


trench electrodes:
SEM image from **TimeSPOT** production batch#2 (Dec 2020)

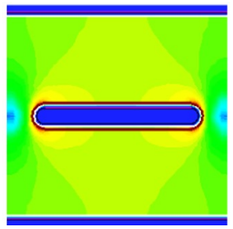
Tails, efficiency and time resolution (1)

Experimental comparison with other geometries

TimeSPOT batch#1 2019 - FBK



1



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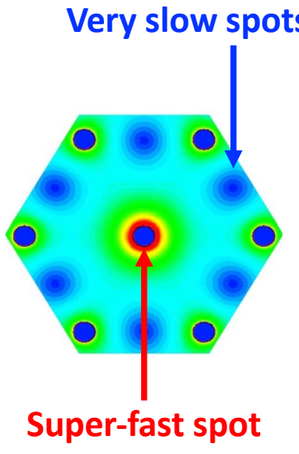

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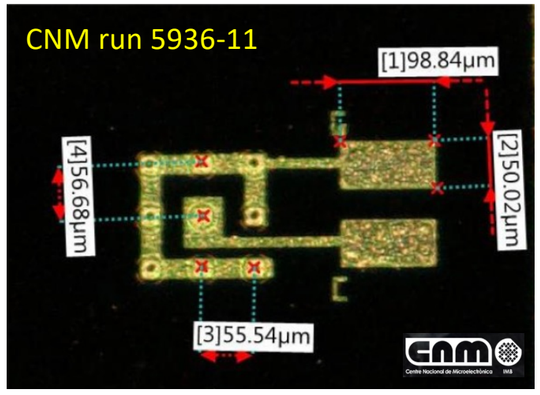
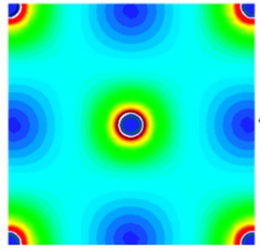
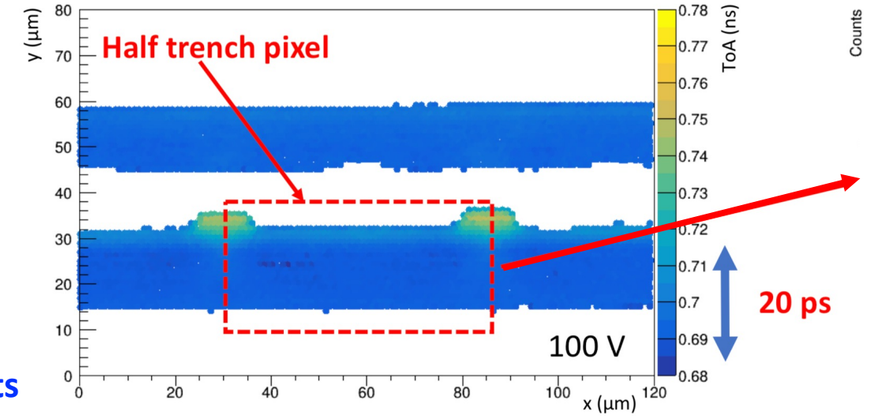
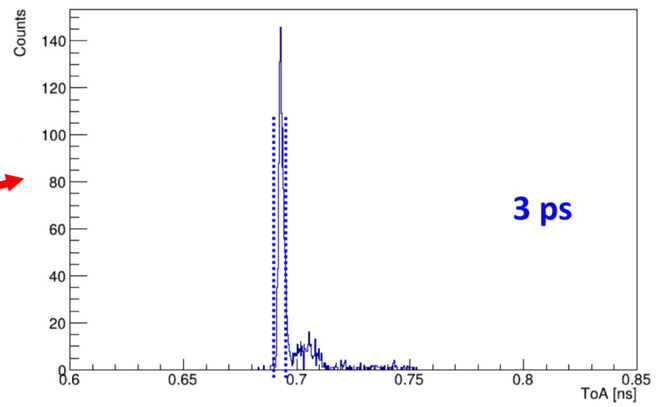
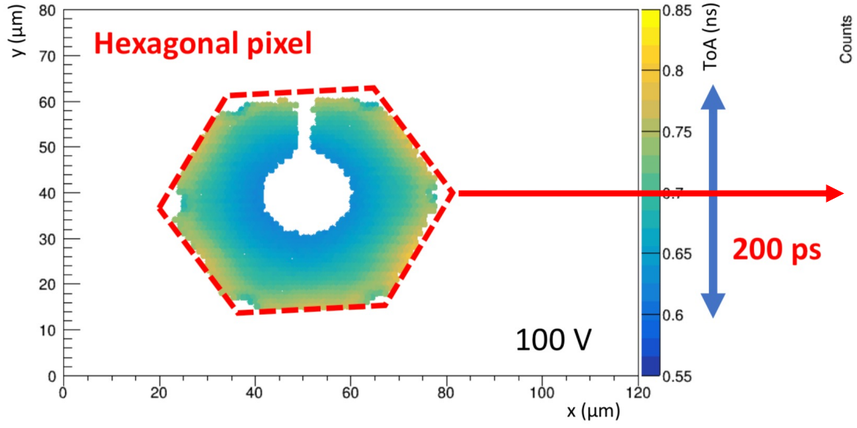


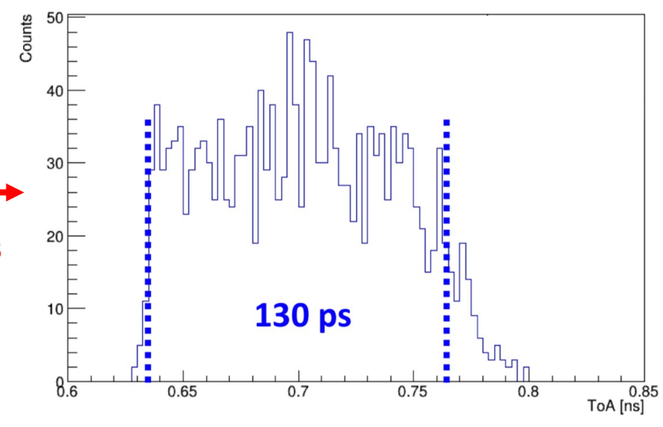


Electric field





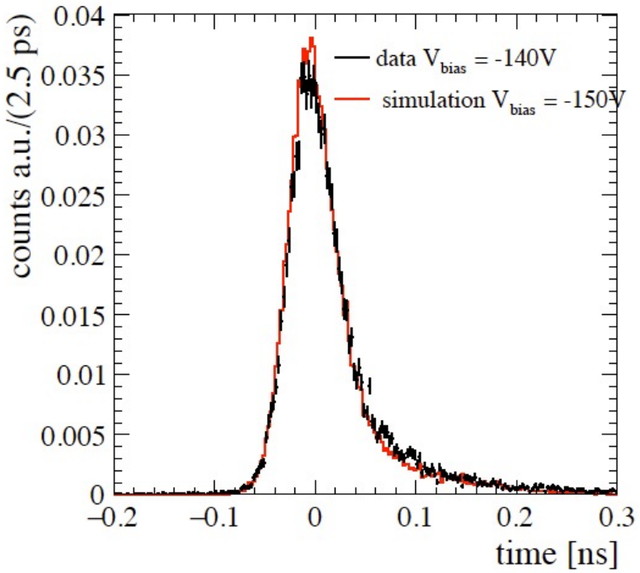




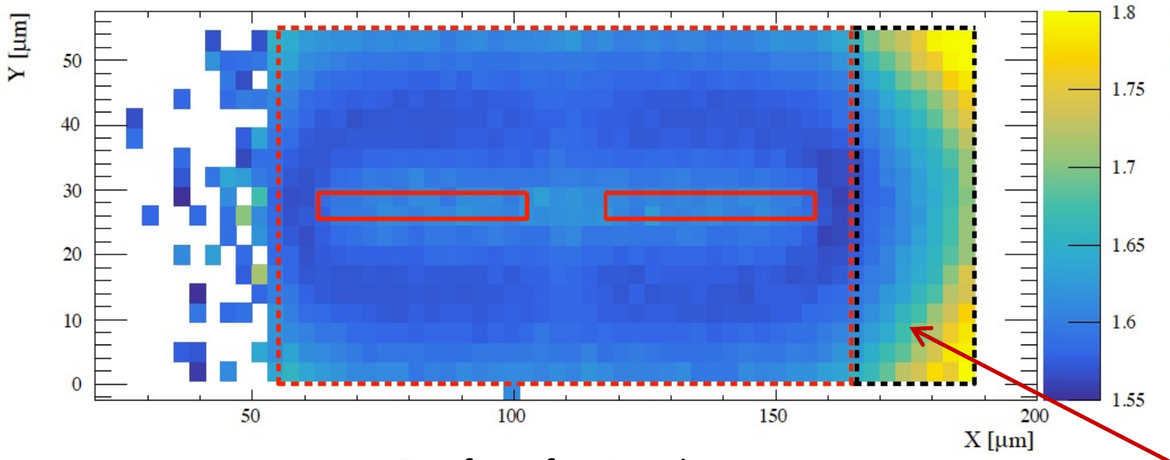
- In 3D sensors, the key for resolution is geometry (**uniformity**), not speed
- Extended slow spots give **tails** which cannot be cut-off arbitrarily
- They can give also substantial **inefficiency** in detection
- It is important to **cross-check resolution with efficiency** in order to perform a correct (un-biased) resolution measurement

Tails, efficiency and time resolution (2)

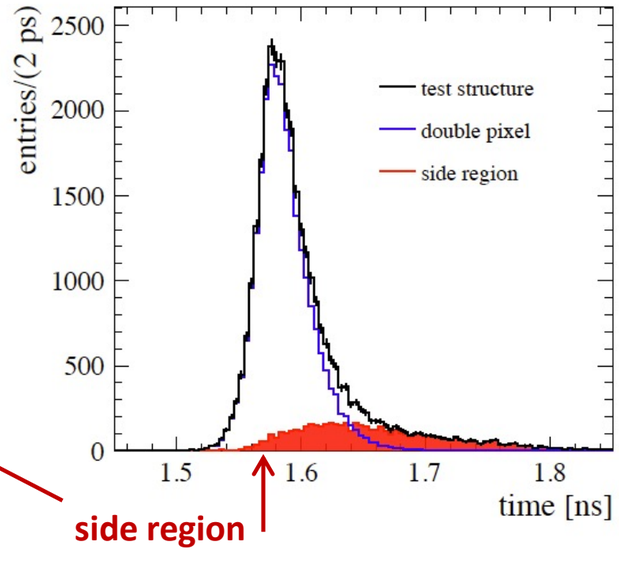
The very special case of the double pixel



PSI test beam data



ToA from front-end response

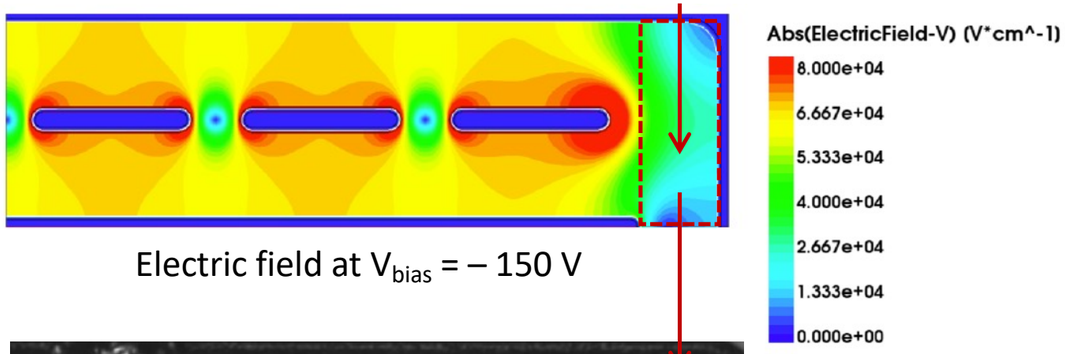


side region

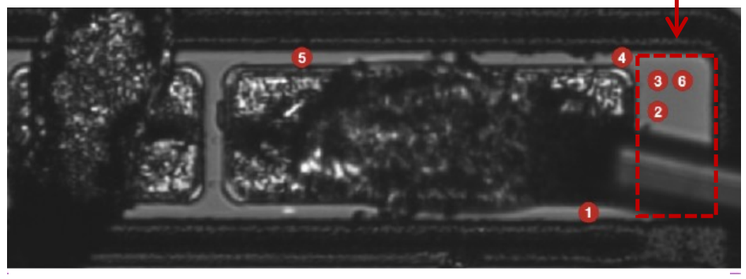
Tails have been studied with very accurate pixel modeling, from the ionization process to the front-end output.

A clear assignation of the tail contribution was done to the (out)side region of the pixel (outside the nominal pixel area in this particular case).

Details of this analysis on:
D. Brundu et al., *Accurate modelling of 3D-trench silicon sensor with enhanced timing performance and comparison with test beam measurements*
JINST 2021 16 P09028.



Electric field at V_{bias} = – 150 V



Double pixel picture

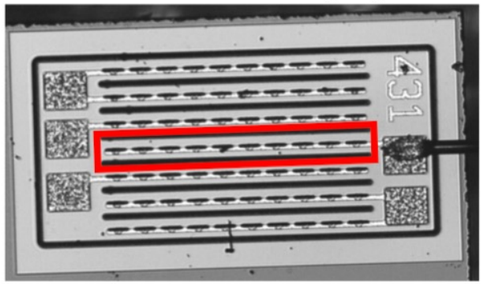
3D-trench silicon sensors

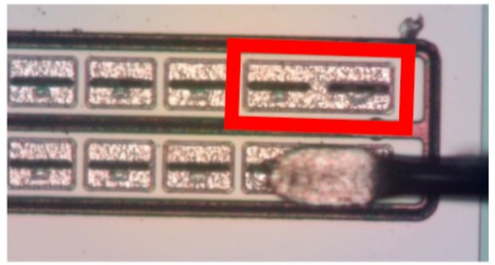
[1] L. Anderlini et al., *Intrinsic time resolution of 3D-trench silicon pixels for charged particle detection*. JINST 15, P09029, 2020.

[2] D. Brundu et al., *Accurate modelling of 3D-trench silicon sensor with enhanced timing performance and comparison with test beam measurements*. JINST 16, P09028, 2021.

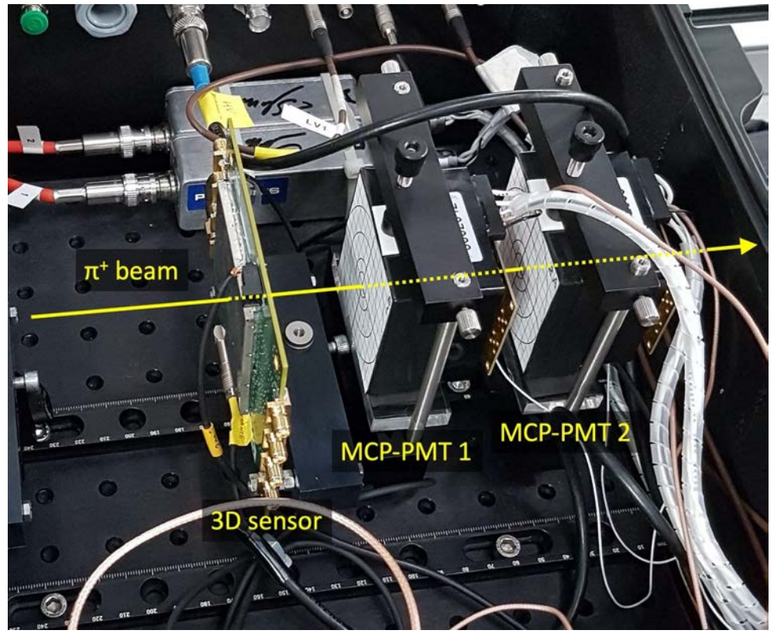
$$\sigma_t \cong \sqrt{\sigma_{un}^2 + \sigma_{ej}^2}$$

Strip pixel 55x550 µm²





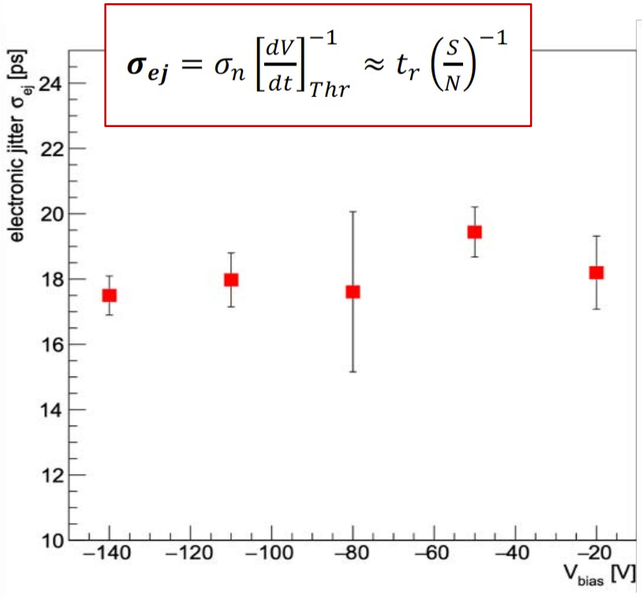
Double pixel 55x110 µm²



π⁺ @ 270 MeV/c ≈ 2 fC MPV

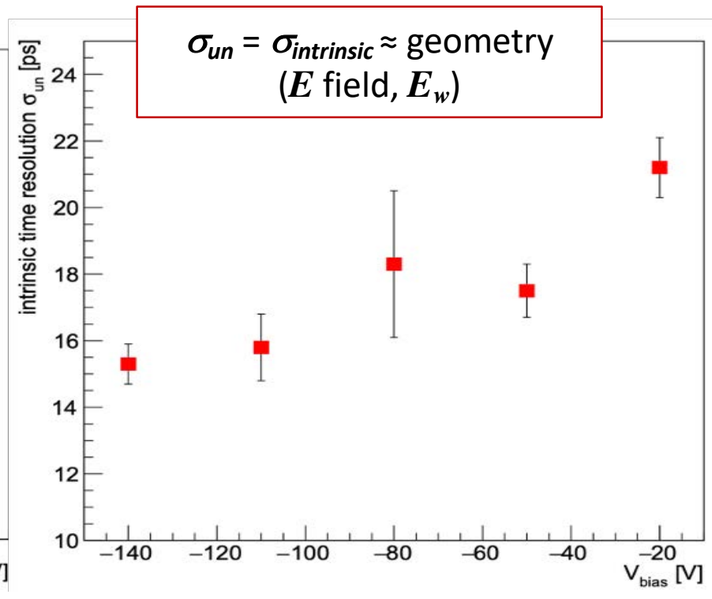
Total σ_t is obtainable as the quadrature sum of the two main contributions

$$\sigma_{ej} = \sigma_n \left[\frac{dV}{dt}\right]^{-1}_{Thr} \approx t_r \left(\frac{S}{N}\right)^{-1}$$



Jitter (electronics only, estimate [1])

$\sigma_{un} = \sigma_{intrinsic} \approx$ geometry ($\boldsymbol{E}$ field, $\boldsymbol{E}_w$)



Intrinsic (sensor only, estimate [1])

σ_t is dominated by the contribution of the front-end electronics σ_{ej}

This estimate is pessimistic especially for the intrinsic resolution as includes inextricable systematic effects (time correlations, extrinsic noise).

Very accurate simulations give *more unbalanced* indications [2]

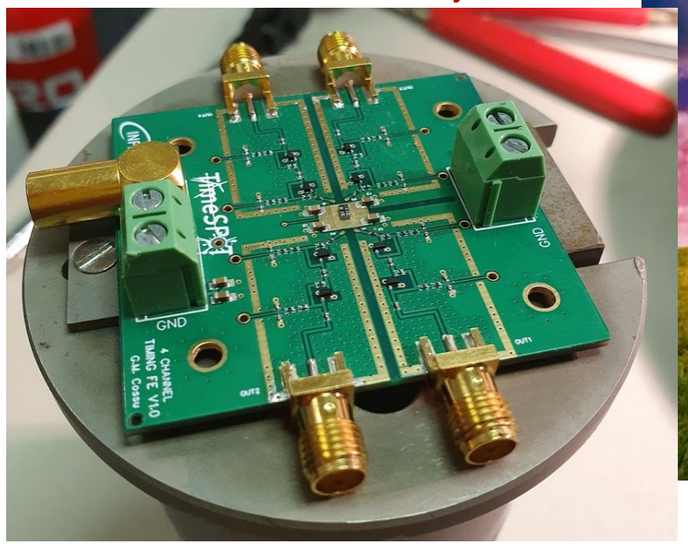
Simulation [2]			Measurement [2]	
V_{bias} [V]	$\sigma_{intrinsic}$ [ps]	σ_t [ps]	V_{bias} [V]	σ_t [ps]
−50	9.6 ± 0.1	18.9 ± 0.2	−50	20.7 ± 0.3
−100	8.0 ± 0.1	16.7 ± 0.2	−110	19.8 ± 0.2
−150	7.0 ± 0.1	16.3 ± 0.2	−140	19.0 ± 0.2

room temperature

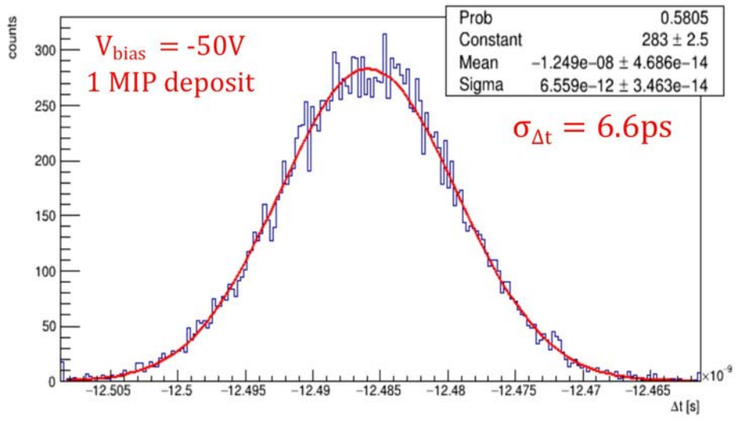
3D-trench pixel readout and custom electronics (ASIC)

Max obtainable performance (TimeSPOT sensor) vs ASIC specifications (e.g., LHCb)

3D-sensor specs: σ_{ej} < 15 ps



WB Si-Ge input stages t_r ≈ 100 ps
Measured σ_{ej} ~ 6.6 ps



LHCb-U2 specs

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Lifetime fluence [1×10^{16} 1 MeV n_{eq}/cm^2]	> 6	> 1
TID lifetime [MGy]	> 28	> 5
Sensor Timestamp per hit [ps]	≤ 35	≤ 35
ASIC Timestamp per hit [ps]	≤ 35	≤ 35
Hit Efficiency [%]	≥ 99	≥ 99
Power per pixel [µW]	≤ 23	≤ 14
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

LHCbU2 specs from physics needs. U2 FTDR preliminary (2020).

- **50 ps per hit on the full chain (*sensor* + AFE + TDC)**
- **High rate (~ 1 TDC per pixel)**
- **Low consumption < 1.5 W/cm^2 (power dissipation issues)**

The TimeSPOT ASIC designer's challenge:

What is the best time resolution we manage to reach (15 ps < σ_{ej} < 50 ps) integrating 1 TDC per pixel (55x55 µm^2) and possibly keeping the consumption in the range of 20-30 µW/pixel ?

Timespot1 ASIC: layout and architecture

Reduced size
(1024 pixels, 6 mm²),
Complete set of functionalities

Digital row: 16x2 (mirrored) TDC + Controls, Conf. registers, I²C I/F)

Analog row (16x2 mirrored AFE)

Block: 512 pixels (16 double rows of 32 pixels)

Matrix: 1024 pixels (2 mirrored blocks + data routing column in between. Can host TSV)

2x Analog (service) columns. Each:

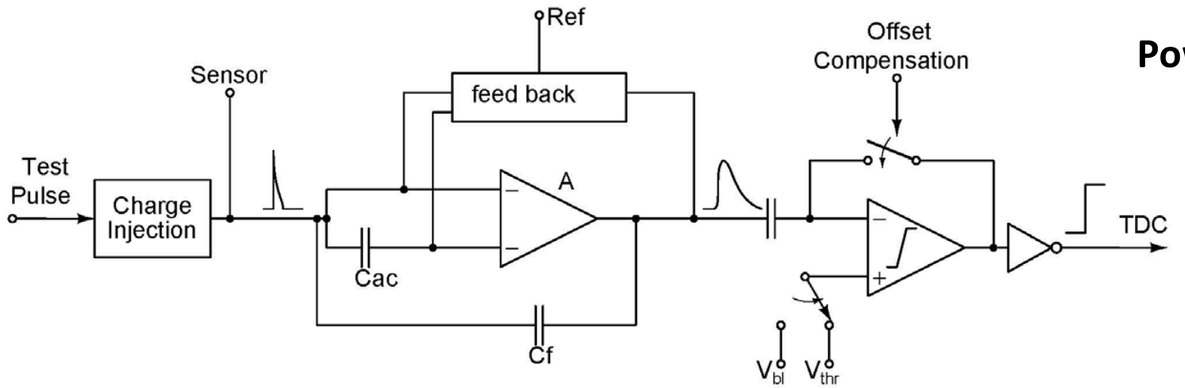
- 1 Band-Gap
- 5 DAC sigma-delta (producing analog levels used by pixels)
- Programmable bias cell (for power consumption)
- bias replicas with source followers.

LVDS driver 8 x 1.28 Gbps
Data stream is highly pad limited

The pixel matrix has no dead area and is 4-side buttable (when using TSV): reduced pixel pitch and RDL to sensor

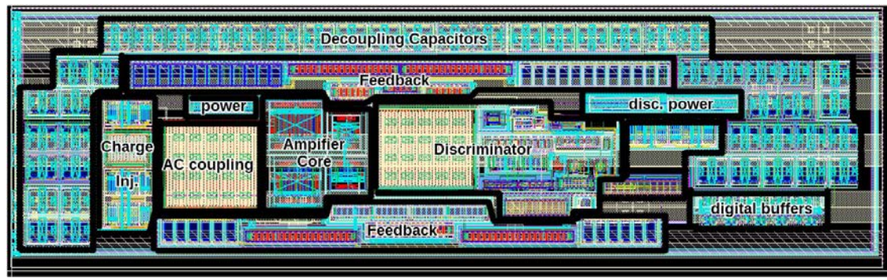
Pixel: Analog Front End and TDC

Inverter core amplifier with double Krummenacher feedback
Leading edge discriminator with discrete-time Offset Compensation (OC)



Power ≈ 15-30 µW (regulable)

50x15 µm²

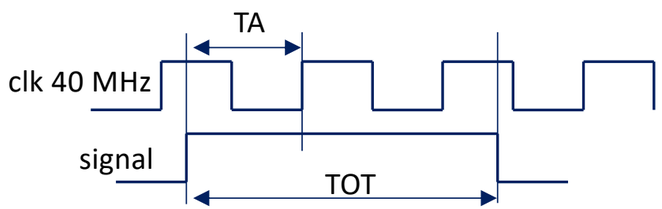


High resolution – "low" consumption TDC based on DCO and Vernier architecture

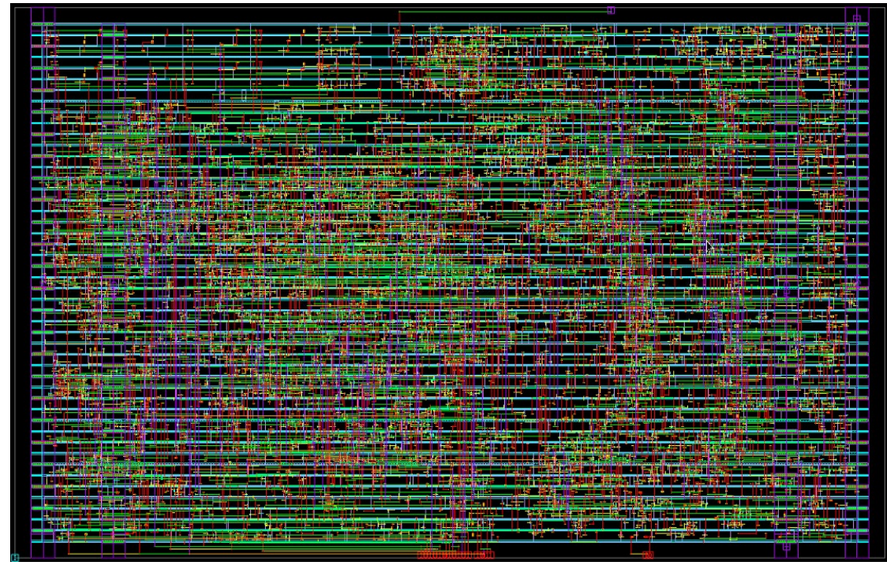
All digital, fully synthesizable architecture (standard cells)

Maximum input signal TDC rate = 3 MHz
24 bits output word (ToA + ToT) serial @160 MHz

Power depends on input rate ≈ 20 µW (stand-by) – 175 µW (3 MHz)

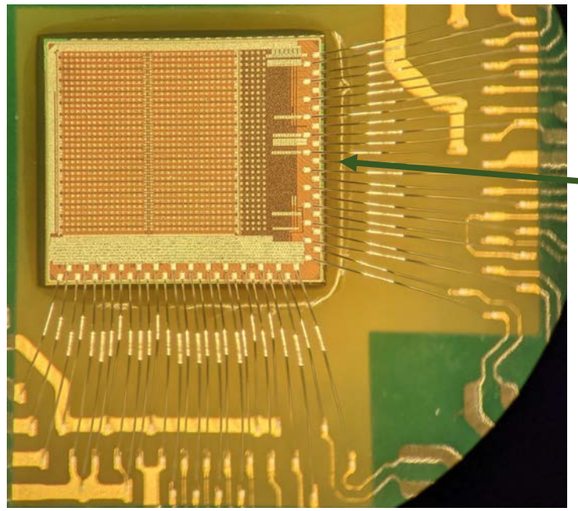


The TDC gives the phase of the signal wrt the master 40MHz clock
The TDC and the counter use the same DCO-generated Clk (~1 GHz)
Clock is active during conversion only



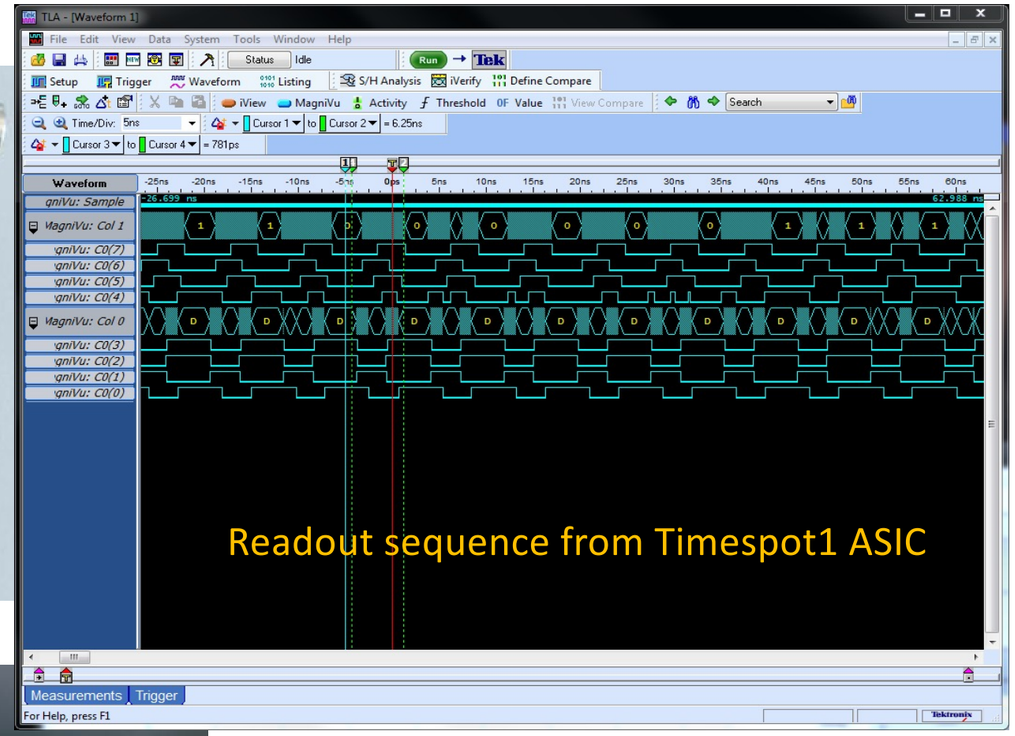
50x31.5 µm²

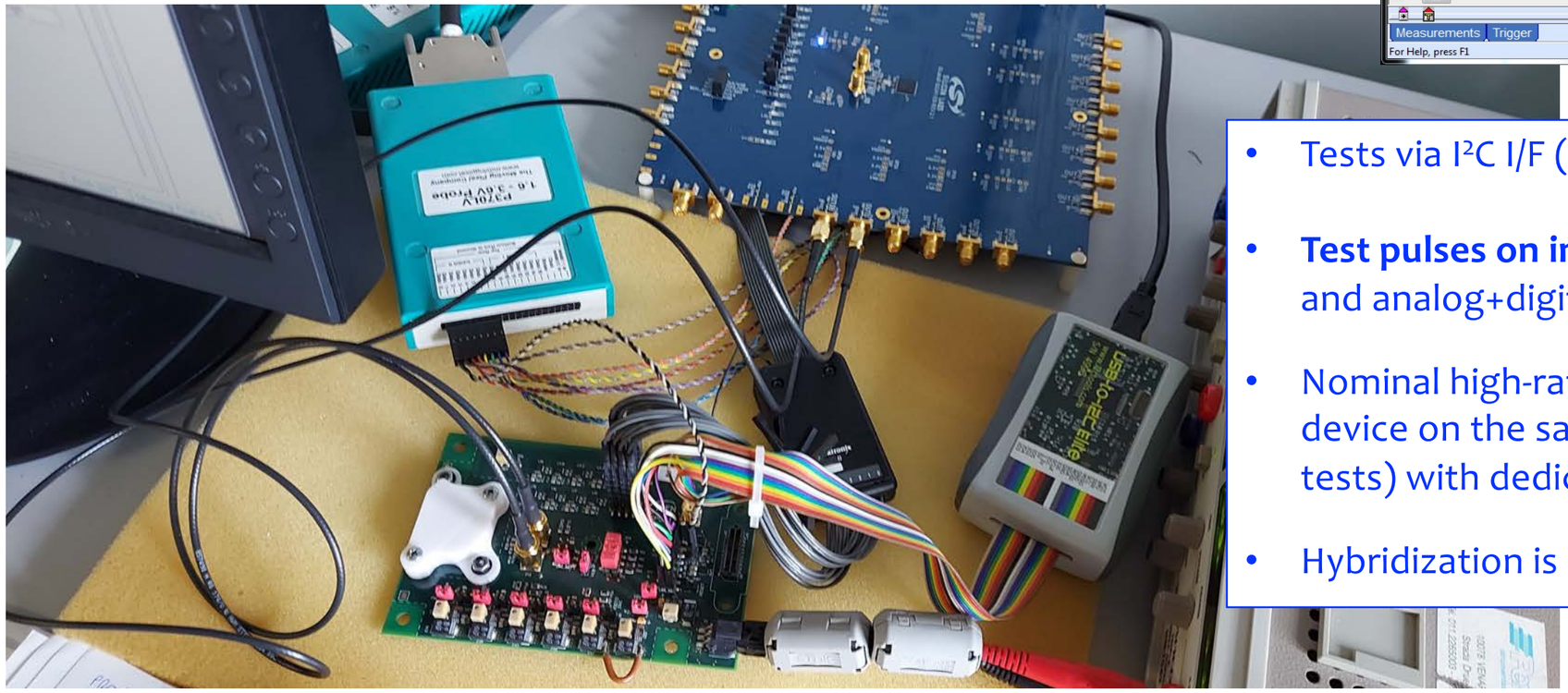
Stand-alone tests (no sensor)



Bonded Timespot1 ASIC

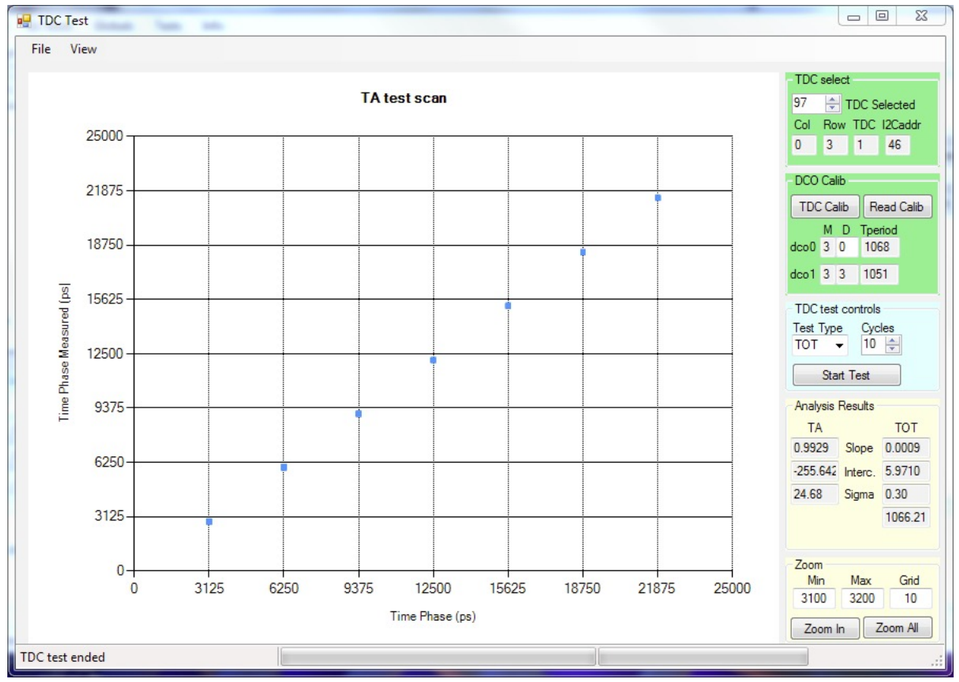
TS1-PCB 120x80 mm²



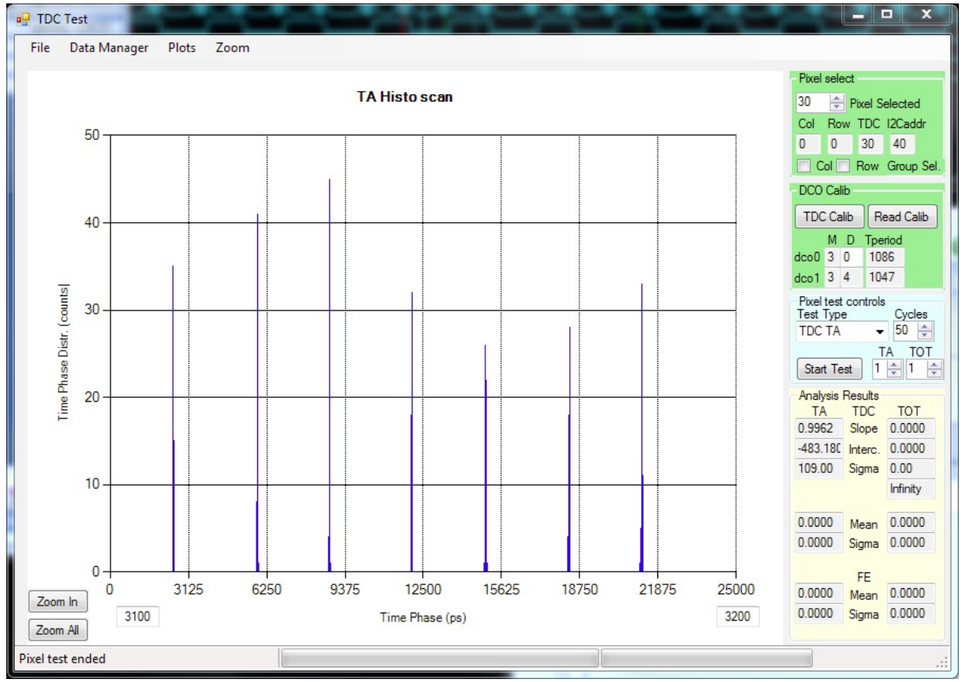


- Tests via I²C I/F (slow: max pulse rate 10 kHz) and TLA
- **Test pulses on individual channels:** digital only (TDC) and analog+digital (AFE+TDC)
- Nominal high-rate tests will be performed on hybridized device on the same PCB (laser pulses and particle beam tests) with dedicated DAQ
- Hybridization is on the way @ IZM

TDC operation and tests



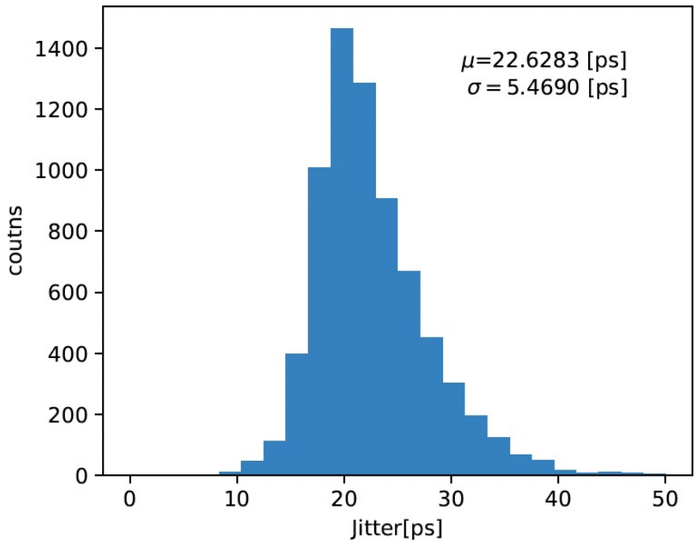
TA linearity on 7 phase positions



TA resolution on 7 phase positions

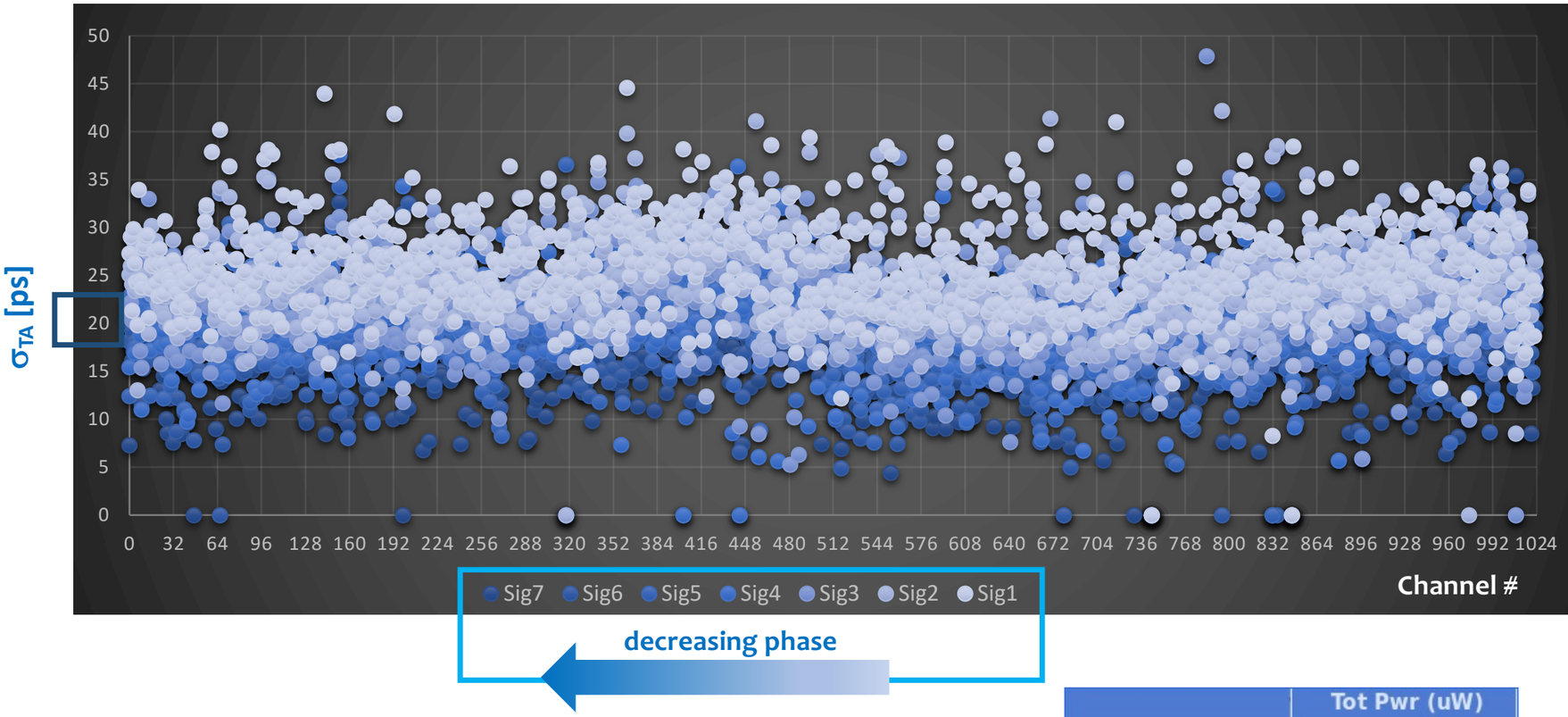
- **DCO calibration**
- auto-tuning of the frequency difference Δf for Vernier mechanism (performed after each reset). It is possible to set 4 different Δf, fixing what we define the ”Venier resolution”
- **TA (Time of Arrival)**
  phase difference between pulse rising edge and the 40 MHz reference clock
  7 possible phase positions
- **TOT (Time over Threshold)**
  32 programmable digital pulse widths. The DCO-set frequency is used as clock for the ToT counters

TDC test results: resolution on TA



Distribution of the TA standard deviation across 1024 channels and 7 phases. Each point is computed from **100** repeated measurements.

All phases, Res = 3, statistics of 100 samples per point



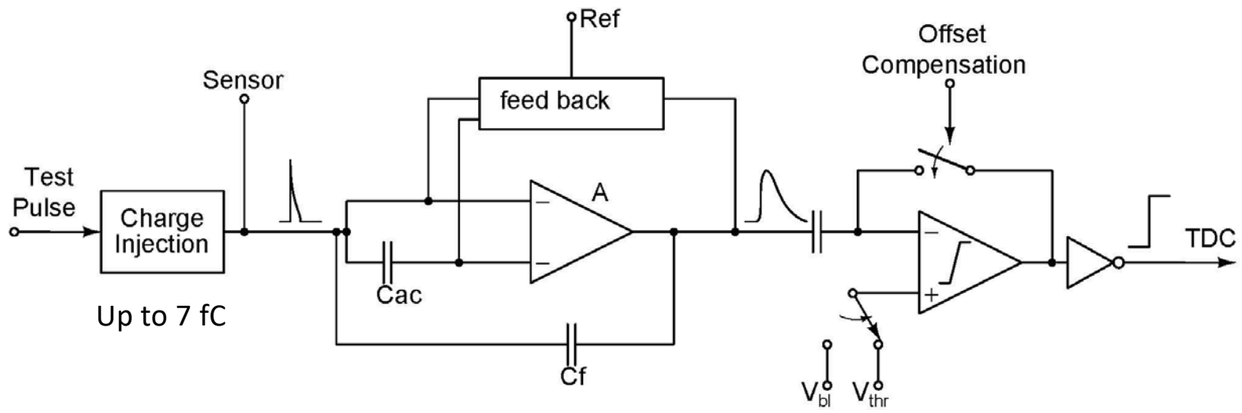
- Average σ_{TA} much better than 50 ps: $\sigma_{TA} = (22.6 \pm 5.5)$ ps
- "only" 14 dead channels out of 1024.
- The TDC design had 4 programmable resolution (Vernier gauges), but the best resolution is obtained with the coarsest one (Res = 3)

  → *The real limit to resolution appear to be the master clock jitter and/or power distribution*
- Signal phase dependence (lower phases behave better) → drift in Vernier operation
- Slight but evident dependence on geographical position of the channel (IR drop?)

	Tot Pwr (uW)
IDLE	20.7
Calibration	552
DAQ 3MHz	175
DAQ 1MHz	69.3
DAQ 500kHz	45.5
DAQ 100kHz	25.7

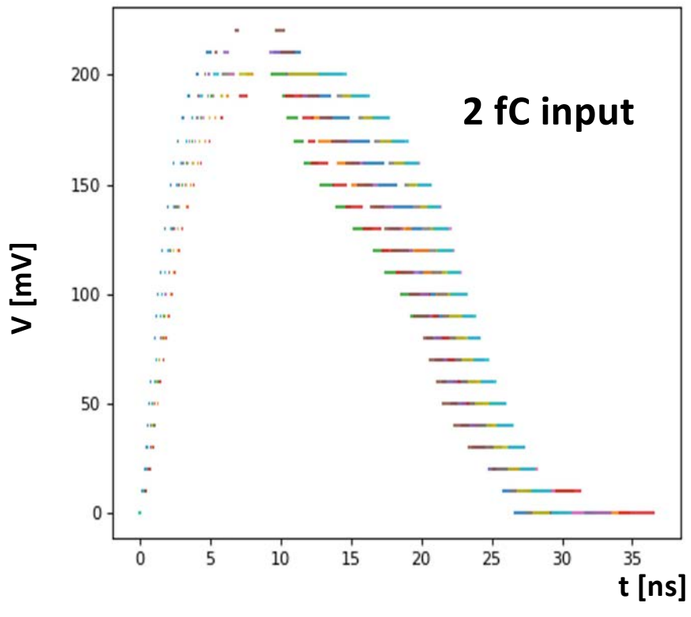
Simulated TDC power consumption (to be tested at high input rate)

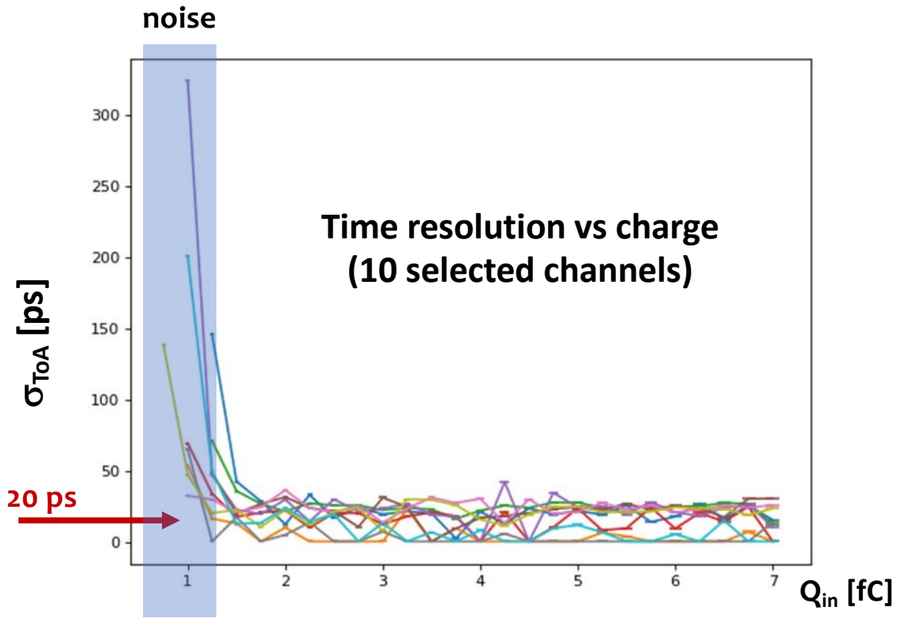
AFE tests



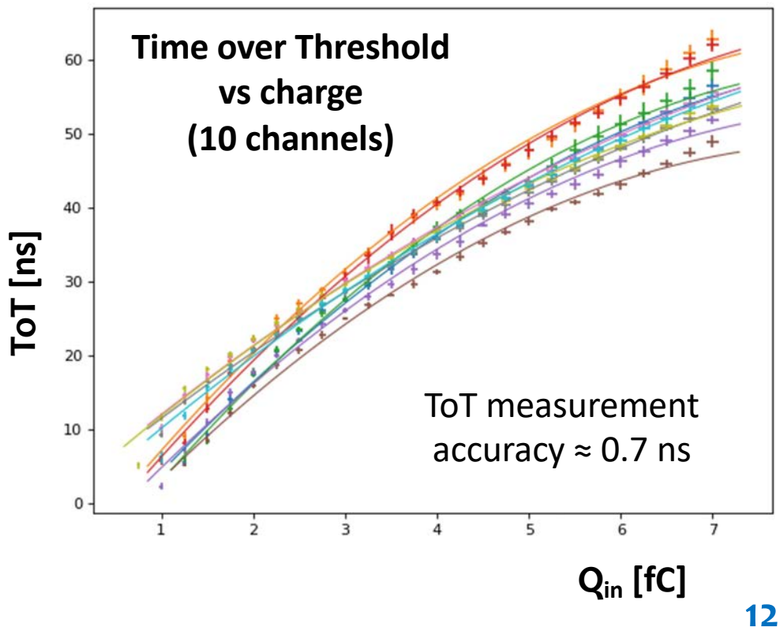
- Pulsed using a **per-pixel charge injection** capacitance
- input charge from 0 to 7 fC.
- The signal is injected with the next reference clock rising-edge → time-0 measurement.
- Discriminator Baseline and Threshold set via 2 independent voltages
- Output is from **Discriminator/TDC only** → CSA signal must be **reconstructed** moving the thresholds

Signal reconstruction by thr scan (10 channels)



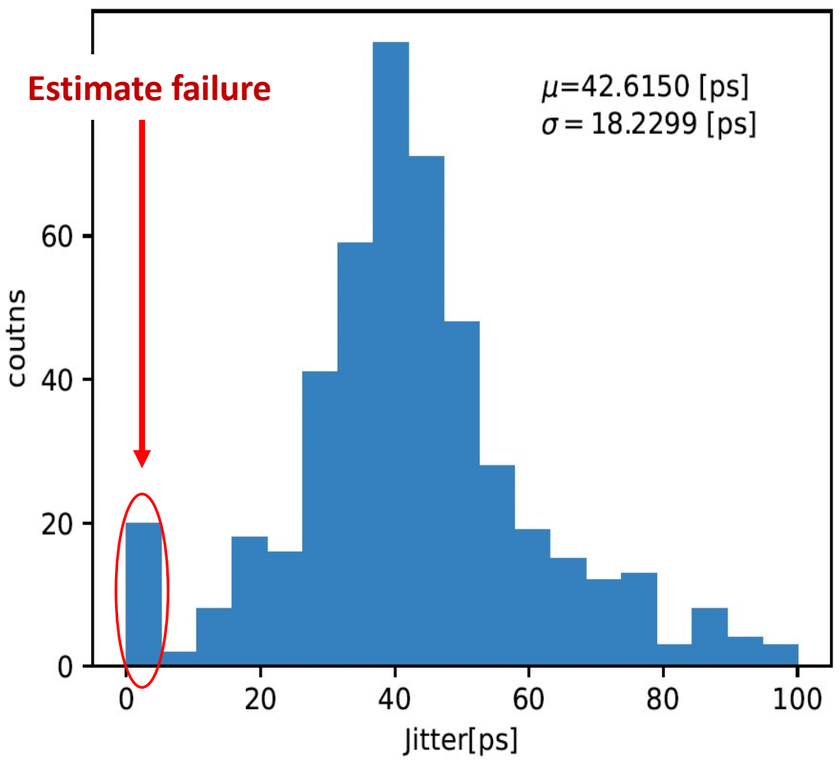


Time resolution "sits down" @ ≈ 20 ps



AFE tests: time resolution σ_{TA} (σ_{ej})

Preliminary



Distribution of TA standard deviation across 512 channels. **Input charge 2 fC (expected MIP).**
Each point computed from 100 repeated measurements.
TDC contribution has been removed.
Power consumption = 15 µW

- AFE intrinsic time resolution CANNOT be measured directly
- It must be **estimated** by subtracting out the TDC contribution:

$$\sigma_{ej,\,estimate} = \begin{cases} \sqrt{\sigma_{FE}^2 - \sigma_{TDC}^2} & \text{if } \sigma_{FE} \geq \sigma_{TDC} \\ 0 & \text{if } \sigma_{FE} < \sigma_{TDC} \end{cases}$$

≈ 40 ps ??

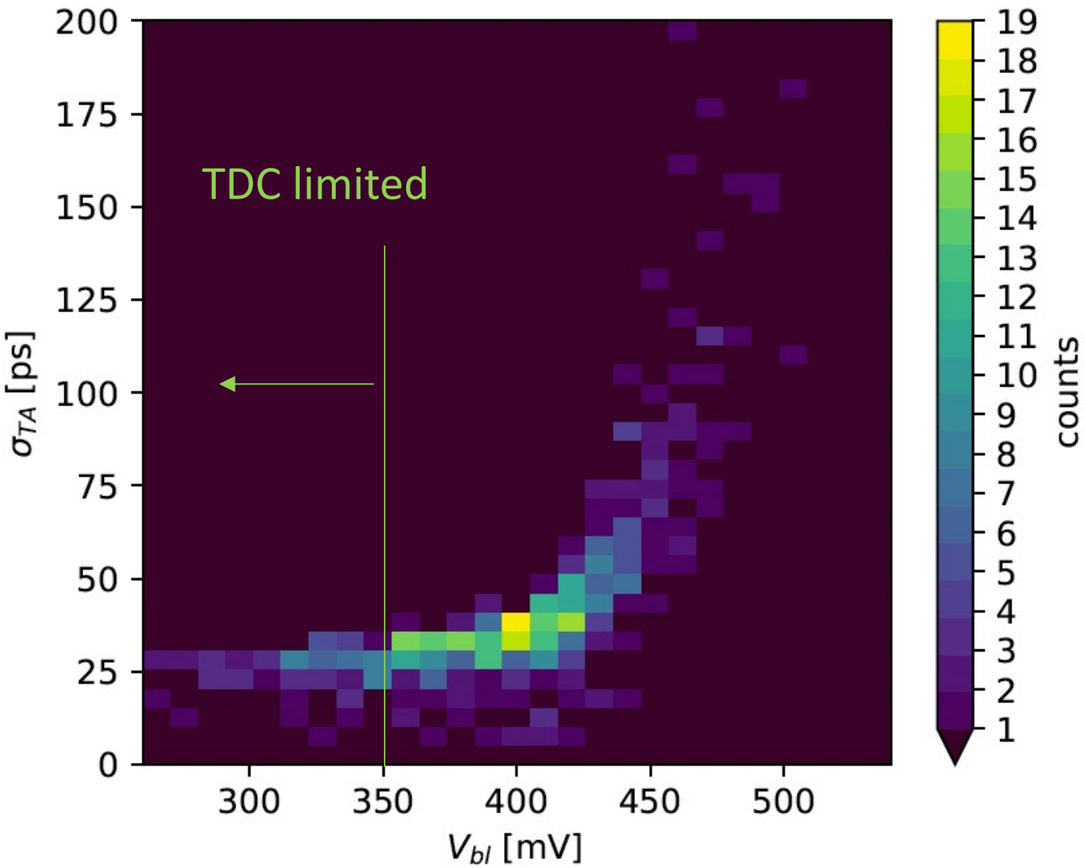
- This produces a strong bias in the estimate
- **However, the AFE appears to have a worst σ_{TA} than the TDC**

- The performance appears much worse than expected from simulations (< 20 ps): *Is there a limit in the circuit or anything else?*

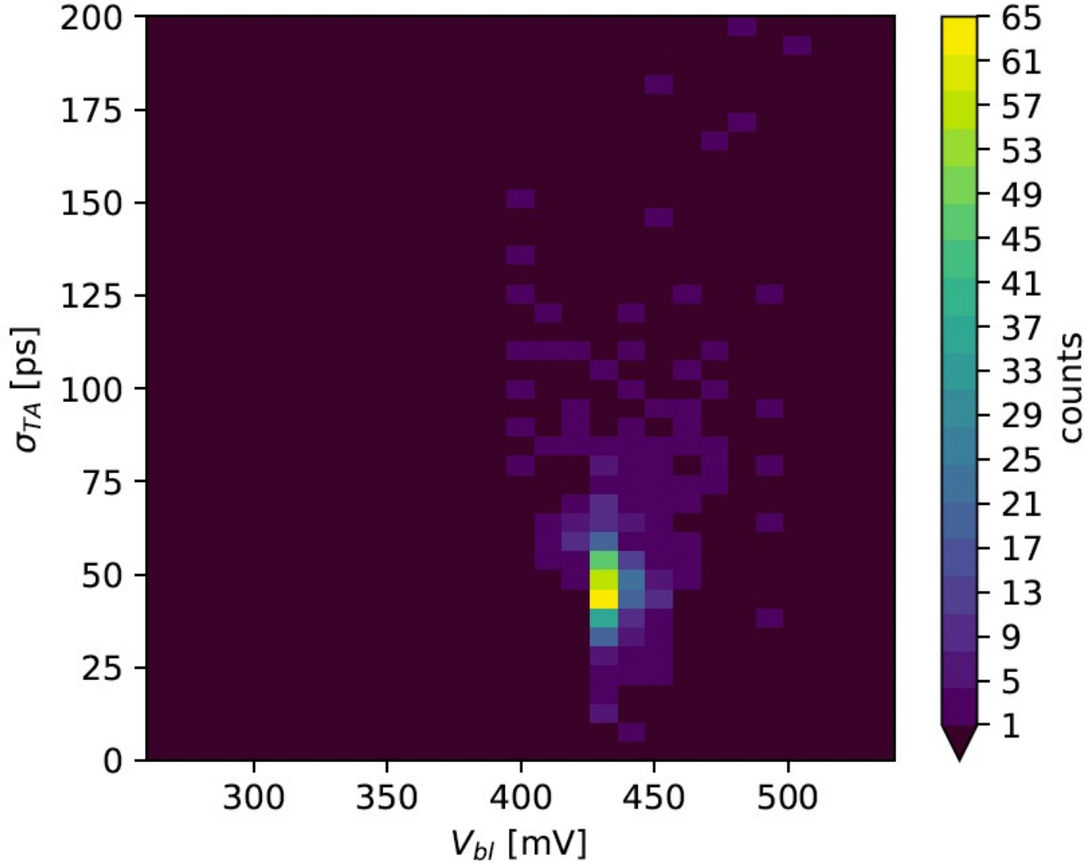
→ **Issue with the Offset Compensation mechanism:**
OC fails when $V_{baseline}$ is set to low values !

OC problem, $V_{baseline}$ and σ_{TA}

The amplifier is working properly, OC is not…



$V_{baseline}$ set at 100 mV:
OC struggles to follow the programmed value without success. At $V_{baseline}$ < 350 V, σ_{TA} sits down at the σ_{TDC} value! → **$\sigma_{TA,\ AFE} \leq \sigma_{TDC} \approx 23$ ps**



$V_{baseline}$ set at 450 mV:
OC works (baseline uniformity), average **$\sigma_{TA,\ AFE} \approx 40$ ps**

Not much can be said yet on the intrinsic performance of the AFE, being limited by OC (worst cases) and TDC (best cases)

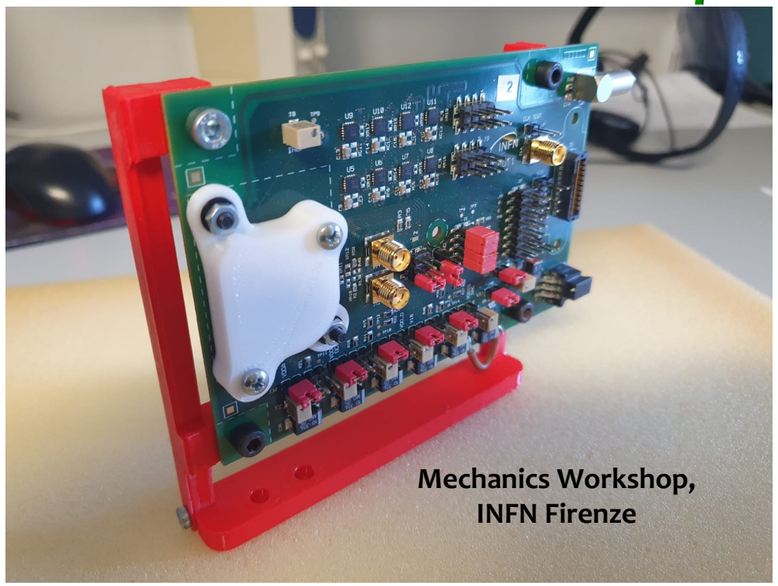
A (preliminary) summary on the 28-nm ASIC

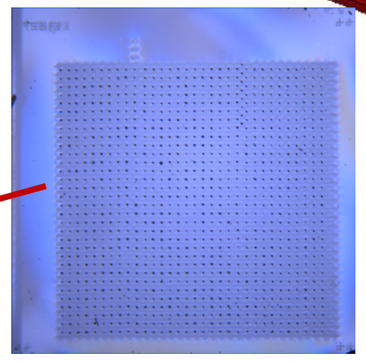
What we learned up to now

- A pixel readout performance **< 30 ps** time resolution (F/E + TDC) is there. It will be **reached** once minor modifications are performed:
  - OC bug correction should be already sufficient,
  - more accurate clock distribution can even improve the performance towards 20 ps
  - Something can still be gained from technology (HPC → HPC+, HVT-LVT accurate choice)
- We think that power budget ("dissipation" budget ~ 1.5 W/cm^2) must be **increased** for higher timing performance. 20 ps or even less are within reach with a moderate increase (~30%)
  - System-level R&D in **cooling** techniques is vital for timing
- Effective timing pixel performance **depends on** ASIC size and "collective" effects
- **Uniformity** across the whole area is a major difficulty in CMOS 28-nm (important IR drops), critical clock tree
- **VERIFICATION** at the full ASIC level is the mainly critical step
- **Full data BW is critical**: >100 Gbps needs innovative solutions in data seralizers and links

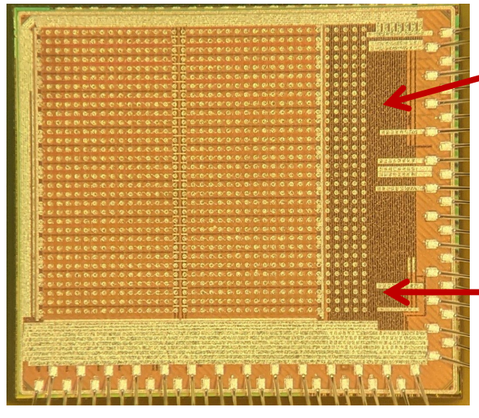
Outlook: Tests under preparation and next steps

The *Timespotter*® demonstrator (end 2021– begin 2022)

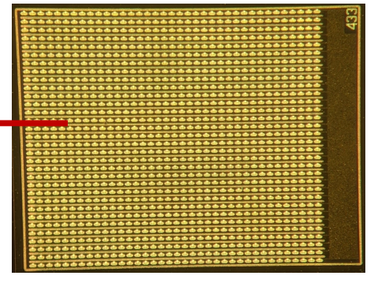




Diamond (Firenze)



Hybridization
(IZM)

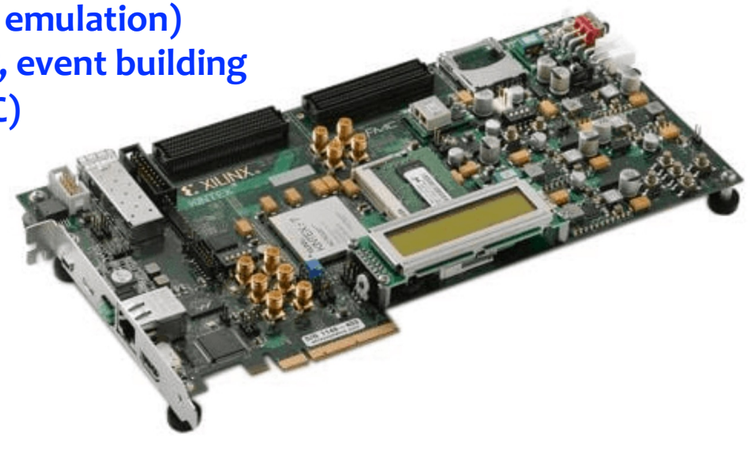


Silicon (FBK)

Readout with

KC705: 1.25Gbps – 58 Dpairs

- F/E Control (and emulation)
- Data-formatting, event building
- Slow control (I²C)



A new version of the ASIC (≈ similar size o slightly larger) has been funded and will be designed starting from next year 2022

The 30th International Workshop on Vertex Detectors

VIRTUAL (Oxford) 27-30 September 2021

THANK YOU everyone!

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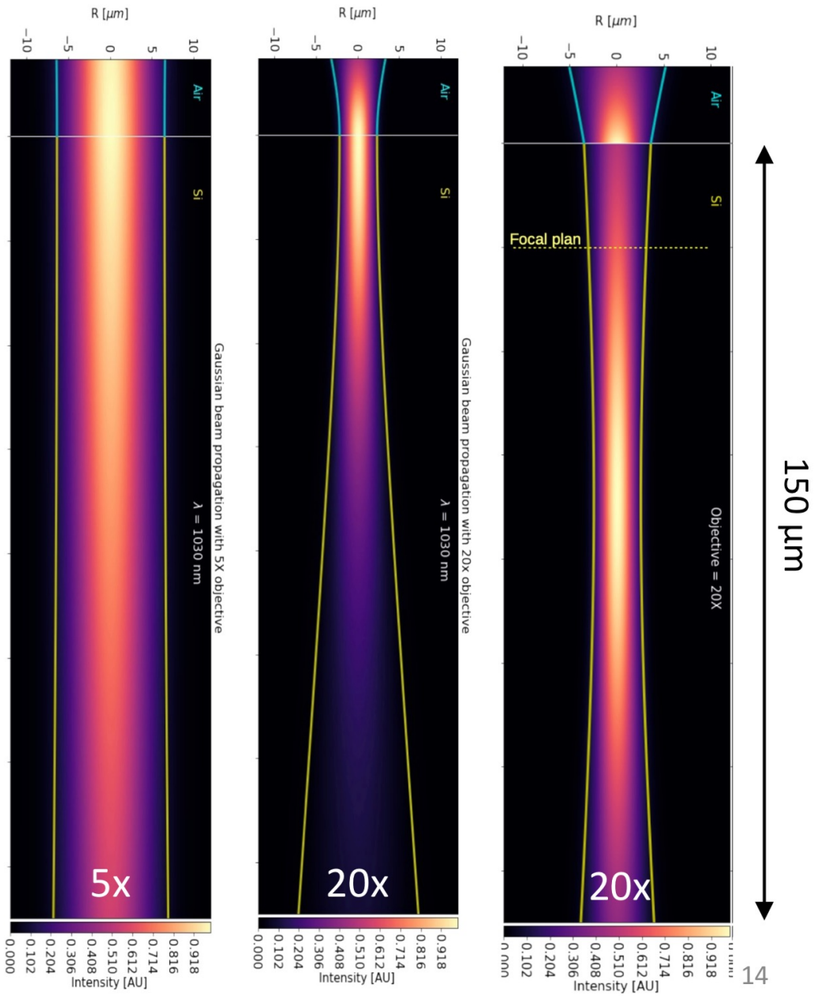
Time resolution: laser-emulated MIP studies



By choosing the waist shape (changing optics) and properly calibrating the laser intensity (using a precision CSA) a MIP-like deposit is generated

Pulsed laser:

- IR Laser (1030 nm), FWHM < 200 fs
- Optical fiber from laser to microscope.
- **Focused spot** of ~ **5** µm
- Observation **camera**
- **XY closed loop stages**
- **Optical laser time reference: accuracy <1ps** using TimeSPOT sensors, custom Si-Ge F/E and 10 MIP-equivalent pulse