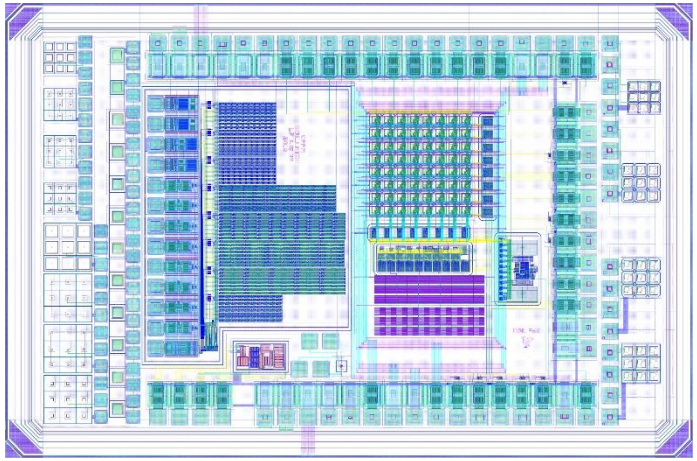
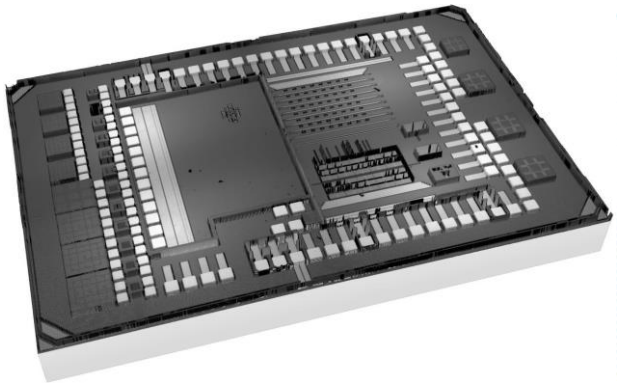
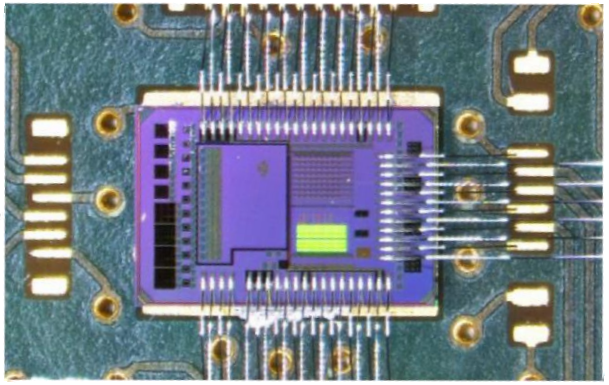




Development of HV-CMOS sensors within the RD50 collaboration

Eva Vilella,

on behalf of CERN-RD50 CMOS Working Group

University of Liverpool

vilella@hep.ph.liv.ac.uk

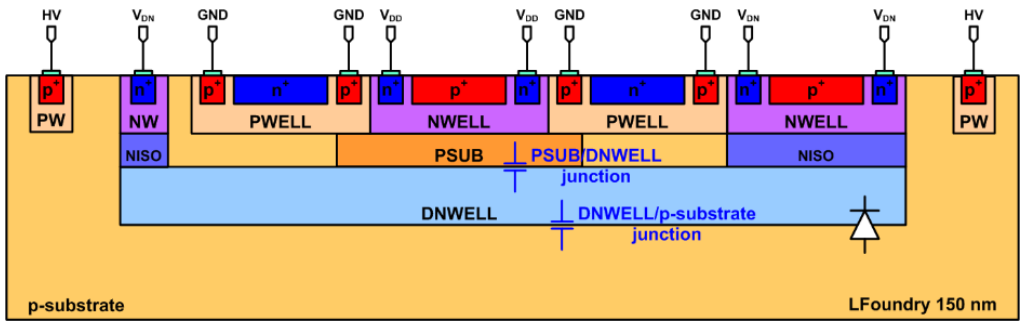
CERN-RD50 CMOS

- **CERN-RD50 collaboration**
  - Radiation hard semiconductor devices for very high luminosity colliders
  - >400 people
  - 64 institutes

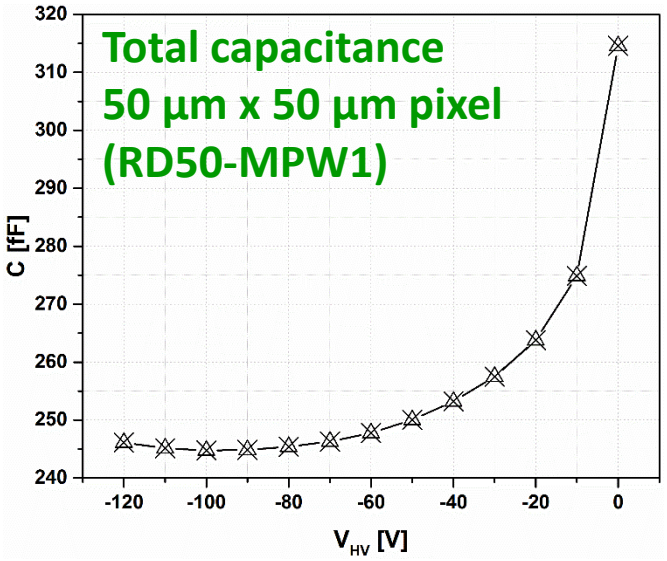
- **CERN-RD50 CMOS Working Group**
  - Programme to study and develop monolithic CMOS sensors with
    - High granularity
    - High radiation tolerance
    - LFoundry 150 nm HV-CMOS
  - Our programme includes
    - ASIC design
    - TCAD simulations
    - DAQ development
    - Performance evaluation
  - Involved resources
    - >40 people
    - 14 institutes

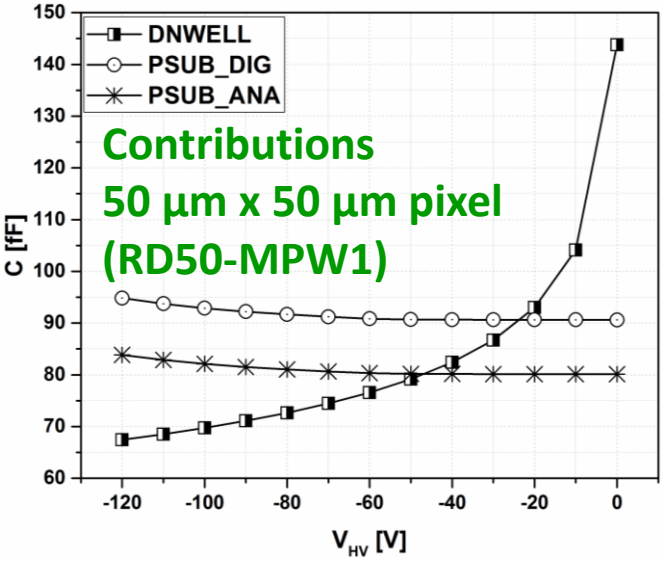
RD50-MPWx chips – Sensing diode

Cross-section



- **Large fill-factor pixel**
- PSUB layer isolates NWELL from DNWELL
  - CMOS electronics in pixel area are possible
- Detector capacitance has 2 contributions
  - P-substrate/DNWELL
  - PSUB/DNWELL
- Total pixel capacitance
  - RD50-MPWx → ~250 fF
- Equivalent Noise Charge (ENC)
  - RD50-MPWx → ~50 e^-

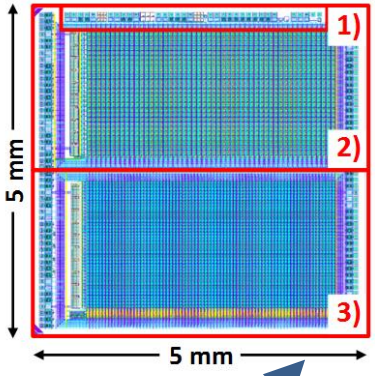




E. Vilella, VERTEX2019

CERN-RD50 CMOS timeline

RD50-MPW1



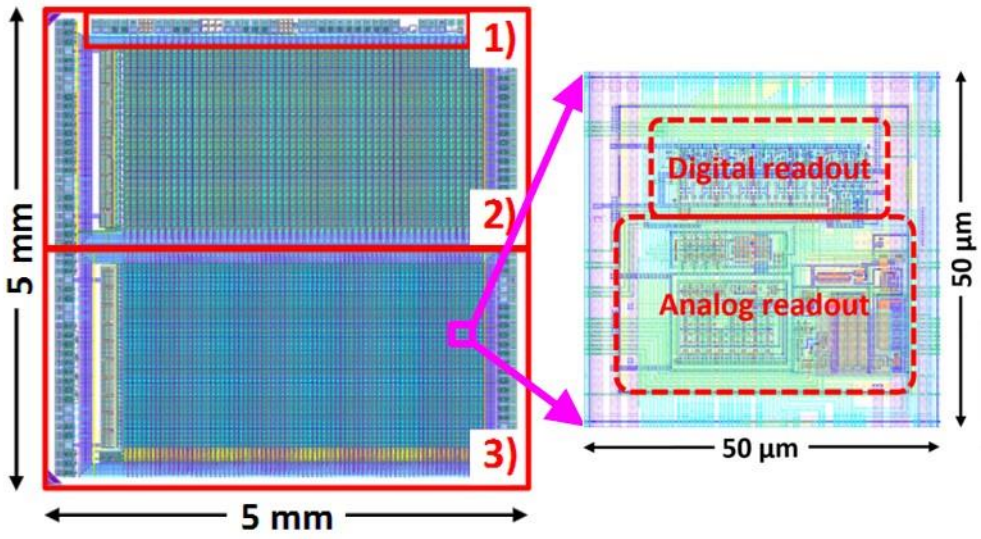
2017 2018 2019 2020 2021 2022 +

RD50-MPW1/2 – ASIC design

RD50-MPW1 (fab-out April 2018)

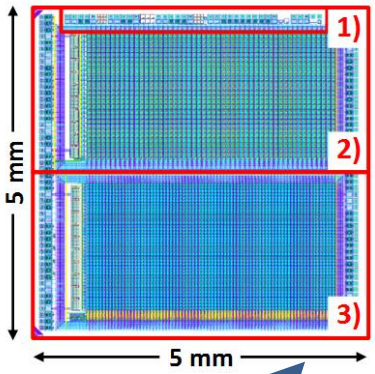
- 150 nm HV-CMOS LFoundry
- 600 and 1.1k Ω·cm wafers

3) Matrix of HV-CMOS pixels with
- **50 µm x 50 µm pixel size**
- **Analogue + digital readout in sensing area of the pixel**
- Continuous readout (FE-I3)
- 40 rows x 78 columns

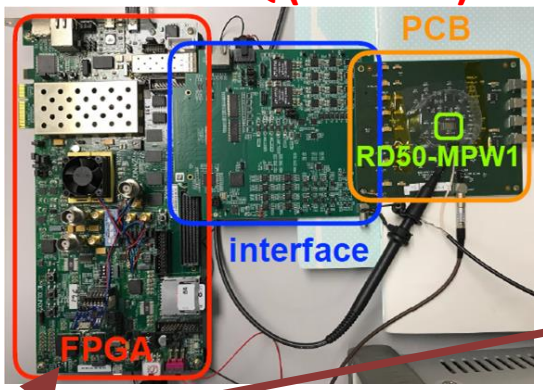


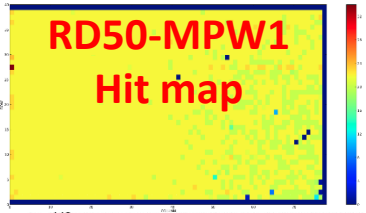
CERN-RD50 CMOS timeline

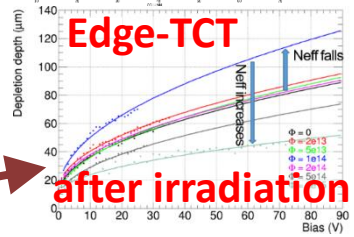
RD50-MPW1



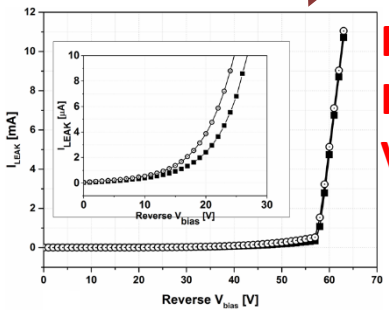
RD50 DAQ (Caribou)







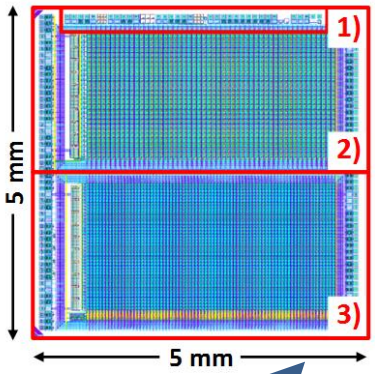
2017 | 2018 | 2019 | 2020 | 2021 | 2022 | +



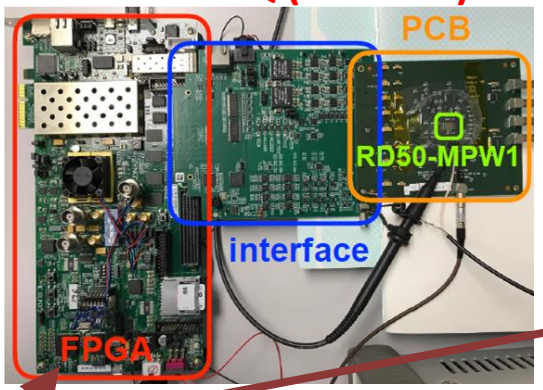
RD50-MPW1
I_LEAK↑
V_BD↓

CERN-RD50 CMOS timeline

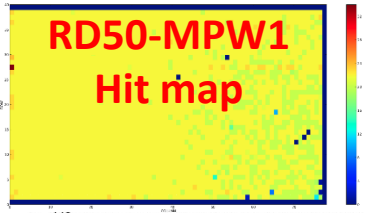
RD50-MPW1



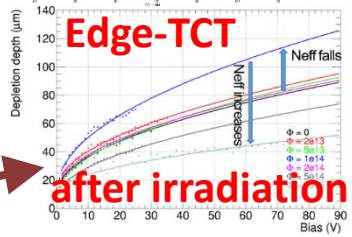
RD50 DAQ (Caribou)



RD50-MPW1
Hit map

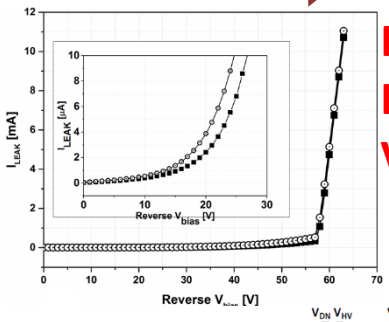


Edge-TCT



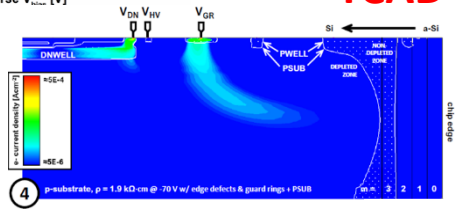
after irradiation

2017 | 2018 | 2019 | 2020 | 2021 | 2022 | +

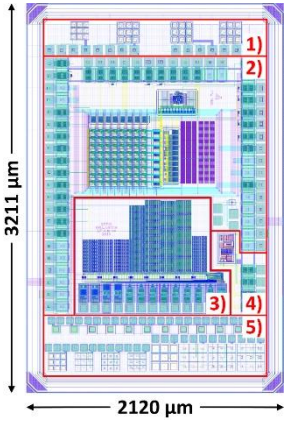


RD50-MPW1
I_LEAK↑
V_BD↓

TCAD



RD50-MPW2



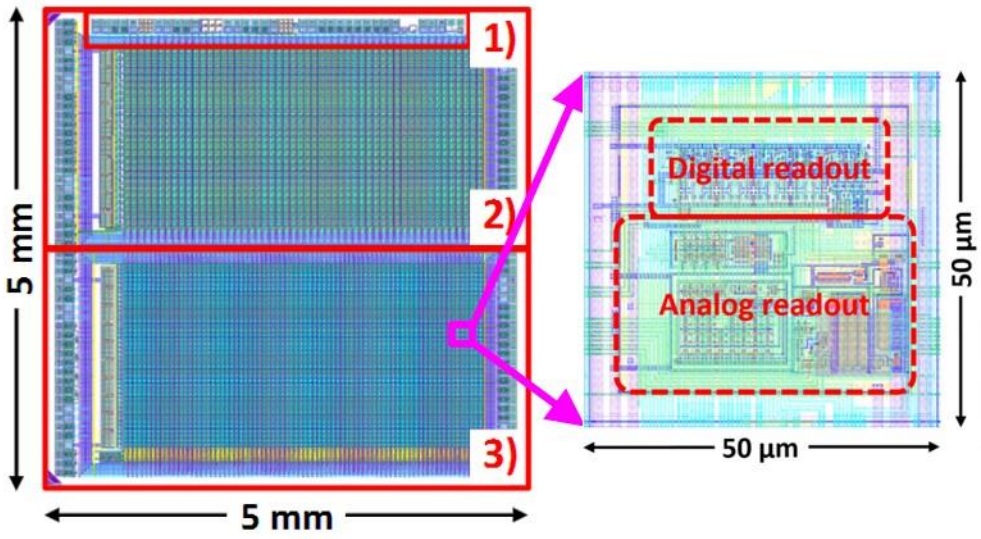
RD50-MPW1/2 – ASIC design

RD50-MPW1 (fab-out April 2018)

- 150 nm HV-CMOS LFoundry
- 600 and 1.1k Ω·cm wafers

3) Matrix of HV-CMOS pixels with

- **50 µm x 50 µm pixel size**
- **Analogue + digital readout in sensing area of the pixel**
- Continuous readout (FE-I3)
- 40 rows x 78 columns

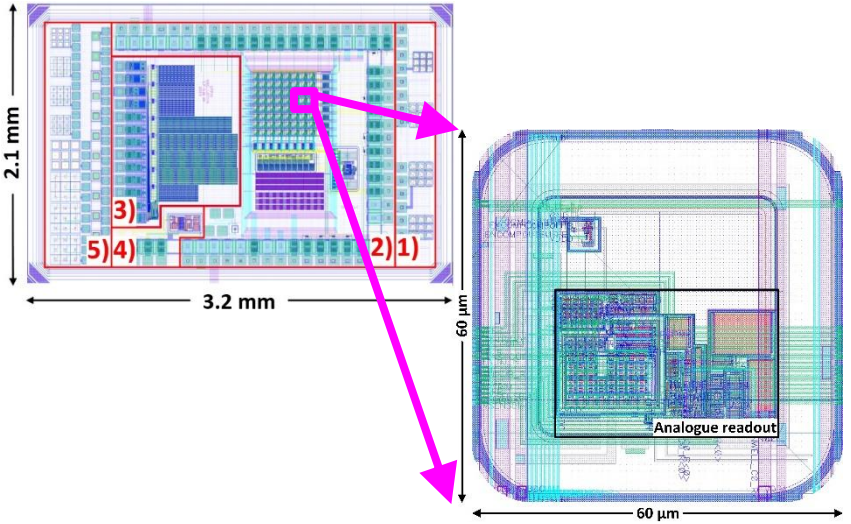


RD50-MPW2 (fab-out January 2020)

- LFoundry 150 nm HV-CMOS
- 10, 100, 1.9k and 3k Ω·cm wafers
- **Techniques to improve ILEAK and VBD**

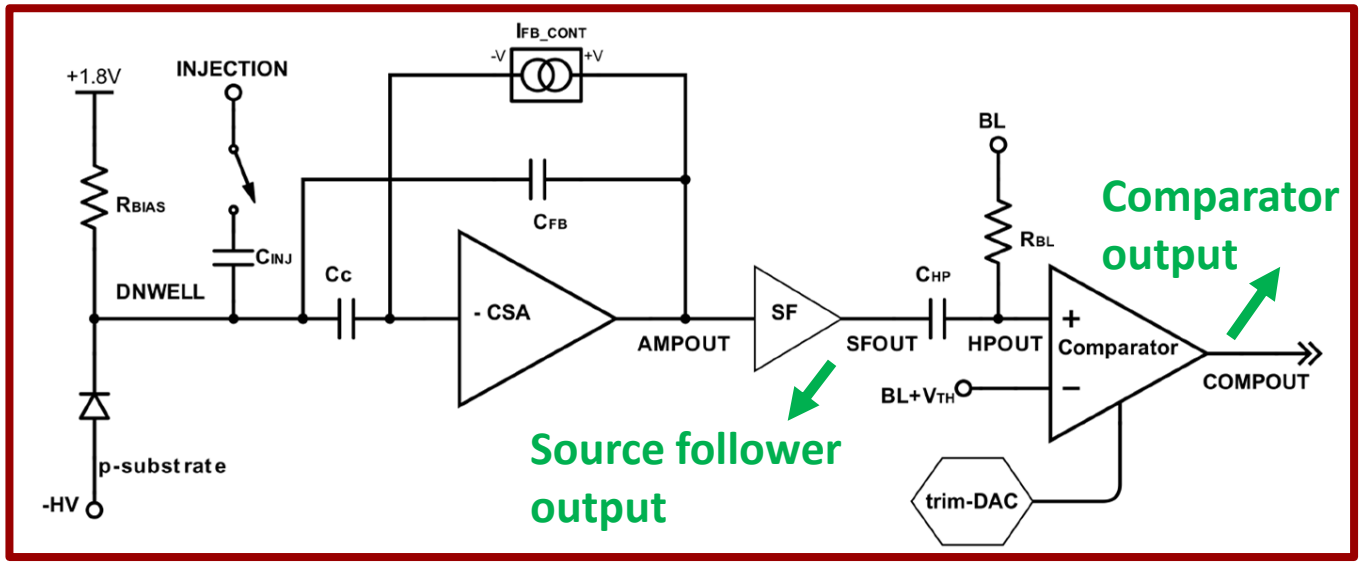
2) Matrix of HV-CMOS pixels with

- 60 µm x 60 µm pixel size
- Improved analogue readout in sensing area of the pixel
- Fast response rate
- 8 rows x 8 columns

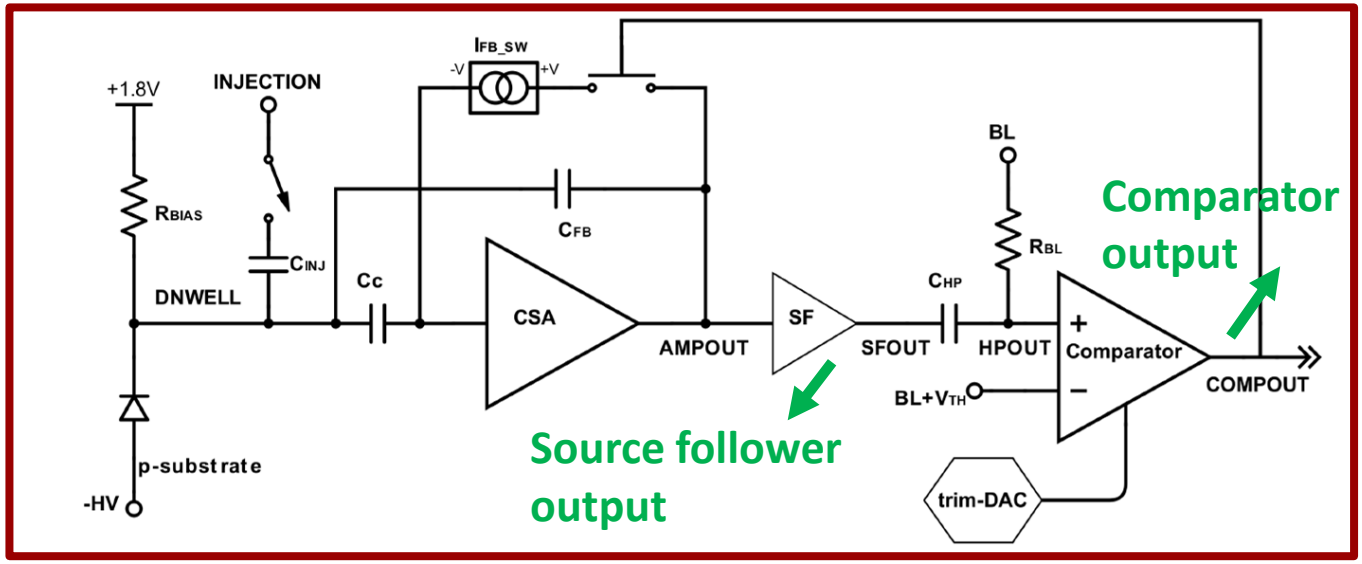


RD50-MPW2 – In-pixel readout (2 flavours)

Continuous reset



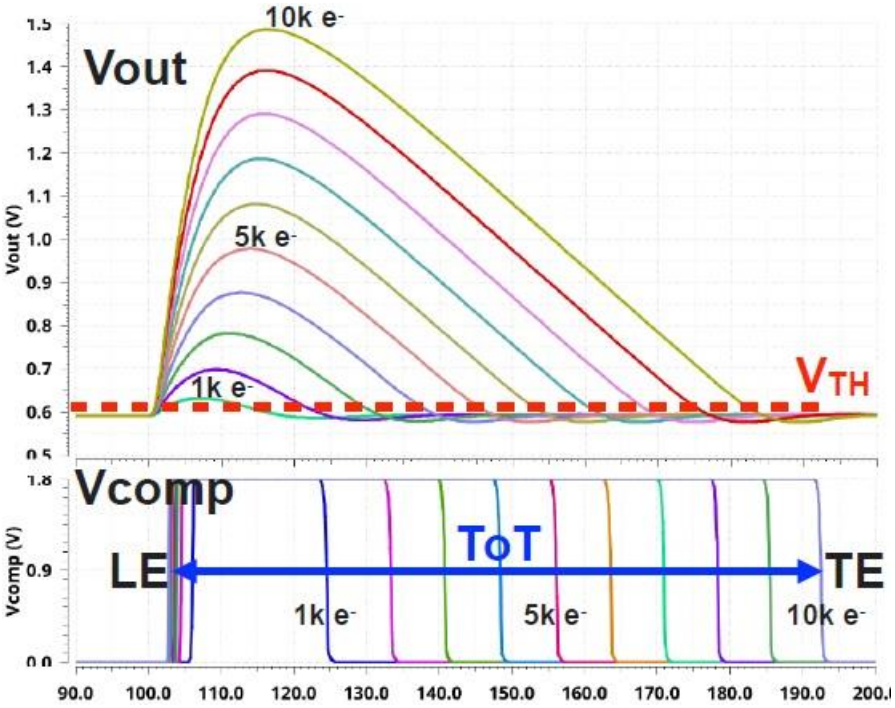
Switched reset



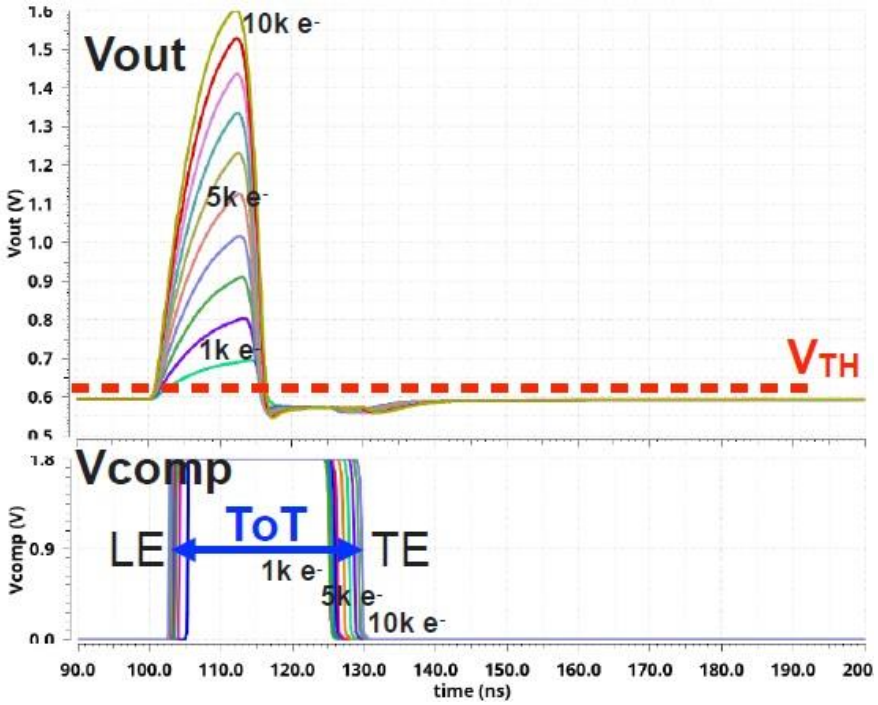
C. Zhang, TWEPP2019

RD50-MPW2 – In-pixel readout (2 flavours)

Continuous reset



Switched reset

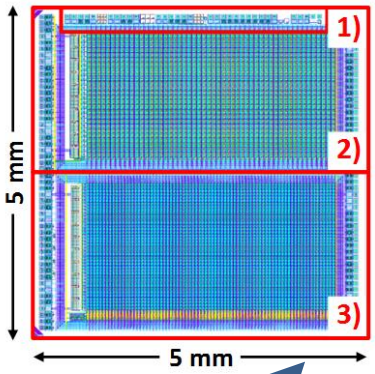


C. Zhang, TWEPP2019

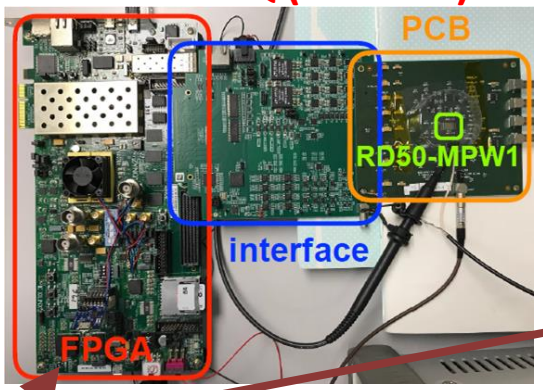
CERN-RD50 CMOS timeline

UNIVERSITY OF LIVERPOOL

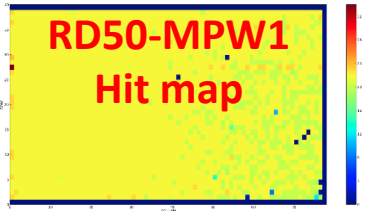
RD50-MPW1



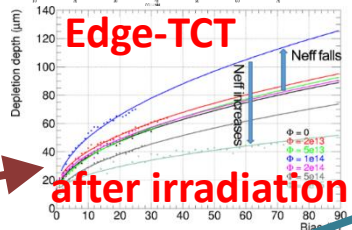
RD50 DAQ (Caribou)



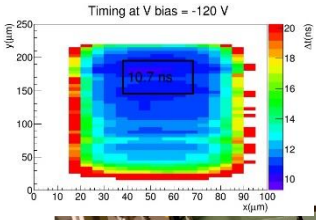
RD50-MPW1 Hit map

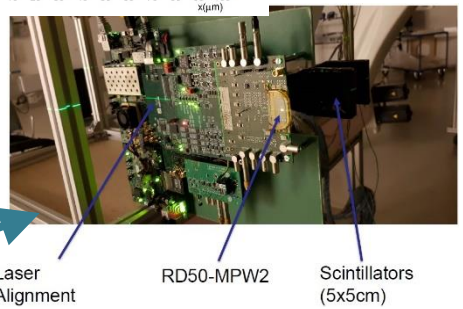


Edge-TCT



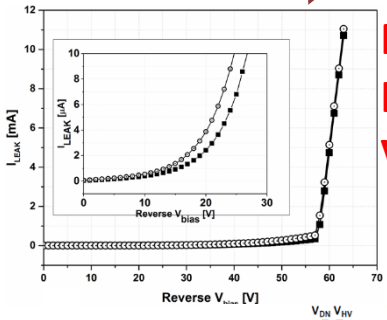
RD50-MPW2 Timing & test beam



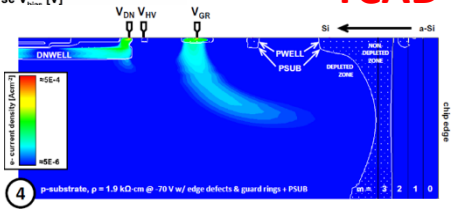


2017 | 2018 | 2019 | 2020 | 2021 | 2022 | +

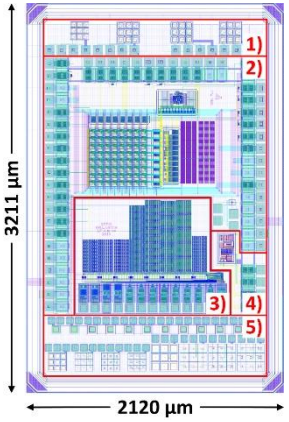
RD50-MPW1 I_LEAK↑ V_BD↓



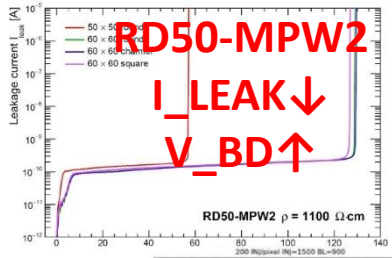
TCAD



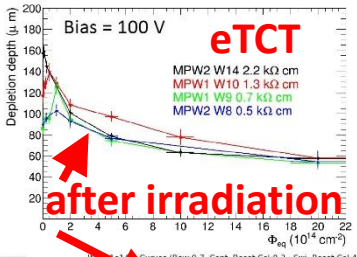
RD50-MPW2



RD50-MPW2 I_LEAK↓ V_BD↑

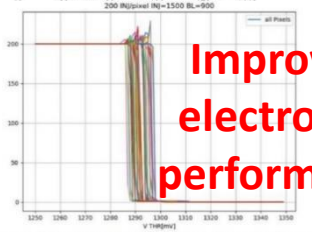


eTCT

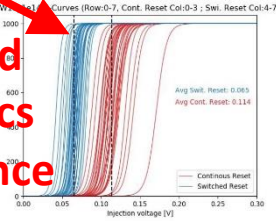


after irradiation

Improved electronics performance



S-curves for all pixels with threshold variation. Trim DA values adjusted. Injection amplitude 1500 mV.

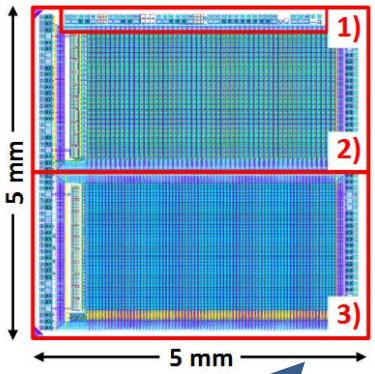


Wafer 13, 1e14N_{eq}

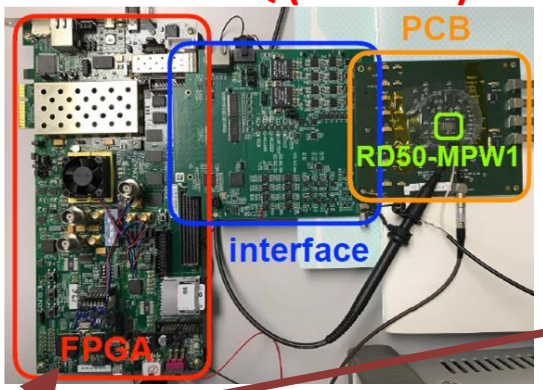
UNIVERSITY OF LIVERPOOL

CERN-RD50 CMOS timeline

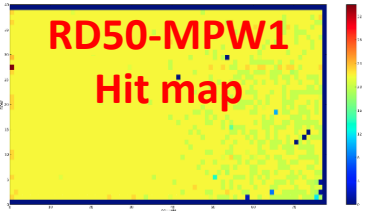
RD50-MPW1



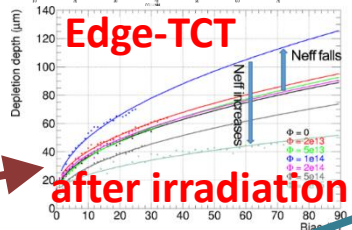
RD50 DAQ (Caribou)



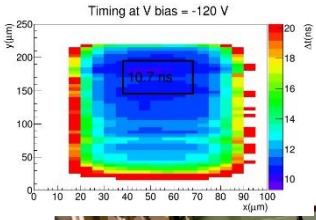
RD50-MPW1 Hit map

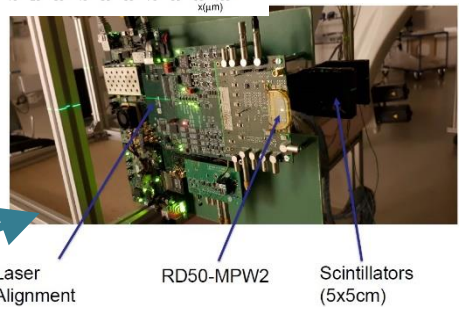


Edge-TCT



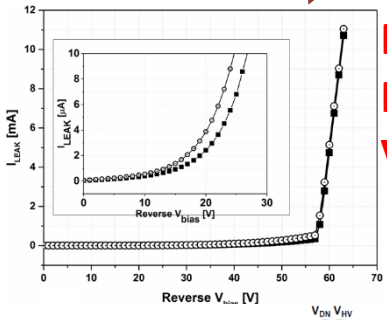
RD50-MPW2 Timing & test beam



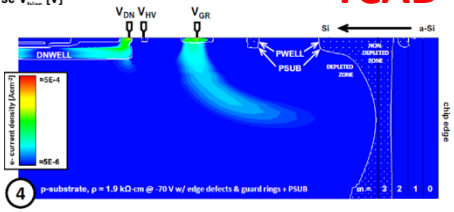


2017 | 2018 | 2019 | 2020 | 2021 | 2022 | +

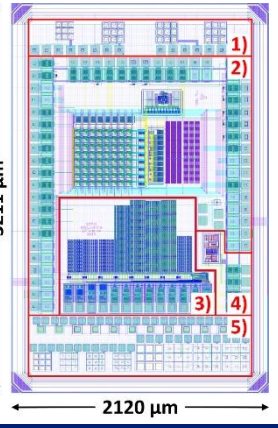
RD50-MPW1 I_LEAK↑ V_BD↓



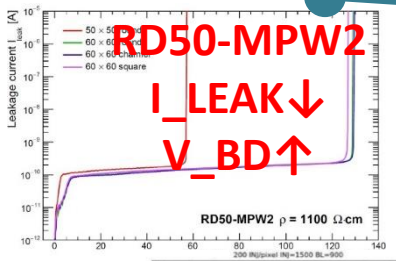
TCAD

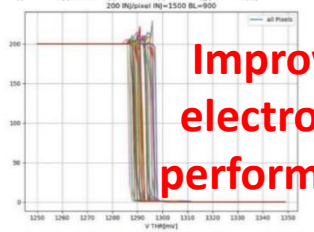


RD50-MPW2



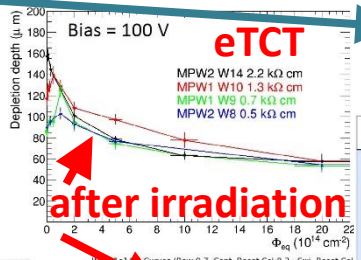
RD50-MPW2 I_LEAK↓ V_BD↑





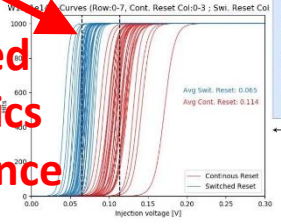
S-curves for all pixels with threshold variation. Trim DA values adjusted. Injection amplitude 1500 mV.

eTCT



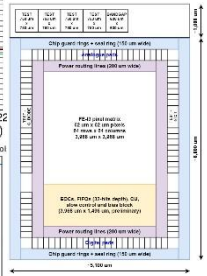
after irradiation

Improved electronics performance

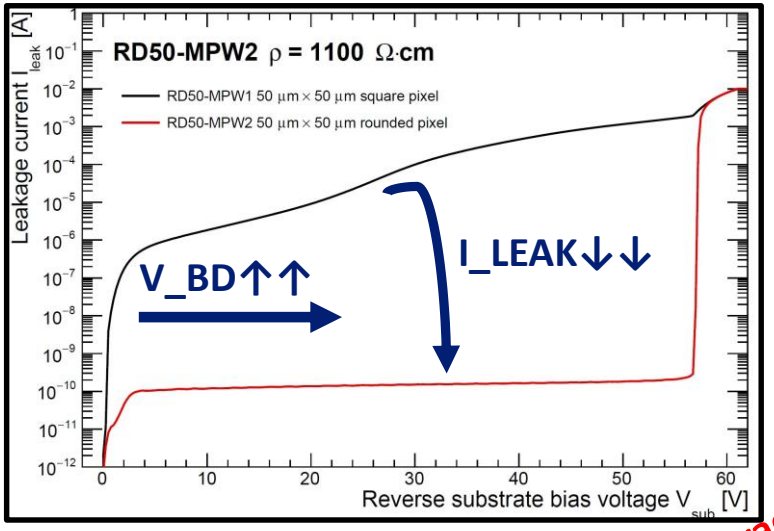


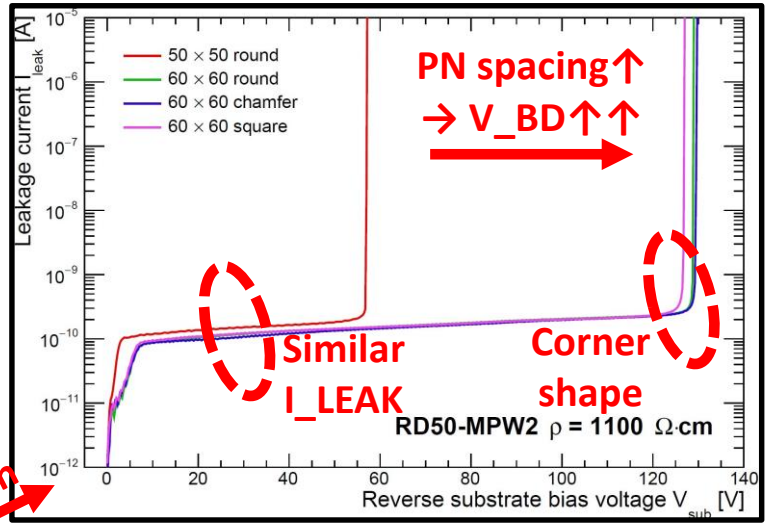
Wafer 13, 1e14N$_{eq}$

RD50-MPW3



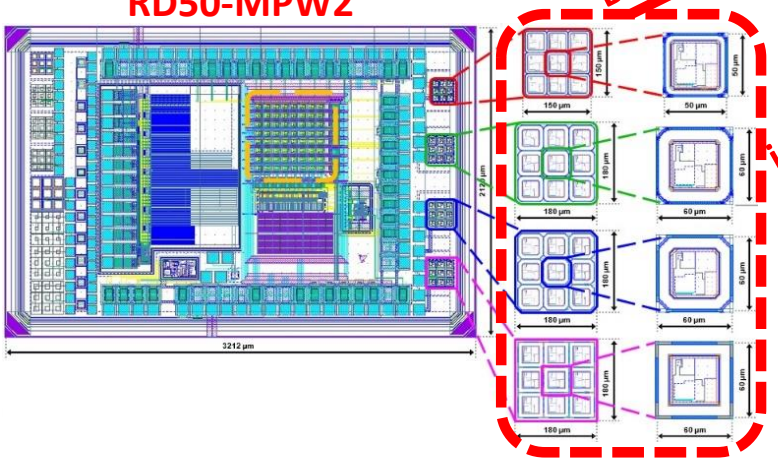
RD50-MPW2 – I(V)





Before irradiation

RD50-MPW2



After irradiation

2 kΩ·cm samples

		10^{13} cm^{-2}		10^{14} cm^{-2}		10^{15} cm^{-2}	
		k	*ILD*	*k*	*ILD*	*k*	*ILD*
round 3 μm	V_{bd} [V]	56	56	58	58	66	66
round 8 μm	V_{bd} [V]	122	122	116	116	132	132
chamf. 8 μm	V_{bd} [V]	122	122	128	128	146	146
square 8 μm	V_{bd} [V]	118	118	126	126	150	150

Fluence↑ → I_LEAK↑, V_BD↑

M. Franks, 36th RD50 WS

A. Catalan, internal 2021

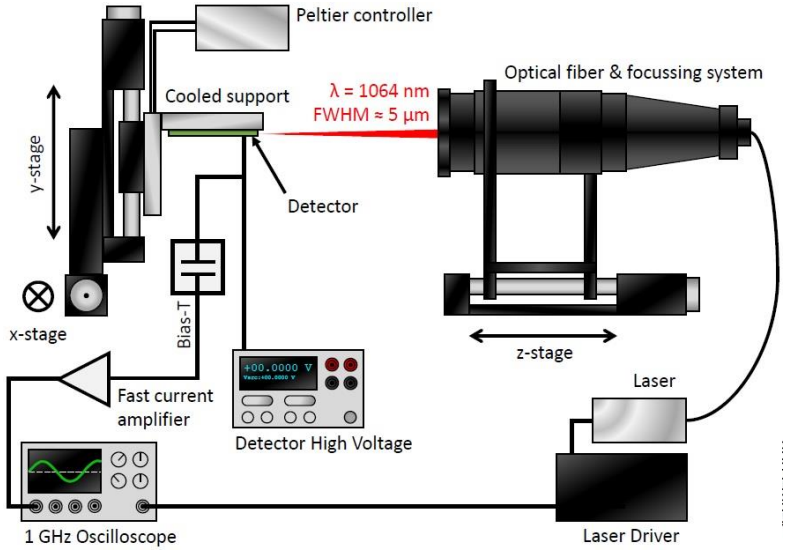
RD50-MPW2 – Timing measurements

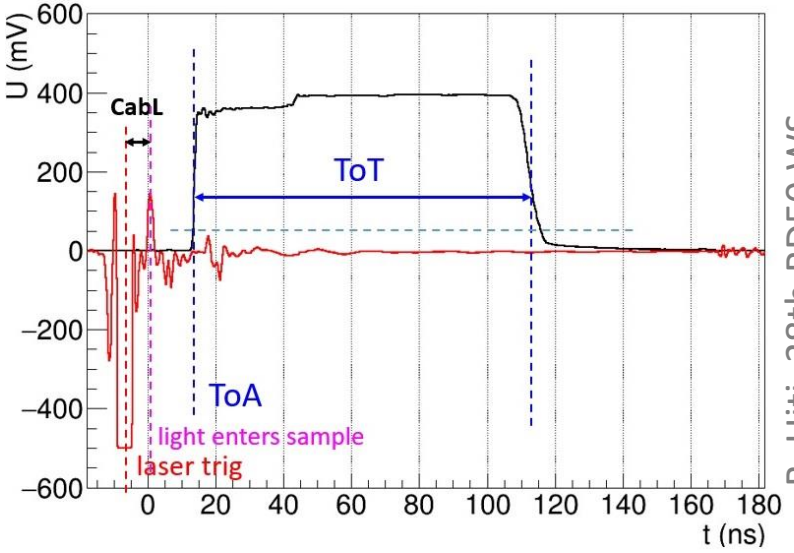
Motivation

- To study time-walk dependence on pixel position (smaller signals on pixel edges → larger time-walk)

Method

- Using edge-TCT setup
- Measure in-pixel comparator output of RD50-MPW2 active matrix
  - **Time Over Threshold (ToT) → signal size**
  - **Time of Arrival (ToA) → time-walk**
- Acquisition triggered by laser driver output, adjustment for cable and fibre length, light hits sample at t = 0
- Change signal size by varying laser power





B. Hiti, 38th RD50 WS

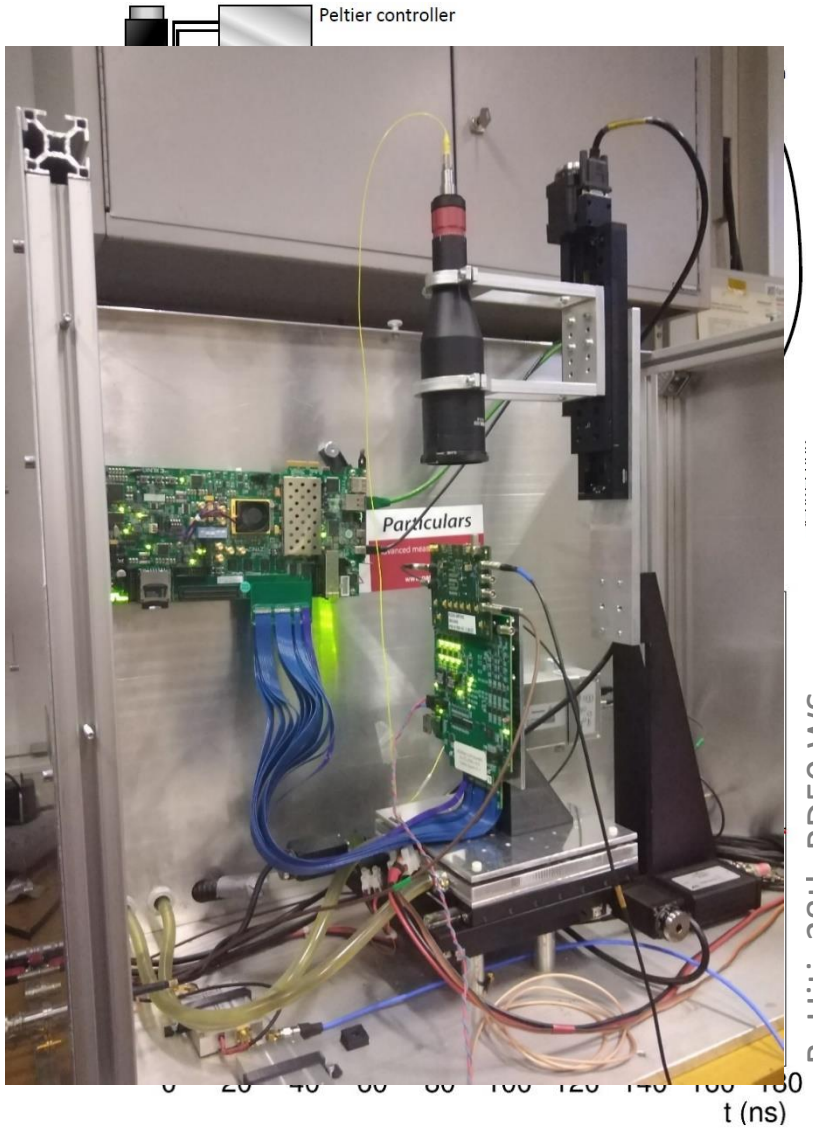
RD50-MPW2 – Timing measurements

Motivation

- To study time-walk dependence on pixel position (smaller signals on pixel edges → larger time-walk)

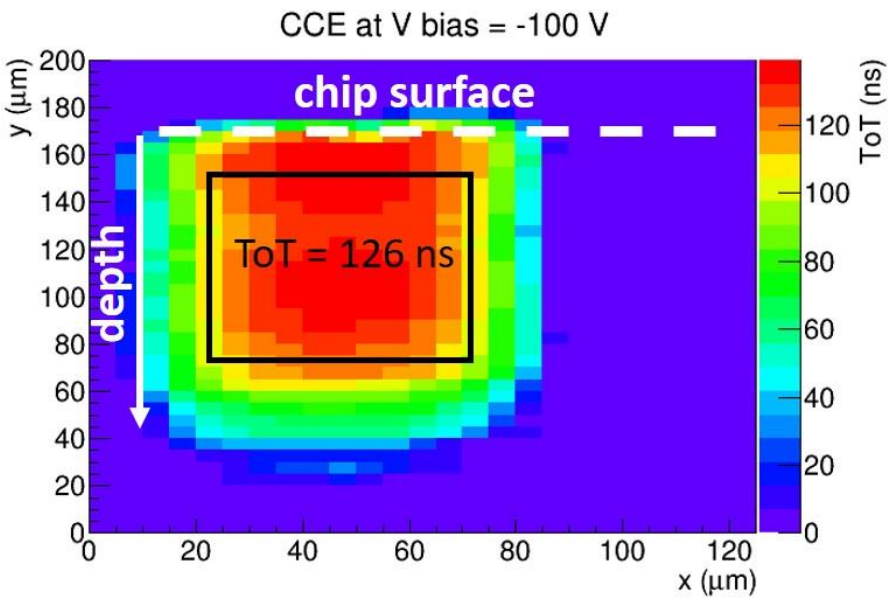
Method

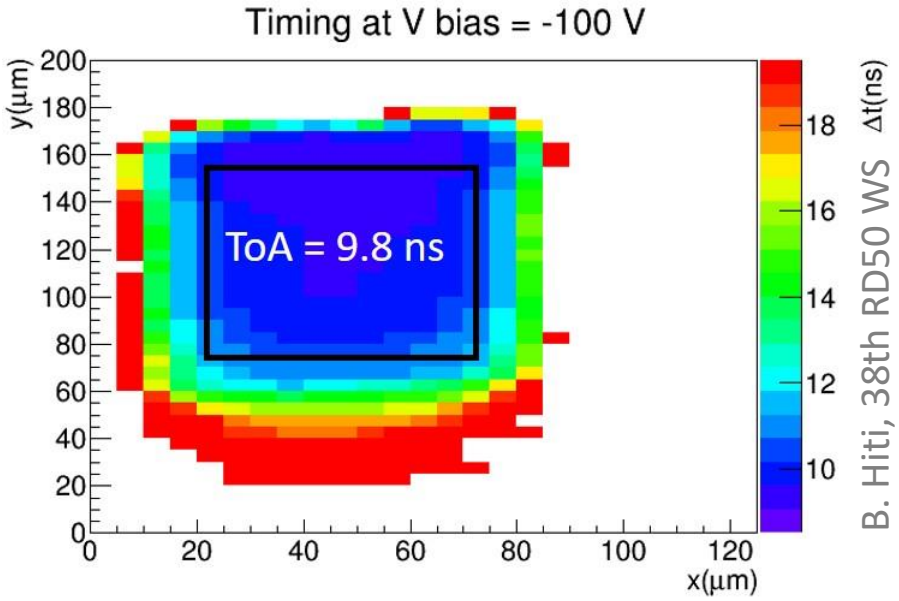
- Using edge-TCT setup
- Measure in-pixel comparator output of RD50-MPW2 active matrix
  - **Time Over Threshold (ToT) → signal size**
  - **Time of Arrival (ToA) → time-walk**
- Acquisition triggered by laser driver output, adjustment for cable and fibre length, light hits sample at t = 0
- Change signal size by varying laser power



B. Hiti, 38th RD50 WS

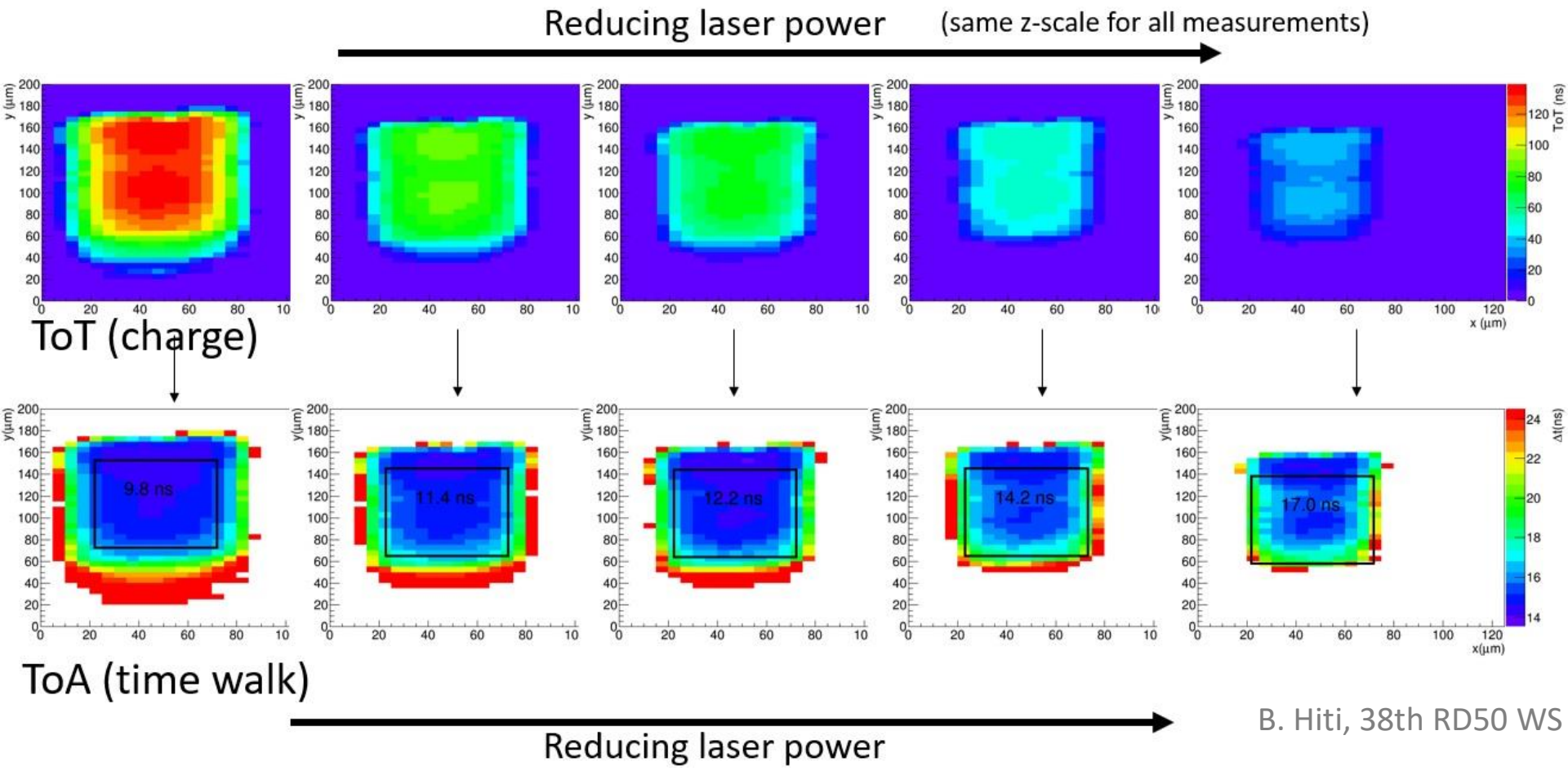
RD50-MPW2 – Timing measurements





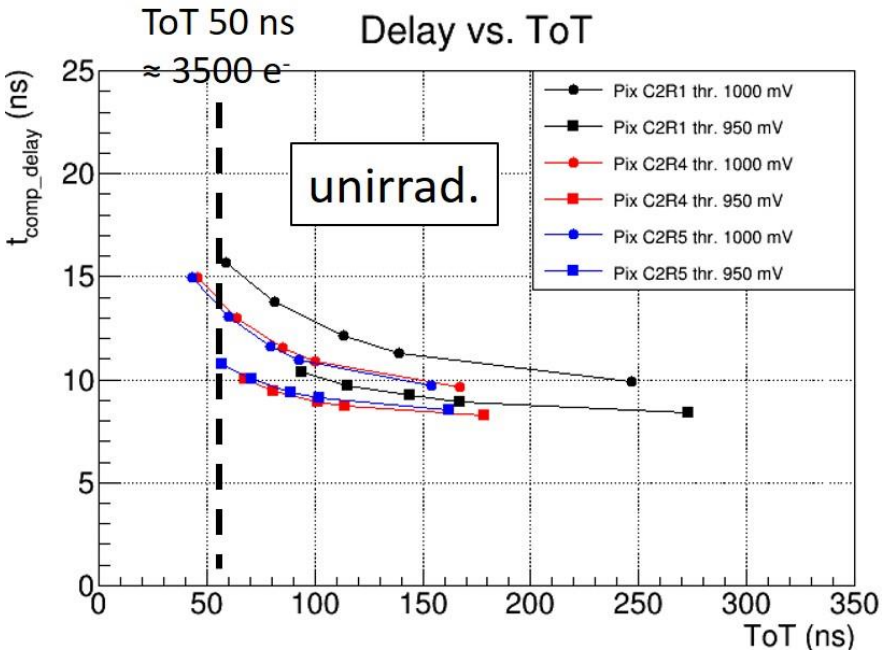
- Example of charge collection (left) and timing (right) measurements
- Evaluate average ToT (left) and ToA (right) in a volume 50 µm x 80 µm (W x H), starting 20 µm below the surface

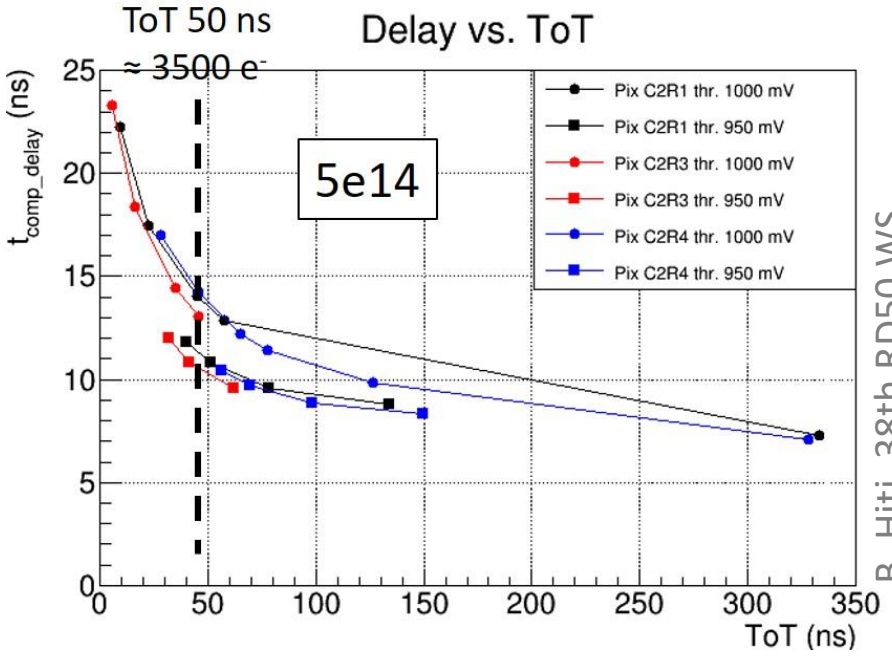
RD50-MPW2 – Timing measurements



- Reducing laser power → lower charge collection/lower ToT, greater time-walk/greater ToA

RD50-MPW2 – Timing measurements



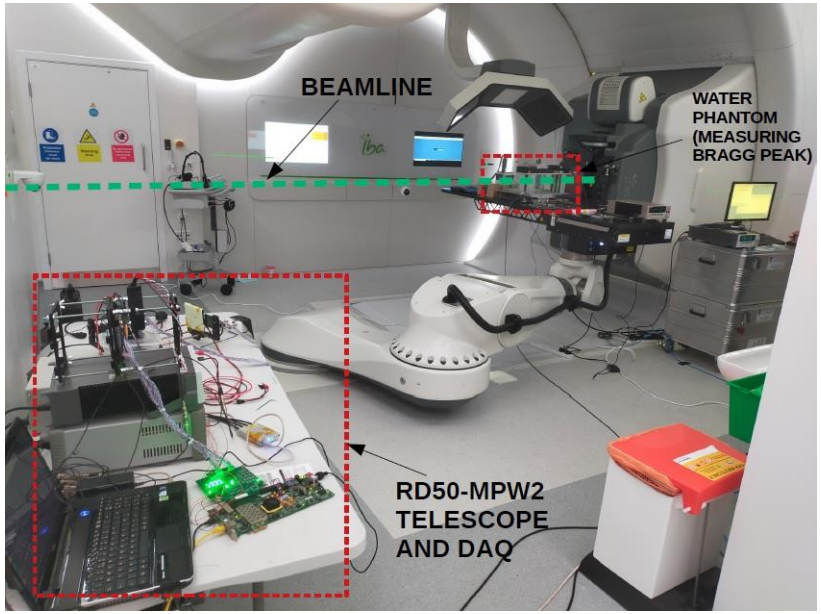


B. Hiti, 38th RD50 WS

- Edge-TCT time-walk measurement in three different pixels before and after irradiation
- Time-walk increases with higher threshold (as expected)
- Significant pixel-to-pixel variations (manufacturing variations)
- Time-walk similar before and after irradiation
- Measurements in low ToT limited by noise level

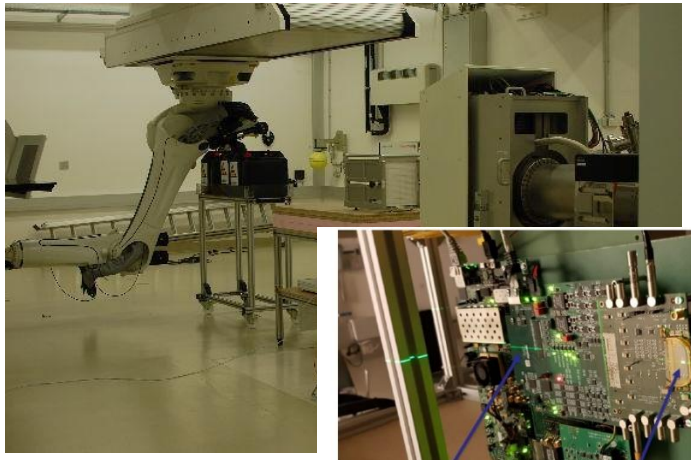
RD50-MPW2 – Test beams

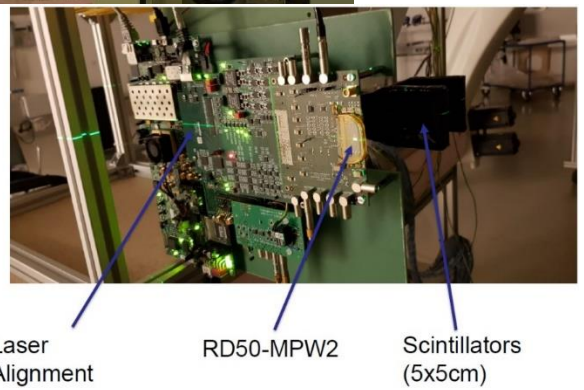
Rutherford Cancer Centre (UK)



S. Powell, TWEPP 2021

MedAustron (Austria)

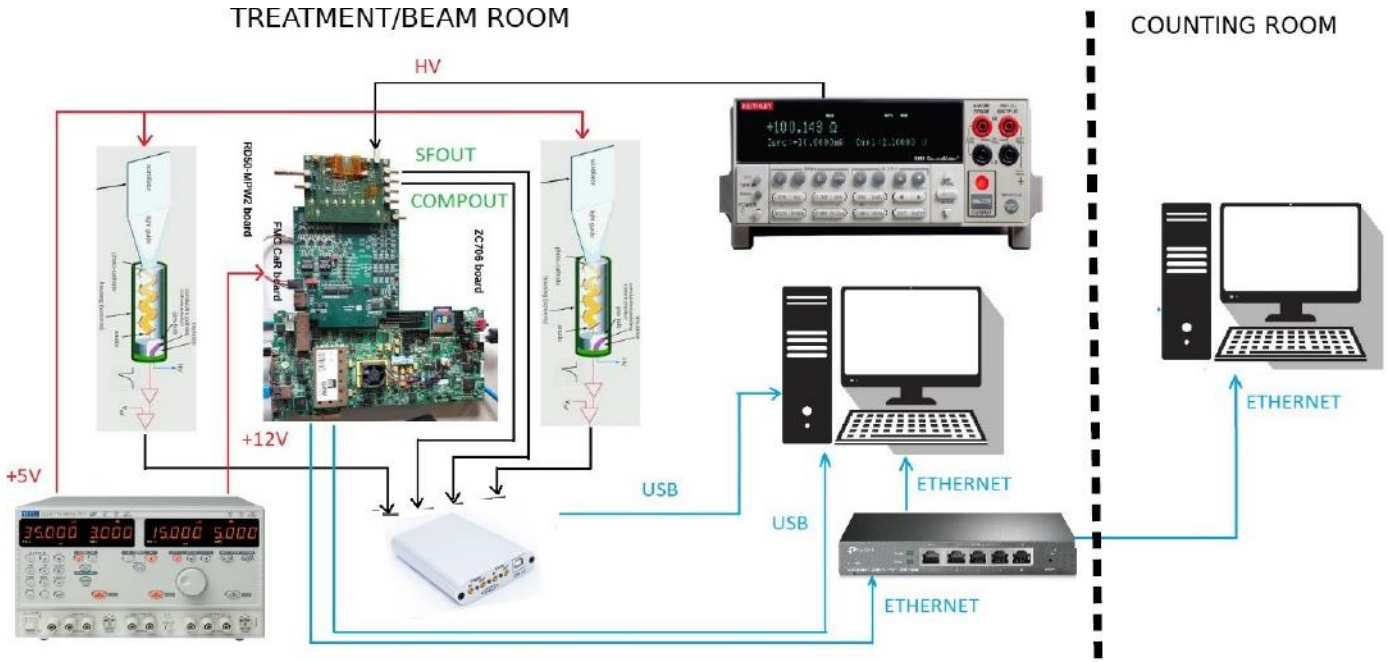


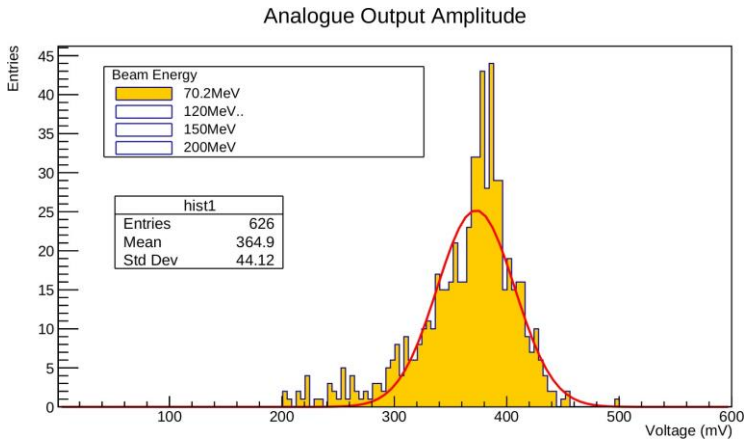


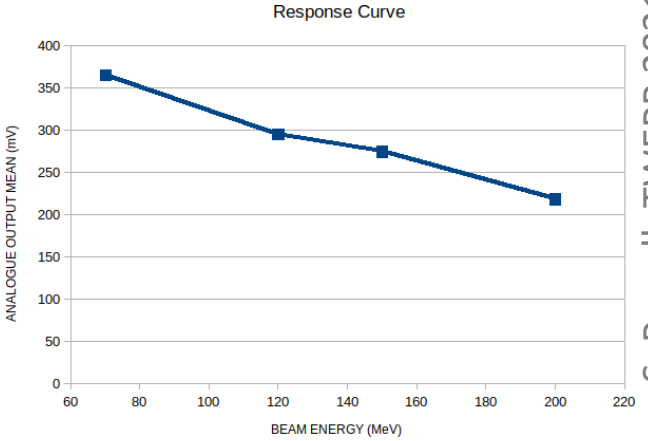
P. Sieberer, TIPP 2021

Parameters	Rutherford (UK)	MedAustron (Austria)
Repetition rate [MHz]	0.1	~3.5
Bunch length	10 µs	5 s with 2.5 s pause
Protons/s	10E7	10E10
Beam energy [MeV]	10-229	60-800

RD50-MPW2 – Test beam (analogue)

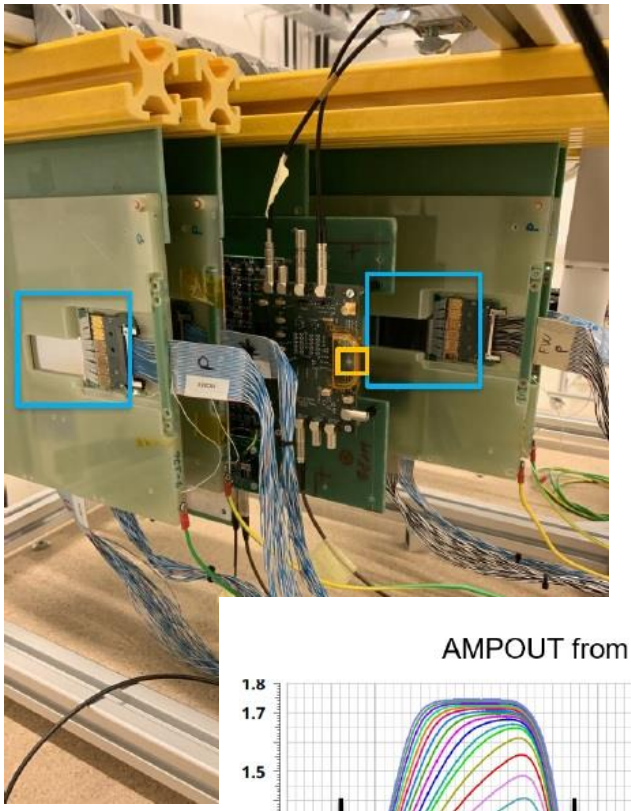




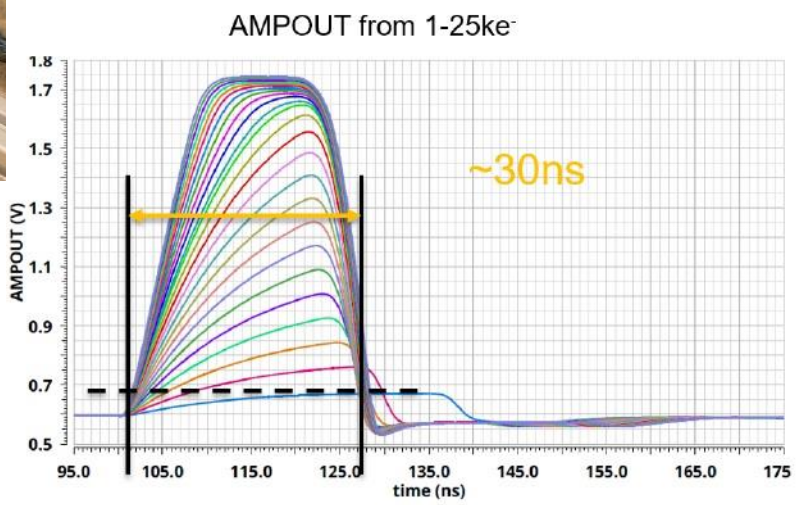


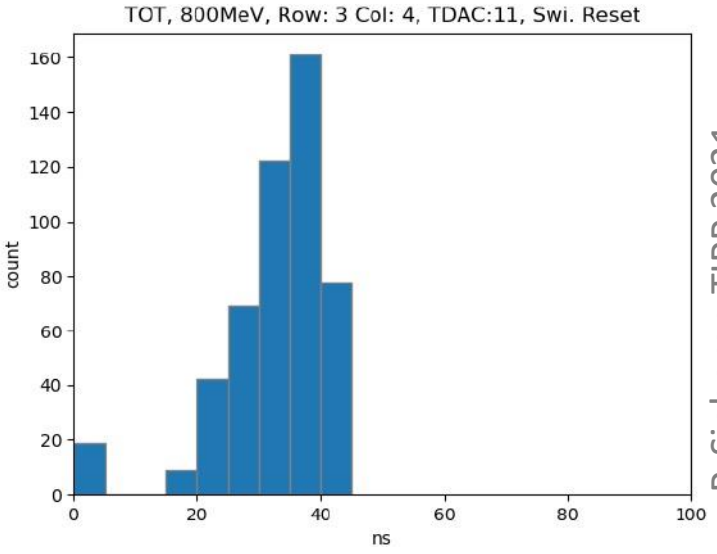
S. Powell, TWEPP 2021

RD50-MPW2 – Test beam (digital)



- **Beam telescope**
  - 2 double sided silicon strip detectors upstream
  - 1 RD50-MPW2
  - 2 double sided silicon strip detectors downstream
  - Triggered by coincidence with AIDA-TLU
  - Standalone firmware (counter in FPGA)
- **Switched reset pixel**
  - Simulations (all energies) → ToT ~30 ns
  - Measurements (800 MeV protons) → in good agreement with simulations





P. Sieberer, TIPP 2021

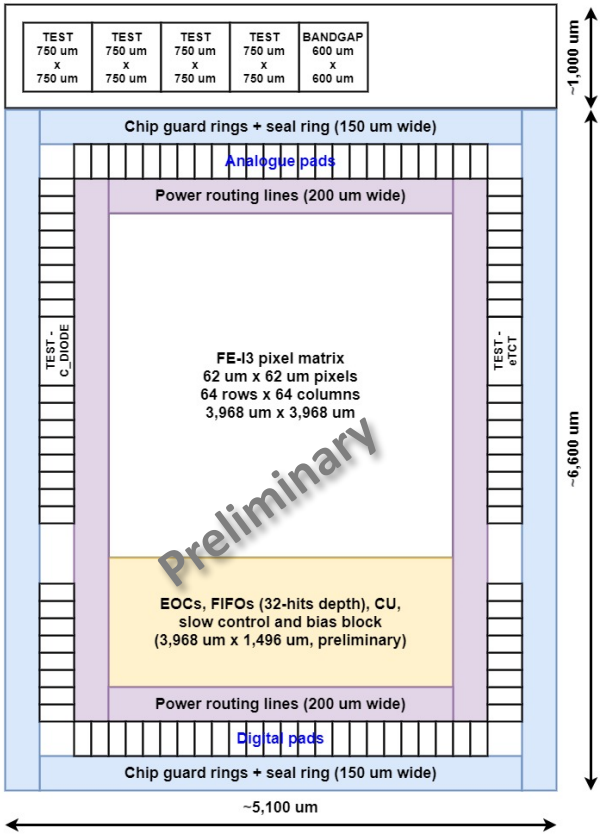
RD50-MPW3 – Motivation

RD50-MPW2

- Very successful chip, but with limitations
  - Reduced number of rows and columns (8 x 8)
  - No pixel digital readout to identify particle hits
  - Very simple TX readout → some measurements too slow or not possible

RD50-MPW3

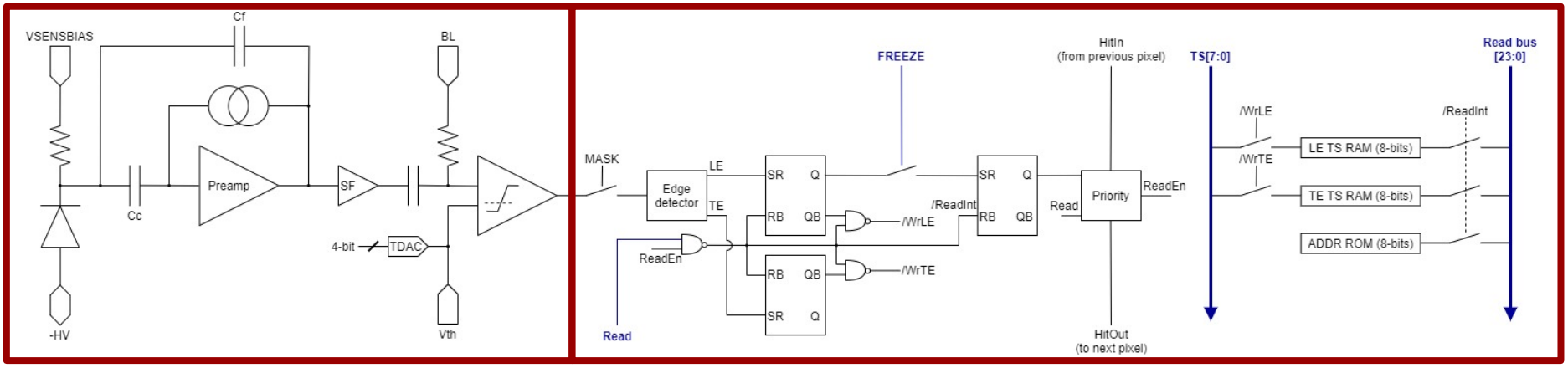
- Larger and more advanced matrix to further study HV-CMOS sensors
  - 64 rows x 64 columns
  - With in-pixel digital readout (FE-I3 style)
  - With optimised peripheral readout for effective pixel configuration and fast data TX
  - With all the lessons learned from RD50-MPW1/2
- Chip submission planned for October 2021 through an MPW shuttle run
- Resistivities (planned): standard, 1.9k and >2k Ω·cm



RD50-MPW3 – Pixel schematic

Analogue readout

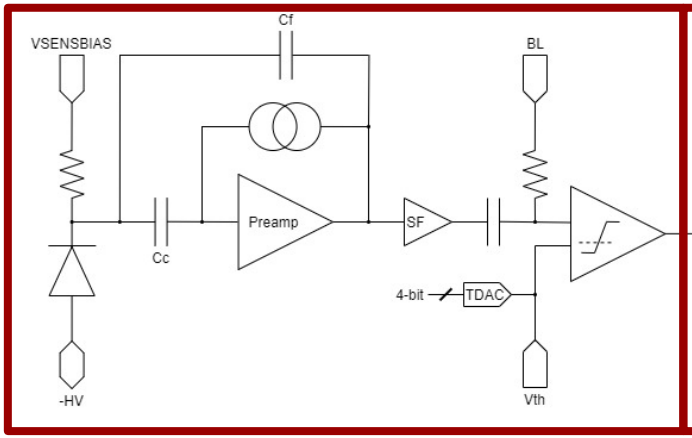
Digital readout



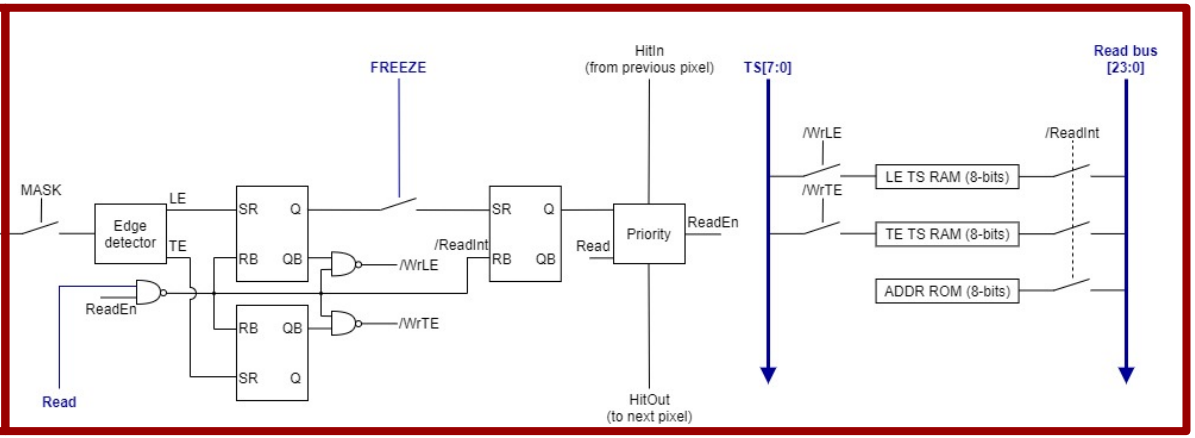
- **Analogue readout** from RD50-MPW2
- **Digital readout**, highly improved, from RD50-MPW1
- New in-pixel logic
  - To mask noisy pixels (MASK)
  - New priority circuit for less-area consuming alternative
  - Possibility to pause digitisation of new hits until readout is complete (FREEZE)
  - **8-bit SRAM shift register** for serial configuration
    - Pixel-trimming to compensate for threshold voltage variations (4-bits)
    - Flag to mask noisy pixels (1-bit)
    - Signals to enable/disable calibration circuit (1-bit), SF output (1-bit), COMP output (1-bit)

RD50-MPW3 – Pixel schematic

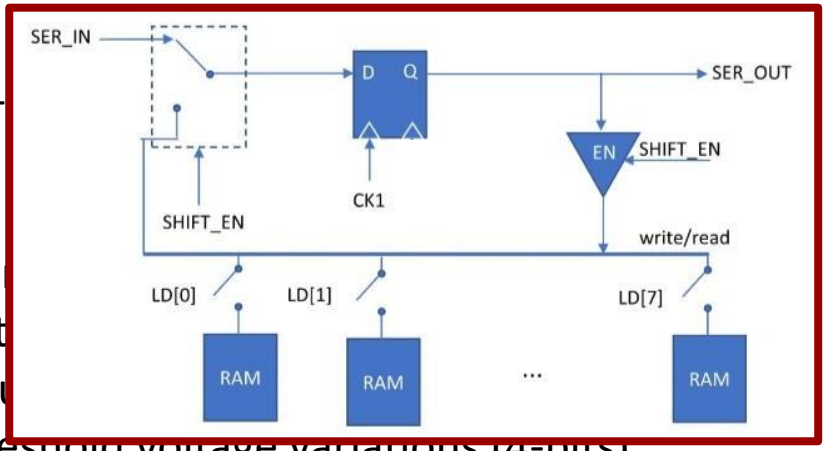
Analogue readout



Digital readout

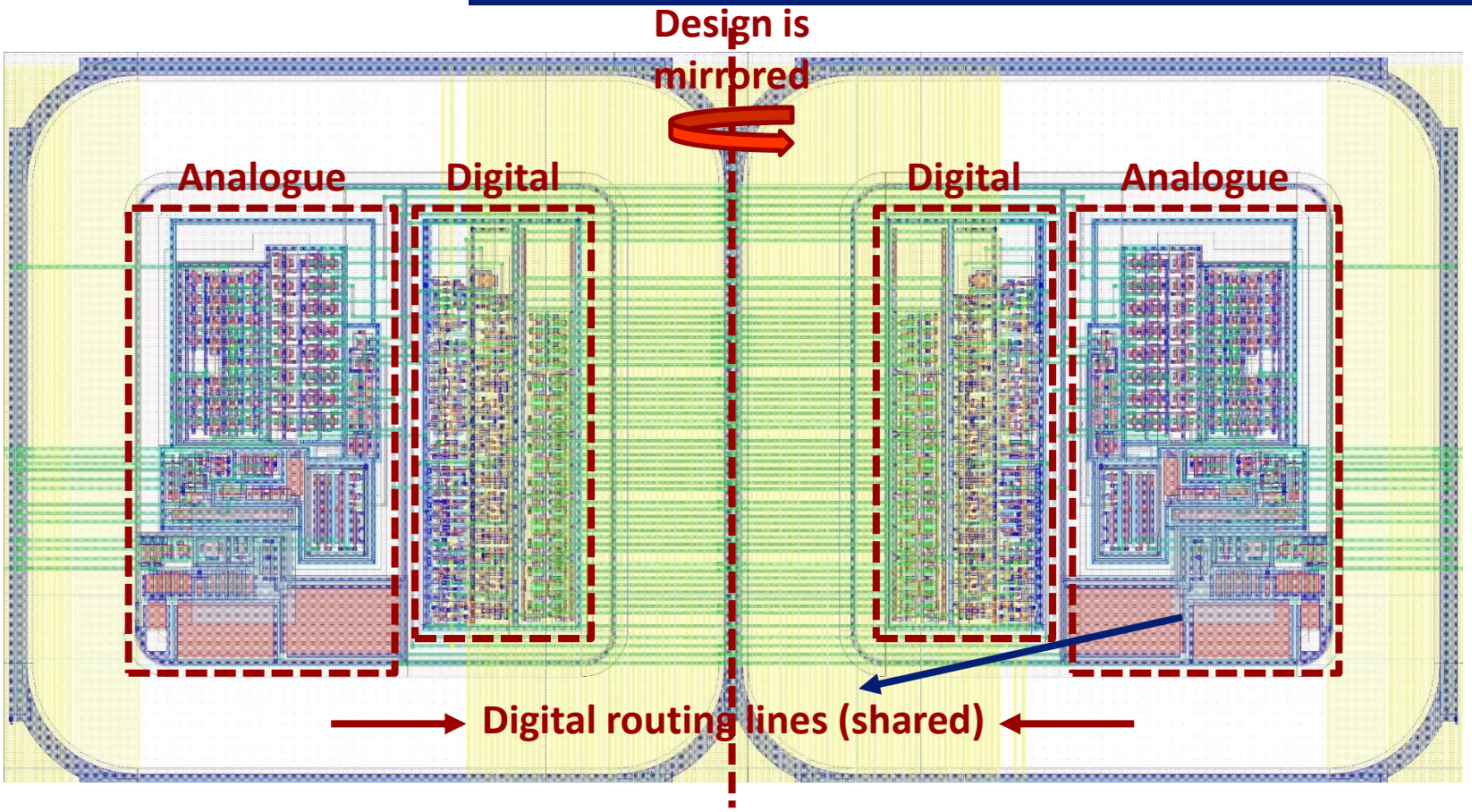


- **Analogue readout** from RD50-MPW2
- **Digital readout**, highly improved, from RD50-
- New in-pixel logic
  - To mask noisy pixels (MASK)
  - New priority circuit for less-area consumi
  - Possibility to pause digitisation of new hit
  - **8-bit SRAM shift register** for serial configu
    - Pixel-trimming to compensate for threshold voltage variations (4-bits)
    - Flag to mask noisy pixels (1-bit)
    - Signals to enable/disable calibration circuit (1-bit), SF output (1-bit), COMP output (1-bit)



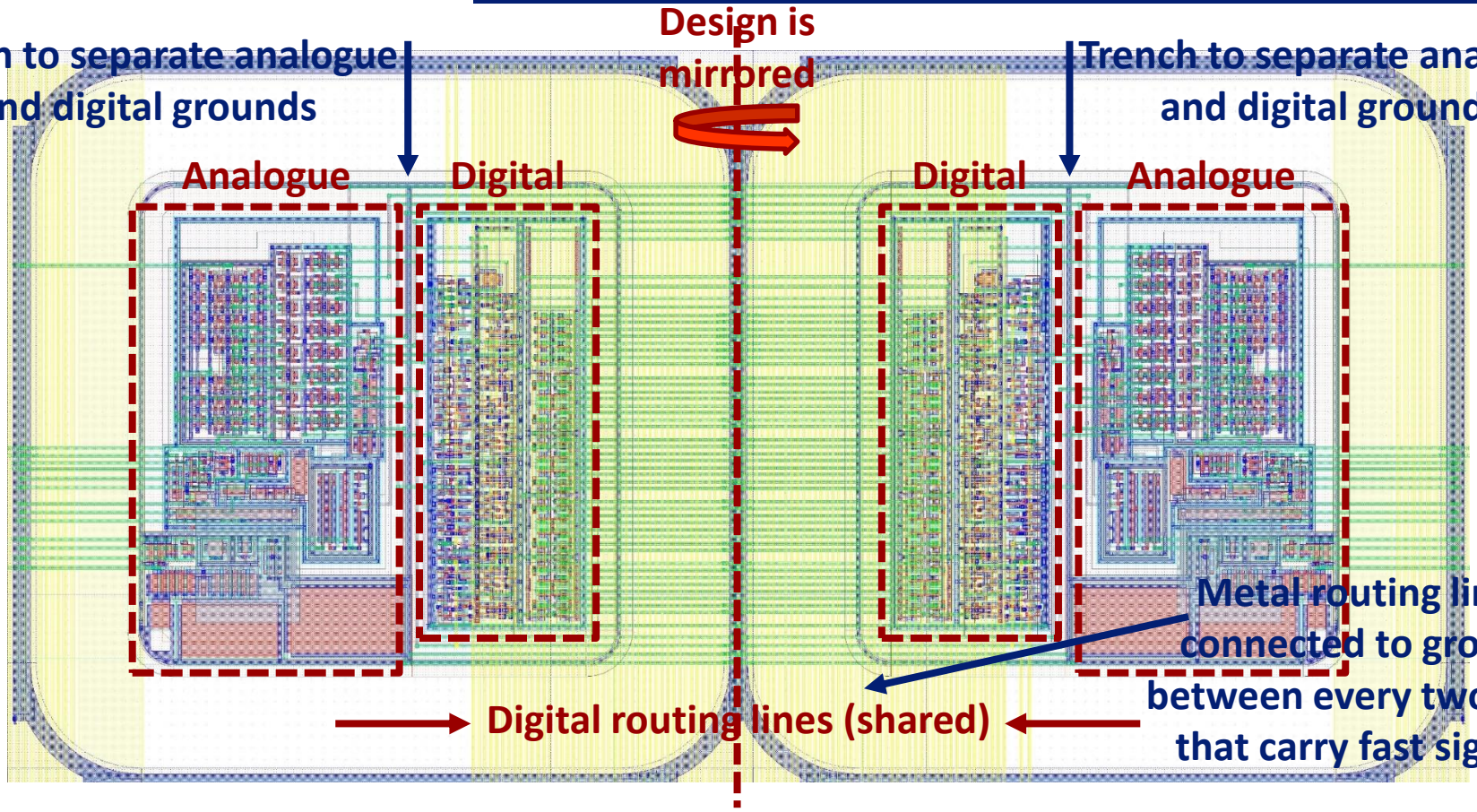
R. Casanova, 38th RD50 WS

RD50-MPW3 – Pixel layout



- **Double column scheme to alleviate routing congestion and minimise crosstalk**
  - Pixels within double column share many signals → ~ x0.5 less routing lines
    - Digital input/outputs (TS IN, TS OUT, ADDR), control signals (Read, Freeze, etc.)
- Pixel size is 62 µm x 62 µm

RD50-MPW3 – Pixel layout



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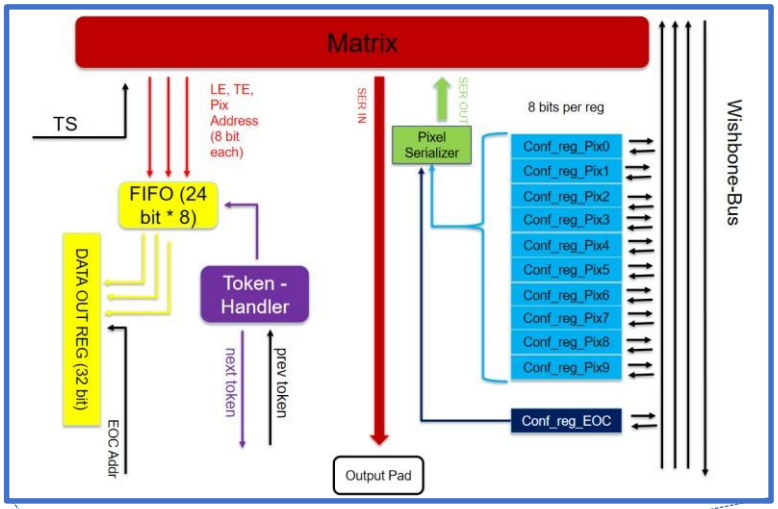
  - Pixels within double column share many signals → ~ x0.5 less routing lines
    - Digital input/outputs (TS IN, TS OUT, ADDR), control signals (Read, Freeze, etc.)
- Pixel size is 62 µm x 62 µm

RD50-MPW3 – EOC + readout + slow control

New EOC architecture - Components

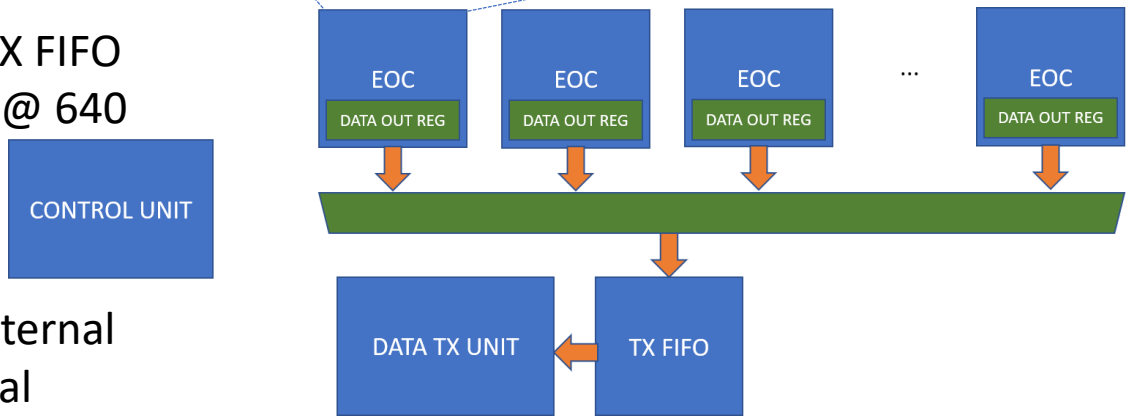
- FIFO stores hit data (LE TS, TE TS and ADDR)
- FSM reads double column
- Token mechanism to determine which EOC is read out



P. Sieberer

Readout

- Pixel is read out immediately after hit (if FIFO is not full)
- CU reads EOCs sequentially
- Data stored temporarily in TX FIFO
- Data TX unit with LVDS port @ 640 Mbps



R. Casanova, 38th RD50 WS

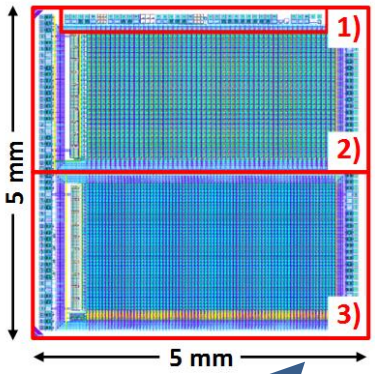
Slow control

- Based on I2C protocol for external communication using internal Wishbone bus

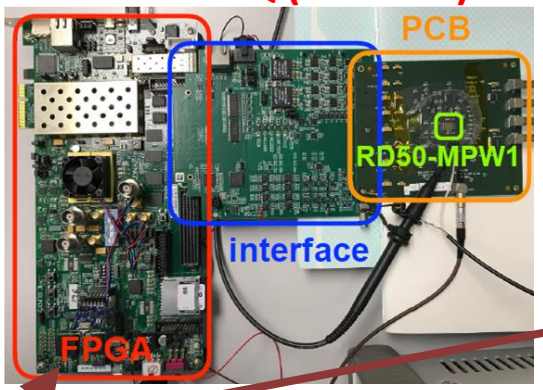
UNIVERSITY OF LIVERPOOL

CERN-RD50 CMOS timeline

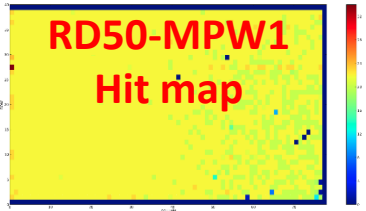
RD50-MPW1



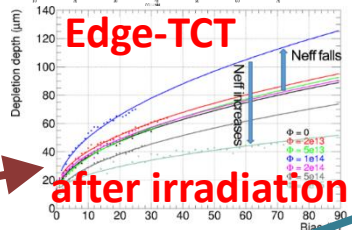
RD50 DAQ (Caribou)



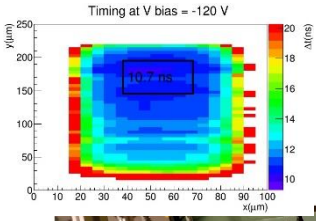
RD50-MPW1 Hit map

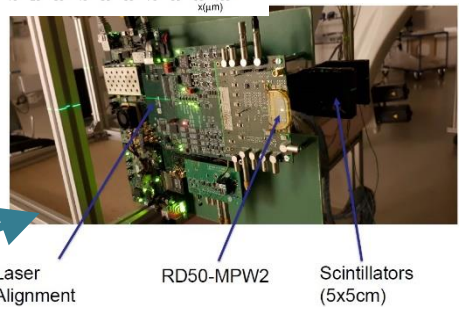


Edge-TCT



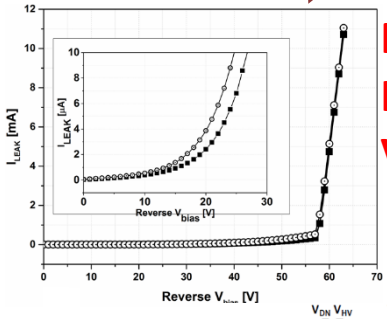
RD50-MPW2 Timing & test beam



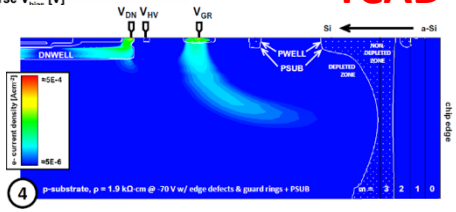


2017 | 2018 | 2019 | 2020 | 2021 | 2022 | +

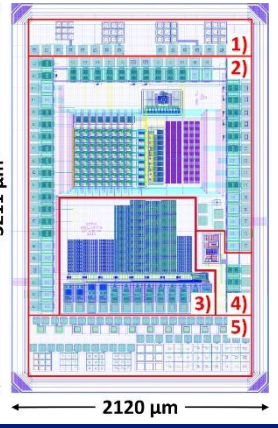
RD50-MPW1 I_LEAK↑ V_BD↓



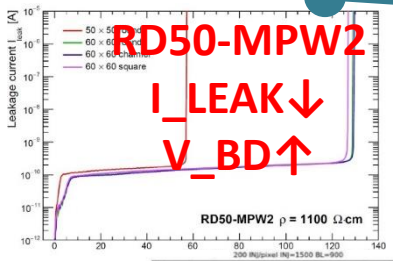
TCAD

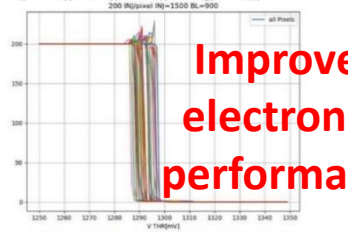


RD50-MPW2



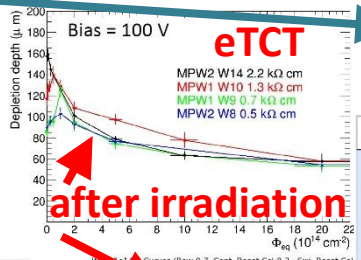
RD50-MPW2 I_LEAK↓ V_BD↑





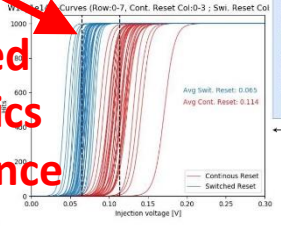
S-curves for all pixels with threshold variation. Trim DA values adjusted. Injection amplitude 1500 mV.

eTCT



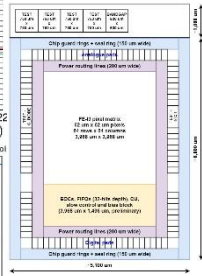
after irradiation

Improved electronics performance



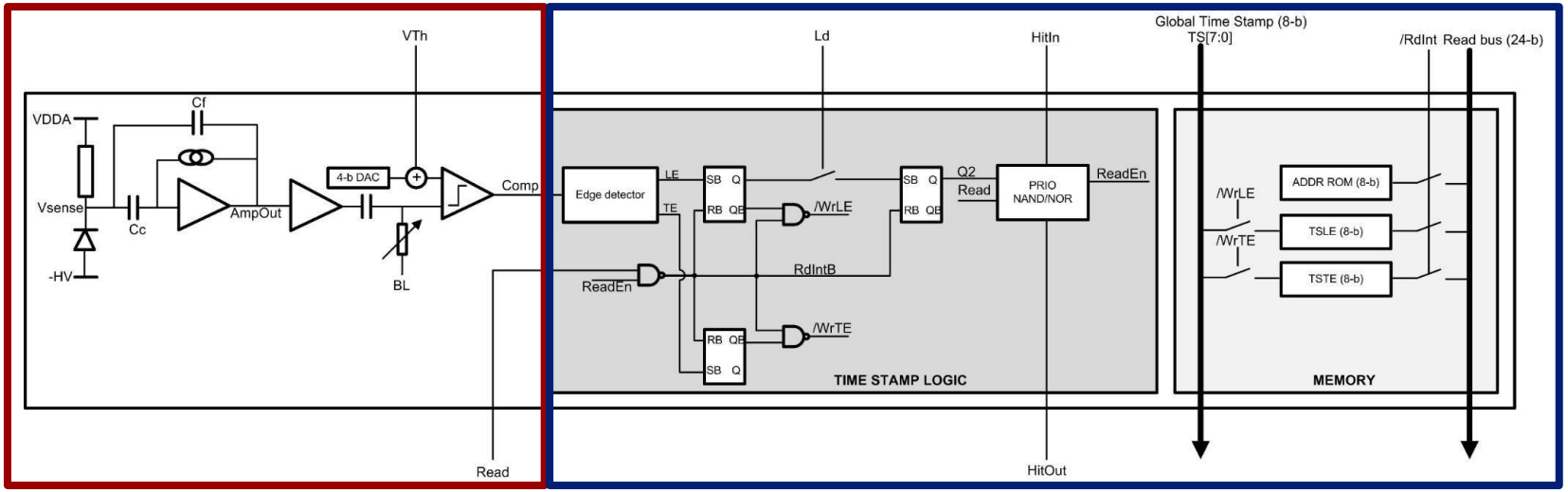
Wafer 13, 1e14N_eq

RD50-MPW3



Back up slides

RD50-MPW1 – In-pixel readout



Analogue readout

- Sensor biasing circuit, CSA, RC-CR filters and CMOS comparator
- CSA with programmable discharging current
- CMOS comparator with global VTH and local 4-bit DAC for fine tuning

Total power consumption is ~ 23 µW

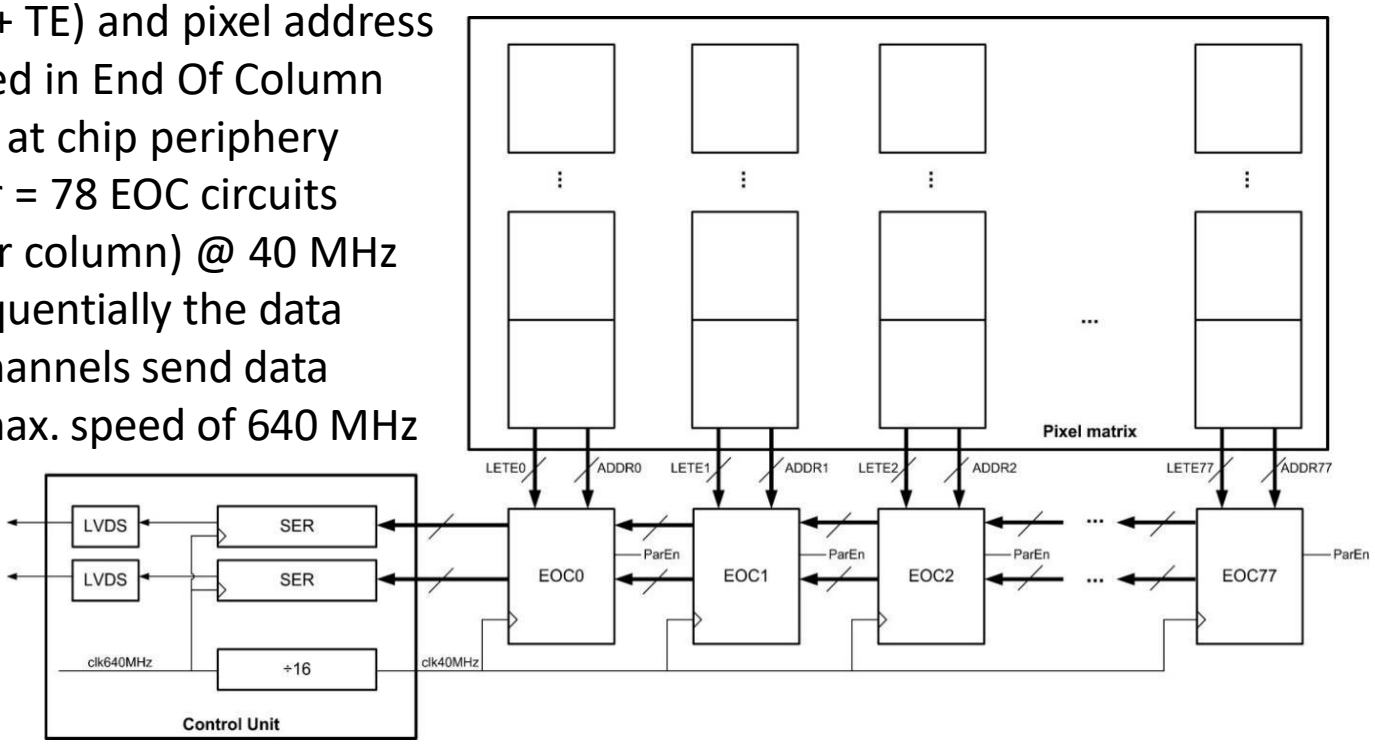
Digital readout

- For each hit
  - ➔ Leading edge (LE) 8-bit DRAM memory
  - ➔ Trailing edge (TE) 8-bit DRAM memory
  - ➔ Address (ADDR) 8-bit ROM memory

  } ➔ TOT = LE – TE (off-chip)
- Global 8-bit Gray encoded time-stamp (40 MHz)
- Continuous readout (synchronous, triggerless and without zero suppression)

RD50-MPW1 – Peripheral readout

- **Continuous readout**
  - ToT info (LE + TE) and pixel address (ADDR) stored in End Of Column (EOC) circuit at chip periphery
  - Shift register = 78 EOC circuits (one EOC per column) @ 40 MHz
  - CU reads sequentially the data
  - 2 serial TX channels send data off-chip @ max. speed of 640 MHz



- **Limitations**
  - Transmission of bare data (no synch. frame, no SOF and no EOF)
  - Columns with no hits are also readout (transmission of zeros!)
  - One pixel only per column is read out every 25 ns * number of columns
  - 2 serial TX channels

RD50-MPW1/2 – DAQ

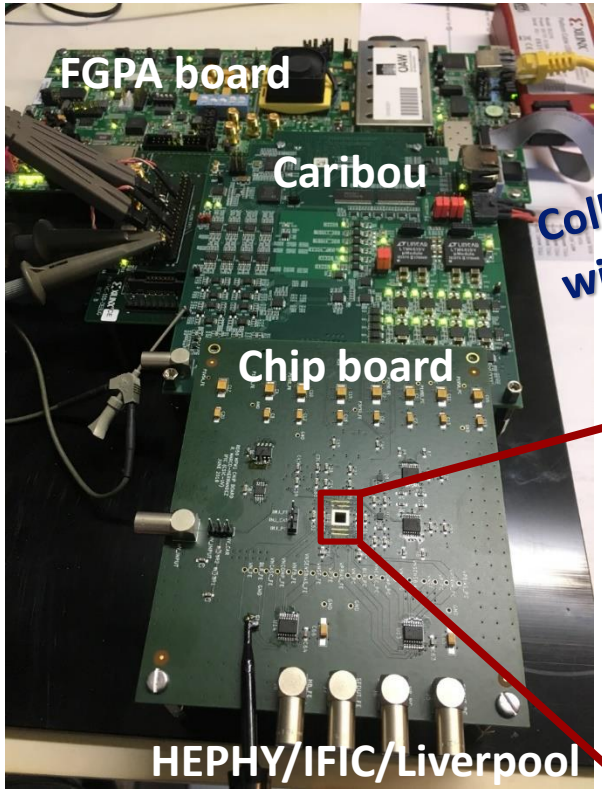
- **Xilinx Zynq-7000 SoC board:**
  - ZC706 (HEPHY, Liverpool)
  - ZC702 (Valencia)
  - Dual-core ARM Cortex-A9
  - Artix 7 FPGA
  - 2 FMC connectors, GbE, 1 GB DDR3 SDRAM, 128 Mb SPI flash memory, SD card, USB, etc.
- **Control and Readout (CaR) board:**
  - Development of Brookhaven National Laboratory
  - Provides common services like power supplies, voltage outputs, ADCs, I2C bus, TLU input, etc.
- **Custom chip board:**
  - Provides chip specific features
  - To be developed for each new device

Chip board Control and Readout (CaR) board

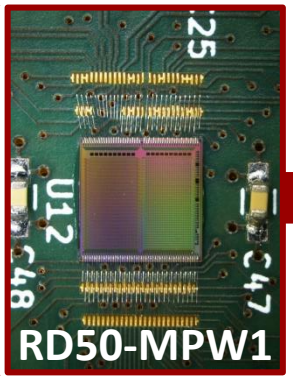
SoC board (ZC706)

I. Irmler, 36th RD50 WS

RD50–MPW1 – DAQ and measurements

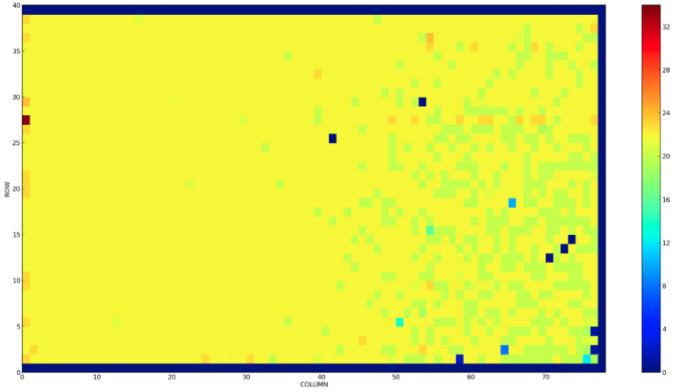


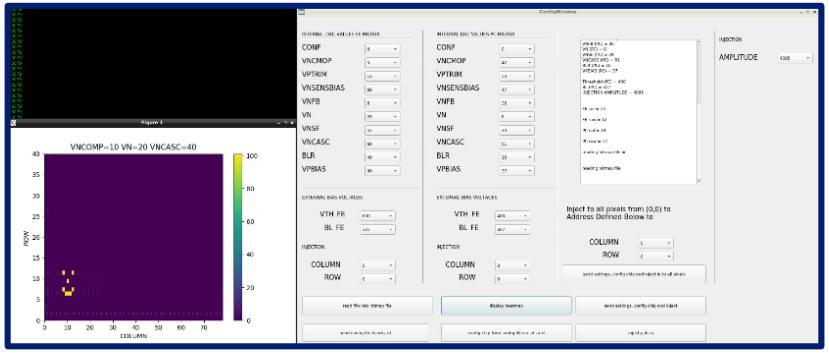
Collaborative effort within CERN-RD50



Hit map

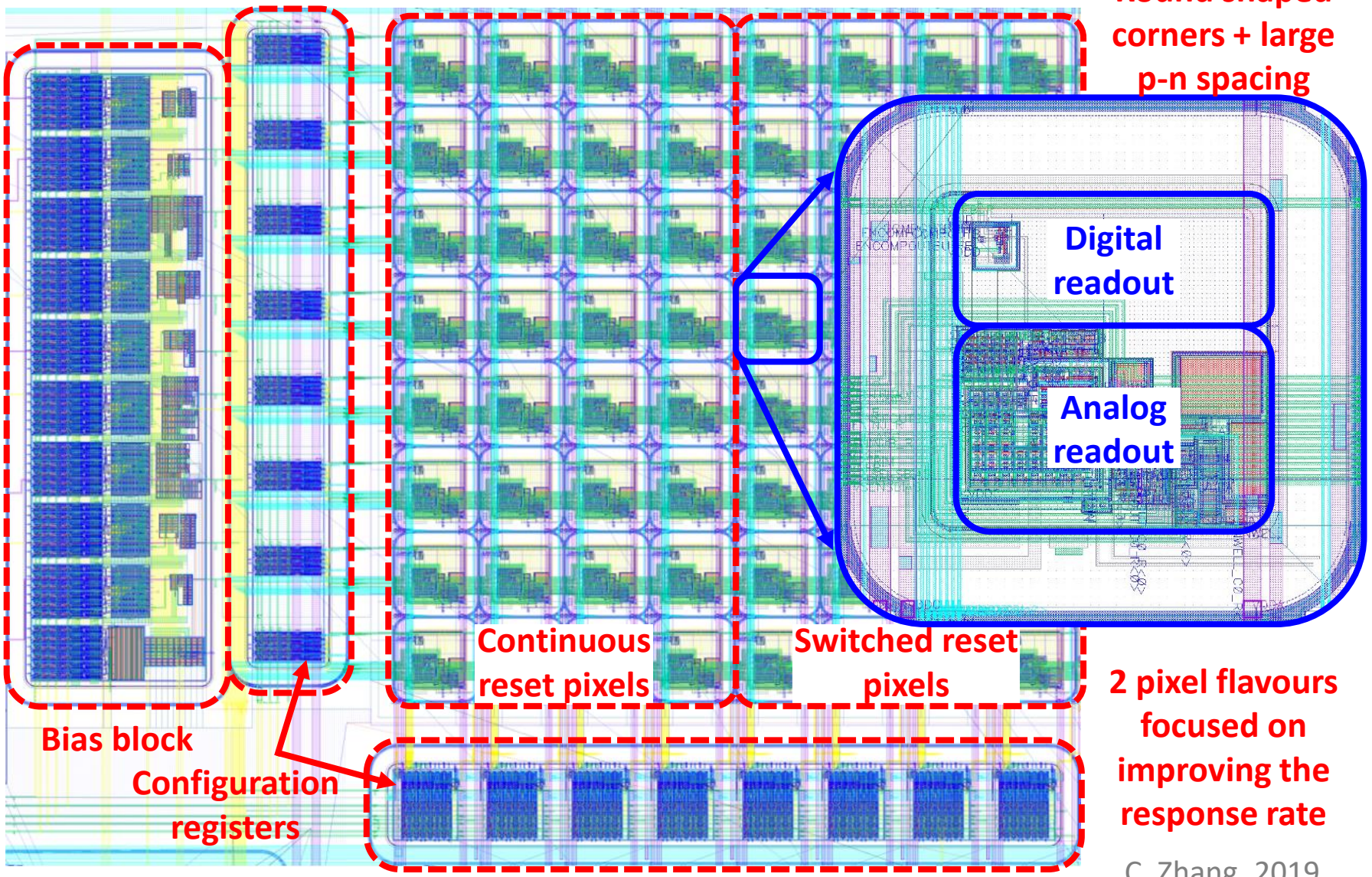
- 22 test pulses sent to each pixel
- Measure how many hits per pixel
- @ 1 MHz clock speed
- Mismatch between sent and measured hits in some pixels



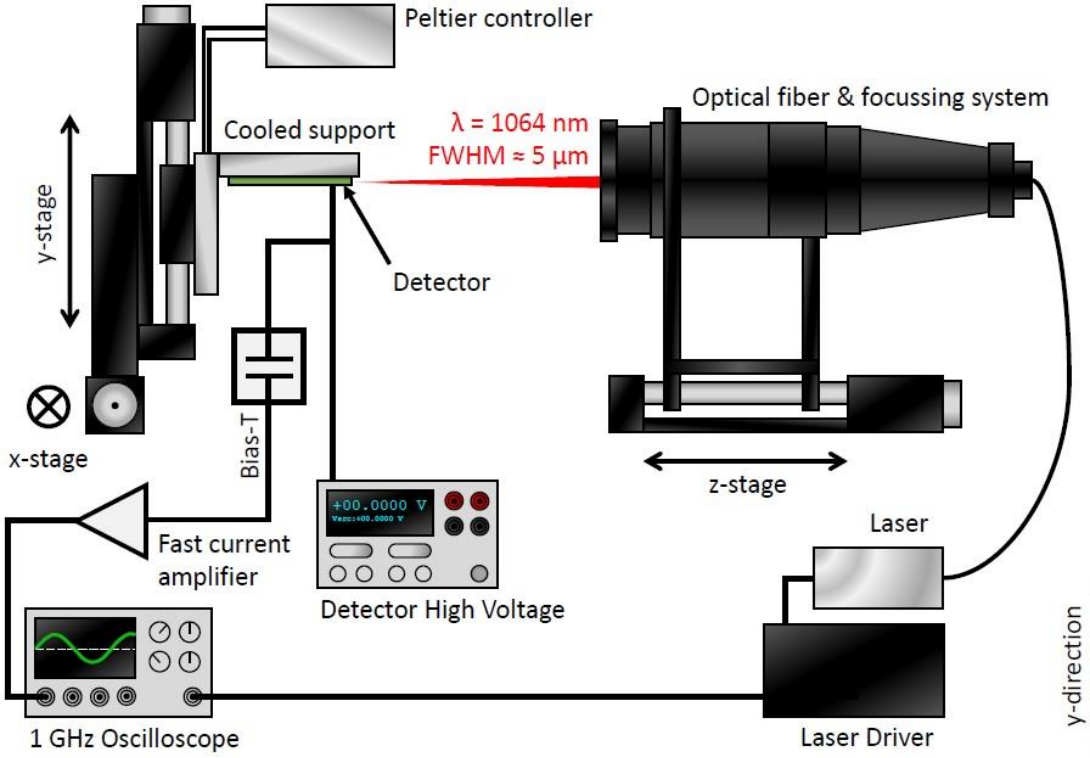


- The chip essentially works, but it has some issues

RD50-MPW2 – Pixel matrix



Edge-Transient Current Technique

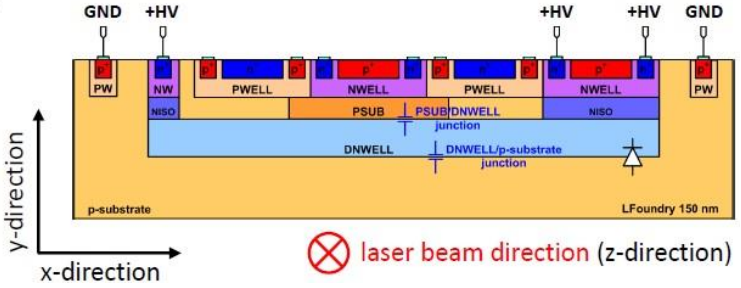


e-TCT measurements

- Beam diameter in the silicon
  - FWHM ~5 µm
- Width of light pulses ~300 ps, repetition rate 500 Hz

Connection scheme

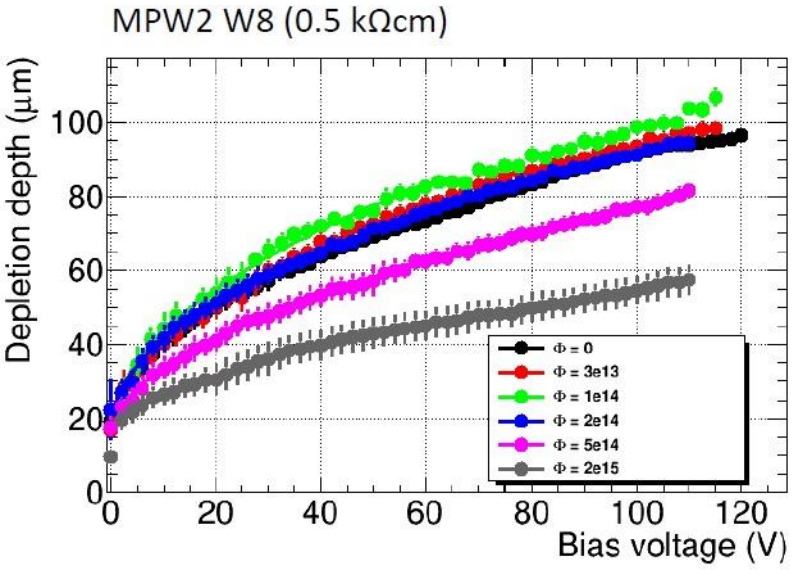
- INNER = +HV
- Sub! = GND

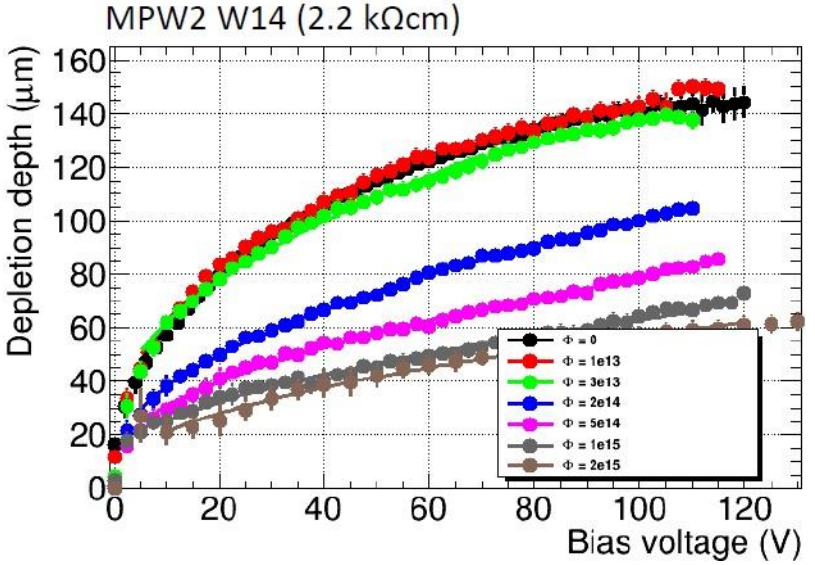


M. Franks, 2020

RD50-MPW2 – eTCT

- Annealed at 60°C for 80 minutes
- Measured at 20°C





I. Mandic, 37th RD50 WS

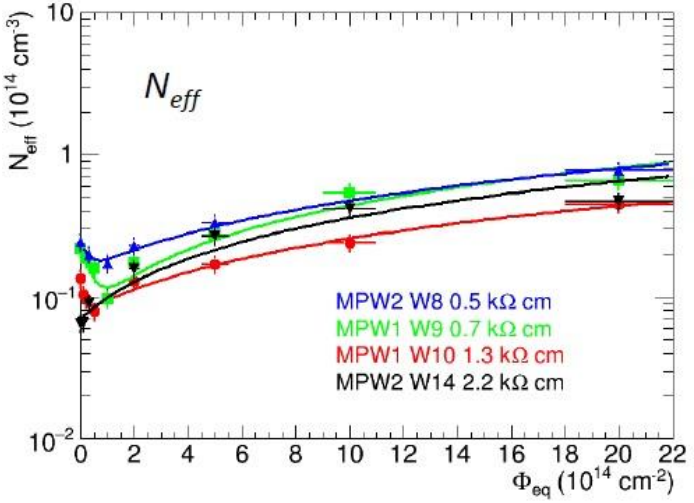
- Fit

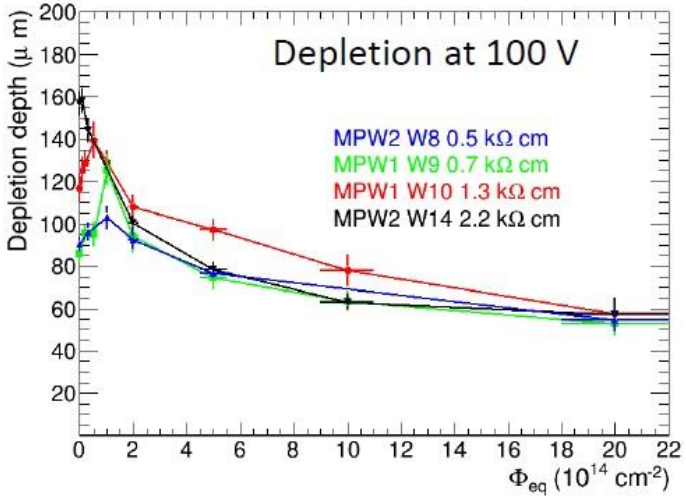
$$W_D = W_{D_0} + \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{e_0 N_{eff}} \cdot V}$$

W_{D0} = depletion depth at 0 V bias voltage
N_{eff} = effective doping concentration
ε_0 = free space permittivity
ε_{Si} = silicon relative permittivity
e_0 = elementary charge

RD50-MPW1/2 – eTCT

- Acceptor removal





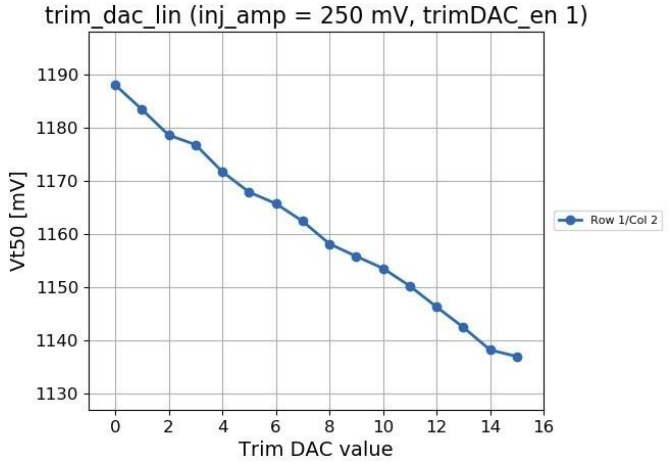
$$N_{eff} = N_{eff0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{eq})) + g_C \cdot \Phi_{eq}$$

Wafer	Nominal initial resistivity [kΩcm]	Measured N_{eff0} [10^{14}cm^{-3}]	[N_c/N_{eff0}]	c [10^{-14} cm^2]	g_c [10^{-2} cm^{-1}]
w8	0.5	0.25±0.04	0.39 ± 0.14	3.5 ± 3.2	3.3 ± 0.6
w9	0.7	0.23±0.03	0.72 ± 0.10	2.5 ± 0.9	3.9 ± 0.6
w10	1.3	0.13±0.02	0.43 ± 0.10	8.1 ± 5.4	1.8 ± 0.3
w14	2.2	0.07±0.01	/	/	2.9 ±0.4

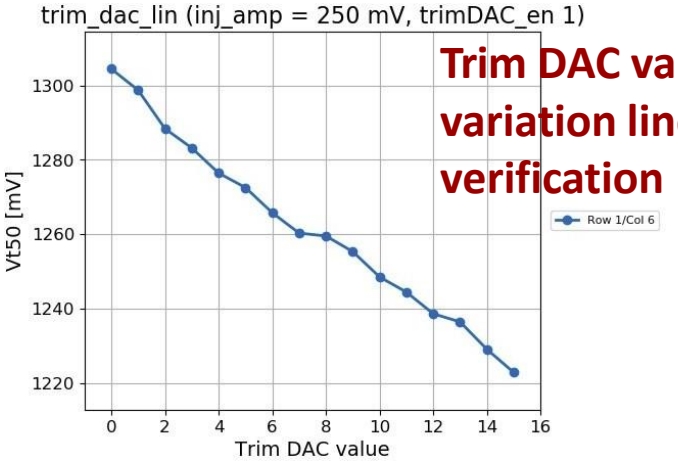
I. Mandic, 37th RD50 WS

- W14: acceptor removal parameters could not be extracted, fit: $Neff = Neff0 + gc \cdot \Phi$
- Large variations of ***Nc/Neff0***
- Large uncertainties of **c**
- ***gc*** larger than typical for p-type silicon (~ 0.017 cm-1)

RD50-MPW2 – S-curves and calibration

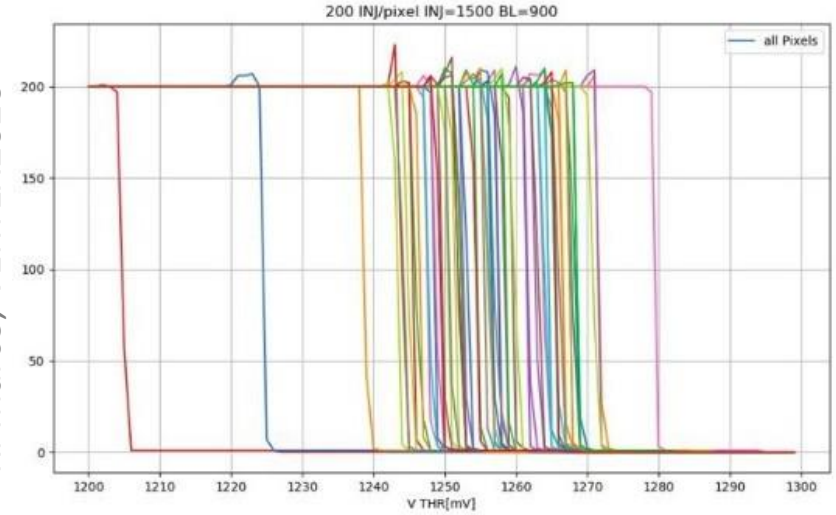


Vt50 (mV) versus trim DAC value for a CR pixel (R1/C2). Injection amplitude 250 mV.

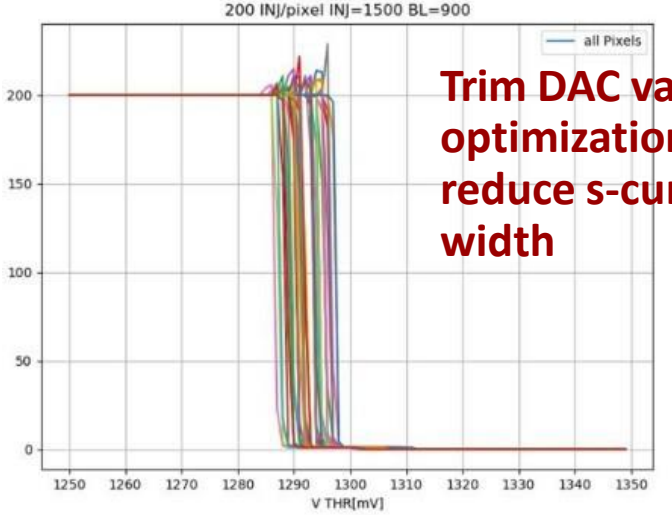


Trim DAC value variation linearity verification

Vt50 (mV) versus trim DAC value for a SR pixel (R1/C6). Injection amplitude 250 mV.



S-curves for all pixels with threshold variation. Trim DAC value 15. Injection amplitude 1500 mV.



Trim DAC value optimization to reduce s-curve width

S-curves for all pixels with threshold variation. Trim DAC values adjusted. Injection amplitude 1500 mV.

RD50-MPW2 – S-curves and calibration

- Summary of gain measurements with in-pixel calibration circuit

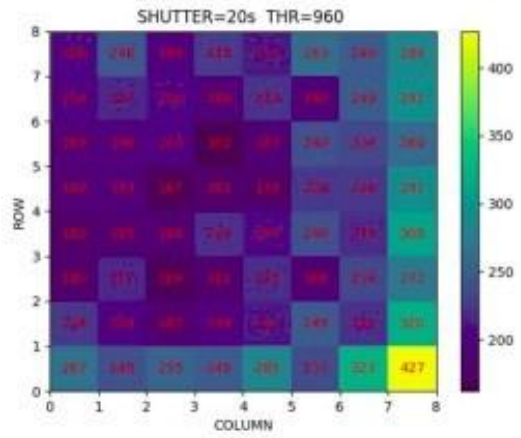
	Vienna		Liverpool		Valencia	
	CR	SR	CR	SR	CR	SR
Bias registers	Nominal values		Nominal values		Nominal values	
BL (mV)	800		900		900	
Linear range (mV)	150-450	150-450	150-400	150-350	150-450	150-450
Linear range[1] (fC)	0.42-1.26	0.42-1.26	0.42-1.12	0.42-1.12	0.42-1.26	0.42-1.26
Gain (mV/mV)	0.9-1.1	1.2-1.4	1.4-1.68	1.96-2.1	1.26-1.4	1.54-1.68
Gain[1] (mV/fC)	321-392	428-500	500-600	700-750	450-500	550-600
[1]Considering C_{inj} 2.8 fF						

R. Marco, VERTEX2020

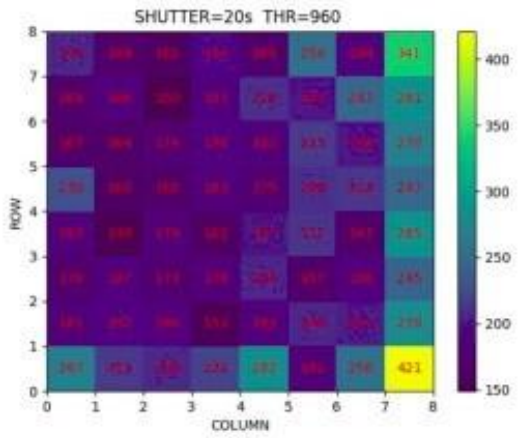
- Values measured at different places with different setups tend to agree
- Baseline value (comparator input DC value) influences the gain measured

RD50-MPW2 – Test with 90-Sr source

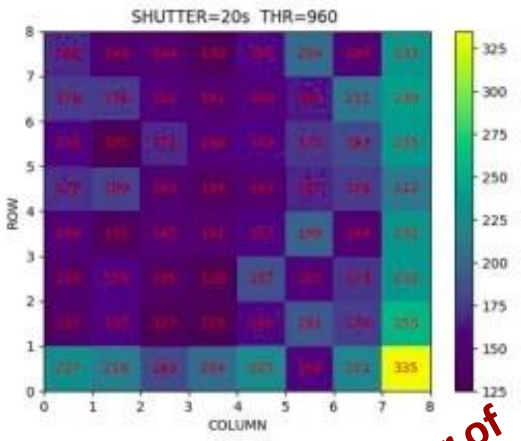
HV = -90V



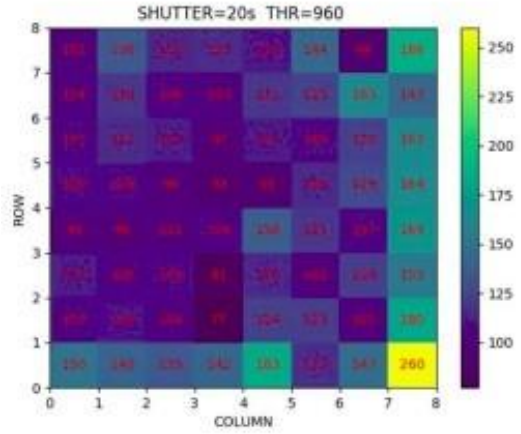
HV = -70V



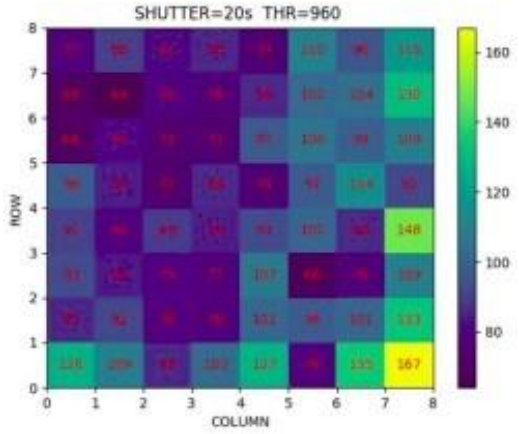
HV = -50V



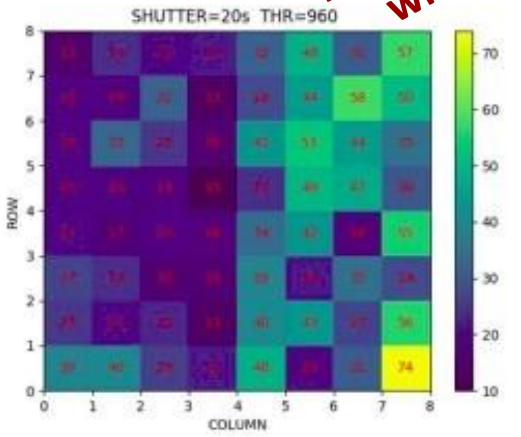
HV = -20V



HV = -10V



HV = 0 V

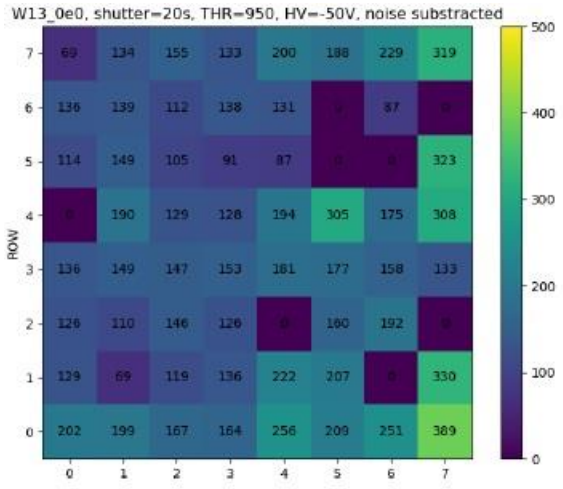


Number of hits increases with HV

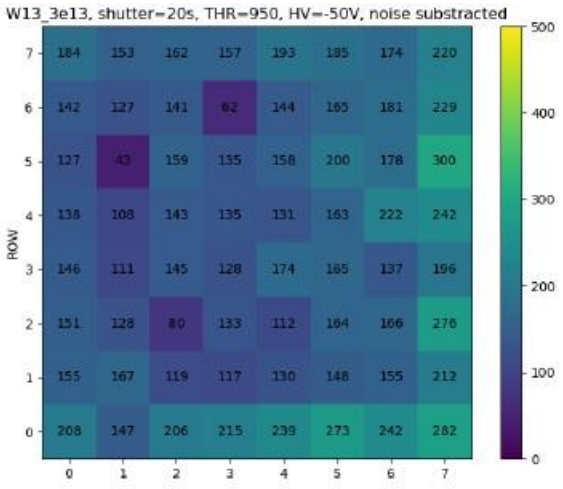
R. Marco, VERTEX2020

RD50-MPW2 – Test with 90-Sr source

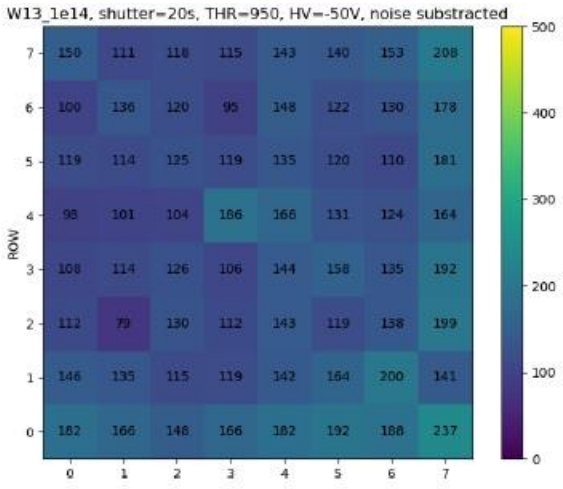
- **Also after irradiation:**
  - HV at -50 V
  - Different fluences
  - Noise subtracted
  - More hits for switched reset pixels
  - Less hits seen for higher fluences (both pixel flavours)



Wafer 13, unirradiated



Wafer 13, 3e13N_{eq}



Wafer 13, 1e14N_{eq}

P. Sieberer, 37th RD50 WS